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Description of item under review for fair use: TABLE I CHARACTERISTICS OF WIDE-BAND-GAP SEMICONDUCTORS AT 300oK. Source: V. R. Manikam and K. Y. Cheong, “Die Attach Materials for High Temperature Applications: A Review,” IEEE Trans. Compon. Packag. Manuf. Technol., vol. 1, no. 4, pp. 457–478, Apr. 2011. Figure 1. Temperature profile for eutectic solders (Sn63Pb37). Source: W.D. Brown and R. K. Ulrich, Advanced Electronic Packaging with Emphasis on Multichip Modules, IEEE Press, 2006. Figure 2. Conceptual views of Ni–Sn TLP bonding process. Source:S. W. Yoon, K. Shiozaki, S. Yasuda, and M. D. Glover, “Highly reliable nickel-tin transient liquid phase bonding technology for high temperature operational power electronics in electrified vehicles,” in Proc. Appl. Power Electron. Conf. Expo., Orlando, FL, Feb. 2012, pp. 478–482. TABLE II VARIOUS CHIP-ATTACH MATERIALS, THEIR PROPERTIES. Source: T. G. Lei, J. N. Calata, S. Luo, X. Chen, and G.-Q. Lu, “Low temperature sintering of nano-scale silver paste for attaching large-area (>100 mm2) chips,” IEEE Trans. Comp. Packag. Technol., vol. 33, no. 1, pp. 98–104, Mar. 2010. TABLE III HOMOLOGOUS TEMPERATURE OF VARIOUS CHIP-ATTACH MATERIALS. Source: J. Lutz, H. Schlangenotto, Semiconductor Power Devices: Physics, Characteristics, Reliability, Springer, 2008. Figure 3. Preparation procedure of nanoscale silver paste. Source: G. Q. Lu, J. N. Calata, Z. Zhang, and J. G. Bai, “A lead-free, low temperature sintering die-attach technique for high-performance and high-temperature packaging,” in Proc. 6th IEEE CPMT High Density Microsys. Design Packag. Comp. Failure Anal. (HDP’04), pp. 42–46, 2004. Figure 4. Shear strengths of different interconnection technologies. Source: M. Knoerr and A. Schletz, “Power semiconductor joining through sintering of silver nanoparticles: Evaluation of influence of parameters time, temperature and pressure on density, strength and reliability,” in Proc. Int. Conf. Integr. Power Electron. Syst., Nuremberg, Germany, pp. 1–6, Mar. 2010. Figure 5. Probability functions for different interconnection technologies with thermal cycling tests between -55°C and +175°C (ΔT=230oK). Source: M. Knoerr, S. Kraft, and A. Schletz, “Reliability assessment of sintered nano-silver die attachment for power semiconductors,” in Proc. 12th Electron. Packag. Technol. Conf., Singapore, pp. 56–61, 2010. Figure 6. Cross sections of copper samples after 800 cycles for (a) cracked SAC305 soldered joint, (b) cracked SN100C soldered joint, and (c) intact sintered-silver joint, and (d) intact sintered-silver joint under low magnification. Source: L. Jiang, “Thermo-mechanical reliability of sintered-silver joint versus lead-free solder for attaching large-area devices,” M.S. thesis, Dept. Mater. Sci. Eng., Virginia Tech., Blacksburg, 2010. Figure 7. (a) Change of thermal impedance and the (b) percentage change of thermal impedance for samples with different chip-attach materials after 500 cycles (−40°C to +125°C). Source: X. Cao, T. Wang, K. D. T. Ngo, and G.-Q. Lu, “Characterization of lead-free solder and sintered nano-silver die-attach layers using thermal impedance,” IEEE Trans. Compon. Packag. Manuf. Technol., vol. 1, no. 4, pp. 495–501, Apr. 2011. Figure 8. Pressure-free silver sintering technology from Henkel SSP-2000. Source: Henkel. (2013). Company Website [online]. Available: http://www.henkel.com Figure 9. Silver epoxy X-pattern dispensed by writing, and fillet coverage along the die edges. Source: M, Lee et al., “The squeezing process of complex epoxy patterns in the die-attaching of large IC-chip,” Int. Conf. Integr. Power Electron., pp.1- 8, 2006. Figure 13. Basics of PT, NPT, and Soft Punch Through (SPT) Technologies. Source: Semikron Incorporation. (2013). Soft Punch Through (SPT) – Setting new Standards in 1200V IGBT [online]. Available: http://www.semikron.com Figure 14. SPT vs. SPT+ IGBT on-state losses at indicated current densities for 1200 V, 1700 V and 3300 V chips at 125°C. Source: Semikron Incorporation. (2013). Next Generation Planar IGBTs with SPT+Technol- ogy [online]. Available:http://www.semikron.com TABLE VI CURRENT CARRYING CAPACITY OF BONDING WIRE. Source: GLX Incorporation. (2013). Current carrying capacity of bonding wire [online]. Available: http://www.circuitsource.com/wiresize.htm Figure 28. Circuitry for four-terminal sensing. Source: IEEE Master Test Guide for Electrical Measurements in Power Circuits, ANSI/IEEE Standard 120-1989. Figure 43. Definitions of turn-off parameters for ABB IGBT. Source: ABB Switzerland Ltd. (2013). Application note 5SYA 2059-04: Applying IGBT and Diode dies [online]. Available: http://www.abb.com Figure 48. Cross section of setup for measuring thermal impedance of half-bridge module in ABB application note. Source: ABB Switzerland Ltd. (2013). Application note 5SYA 2059-04: Applying IGBT and Diode dies [online]. Available: http://www.abb.com TABLE XII. COMPONENTS AND CONDITIONS OF SILVER STRIKE SOLUTION. Source: T. G. Lei, “Thermo-Mechanical Reliability of Low-Temperature Sintered Attachme- nts on Direct Bonded Aluminum (DBA) Substrate for High-Temperature Electronics Packaging,” Ph.D. dissertation, Dept. Mater. Sci. Eng., Virginia Tech., Blacksburg, 2010. TABLE XIII. COMPONENTS AND CONDITIONS OF SILVER PLATING SOLUTION. Source: T. G. Lei, “Thermo-Mechanical Reliability of Low-Temperature Sintered Attachme- nts on Direct Bonded Aluminum (DBA) Substrate for High-Temperature Electronics Packaging,” Ph.D. dissertation, Dept. Mater. Sci. Eng., Virginia Tech., Blacksburg, 2010.

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