DEGRADATION IN LEAD ZIRCONATE TITANATE THIN FILM CAPACITORS FOR NON-VOLATILE MEMORY APPLICATIONS

by

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(ABSTRACT)

A study of the degradation of ferroelectric properties in Lead Zirconate Titanate (PZT) thin film capacitors is presented in this work. Metal - Ferroelectric - Metal capacitors were prepared by sputtering and metal organic decomposition (MOD) techniques. Samples with several different film thicknesses were considered in this study. Depolarization, leading to imprint has been studied at various temperatures. Changes in the dielectric properties of the capacitors as a function of the number of fatigue cycles is presented.

Impedance and modulus spectroscopic techniques have been applied to study the effect of degradation on the ferroelectric thin film. It has been shown that with accurate low frequency impedance measurement equipment, new insight can be gained on the mechanisms of degradation in ferroelectric capacitors.

Acknowledgments

I wish to thank my advisor Dr. Seshu B. Desu for giving me the opportunity to work in the Thin Films Characterization Lab. Not only did he make it possible for me to continue my graduate studies beyond the first nine months, but also, he gave me the key to the enchanting world of ferroelectric memories and ably guided me through its many challenging problems.

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I must thank Dr. Desu for letting me be a part of an industrious, pragmatic, competitive and yet very friendly research group, the likes of whom, I fear, I might never find again.

How can I even begin to acknowledge my indebtedness to my family. To attempt to express my gratitude to my father, mother and my sister within the bounds of this "Acknowledgments", would be to humiliate them. However, I must say that their indomitable courage in the face of disaster and unfaltering faith in hard work have been the guiding lights in the last two years of my life.

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Chapter I. Introduction

1.1 Background

A generation of memory designers have dreamt of an ideal nonvolatile memory - one which would offer low cost per bit, high density, fast random access, WRITE/READ and cycle times of equal duration, low power consumption, operation over a wide temperature range, a single low-voltage power supply, a high degree of radiation tolerance and, of course, inherent nonvolatility. Their dreams have not yet been fulfilled. Although nonvolatility is a desirable feature, it is often sacrificed in favor of other more important properties. The engineering goal has reduced to one of minimizing the impact of this trade-off.

Present day nonvolatile memory applications generally fall into several broad areas. The first includes low-density memories for use in TV tuners, postage meters, and automotive applications. A second group consists of various types of nonvolatile storage of microprogram control and remote handling of these systems. A third group includes radiation hard applications.

Two other areas where wide-scale application depends on future technological progress are solid-state disks and electronic image storage, both of which require large amounts of high-density, cost-effective nonvolatile memory.

Ferroelectric technology, which is fast maturing , but still has not come of age, could become the ideal technology for solid-state disks.

In the tremendously competitive world of commercial memory production, ferroelectric memory is still in its infancy. Its position in the nonvolatile memory market has to be viewed in the proper historical perspective.

1.2 A memorable history of non-volatile cells

In 1967, Kahng and Sze [2] had introduced the first nonvolatile semiconductor memory. A conventional p-channel MOSFET was modified to incorporate a floating metal gate. Charge storage on the floating gate enabled one to electrically alter the transistor threshold voltage between a low and a high value to represent logic 1's and 0's.

Thereafter, floating-gate nonvolatile memories have made steady progress. A variety of such memories are available today, each providing a different trade-off between erasability, cell size, and endurance reliability. The original metal floating gate became polysilicon in 1970 [3]. A combination of erasing by tunneling and programming by hot-electron method seemed to be the dream target of all memory designers in the 1970's.

However, in 1980, Intel introduced the 2816, a 16-kb 10,000 write/erase cycle EEPROM which exclusively used electron tunneling for WRITE and ERASE operations [4]. This polarized the memory design activity towards electrical write and erase and the tunneling erase concept was sent to hibernation - at least for the moment.

In addition to the fact that EEPROMs are 2 to 3 times larger than UVEPROMs, endurance reliability proved to be an important issue for EEPROMs - tunnel oxides tend to possess low breakdown limits. Improvement can be achieved by adding an error detection circuit, which would invariably cost some more real estate. Today, EEPROM stands as an important technology, with a somewhat uncertain future.

The old promise of hot-electron programming and tunnel ERASE was rediscovered around 1984. The aim was to achieve a single transistor EEPROM cell. The cell size and endurance reliability were improved by this method but unlike the previous EEPROMs, these cannot be erased by the entire chip or large sections thereof. Hence the term FLASH ERASE and the name FLASH (E)EPROM.

Apart from the floating - gate memories, metal-nitride-oxide-silicon (MNOS) memory transistors have also been in production and development since 1967 [5]. MNOS is a serious competitor of EEPROM, especially in Japan, due to the strong technological backing provided by HITACHI. In contrast to the original Kahng/Sze cell which used floating-gate storage and thin-oxide tunneling, the MNOS cell uses nitride storage and thin-oxide tunneling. MNOS however, suffers from data retention problems.

1.3 Ferroelectrics for nonvolatile memories

Ferroelectric nonvolatile memory is an old idea that holds exciting new possibilities. Since 1963, several studies on ferroelectric memories have been published. The initial idea was to use a ferroelectric thin film, which can be permanently polarized by an electric voltage pulse, as the gate dielectric of a transistor. Good endurance and fast WRITE time (~10 ns) are two of its most attractive features. However, read errors might occur in such a memory cell due to the absence of a well defined threshold voltage for polarization.

In 1987, a new concept of ferroelectric memory was introduced. The key idea was to use a ferroelectric thin film as the dielectric in the capacitor of a DRAM cell. Due to the fact that such a cell is refreshed every time it is read, READ disturbances could be avoided.

If extreme endurance (10^{16} write/read cycles), good data retention and manufacturability could be achieved, this could be the ideal memory. Ferroelectric memory can potentially match DRAM in WRITE and READ speed and beat DRAM in cell size, with nonvolatility offered as a bonus.

However, if the challenges of compatibility with silicon technology, defect density and reliability cannot be achieved, ferroelectrics might well become part of a whole genre of what might be called - distant memories.

Table 1.1 gives a feature by feature comparison among the various modern nonvolatile memories. The low density (e.g. 4 kbit) versions of ferroelectric random access memories (FRAMs) can compete with both EEPROMs and battery-backed SRAMs. When compared to EEPROM, FRAM has a much faster write cycle time (200 ns/byte versus 2000 ns/byte) and longer write endurance (10^{10} maximum write/erase cycles versus 10^4-10^5). The erase, write and access times are essentially equal. This is important for those applications that are not read-mostly, like the SRAM applications. EEPROM is a good read-mostly memory, but it cannot perform well as a read/write memory. Compared to SRAMs, FRAMs have similar read/write cycle times, but FRAMs are nonvolatile without a battery.

Usually, nonvolatility in SRAMs is achieved in one of two ways. The first way is to buy an SRAM with a battery enclosed and the second way is to use the system - level lithium battery. In either case, SRAM nonvolatility endurance is a function of battery life - it might range from 6 months to 10 years. In contrast, FRAM endurance is a function of the number of cycles, not the length of time. This is an important difference which may make the FRAM device much more reliable than a battery backed SRAM.

Table 1.1. Comparison of important features of some non-volatile memories [1].

FEATURE	EPROM	NAND EEPROM	Full-Featured EEPROM	Flash EEPROM	Stepped-Gate Flash	MNOS (SNOS)	Ferroelectric	Battery-Backed DRAM	Battery-Backed SRAM
Density	4Mbytes	4Mbytes	1Mbyte	1Mbyte	1Mbyte	64K	16K	16 Mbytes (Proj)	256K
Die Size (mm2)	83.4	163	91.5	38	51	25	25	N/A	N/A
Cell Size (μm2)	11.9	12.9	30.4	15.2	24.6	120	270	3.4	N/A
Elements/Cell	1	1.25	2	1	1.5	2	2	2	6
Lithography (μm)	1	0.5	1	1	1	2	1.5	0.5	1.2
Typ. Access Time (nsec)	90	1600	110	90	150	200	100	1000	45
Current Consumption									
Operating (mA)	20	20	66	8	N/A	30	5	5	120
Standby (μA)	10	10	100	4	N/A	10	10	.5	1
Write/Erase Voltage	12.5/-	22/17	16/16	12/12	21/21	15/15	5/5	1.5/1.5	5(3 hold)
Charge Pump	No	Yes	Yes	No	No	Yes	Not Nec.	Not Nec.	Not Nec.
Write Speed (μsec/byte)	.5	4000	2000	10	.5	5000	.2	1	.045
Erase Speed (sec)	1200/mem	.01/4 Kbyte	.002/byte	.9/mem	5/mem	.005/mem	1e-7/byte	1e-6/bit	45e-9bit
Max Write/Erase Cycles	1e2 to 1e3	1e4 to 1e5	1e4 to 1e5	1e5	1e2 to 1e3	1e5	1e10	Infinity	Infinity
Min Erase Block Size	All bits	4 Kbytes	1 byte	All bits	128 bytes	32 bytes	1 byte	1 bit	1 bit
Radiation Tolerance (Rads)	1e5	1e5	1e5	N/A	N/A	1e6	1e7 to 1e8	0	Low
Retention (Years)	>10	>10	>10	>10	>10	>10	>10	5@2AH Battery	4@35mAH Battery
Manufacturer	Intel	Toshiba	Mitsubishi	Intel	Seeq	Hitachi	Ramtron	Hitachi	Dallas Semi

A very high density FRAM process with cell size similar to DRAM can be developed. These parts can compete with DRAMs and ferromagnetic disk memories. Scalability should not be a problem - in fact FRAM cells should turn out to be more scalable than DRAM cells because the ferroelectric capacitors have a much higher dielectric constant (>1000) than CMOS SiO_2 capacitors. Thus only a very small capacitor area, perhaps the area of a contact via, is sufficient for storage purposes.

1.4 Ferroelectric materials for nonvolatile memories

Below the Curie Temperature, a ferroelectric material has a directional spontaneous electrical polarization due to a non-centrosymmetric atomic unit cell (figure 1.1). This polarization, caused by the displacement of anions and cations in the cell, can be switched by an electric field. The polarization state is stabilized by the formation of domains of identically oriented unit cells, when the external field is withdrawn. The presence of two equally stable electrically switchable states makes ferroelectric materials ideal for nonvolatile binary data storage purposes. By using thin films, the switching voltage can be scaled to less than those normally used in a modern day integrated circuit.

But for memory applications, the Metal - Ferroelectric - Metal (MFM) capacitors must comply with certain requirements. These will be critical in determining the characteristics and organizational aspects of the memory.

For reliable detection, a switching polarization larger than 10fC/cm^2 is needed. This is dictated by noise margin considerations. This level has to be reached within a short time (<10ns) and at voltages below the standard IC supply voltages. A nominal supply voltage of 5V is generally assumed, but in future, this may reduce to 3.3V. These

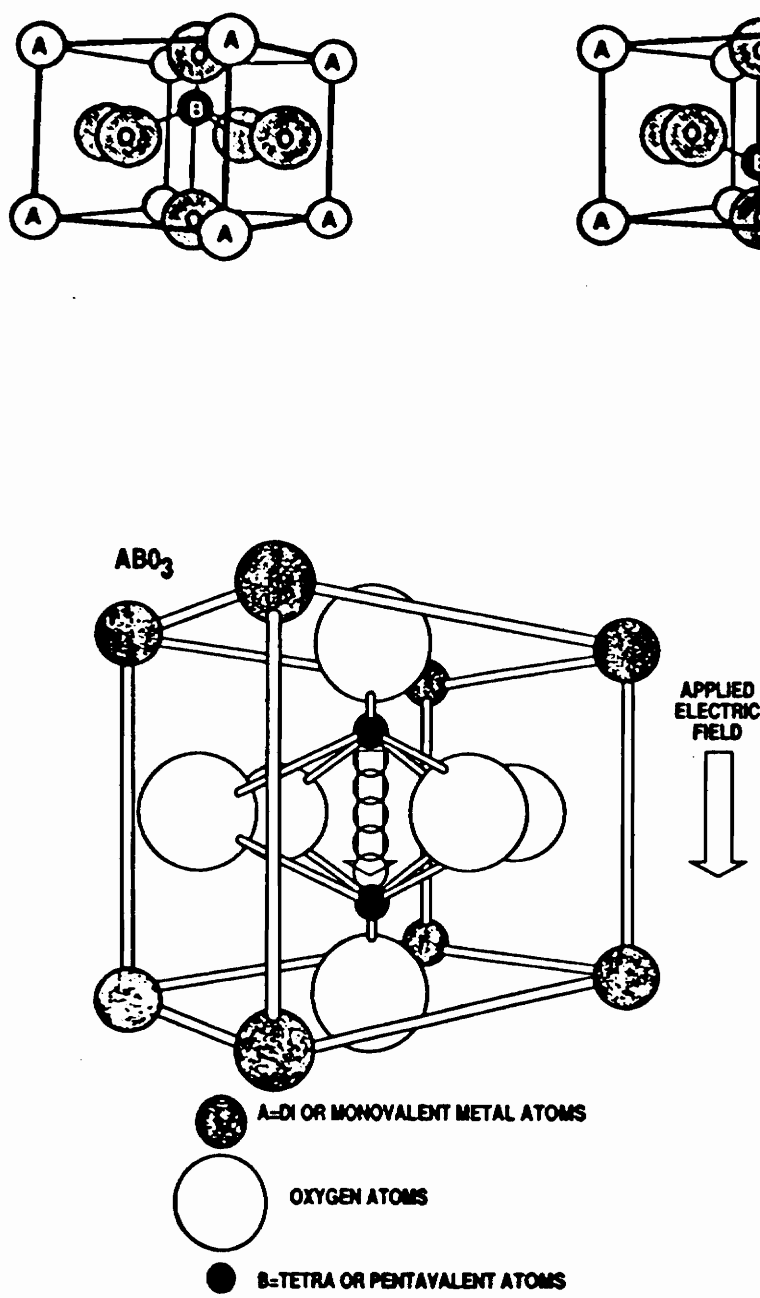


Fig 1.1 Perovskite structure ABO_3. Displacement of central atom B causes dipole moment.

requirements can be met with films of thickness < 500 nm and of materials with small coercive field (Ec) strengths. The number of allowed reversal operations has to be large (10^{14}-10^{15}) and the stability of the poled layers has to be very good (10 years without external voltage).

The most studied materials for memory at this moment are Lead Zirconate Titanates, $PbZr_xTi_{1-x}O_3$ (PZT) (figure 1.1). This is because such PZT films with thicknesses between 50 to 400 nm fulfill the requirements to a great degree. Additionally, it has been seen that its processing can be done in combination with standard integrated circuit processing [6].

An important parameter that has been found to influence the properties of the ferroelectric capacitors are the materials of the electrodes. Due to the reactivity of PZT and the relatively high processing temperatures (>600^{o}C) inert bottom electrode materials have to be applied. Pt-based electrodes are used which are deposited onto SiO_2 or Si_3N_4 by sputtering [7]. Adhesion is improved by means of a thin Ti-film. Inspite of being reasonably inert, the Pt-bottom electrode does affect the ferroelectric properties of the PZT films and might cause problems during subsequent processing. Even then, Pt-bottom electrodes are used almost always in integrated devices. Other conducting materials like RuO_2, ReO_3, $CoSi_2$ and TiN have been investigated as substitute electrode materials [8], but among these only RuO_2 has proved to be a viable alternative. Pt is also used as the top electrode material.

1.5 Ferroelectric memory cell processing

Usually, the basic structure of a ferroelectric memory cell consists of a ferroelectric capacitor as a storage element with one electrode connected to a MOS transistor (figures 1.2a, 1.2b). This transistor acts as a select switch that connects the storage node to the bitline when the cell is selected or isolates it when it is not selected. Figures 1.2a and 1.2b show cross-sections of two different ways in which such a capacitor can be connected to a MOS transistor. In figure 1.2a the capacitor is located on top of the field oxide next to the transistor. However, to increase the density, the capacitor can be positioned on top of the MOS transistor [9]. In figure 1.2b the capacitor is shown to be positioned inside the contact hole.

The processing can be divided into three major phases. In phase I, the transistor is processed in a standard CMOS process up to the passivation layer before the contact hole is etched. In phase II, the ferroelectric (bottom electrode - ferroelectric thin film - top electrode) capacitor is deposited and structured. In phase III, the last part of the processing including the deposition of the isolation layer around the capacitor is done, following standard CMOS processing.

Ferroelectric processing demands use of reactive materials that are not commonly used in standard silicon processing. This calls for adoption of special precautionary measures to prevent the ferroelectric processing from affecting the standard devices on the one hand, and the latter CMOS processing from damaging the ferroelectric properties on the other. Addition of suitable barrier layers and modification of ferroelectric capacitor processing to conform with the back-end processing are two simple solutions that can be considered.

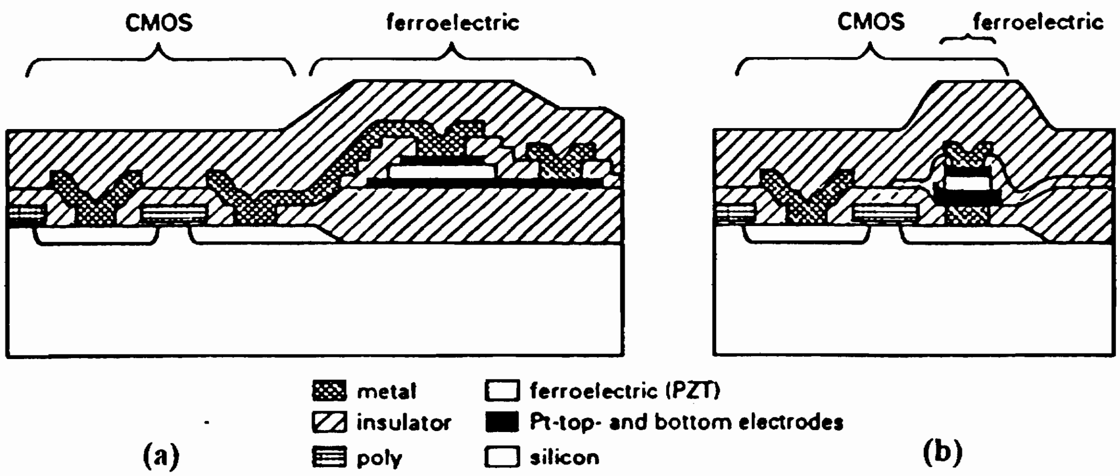


Fig 1.2 Cross sectional views of ferroelectric capacitors integrated with MOS transistors - two different configurations.

1.6 Electrical characteristics of the ferroelectric capacitors

The most fundamental characterization method of any ferroelectric material is the measurement of the hysteresis loop of the polarization versus electric field (or voltage). This loop can be obtained by means of the so-called Sawyer-Tower circuit (figure 1.3). In this circuit, a linear capacitor is placed in series with the ferroelectric capacitor-under-test (CUT). Across this entire series circuit, a sinusoidal signal of reasonably low frequency (~1 KHz) is applied. The output is taken across the linear capacitor. The input sinusoid and the output signal are fed into the x and the y channels of an oscilloscope respectively. When the oscilloscope is run in the x-y mode, what is obtained is the hysteresis loop of the CUT. Two important conditions for obtaining the hysteresis loop are:

i) the applied sinusoidal signal must have an amplitude sufficient to produce a field greater than the coercive field of the CUT, and

ii) the linear capacitance should be at least 10 times the capacitance of the ferroelectric capacitor.

The latter requirement is important because negligible voltage should drop across the linear capacitor and almost all the voltage should drop across the ferroelectric capacitor in the voltage divider circuit formed by the two capacitors.

Apart from the hysteresis loop, other characterization methods include measurement of the current versus voltage (I-V curve), and small signal ac capacitance versus applied field (C-V). These methods provide useful information about the ferroelectric behavior of the thin film capacitors. DC impedance measurements (e.g. current versus time at a constant voltage) can be useful for determining time dependent breakdown strengths. Other characterization methods include pulse polarization

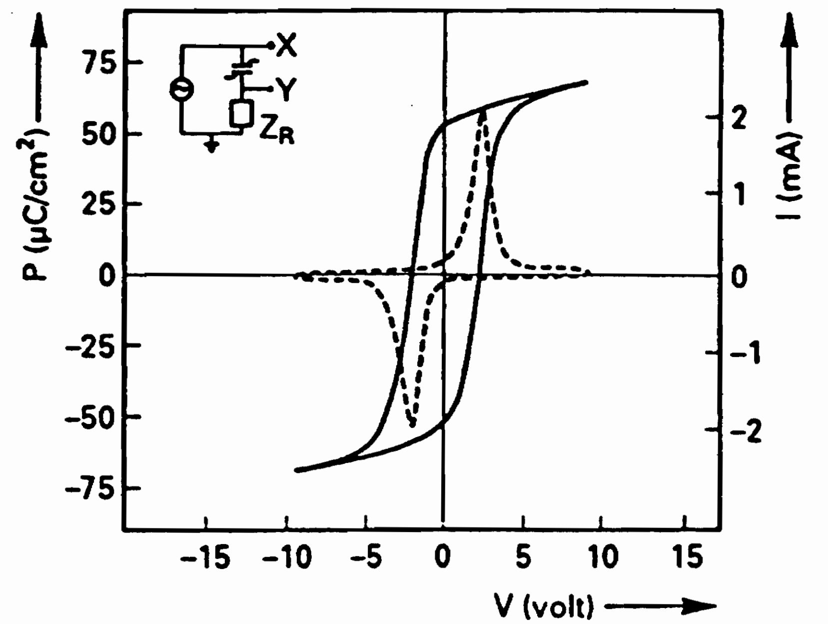


Fig 1.3 Hysteresis loop and Sawyer - Tower Circuit.

Z_R is a capacitor for hysteresis loop measurement.

Z_R is a resistor for current measurement.

measurement techniques which merit special discussion and shall be described in a later section.

The endurance, i.e., the ability to withstand a large number of switching cycles is a point of major importance for non-volatile memory applications. It is determined by the fatigue behavior, i.e. the degradation in ferroelectric properties (e.g. remanent polarization) caused by repeated polarization reversals. The fatigue is found to depend on the ferroelectric thin film properties, on the test conditions and on the nature of the electrodes. Although there is no real understanding of the degradation phenomena leading to fatigue, the optimization of the film and electrode properties has led to reported fatigue lifetimes exceeding 10^{12} switching cycles. Figure 1.4 shows fatigue in a standard ferroelectric capacitor.

Changes of properties like the remanent polarization of ferroelectric films occurring over a time scale of typically hundreds of seconds up to several years can be termed as aging, while retention refers to the time the ferroelectric capacitor can remember the data stored in it when the power supply is withdrawn. As is expected, retention and aging are found to be closely related to one another.

Fatigue and retention measurement tests are very time consuming in nature. In order to predict the long term reliability of a ferroelectric capacitor on the basis of short term accelerated tests, an in depth knowledge of the phenomena of fatigue and aging is essential.

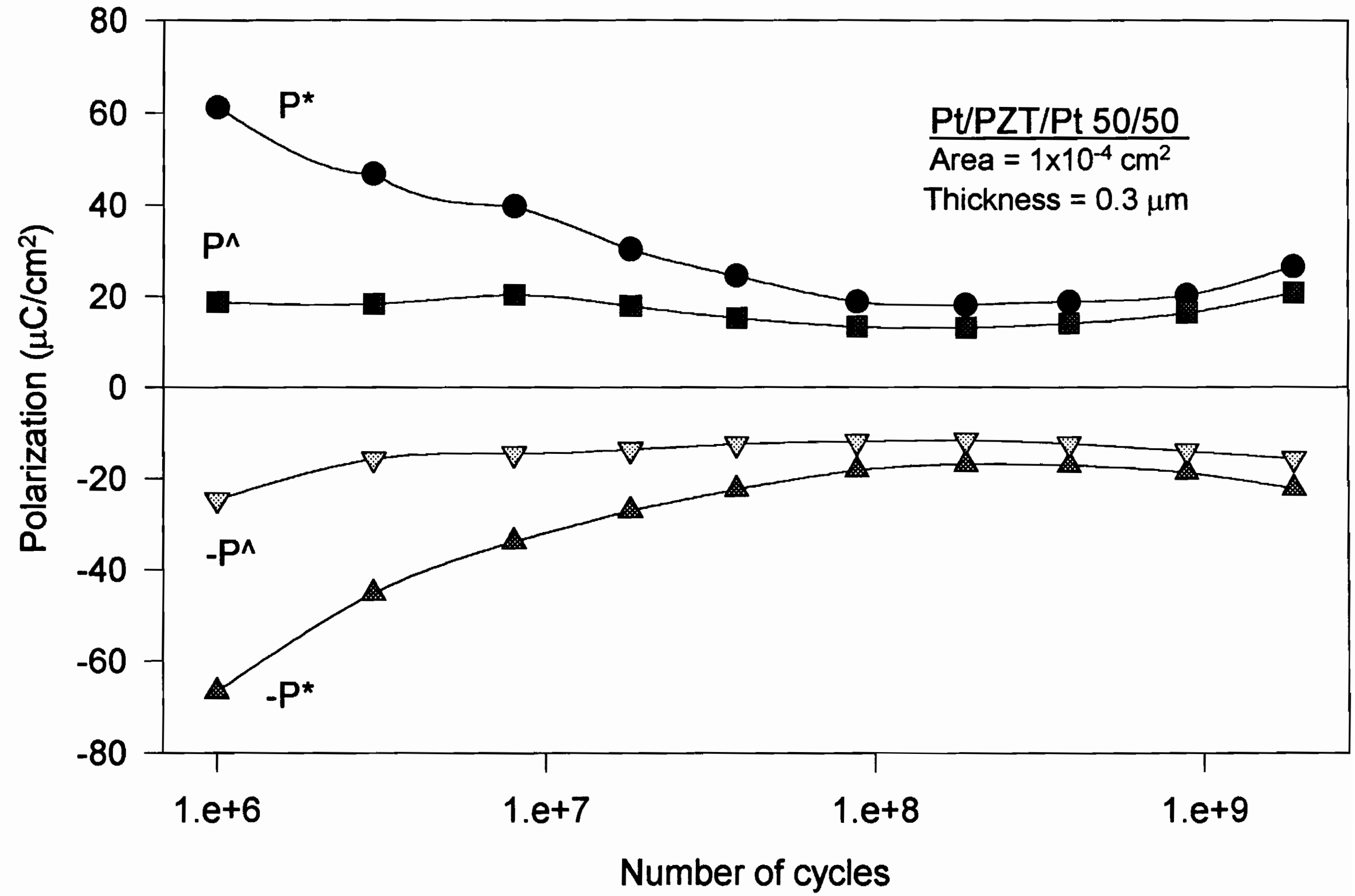


Fig 1.4 Fatigue in PZT capacitor

1.7 Different types of Ferroelectric memory

Ferroelectric memories can be realized in the form of different memory cell structures. The shadow memory cell [10] consists essentially of two parts (figure 1.5a). An SRAM cell, that can be a full fledged CMOS cell or an NMOS cell with polysilicon resistor loads, and two ferroelectric capacitors for the non-volatile data storage. These capacitors are isolated from the SRAM cell by MOS transistors. These isolating transistors, whose gates are controlled by the STORE lines, are off in the normal mode and the SRAM cell is operated without affecting the ferroelectric capacitors. During the STORE operation, which takes place before the power removal, and the RECALL operation, which takes place after the power removal, the two transistors are turned on. During the STORE operation, the data in the SRAM cell is written in the ferroelectric capacitors by switching their polarization in the appropriate manner. During the RECALL operation, this polarization sets the SRAM back to its original state. Due to the fact that these operations shall be performed a limited number of times, the fatigue requirements imposed on a ferroelectric capacitor incorporated in such a cell, are not very high. Though this memory structure is safe, it has the drawback of large cell size and it is thus only suitable for memories with a limited number of bytes.

Higher densities can be achieved by memory cells of the type [9, 10] shown in figure 1.5b. In this case, the ferroelectric capacitor forms an integral part of the memory cell. In fact this cell is a DRAM cell with a thin ferroelectric film as the capacitor dielectric. Since the dielectric constant of this material is high, this cell can also be used as a normal DRAM cell. The data in the cell will be stored as charge on the capacitor which has to be refreshed regularly. For a non-volatile memory the data in the cell will be stored by the directional polarization of the ferroelectric layer which also eliminates the need for

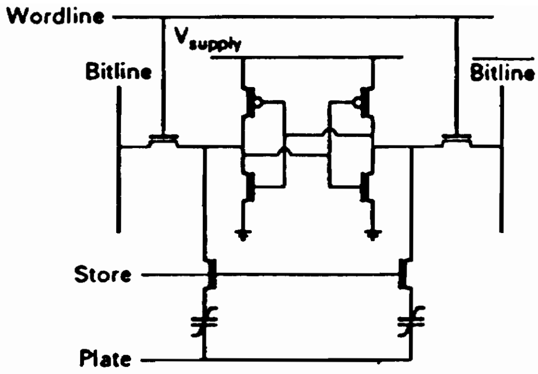


Fig 1.5a Ferroelectric shadow memory cell.

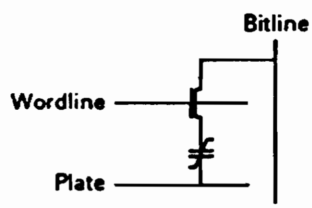


Fig 1.5b DRAM type ferroelectric non-volatile cell.

a refresh cycle. This cell which allows very high densities puts rather stringent requirements on the ferroelectric layers, especially with respect to the endurance. The polarization of the ferroelectric layer has to be switched for reading as well as writing. Therefore a large number of polarization reversals has to be guaranteed. Memories that allow the selection of either the DRAM mode of operation or the non-volatile mode are very useful if a limited endurance has to be specified [12]. The detection of the written data in a memory cell is commonly done via a comparison with a reference cell. This reference cell will be accessed many more times than each memory cell. So for reliable reading, the fatigue and the aging characteristics have to be independent of the number of accesses to the cells or else other detection principles have to implemented. Mostly these will increase the access time. Reference cell problems can be avoided by using two memory cells for storing one bit. In one cell the data and in the other one the inverted data can be stored. The detection of the written data (reading the cell) is done via a comparison of the contents of both cells. Now both the cells are always accessed together and the reading is done in a differential way so that the absolute values are not so important anymore. The two memory cells per bit concept is also often used to increase the read speed of the memory. Of course, this is achieved at the cost of some extra space.

1.8 Hysteresis measurement using RT66A (Standardized Ferroelectric Test System, Radiant Technology, Inc.)

Figure 1.6 shows the basic block diagram of the RT66A standard ferroelectric test system [13]. The CHARGE software of the RT66A standard ferroelectric test system performs the hysteresis measurement.

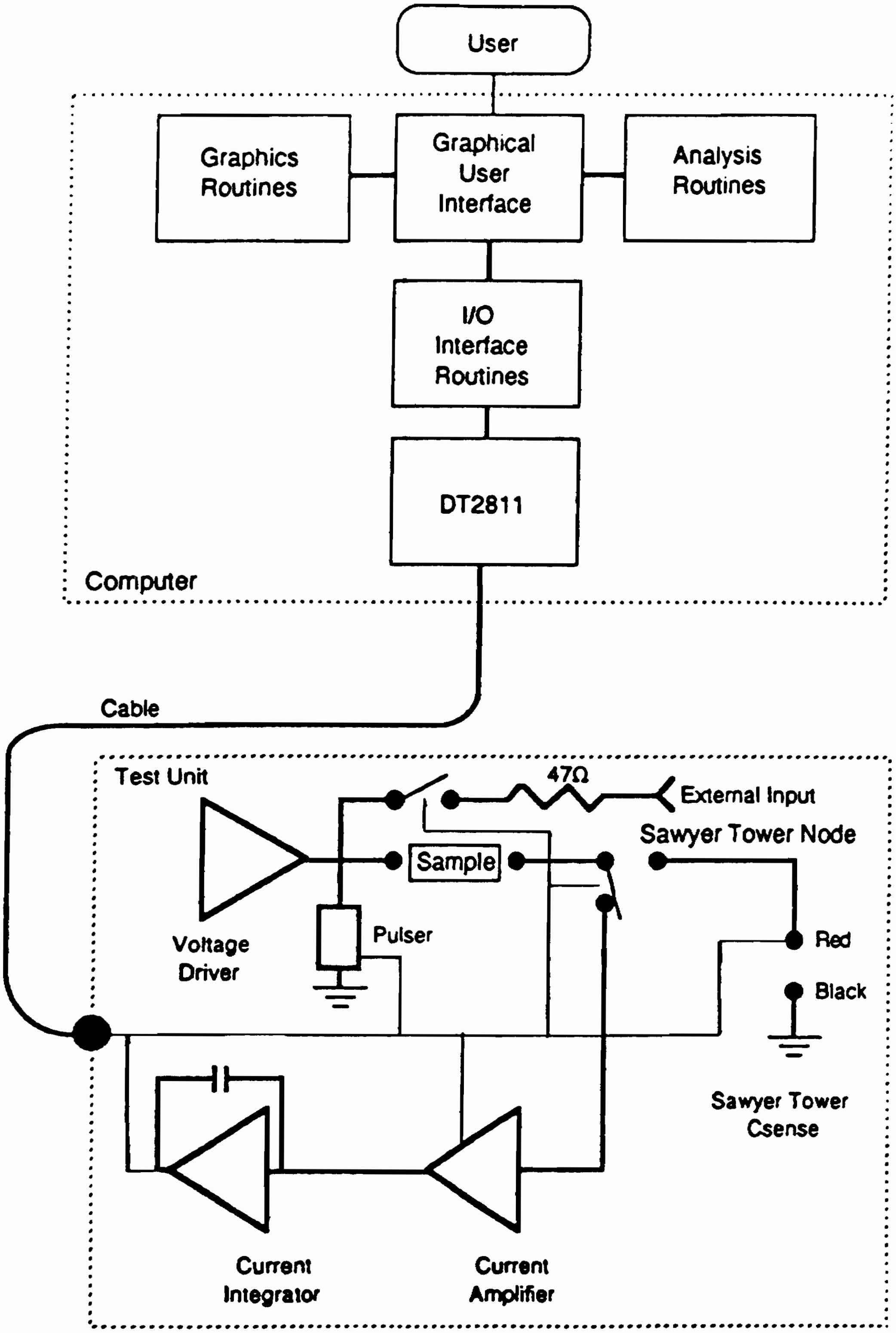


Fig 1.6 Block diagram of RT66A Standardized Ferroelectric Test System Set-up [13].

1.8.1 User selections:

Among other parameters, the user can select the following features of the measurement signal:

Vmax (Peak voltage of the drive signal), Direction of hysteresis (positive or negative), and the number of discrete voltage steps in the hysteresis.

1.8.2 Signal Description:

The system generates a single triangle wave beginning at 0 volts and stepping in discrete voltage intervals to the assigned Vmax, then back to 0 volts, then to -Vmax, and then back to 0 volts. Vmax can be either positive or negative. The size of the voltage step used is calculated using the following equation:

$$|V_{step}| = |V_{max} * 4/(\text{Number of hysteresis loop points})|$$

The integrating capacitor in the test unit is shorted before the hysteresis test is run. One hysteresis is run to preset the capacitor to the appropriate remanent polarization. After a 1 second waiting time, a second hysteresis is run while the integrating capacitor collects charge from the virtual ground. The voltage at the output of the integrating capacitor is measured by an A/D converter after each voltage step. An example test signal is shown in figure 1.7.

Example:

Signal Plot:

Vmax	=	5.00 V
Number of Steps	=	200
|Vstep|	=	100 mV
Seconds/Step	=	1.1 ms in slow mode.
Seconds/Loop	=	~220 ms

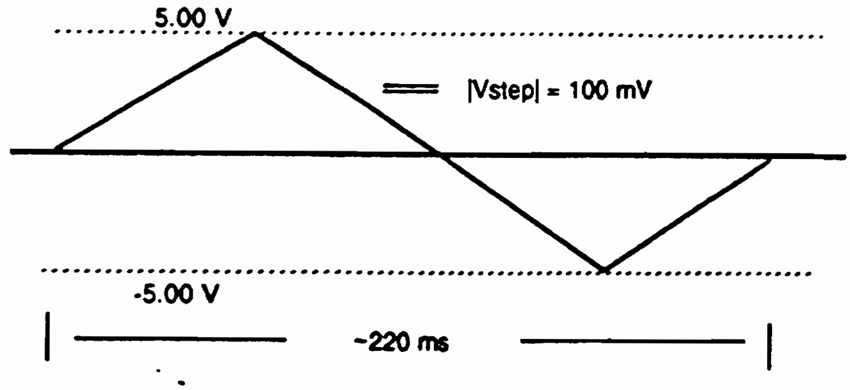


Fig 1.7 An example hysteresis test signal [13].

Example:

Signal Plot:

Vmax = 5.00 Volts

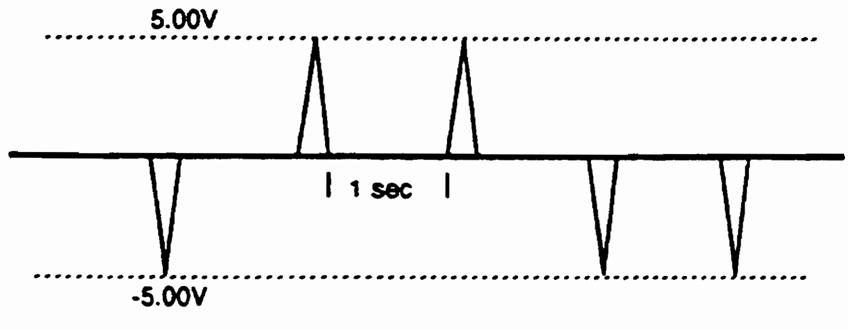


Fig 1.8 An example pulse polarization measurement signal [13].

1.9 Pulse polarization measurement

In an actual memory circuit, the READ and WRITE operations are carried out by voltage pulses applied across the ferroelectric capacitor. During the READ operation, switching and non-switching currents obtained by the application of appropriate pulses are converted into voltage and are used for sensing the stored data.

In order to simulate the actual read/write operations and to estimate the resulting switched and unswitched polarizations, a special measurement technique called Pulse Polarization Measurement Technique is adopted. The details of this technique, as implemented in the RT66A ferroelectric test system, are discussed below.

Basically, the pulsed polarization test consists of a sequence of five triangular pulses, each pulse being separated from the previous one by 1 second. The polarity of the various pulses is determined by a user defined quantity called Vmax. If Vmax is positive, the pulse sequence is of one type and if it is negative, the pulse sequence will be of an exact complementary type.

Pulse #1: -Vmax

Pulse #2: Vmax

Pulse #3: Vmax

Pulse #4: -Vmax

Pulse #5: -Vmax

1.9.1 Measurement Signal Definitions

Pr(X) = remanent polarization state at zero volts after application of X volts.

Ps(X) = the polarization state at X volts.

P* = Ps(Vmax) - Pr(-Vmax): The polarization transferred out of the capacitor traversing from zero to Vmax volts when the capacitor starts at Pr(-Vmax).

P*r = Pr(Vmax) - Pr(-Vmax): The polarization remaining out of the sample capacitor after returning to zero volts from Vmax, when the capacitor starts at Pr(-Vmax).

P^ = Ps(Vmax) - Pr(Vmax): The polarization transferred out of the capacitor traversing from zero to Vmax volts when the capacitor starts at Pr(Vmax).

P^r = Pr(Vmax) - Pr(Vmax): The polarization remaining out of the sample capacitor after returning to zero volts from Vmax, when the capacitor starts at Pr(Vmax).

1.9.2 Measurement

The first pulse presets the sample capacitor to Pr(-Vmax). For the next four pulses, the integrating capacitor is zeroed out prior to each pulse. A measure of the voltage across the integrating capacitor is made at the top and bottom of each pulse. The parameter measured at each point is shown below.

Pulse #	Voltage Applied	Parameter Measured
1	-Vmax	-
1	0	-
2	Vmax	P*
2	0	P*r
3	Vmax	P^
3	0	P^r
4	-Vmax	-P*
4	0	-P*r
5	-Vmax	-P^
5	0	-P^r

Figure 1.8 shows an example of pulse polarization measurement signals while figure 1.9 explains the various pulse polarization measurement quantities in relation to a hysteresis curve.

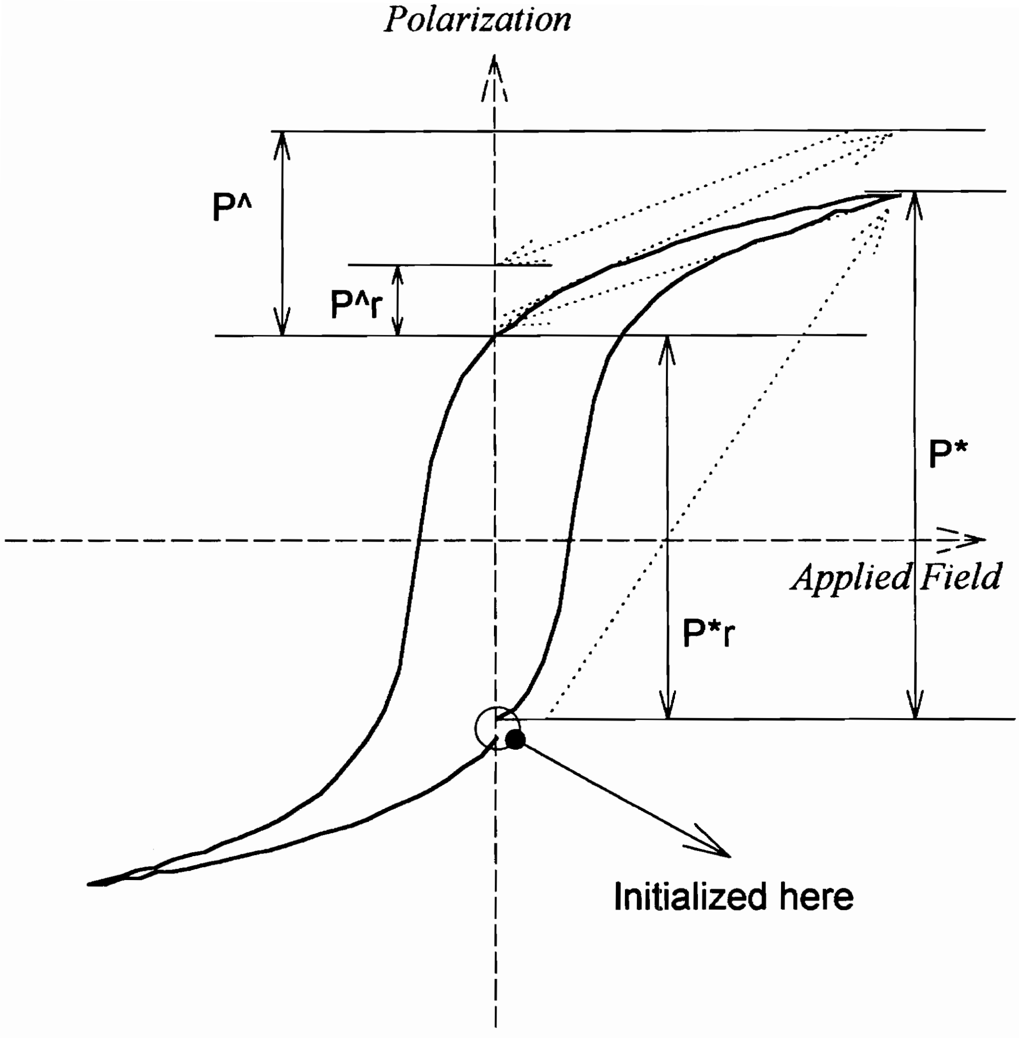


Fig 1.9 Pulse polarization measurement parameters in relation to the hysteresis curve.

Chapter II. Depolarization and Imprint

2.1 Introduction

The prime manifestation of degradation in a metal-ferroelectric-metal (MFM) capacitor is the progressive reduction in the remanent polarization values (+Pr and -Pr) with number of read/write cycles. The detection circuitry associated with any memory cell imposes certain requirements on the characteristics of the MFM capacitor. From an engineering standpoint, the design of the data read-out circuit, including the sense amplifier, poses the biggest challenge. The unipolar data read-out is carried out in one of the following two ways.

i) Sensing the difference in the voltages in the bit lines corresponding to the data "1" and the data "0", that is, sensing the difference between the switchable (P*) and the nonswitchable (P^) polarizations [14],

or,

ii) Sensing the difference of bit line voltage between the data "1" and a pre-defined reference level or the data "0" and the reference level.

In the first case, the difference between the switchable polarization and the nonswitchable polarization should be greater than a minimum threshold value known as the noise margin. In the second case, two different noise margins have to be defined - one for the detection of a "1" and another for a "0". These noise margins should remain at the minimum value determined by the actual temperature range, voltage range, read/write cycles, data retention time, and other factors.

Thus, the noise margin requirement is directly related to the minimum value requirements of the switchable and nonswitchable polarizations of an MFM capacitor [14]. If the degradation of the capacitor progresses so much that the noise margin requirements are not met, read failure will occur and the memory cell will be rendered virtually useless.

Thus, at all costs, the detection circuitry should be able to distinguish between a stored "1" and a stored "0". This ability may get destroyed by simple fatigue. But it has been observed that even if the capacitor is not fatigued to a great extent, it might show a tendency to depolarize in one particular direction and hence lose the stored information. Researchers prefer to call this "imprint" - one particular state - "1" or "0" - is being etched into memory by writing it over and over again. As a result, the memory cell may develop a tendency to fail to accept the opposite state when that state is written. In other words, after repeatedly writing "1"s in a memory cell, if an attempt is made to write a "0", the capacitor may fail to store it under certain operational conditions.

2.2 Reported observations of Imprint

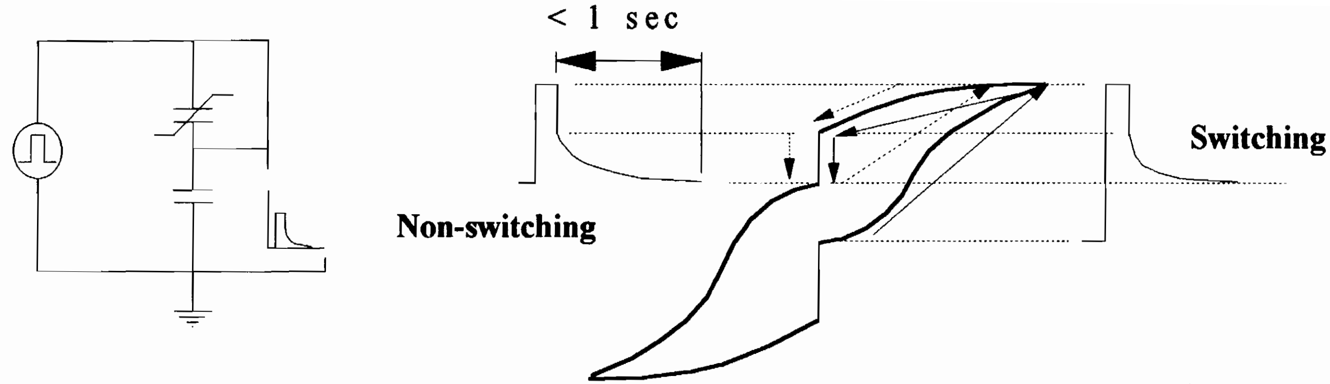
Unlike fatigue and retention, there is no single unique test scheme to evaluate imprint. Several researchers have proposed several different ways to observe imprint. However, all the different ways show us that rapid depolarization, i.e. fast decay of polarization is the main reason behind loss of information. This depolarization can be enhanced by certain circumstances like repeated writing of one particular state, or by temperature or field. This increased depolarization, if extreme, can lead to read/write failure.

N. Abt [15] had reported that simply applying two pulses of the same polarity produces a remanent polarization in a PZT capacitor. This "anomalous remanent polarization", which they called ΔP0 (figure 2.1), is found to increase when a large number of pulses of a polarity opposite to the ΔP0 measuring pulses are applied to the capacitor. This ΔP0 can be linked to depolarization due to the fact that in between the two measuring pulses of the same polarity, a rapid decay of polarization occurs and this results in a remanent polarization when the second pulse is applied. Abt observed this ΔP0 even without any external stress application and called the resulting phenomenon as imprint. [In the nomenclature followed in the present work, ΔP0 is equivalent to P^r].

R. Nasby et. al. [16] had observed that after fatiguing a PZT capacitor, the depolarization significantly increased. They called it "Rapid Depolarization" (figure 2.2). J. Benedetto et. al.[17] observed the same effect by applying single sided pulse train and called the phenomenon "fast decay" (figure 2.2). Recently, T. Mihara et. al. [14] reported observing imprint in sol-gel PZT by pre-fatiguing a sample by applying a number ($\sim10^7$) of bipolar pulses and then applying single sided pulses under various stress conditions (figure 2.2).

2.3 Proposed mechanisms of Imprint

Recently, imprint has become the subject of tremendous research activity due to the fact that it represents the single most important failure mechanism that a ferroelectric memory element might suffer. However, the precise reasons behind the phenomenon of



N. Abt et al :

Pulse measurement with no external stress and named the decay - *"imprint"*

Fig 2.1 N. Abt's [15] observation of "anomalous remanent polarization".

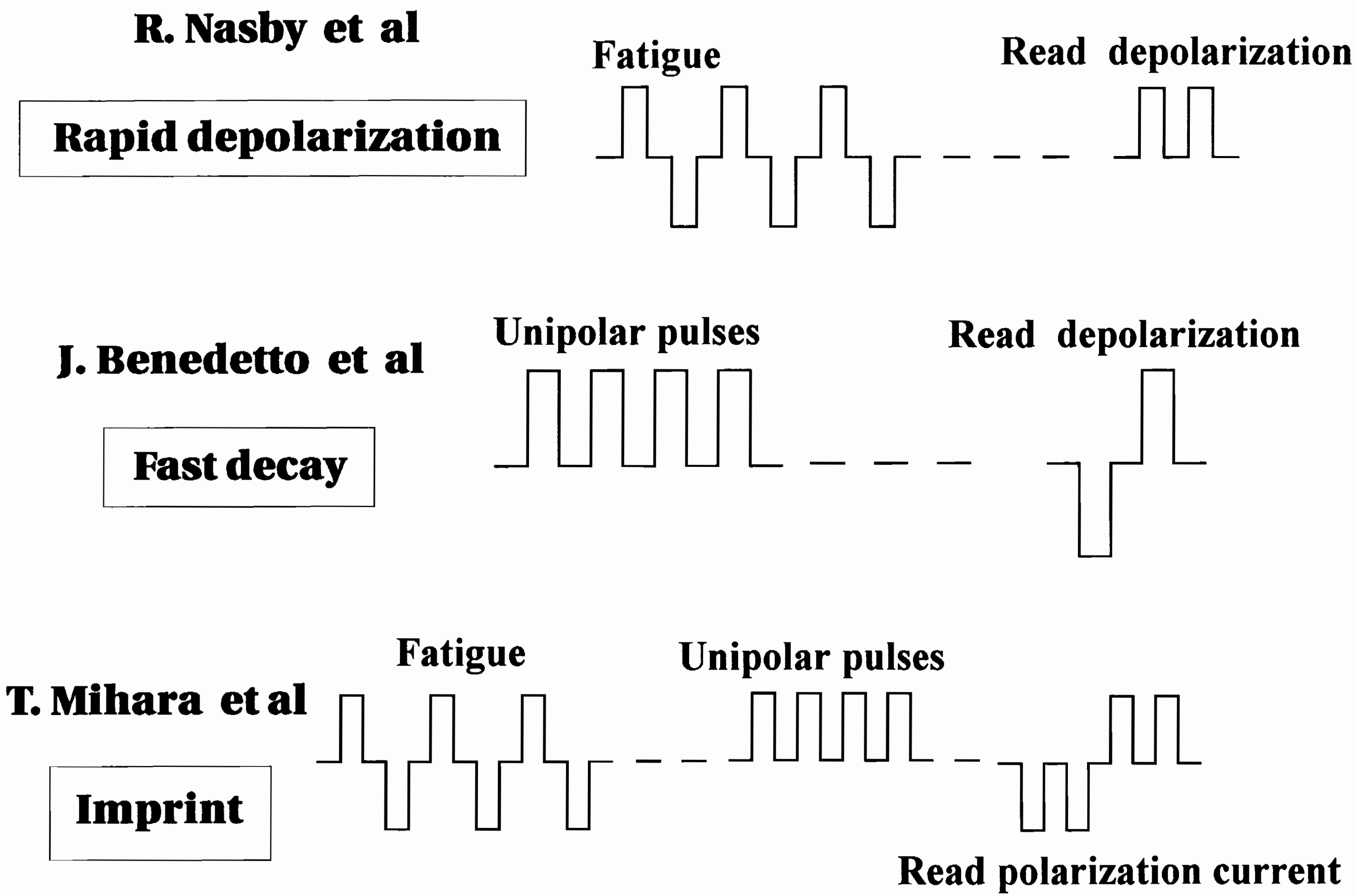


Fig 2.2 Test Signals for accelerated imprint

imprint are yet to be ascertained. The reasons that are suggested in the literature are mostly speculative in nature. Among the various reasons cited the following are of interest:

1. Thermal energy may randomize those domains which are sufficiently small (~ 100 Angstroms) such that the thermal energy is comparable to their domain energy [15].

2. In the absence of an external field, depolarization may occur due to film stress driven surface energy of domains may exceed the domain's volume energy. This may cause the domains to collapse. However, in order to explain the fact that the depolarization is not equal in both directions, it is suggested that the stress vector adds differently to the two opposite directions of applied field [15].

3. For compositions close to the morphotropic phase boundary, an applied external field may cause phase transformation from tetragonal to rhombohedral phase. The rhombohedral phase is responsible for contributing to polarization. However, withdrawal of external field might cause reversal of the phase and hence depolarization [15].

4. Application of external field may cause internal space charge build - up. This space charge polarization could add to the total polarization which might vanish with the withdrawal of the field as then the space charge may disperse. Additionally, the space charge field may cause a partial polarization reversal of the spontaneous polarization [17].

5. Applying a large number of unipolar pulses may cause rotation of new 90^{o} domains at high temperatures. This in turn will cause a shift in the hysteresis curve due to

internal field formation by asymmetric potential barrier across the new domains. While this will result in higher P* and P^ in one direction, it will lead to a reduction in both P* and P^ in the opposite direction. Charges trapped in the space charge layer will cause an internal field and this will cause a shift in the hysteresis loop and hence asymmetrical switching properties [14].

Apart from the above mechanisms, a few others may also be plausible. When an external field is applied in one direction, most of the domains switch in that direction, while a few are oriented in the opposite direction. When this field is reduced to 0, the remanent polarization (Pr) creates an internal field (Ei) in a direction opposite to the previously applied field. This field may cause some previously switched domains to switch to the opposite direction (i.e. direction of Ei). Thus, this internal field assists in the depolarization [18] (figure 2.3).

A linearly capacitive interlayer is formed due to the interfacial space charge build-up. This may be an important reason for the depolarization. This can be verified by the simulation of the linearly capacitive layers by means of an external linear capacitor of approximately the correct value [18] (figure 2.4).

2.4 The Imprint process

In a virgin sample, application of an external field of sufficient value results in the alignment of a majority of the domains in the direction of the applied field (figure 2.5) [18]. A few domains, however, remain directed in the opposite direction. Upon removal of the external field, the net polarization reduces and stabilizes to a value Pr (<Ps). This

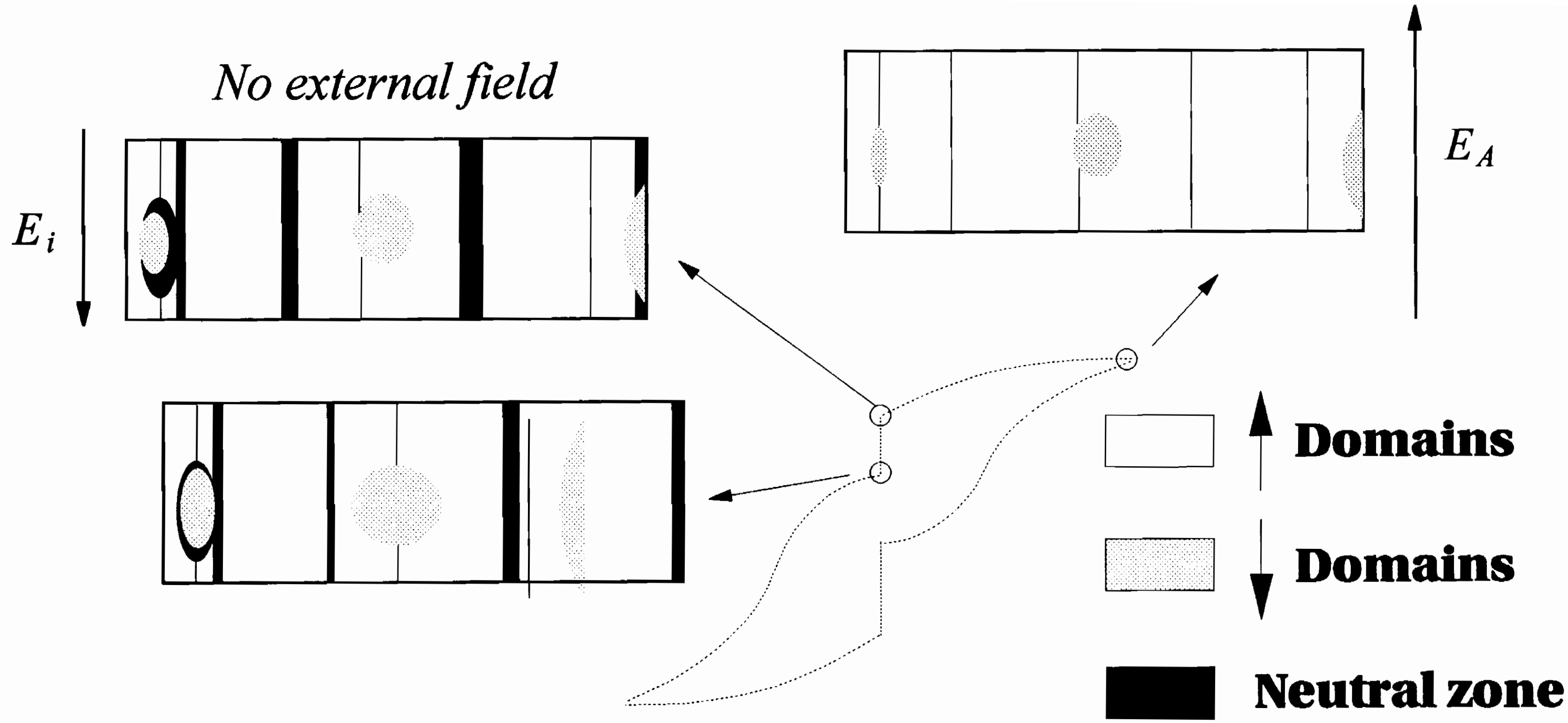


Fig 2.3 Polarization reversal due to internal field generated by remanent polarization.

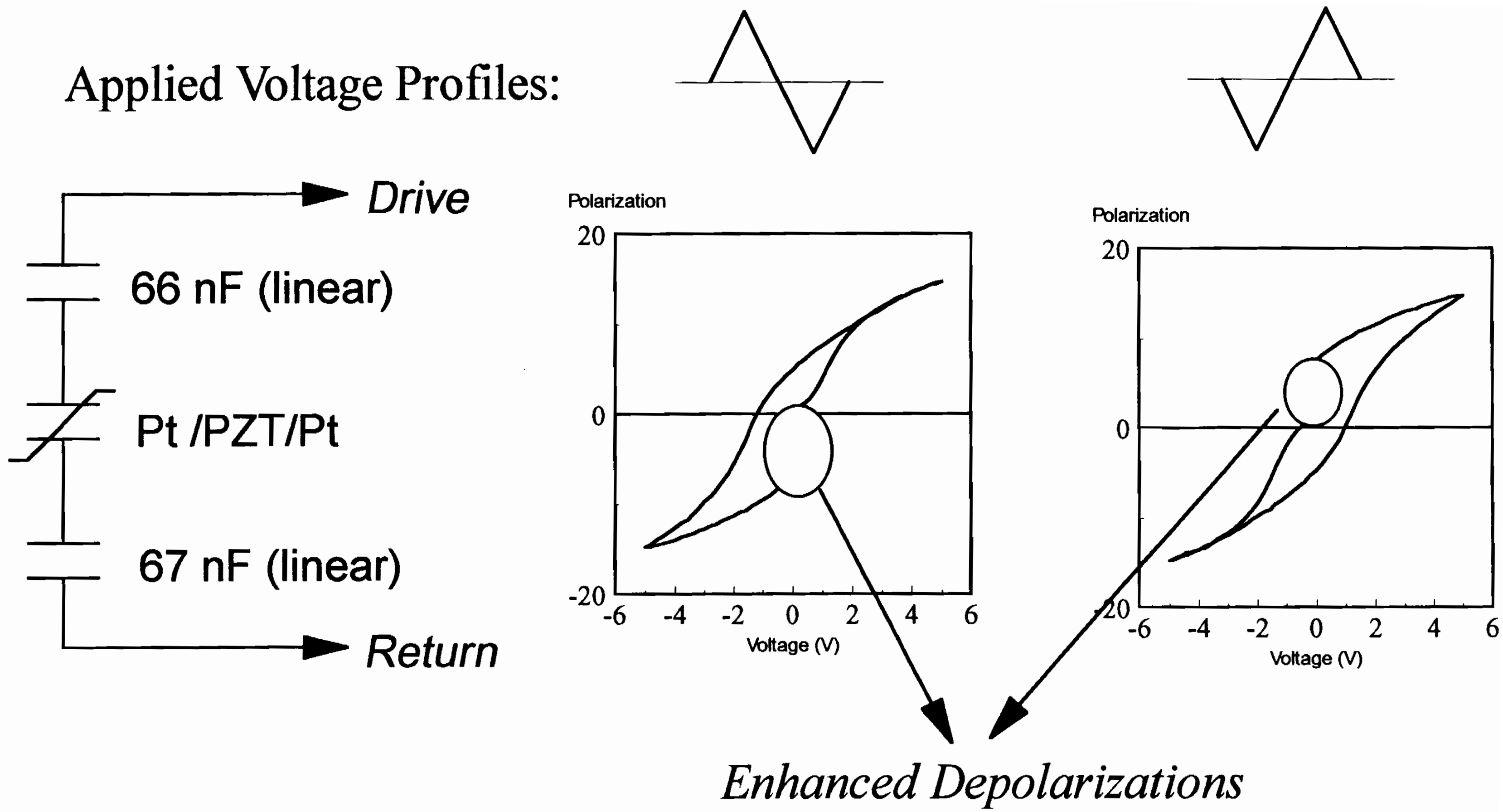


Fig 2.4 Linearly capacitive interlayer or interface

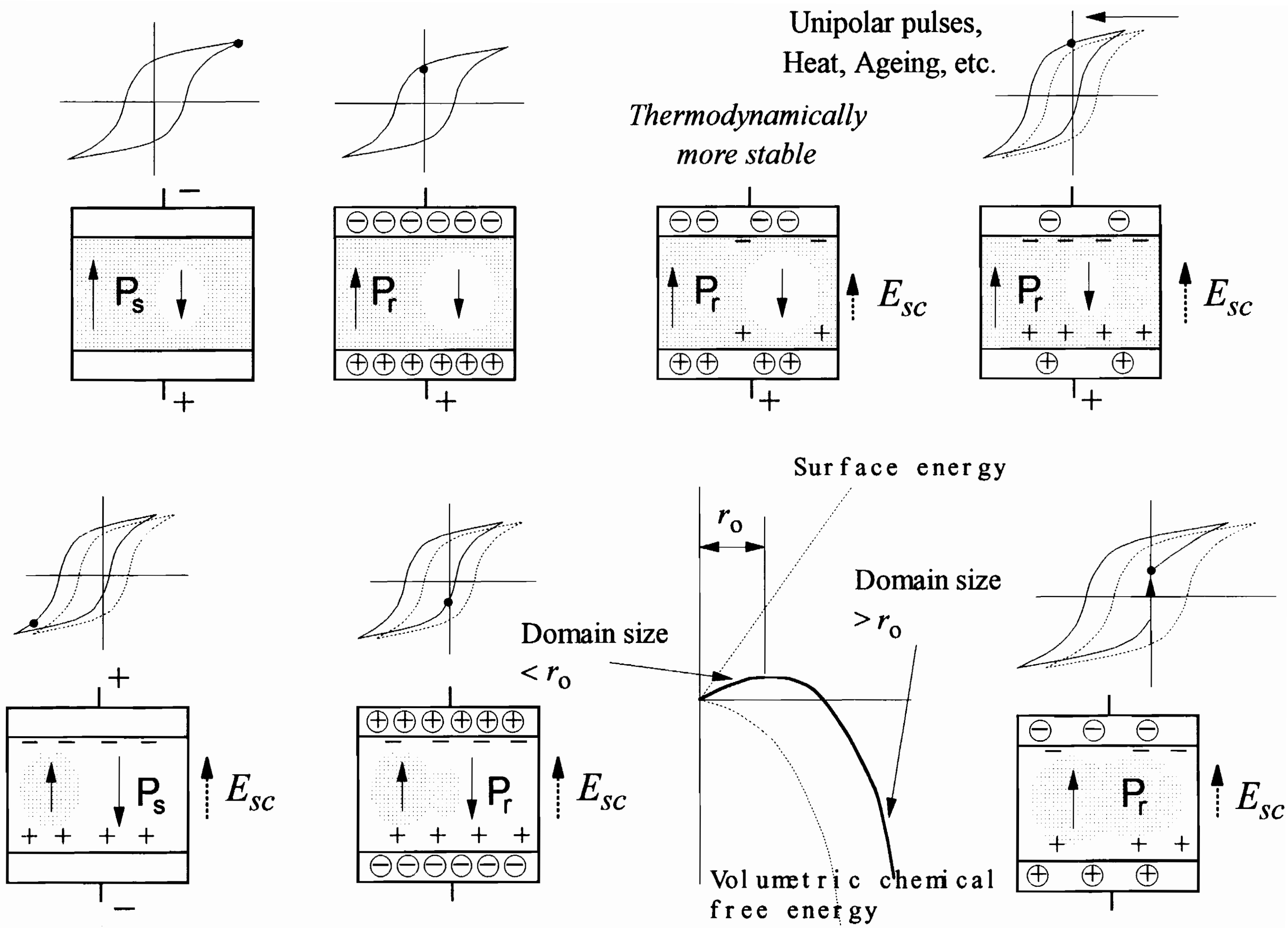


Fig 2.5 Summary of Imprint process

means that some more domains are switched back to the opposite direction. Charges are induced in the electrodes appropriately to maintain the electrical neutrality of the whole M-F-M system.

These charges that accumulate in the electrodes can also exist in the metal - ferroelectric interface. In fact, it has been found that such a distribution of charges may be thermodynamically more stable than charges exclusively on electrodes. These charges that may exist within the interface will give rise to an electric field internally. This is designated as E_{SC} and it acts in the same direction as Pr.

This field E_{SC} can be increased in magnitude under certain circumstances like application of a large number of unipolar pulses in the same direction as E_{SC}, heating the sample etc. That the internal field is created and increased in magnitude, can be seen from the progressive shift in the hysteresis loop of the MFM capacitor. It is obvious that since Esc acts in the direction of Pr, it will cause a few oppositely oriented domains to switch in the direction of Pr.

Now, if an external field is applied across the MFM capacitor in a direction opposite to the previously applied field, then a majority of the domains will be switched in its direction creating a corresponding Ps. However, there are a small number of domains who will not respond to this external field and remain oriented in their previous direction These domains will be supported by the in-built space-charge field E_{SC}.

If the external field is now withdrawn, the remaining polarization in the sample is Pr (<Ps). Some of the domains which were oriented in the direction of Pr (or Ps) will now have reverted back to the opposite direction due to the withdrawal of the applied field. These opposite domains are still supported by the space-charge field E_{SC}. If these oppositely oriented domains acquire sizes greater than or equal to the critical size for domain growth, then nucleation and growth of these domains will follow. The critical

domain size is determined by surface energy and volumetric free energy. This growth of domains will take place at the cost of the domains oriented along the direction of Pr. As a result, Pr will go down drastically and a majority of the domains will be directed opposite to it. Thus the net polarization of the capacitor will be reversed.

This phenomenon is very aptly called "imprint" because the MFM capacitor behaves as though the previous state were "imprinted" on it, preventing it from registering the opposite state.

2.5 Imprint measurements

Though imprint may be called the most critical reliability issue in MFM capacitors, it is not common to observe complete polarization reversal under ordinary conditions. Special circumstances, like increased temperature, number of read/write cycles or magnitude of read/write pulses are important factors in causing the MFM capacitors to exhibit enhanced degradation.

While the maximum temperature that a modern day integrated circuit may have to operate under is around 85°C, and the supply voltages are also well regulated and within well-defined upper bounds, the special circumstances are necessary to enhance degradation and perform accelerated tests. Test acceleration is required not only to save time or determine the approximate "life" of the device, but it might also lead us to understand better the exact mechanisms that result in degradation of any kind. Apart from the test conditions, another factor is of some importance. This is the method of preparation of the capacitor film. Most of the imprint studies reported were based on sol-gel samples. It would definitely be of interest to see how samples prepared under different processes/methods would behave under identical test conditions.

2.6 Samples

The test samples chosen for this study were made by two different methods: (1) Metal Organic Decomposition (MOD) (which is similar to sol-gel) and (2) sputtering. All samples had the same compositions: $PbZr_xTi_{1-x}O_3$ with x = 0.5 and 10% excess PbO.

Films of four different thicknesses were made by the MOD method. These thicknesses were: 0.239 μm, 0.359 μm, 0.473 μm and 0.588 μm. The sputtered sample had a film thickness of 0.35 μm. The MOD samples had top electrode areas of 4.85×10^{-4} cm^2 while the sputtered sample electrodes were a little smaller: 1×10^{-4} cm^2. Measurements were taken at four different temperatures, viz., 25°C, 50°C, 75°C and 100°C.

2.7 Test signals

The test signals were applied according the following scheme:

At first, the capacitor under test (CUT) was fatigued with 10^8 bipolar pulses (100 seconds @ 1 MHz). Thereafter, it was subjected to a cumulative 1.888×10^9 cycles of negative unipolar pulses and then 1.888×10^9 cycles of positive unipolar pulses. The unipolar pulses were applied for 1888 seconds (31minutes, 28 seconds) @ 1 MHz.

The signal generator used to supply the pulses was a HP 8116A pulse/function generator. This generator has a pulse magnitude upper/lower limit of +8V/-8V. This was crucial in determining the field to be applied to the samples. The field was chosen as 136 kV/cm since the thickest sample was 0.588 μm in thickness and we could apply a maximum of only 8 V across it. This field of 136 kV/cm was applied across both the MOD and sputtered capacitors and samples of all thicknesses.

2.8 Observation of imprint

The observation of imprint can be both qualitative and quantitative. The RT66A test system allows us to make a qualitative judgment as to the extent of depolarization that can occur in an MFM capacitor. During hysteresis measurement, the software, CHARGE, initializes the MFM capacitor to the appropriate Pr by applying a pulse of suitable polarity. After the application of this initialization pulse, the software waits for 1 second. During this wait period, the capacitor undergoes some depolarization. This is very useful in making a qualitative idea about the extent of rapid depolarization that may occur in the capacitor.

The quantitative estimate can be made from the parameters +P^r and -P^r which are two of the eight parameters measured by the pulsed polarization measurement. Ideally (in case of no depolarization), P^r should be equal to 0. But in between the pulses 1 and 2, the time lapse is 1 second, which is sufficient for some depolarization to take place. So, when pulse 2 is applied, the capacitor follows the double arrows and moves from Pr' to Ps to Pr. Thus, there is a net remanent polarization of magnitude Pr - Pr'. This gives rise to a non-zero P^r value. Furthermore, it is seen that larger the depolarization, larger is the value of P^r. Thus, we can have a quantitative estimate of the depolarization by means of the parameter P^r.

2.9 Correlations among internal field, shift in hysteresis curve and depolarization

Figure 2.6 summarizes the effect of an internal field on the hysteresis curves measured by the CHARGE option of RT66A. This causes the depolarization to be enhanced in one direction compared to the other.

2.10 Imprint at various temperatures

The extent of imprint observed in various capacitors at various temperatures are presented in figures A-1 through A-8 (Appendix).

2.10.1 Initially:

The depolarization in the MOD and sputtered virgin samples gradually increase with temperature. This may be due to increased space charge accumulation at higher temperatures (figure 2.7).

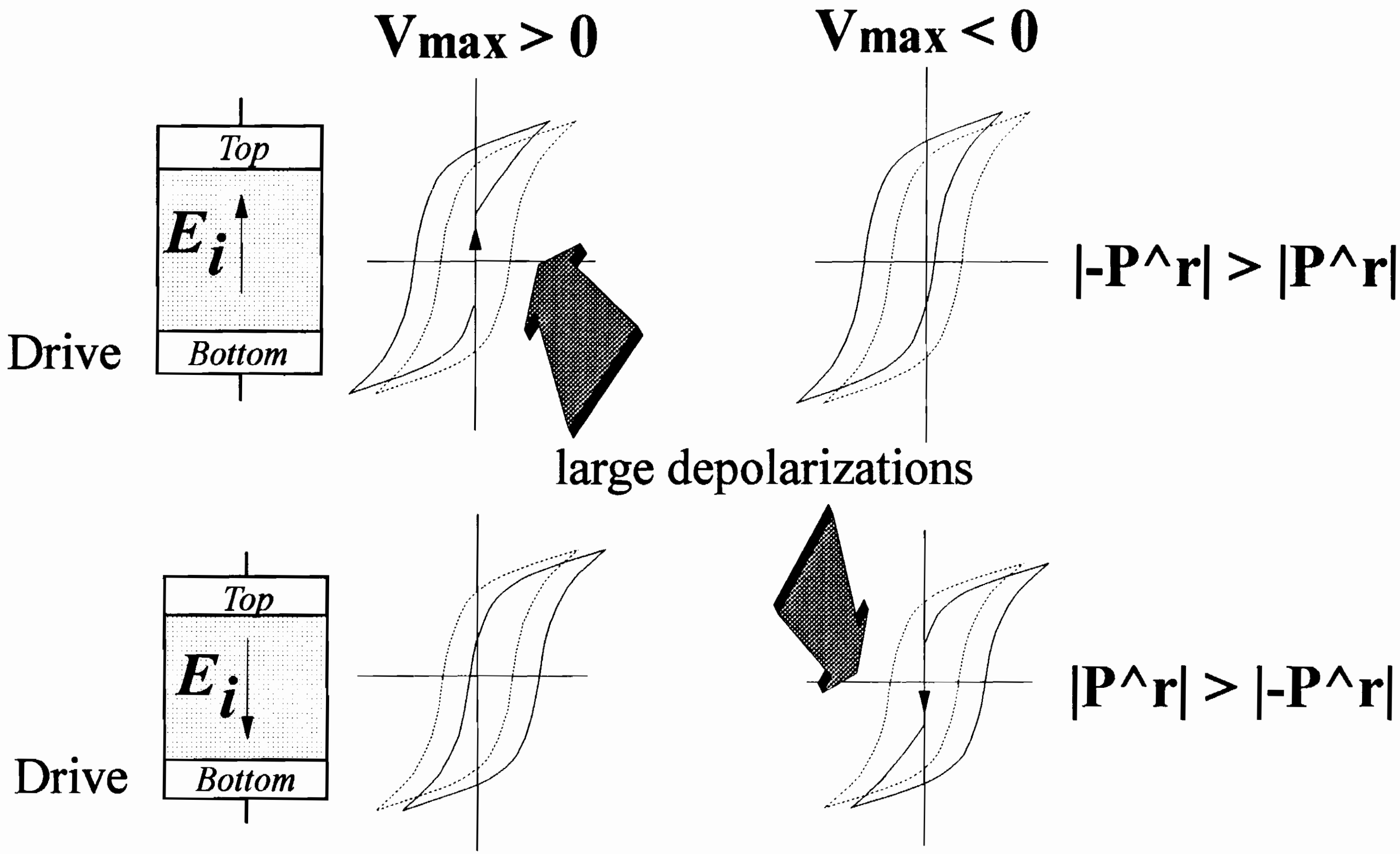


Fig 2.6 Correlations among internal field, hysteresis and depolarization.

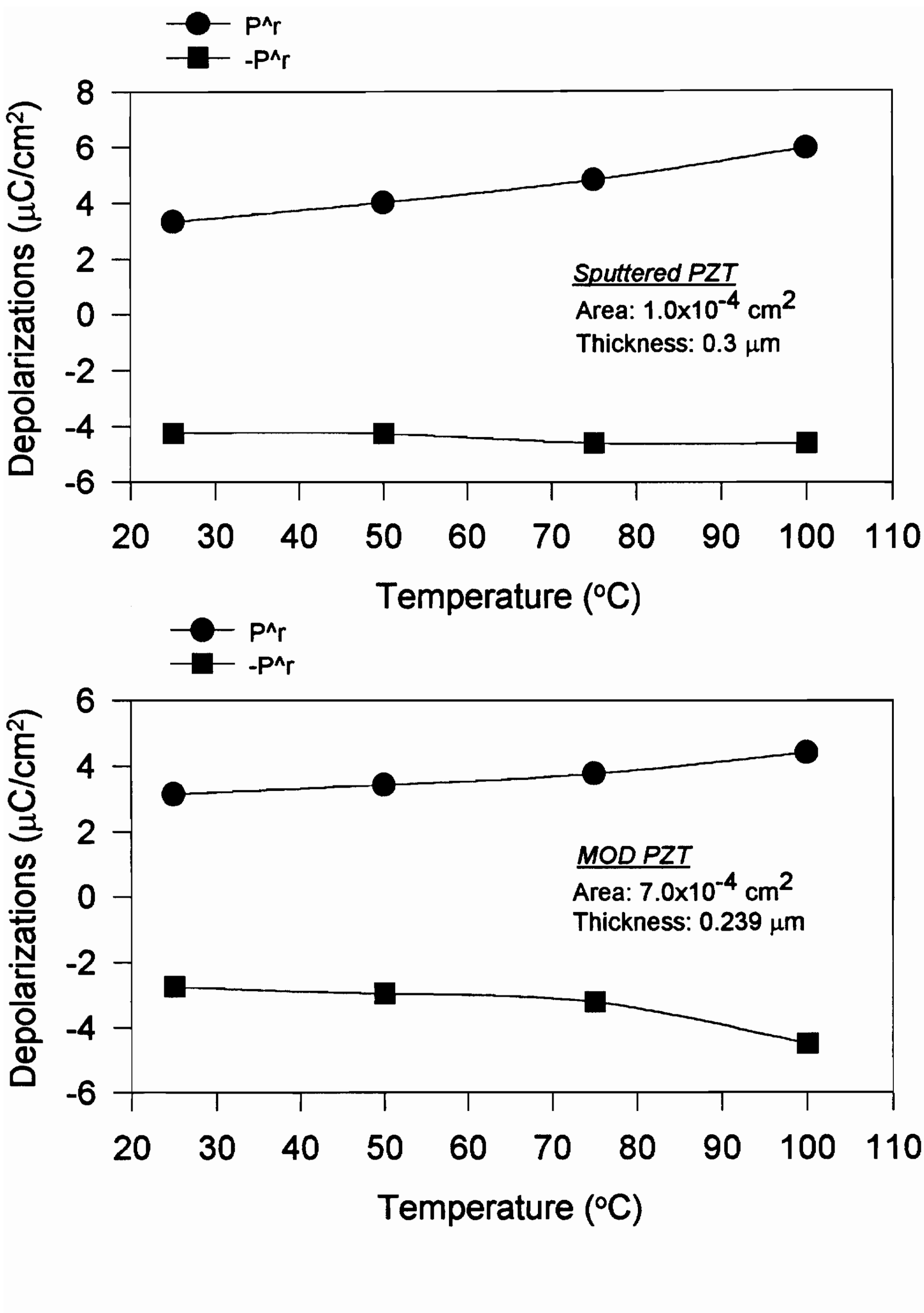


Fig 2.7 Sputtered PZT, MOD PZT, initially.

2.10.2 After Fatigue:

It is generally assumed that fatigue and temperature both cause an increase in the space charge accumulation, thereby contributing to an increase in depolarization. But the mechanism by which each of them cause the space - charge accumulation may not be the same. This is suggested by the two figures (after fatigue). Both in sputtered and in MOD PZT capacitors, the depolarization is less at 50^{O}C than 25^{O}C, after fatigue with bipolar pulses. However, at much higher temperatures the depolarization is found to be higher. From this, it may be inferred that the two mechanisms of fatigue and temperature are not identical. In fact, at reasonably low temperatures, they might oppose one another. However, at higher temperatures, one of them dominates (figure 2.8).

2.10.3 After Negative Pulses:

Similar to fatigue with bipolar pulses, negative pulses also show the curious effect when observed over various temperatures. Depolarization does not necessarily increase with temperature even in this case. In fact it shows a tendency to decrease at around 50^{O}C and then increase at higher temperatures. Further studies are required to confirm this effect (figure 2.9).

2.10.4 After Positive Pulses:

The effect of temperature is very similar to the previous two cases (figure 2.10).

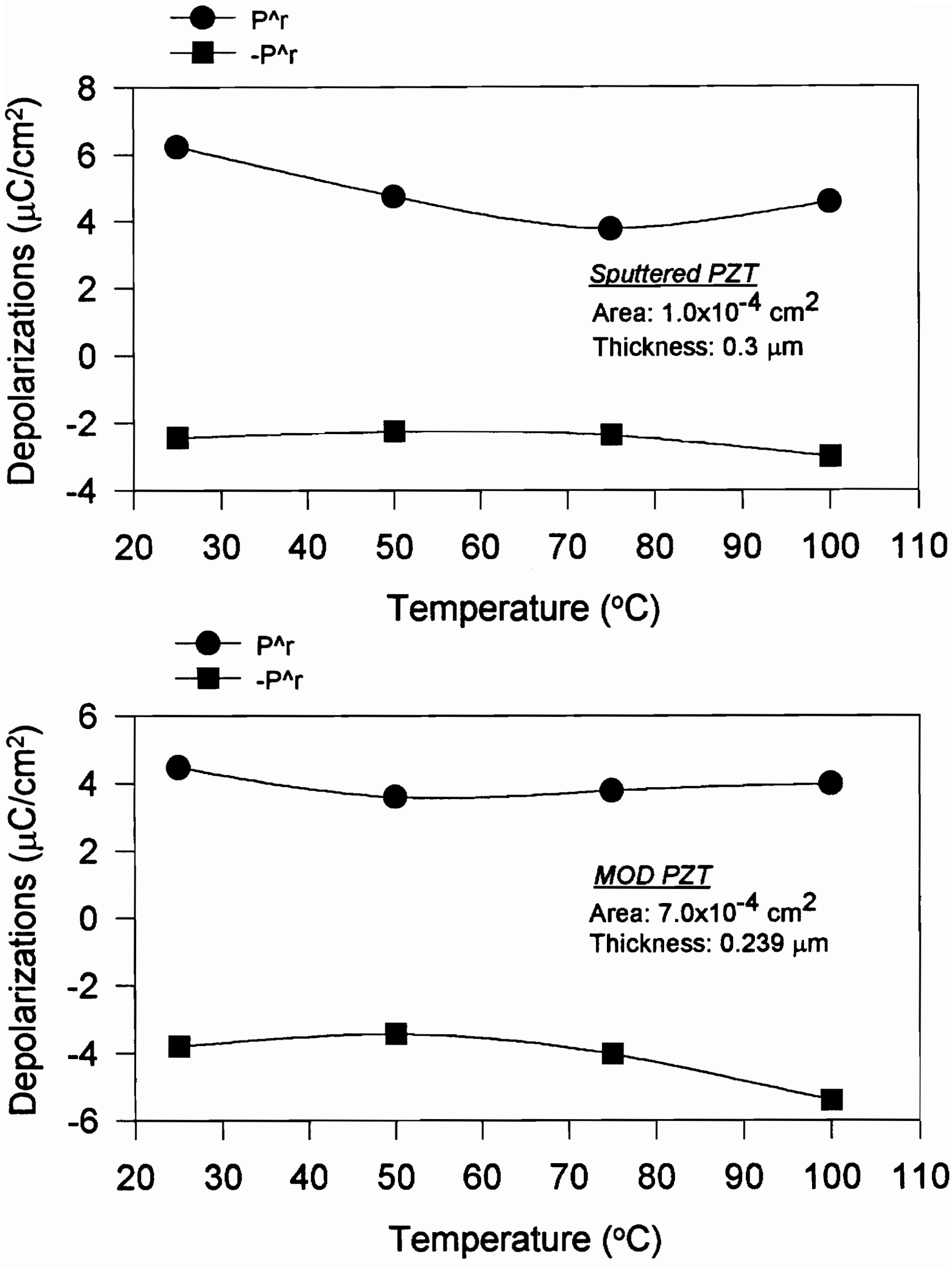
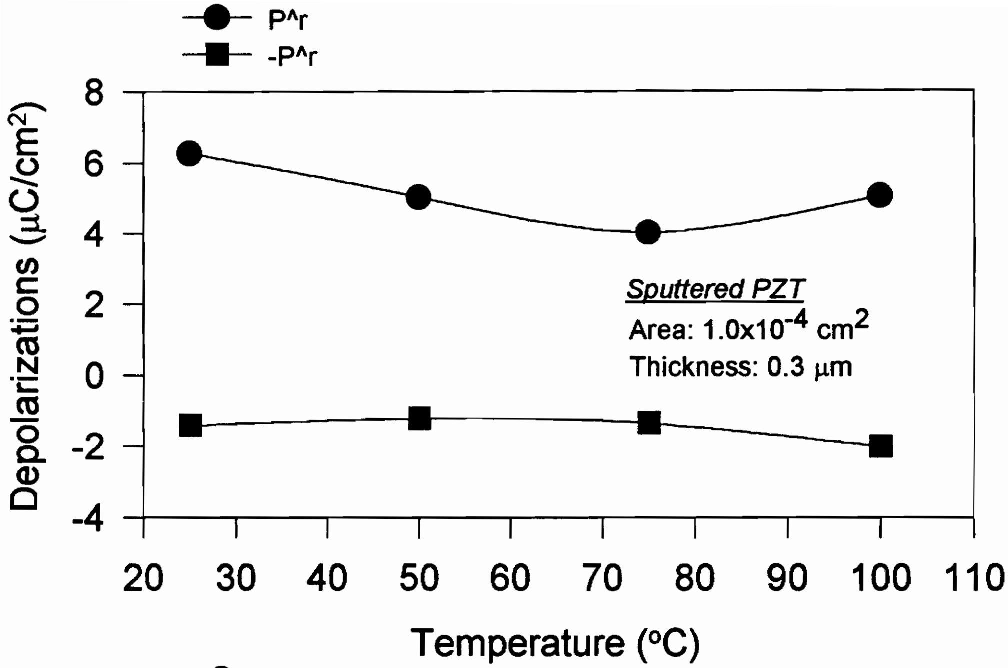


Fig 2.8 Sputtered PZT, MOD PZT, after fatigue.



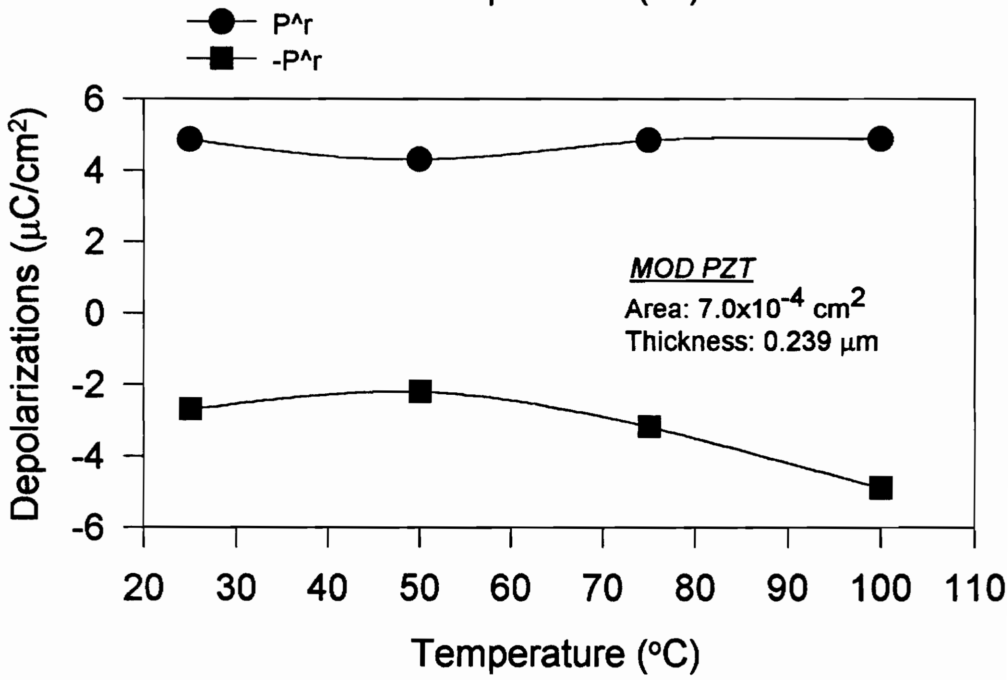


Fig 2.9 Sputtered PZT, MOD PZT, after negative pulses.

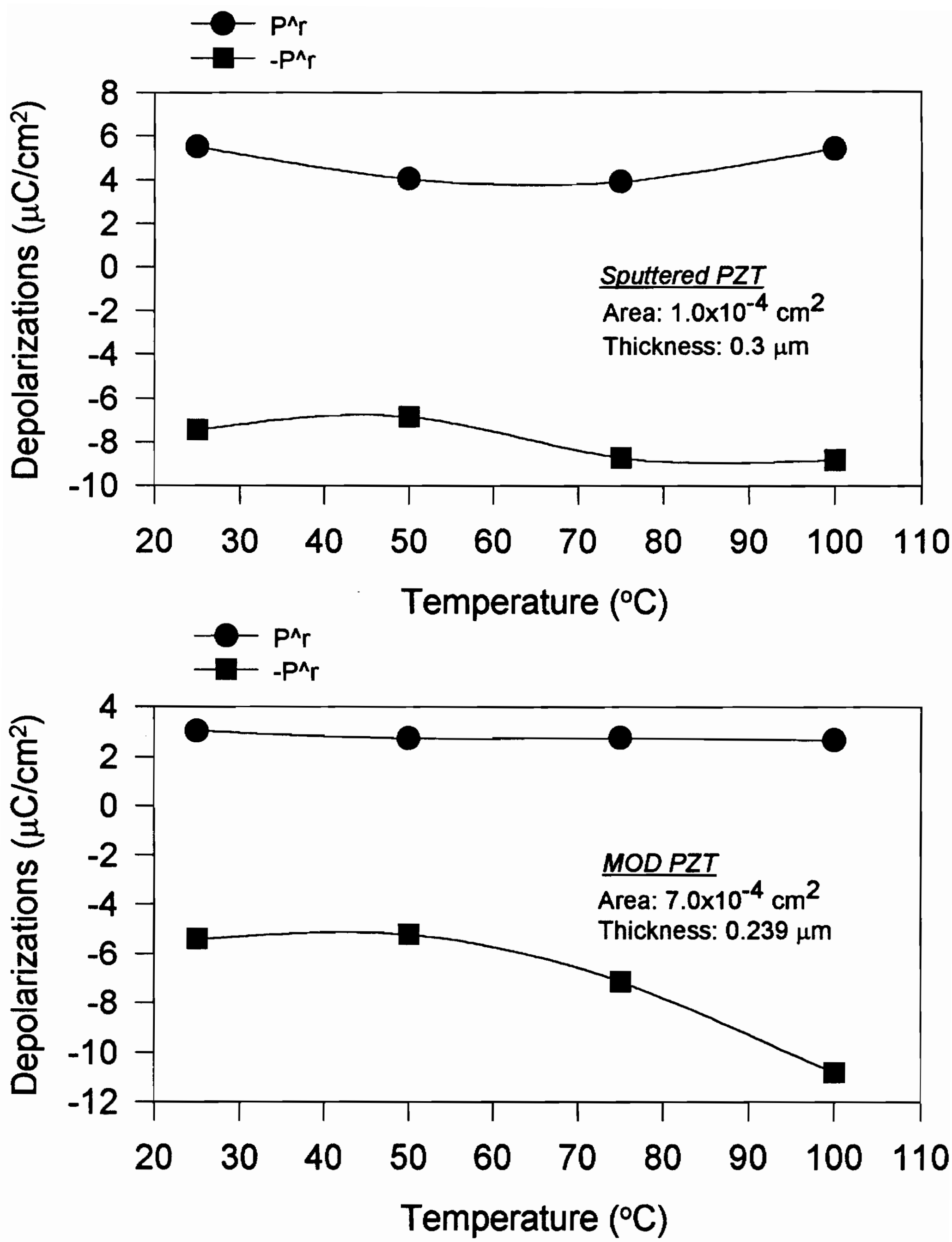


Fig 2.10 Sputtered PZT, MOD PZT, after positive pulses.

2.11 Effect of initial depolarization

It has been observed that the extent of imprint is as much dependent on fatigue and unipolar pulses and temperature, as it is on the processing methods. The different processing histories of the two electrodes (bottom and top) of an MFM capacitor are instrumental in determining the nature of the two M-F interfaces, The difference in these two interfaces sometimes cause an asymmetry in the hysteresis curve. But the most important effect of this asymmetry is reflected in the difference in the magnitude of initial depolarizations in the two opposite directions.

Surprisingly, it has been observed, in the sputtered PZT samples, the differences in the initial depolarizations cause +P^r to be greater than -P^r. However, in the case of MOD PZT samples, the situation is exactly the opposite. +P^r is less than -P^r in the virgin sample. This difference is further enhanced once the samples are subjected to fatigue by bipolar symmetric pulses. In the case of sputtered samples, P^r becomes much larger than -P^r and in the MOD capacitors, -P^r becomes much larger than +P^r.

This inherent asymmetry in the capacitor's ability to store information is only enhanced by the unipolar pulses. Indeed, we find that for sputtered samples, negative pulses cause much more depolarization (increase in +P^r) than is caused by positive pulses (increase in -P^r). In contrast, in MOD samples, the application of positive pulses will cause much larger depolarizations and hence stronger imprint, than negative pulses, especially at higher temperatures.

2.12 Effect of sample thickness

An identical electric field of 136 kV/cm was applied for pulsed polarization measurements conducted on the MOD PZT samples of various thicknesses. The hysteresis curves were also obtained using triangular waves of appropriate amplitude to produce the same fields across the samples.

Measurements were conducted at two temperatures - $25^{o}C$ and $85^{o}C$. The high temperature value of $85^{o}C$ was chosen as that is reported to be the highest temperature under which a modern day IC has to operate.

Figures A-9 through A-16 (Appendix) show the result of imprint measurement on the MOD samples of different thicknesses at the two temperatures of $25^{o}C$ and $85^{o}C$. Figure 2.12 summarizes the effect of negative pulses on the samples fatigued identically with bipolar pulses (10^8 cycles).

The depolarization results are very contradictory at the two temperatures. While at $25^{o}C$, the thicker samples show increased depolarization, at $85^{o}C$, the thicker samples show much less depolarization. This result is very intriguing, particularly because it is usually seen (next chapter), that the thicker samples show faster degradation compared to thinner samples at the same applied field strength due to higher fields appearing across the interfacial layers. This is supposed to speed up degradation and is seen to be true at $25^{o}C$. But at $85^{o}C$, the effect is quite contradictory.

This observation may be used to emphasize our previous conclusion that degradation due to temperature and that due to fatigue may be due to fundamentally different and somewhat opposing mechanisms.

Further studies are required to determine the true nature of the above mechanisms.

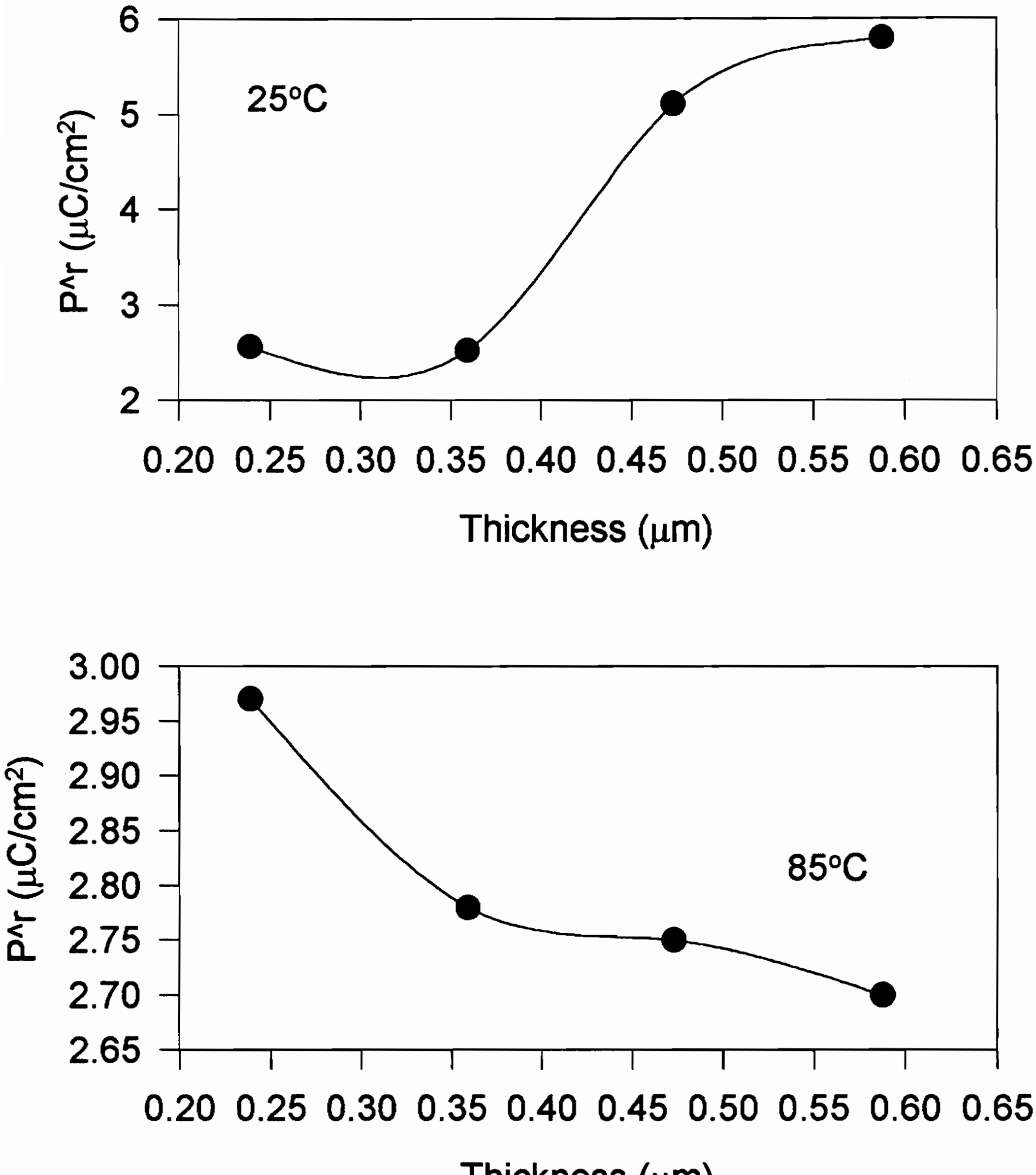


Fig 2.11 Depolarization after fatigue with negative pulses for samples with different thicknesses.

Chapter III. Degradation of Dielectric Properties

3.1 Objective

The objective of this chapter is to present the dependence of the dielectric constant of the metal-ferroelectric-metal capacitor on the number of read/write operations (i.e., fatigue cycles) performed on it.

3.2 Samples

Pt/PZT/Pt thin film capacitors of four different thicknesses were used in this study. The samples were prepared by metal organic decomposition (MOD) method. The film thicknesses were 0.239 μm, 0.359 μm, 0.473 μm and 0.588 μm which were accurately determined by Variable Angle Spectroscopic Ellipsometry.

3.3 Capacitance-Voltage Measurements:

Capacitance-Voltage (C-V) measurement has proved to be a useful method of determining the space-charge effects in ferroelectric thin films [19]. The C-V measurement data reported here have all been taken using a Hewlett Packard low frequency impedance analyzer (HP 4192A). The voltage is increased in a very slow ramp - 0 to 5V in 2 minutes.

Upon this slow ramp is superimposed a very small (50 mV) amplitude signal oscillating with a frequency of 10 kHz.

The capacitance measured by such a signal is supposed to be a complicated function of the capacitance at 10 KHz summed with the capacitance at the fundamental frequency of the Fourier Transform of the slow voltage ramp. The capacitance due to the space charges in the electrode - film interface is assumed to be high compared to the capacitance due the bulk because of the fact that the space charge layer is extremely thin. At extremely low frequencies, the highest capacitance will be detected. Thus, at the frequency of the principal component of the slow voltage ramp, the interfacial space charge layer capacitance will be of prime importance. (The space charge concentration at the grain boundaries is assumed to be very small. This is because the grains in PZT thin films are columnar in structure and usually extend from one electrode to the other.) One can also obtain a hysteresis curve using an a.c. signal of a frequency reasonably higher than the above frequency. This hysteresis curve should not reflect the space charge contribution. This curve may be used to elicit C-V information [20]. Thus, if one subtracts one C-V curve from the other, one can isolate the space charge effect. The hysteresis curve obtained by using RT66A is not an a.c. hysteresis curve. It is measured by means of a voltage ramp and hence cannot be used for the space charge effect study in conjunction with the C-V data from the impedance analyzer.

In this study, C-V curves have been used to study the degradation (figure 3.1) of the ferroelectric thin films due to fatigue. It was generally found (figure 3.2) that the C-V curves became shorter with fatigue cycles. The tips of the C-V curves (corresponding to the coercive voltages) became increasingly blunt. The overall capacitance of the thin film capacitor decreased. The reason behind the decrease in the size of the C-V curve can be

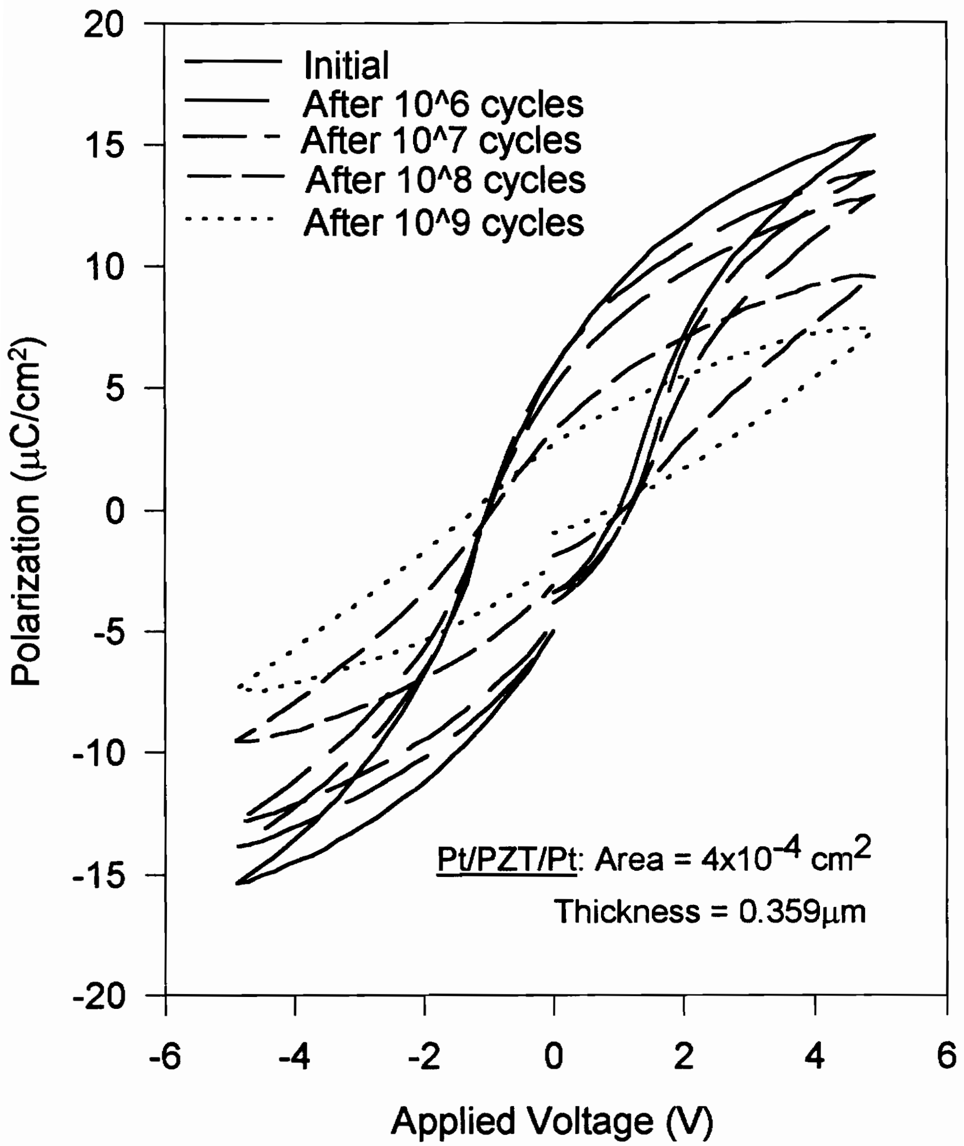


Fig 3.1 Hysteresis Curves.

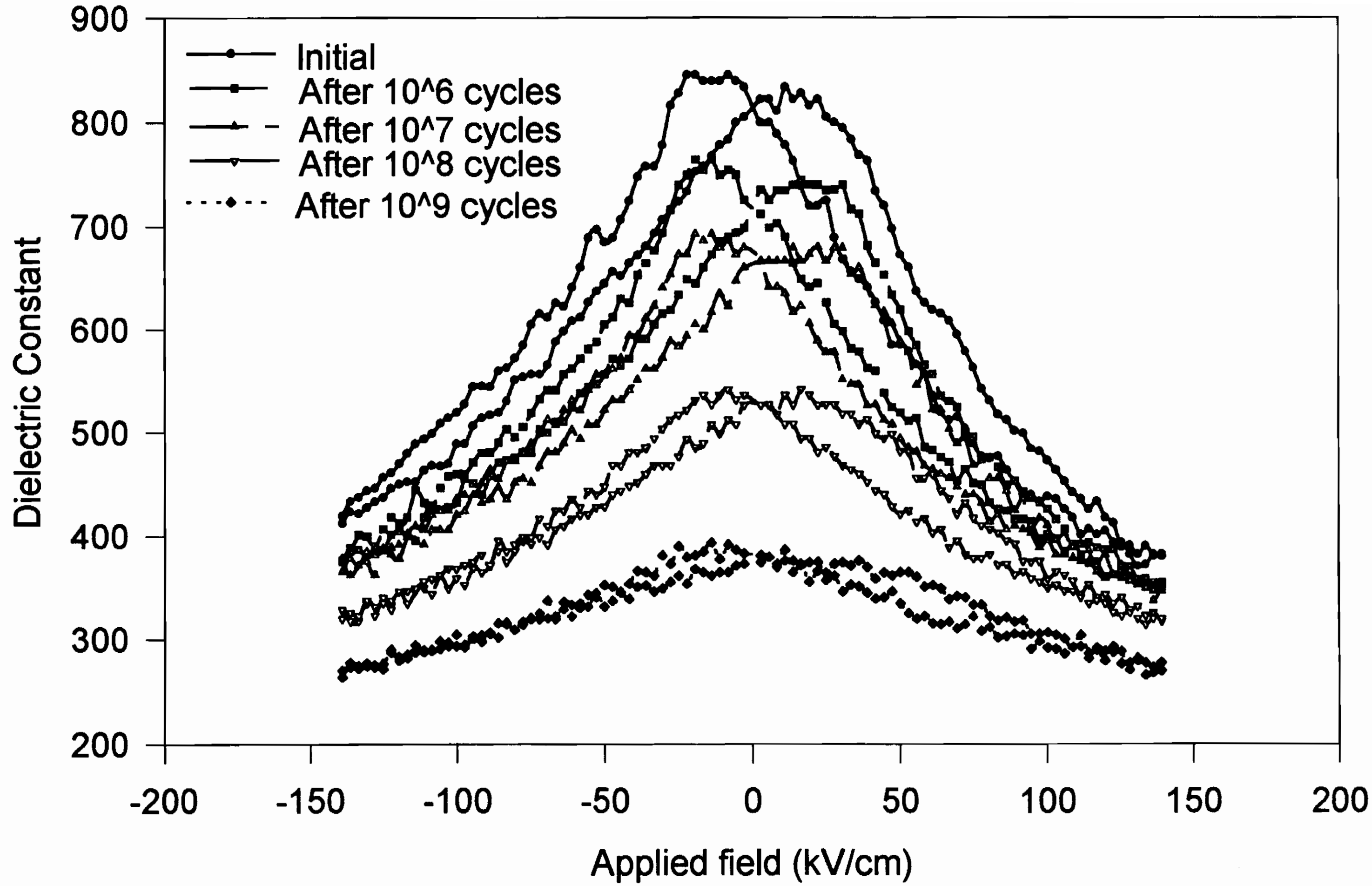


Fig 3.2 Dielectric Constant versus Field with Fatigue

attributed to an increase in the width of the depletion layer at the interface. The depletion capacitance thus decreases causing the total capacitance to decrease as well.

3.4 Leakage Current:

The d.c. leakage current of the thin film capacitor was measured at 136 kV/cm after various degrees of fatigue. The leakage current showed (figure 3.3) a general trend to increase with the number of fatigue cycles. This may be due to an increase in the conductivity along the grain boundaries and/or a decrease in the Schottky barrier height in the metal-ferroelectric interface due to a change in the work function resulting from space charge accumulation.

3.5 Dielectric Constant versus Fatigue:

The dielectric constant is found to increase with the thickness of the sample (figure 3.4). However, the thicker the sample, the faster the degradation (figure 3.5) of the dielectric constant with fatigue. This may be due to one or both of the following reasons:

i) The thicker samples may possess more defects;

ii) The same electric field (136 kV/cm) is applied to all the samples. The interfacial layer is believed to possess the same width in all samples regardless of the film thickness. This

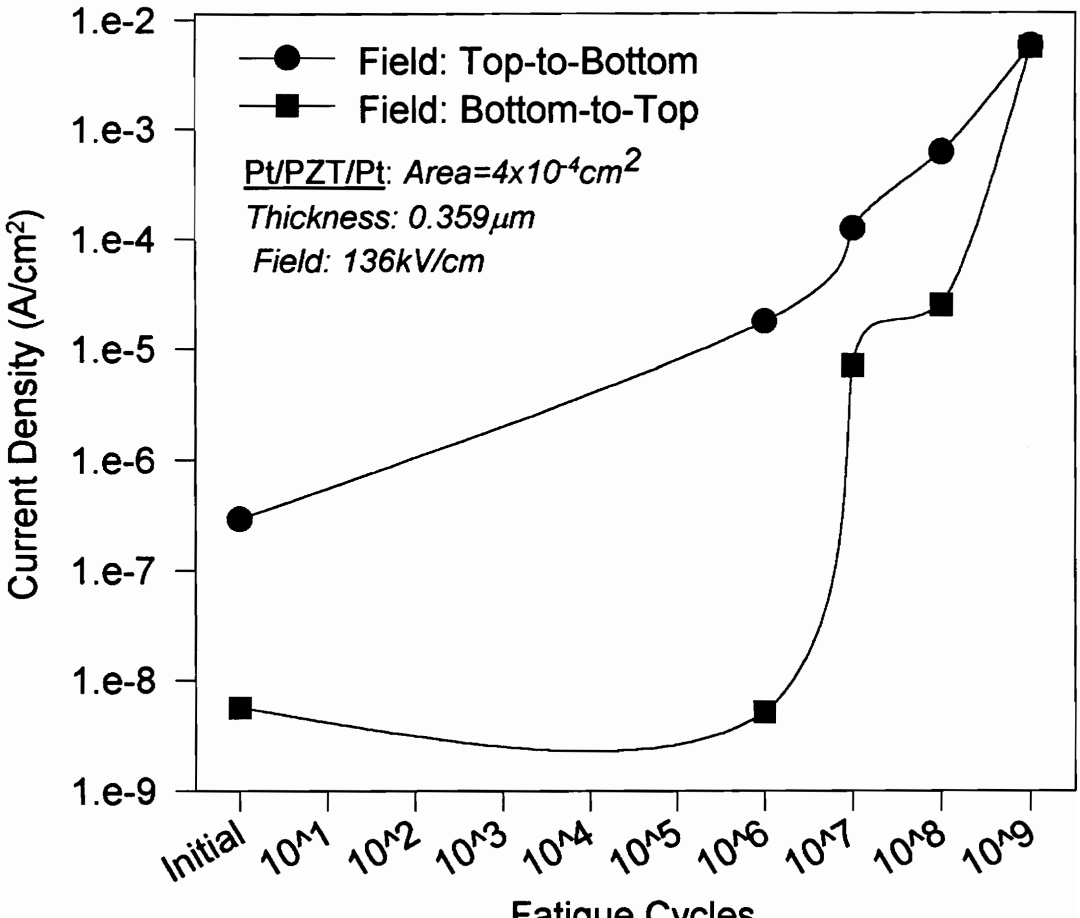


Fig 3.3 Leakage Current versus Fatigue Cycles.

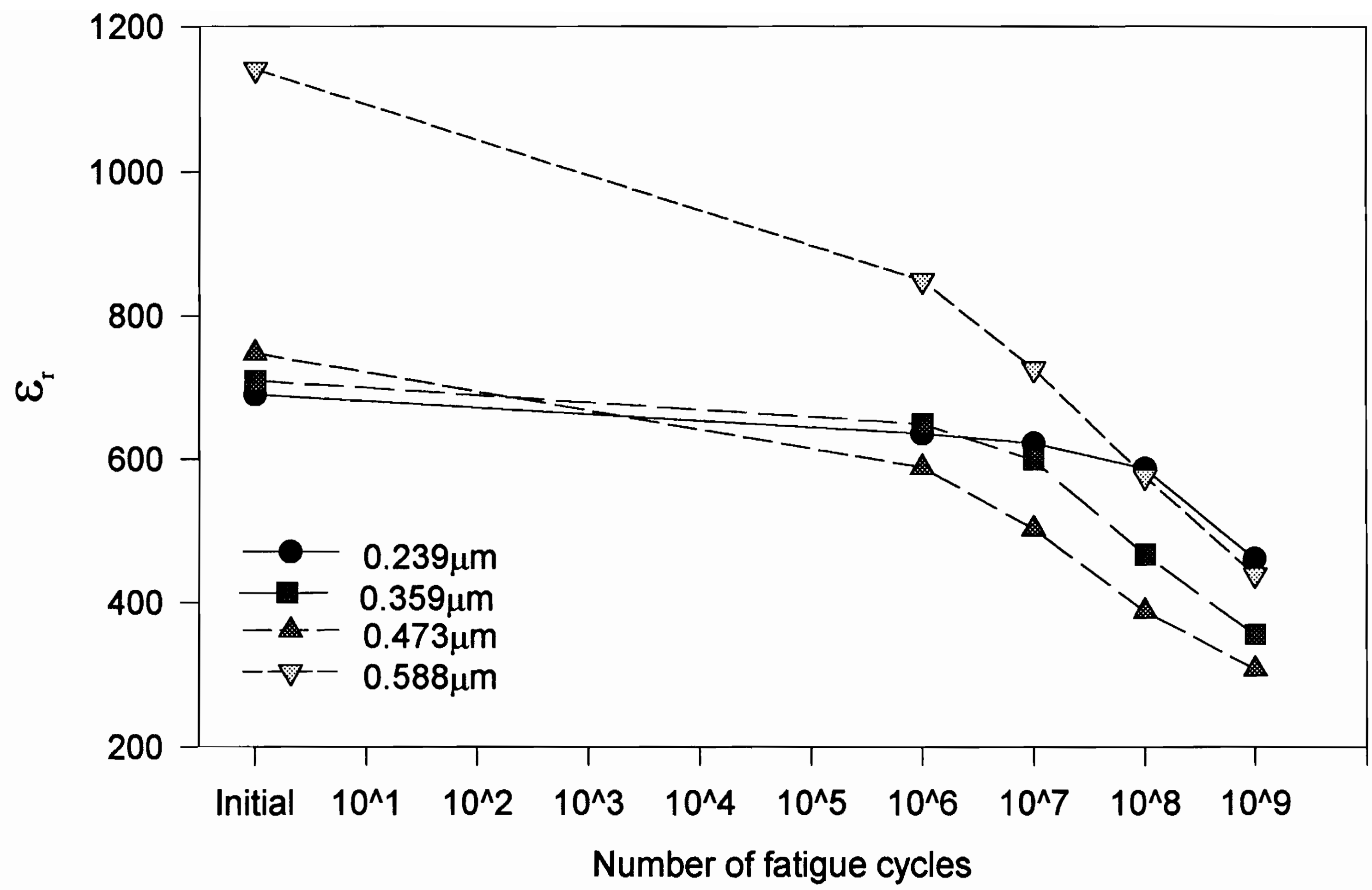


Fig 3.4 Degradation of Dielectric Constant with Fatigue

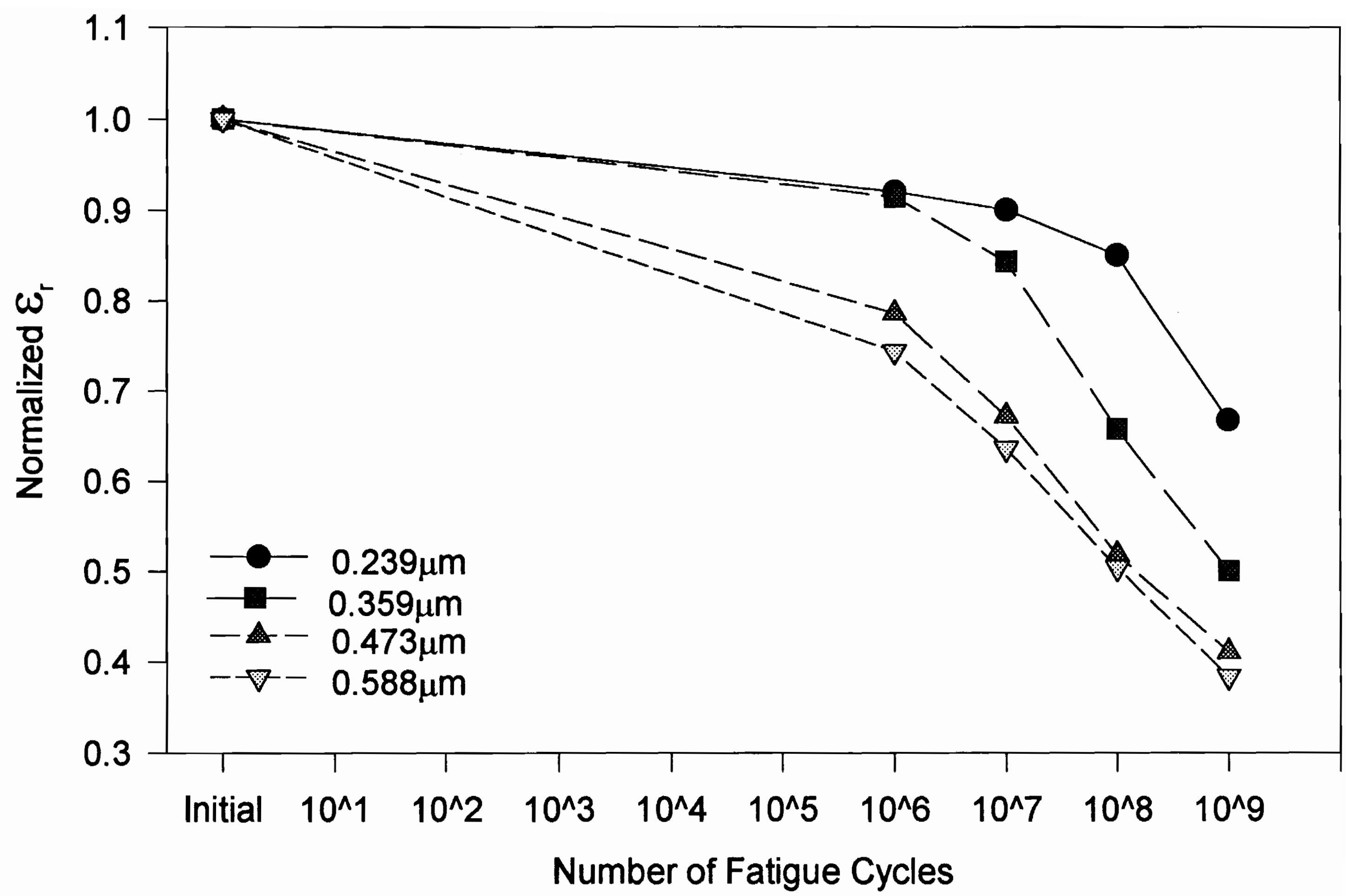


Fig 3.5 Normalized Dielectric Constant with Fatigue

means there will be a higher field acting in the interface of the thicker samples than in the thinner samples. This might result in faster degradation in the thicker samples.

The latter observation is another re-affirmation of the fact that the interfacial layer plays the most crucial role in the degradation of ferroelectric capacitors. Endurance improvement of ferroelectric capacitors is contingent upon the minimization of the interfacial defect layer.

3.6 Impedance and Modulus Spectroscopic Techniques:

An example equivalent circuit of a PZT capacitor is shown in figure 3.6. This figure is not very accurate because the metal - ferroelectric interface and the grain boundary R-C components are shown to be identical. However, this simplifying assumption is made for the purposes of the present discussion, since both these R-C components are considerably higher than the R-C component corresponding to the grain boundaries.

Impedance and Modulus Spectroscopic Techniques can be very useful in identifying the different R-C components in the equivalent circuit of any dielectric medium [21]. The total impedance of a simple R-C circuit can be expressed as: $Z=R+jX$, where $X = 1/(j\omega C)$. In Impedance plane plots (figure 3.7) R is plotted against $-X$ at various frequencies. The effects of the various R-C components can be separately identified iff the various C's are at least 100 times different from one another. By magnifying the high frequency region of this curve, one can identify the extremely small loop corresponding to the small capacitance of 4 pF. Impedance plane plots may not always be very efficient when it comes to identifying the various R-C components, when the various C's do not

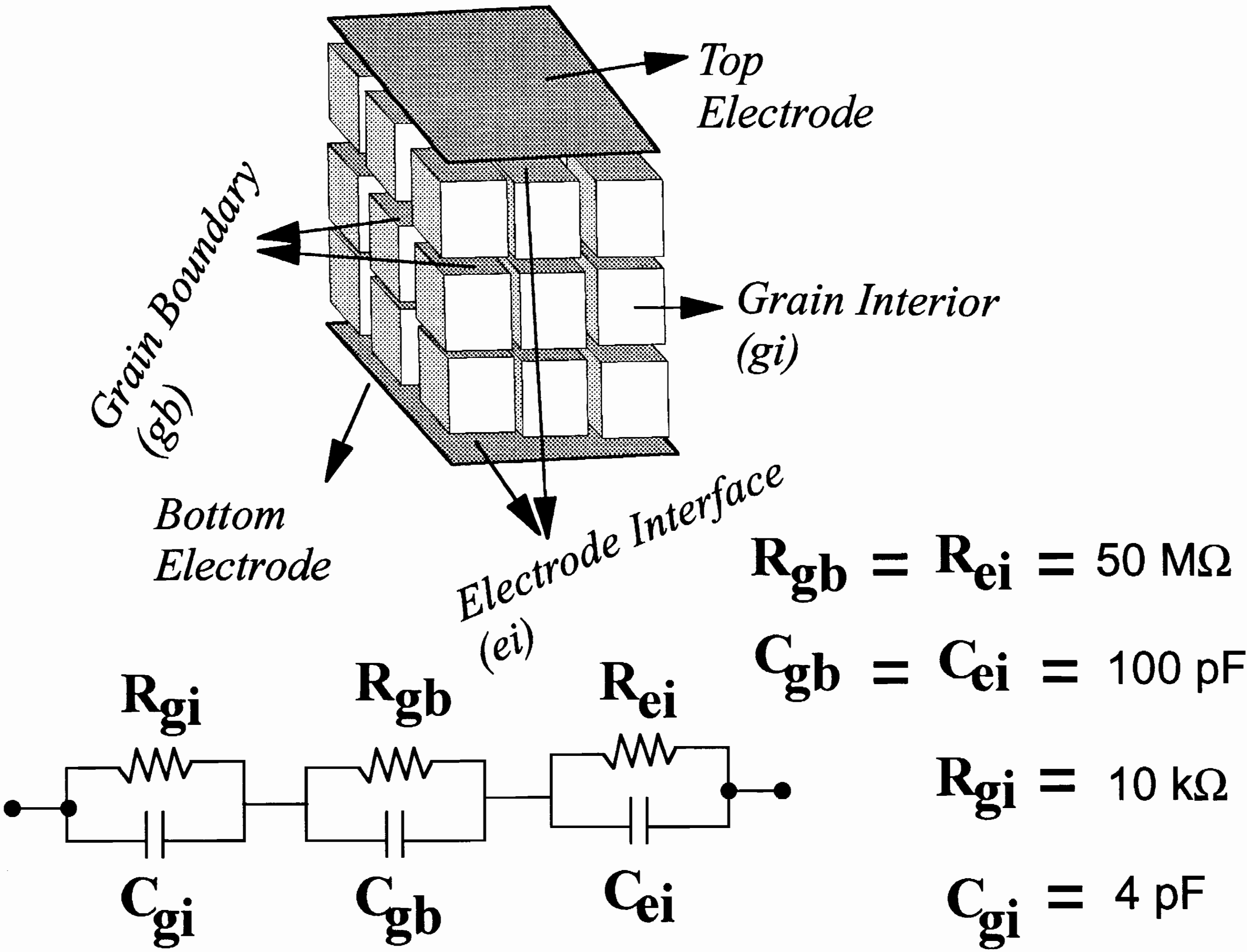


Fig 3.6 An example R-C circuit

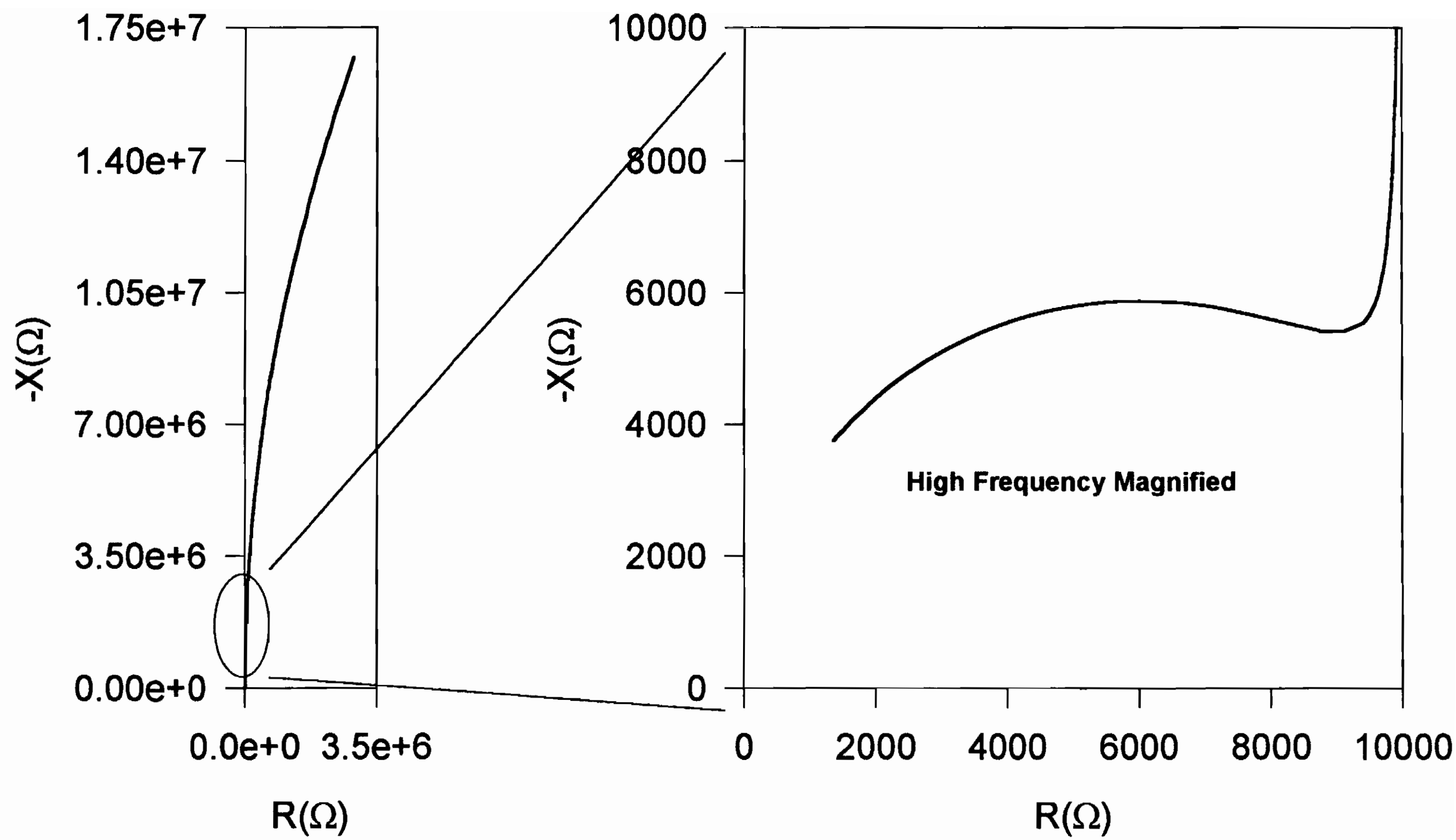


Fig 3.7 Impedance Plane Plot

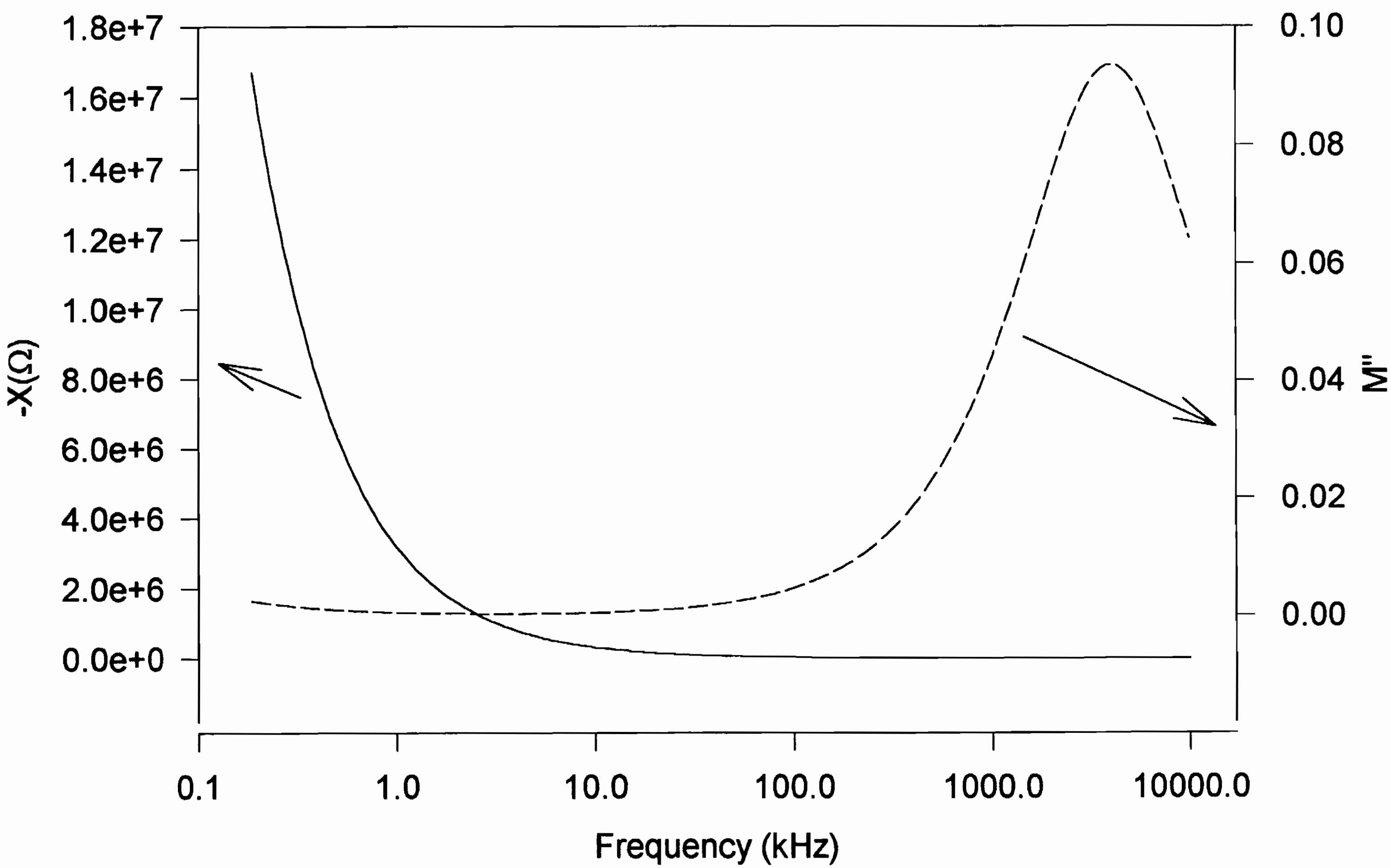


Fig 3.8 Impedance and Modulus Spectra of example circuit

differ from one another by factors greater than 100. Though the example circuit does not elucidate this problem, one can very well imagine the difficulties that might arise in actual cases where the grain boundaries and the interfaces will, most likely, have similar C's but different R's. However, one can use the Impedance Spectrum (X versus ω) and Modulus Spectrum ($\omega C_C R$ versus ω) (figure 3.8) together and work around this problem. C_C is the capacitance of a capacitor with the same area as the capacitor under consideration with air as dielectric.

If there are two R-C components with comparable C's but different R's, then there would be two different peaks in the Modulus Spectrum where the peaks are proportional to 1/C. Similarly, for two R-C components with comparable R's but different C's, the Impedance Spectrum will show two separate peaks (in this case, the peaks are proportional to R).

The applicability of the above spectroscopic techniques is limited only by the accuracy and range of the laboratory impedance analyzer. HP 4192A low frequency impedance analyzer can measure impedances in the frequency range of 5 Hz to 13 MHz. The upper limit of the measured impedance value is approximately 1.3 MΩ. This latter can prove to be the most important limitation in the application of the spectroscopic techniques.

3.6.1 The Impedance Spectra:

The data shows (figure 3.9) that the impedance spectra have low frequency peaks which are beyond the scope of the analyzer. However, with increasing fatigue cycles, this peak shifts to the right. Now this low frequency component must be due to the interface,

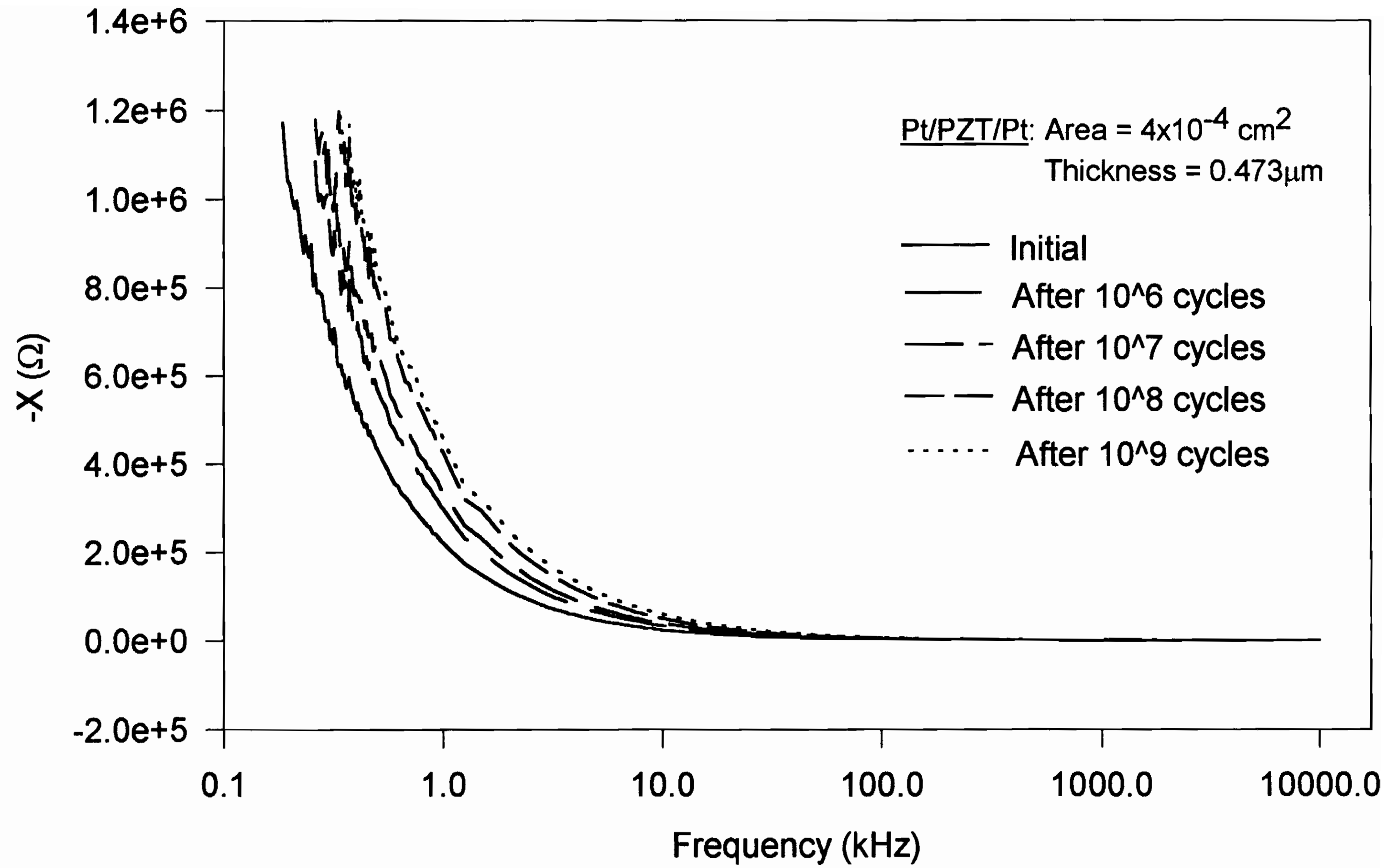


Fig 3.9 Impedance Spectrum of Pt/PZT/Pt

which has both a high C and a high R compared to the grain interiors. Since the position of a peak in the frequency spectrum is determined by the 1/(RC) value, the right shift of the low frequency peak implies that RC is decreasing. It is our belief that C is decreasing gradually with fatigue, since the depletion width at the interface is increasing. But we do not have much evidence to say that R is also decreasing at the interface with fatigue. In any case, an impedance analyzer tuned to work in really low frequencies (less than 1 Hz) and capable of reading very high impedance values (greater than 10 MΩ) is necessary in order that we can accurately analyze the effect of fatigue.

3.6.2 The Modulus Spectra:

The Modulus Spectra after various fatigue cycles (figure 3.10) all show a peak at around 4 MHz which increases in height with fatigue. Remembering the fact that the height of a modulus spectrum peak is proportional to 1/C, we can understand that the value of the capacitance corresponding to the particular R-C element being considered, is decreasing steadily with fatigue. Since the peak (determined by RC product) remains more or less at the same position, the corresponding resistance may be increasing at the same time. Now, we have to understand what this R-C component corresponds to. We can rule out the interface because unlike this component, the interface has a very large RC value and is expected to show up at very low frequencies only. Similarly, it is also believed that the RC of the grain boundary regions is also very high. It is thus possible that the peak corresponds to the grain interior.

The increasing height of the high frequency peak may indicate that the capacitance corresponding to the grain interiors is gradually *decreasing* with fatigue. However, we do

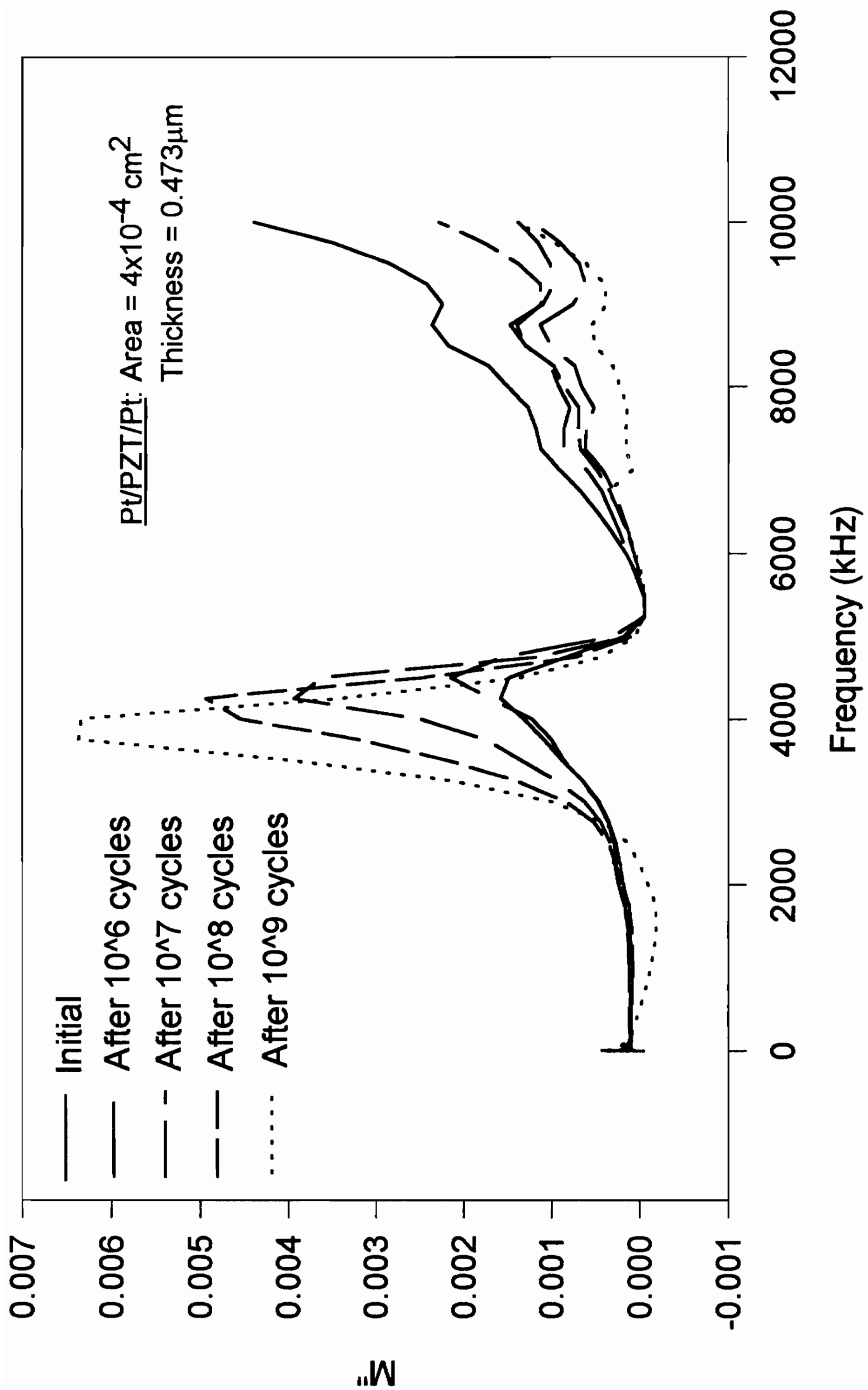


Fig 3.10 Modulus Spectrum of Pt/PZT/Pt

not have any other evidence that can support such a possibility. At this moment, we still do not have a complete understanding of the degradation mechanism(s). Further studies need to be done to gain more knowledge in this regard.

3.7 Summary:

Dielectric constant of MOD Pt/PZT/Pt capacitors are found to decrease steadily with fatigue. Thicker samples tend to degrade faster than thinner samples with the same electric field. Leakage current is also found to increase with number of fatigue cycles. Impedance and Modulus Spectroscopic techniques have been suggested for getting a better picture of the degradation process. However, the latter techniques call for better low frequency measurement equipment with higher upper limit of impedance.

Appendix

The figures in the following pages (figures A-1 through A-16) show the detailed results of the imprint tests performed on the various Pt/PZT/Pt samples. The summary of the results has been presented in Chapter II.

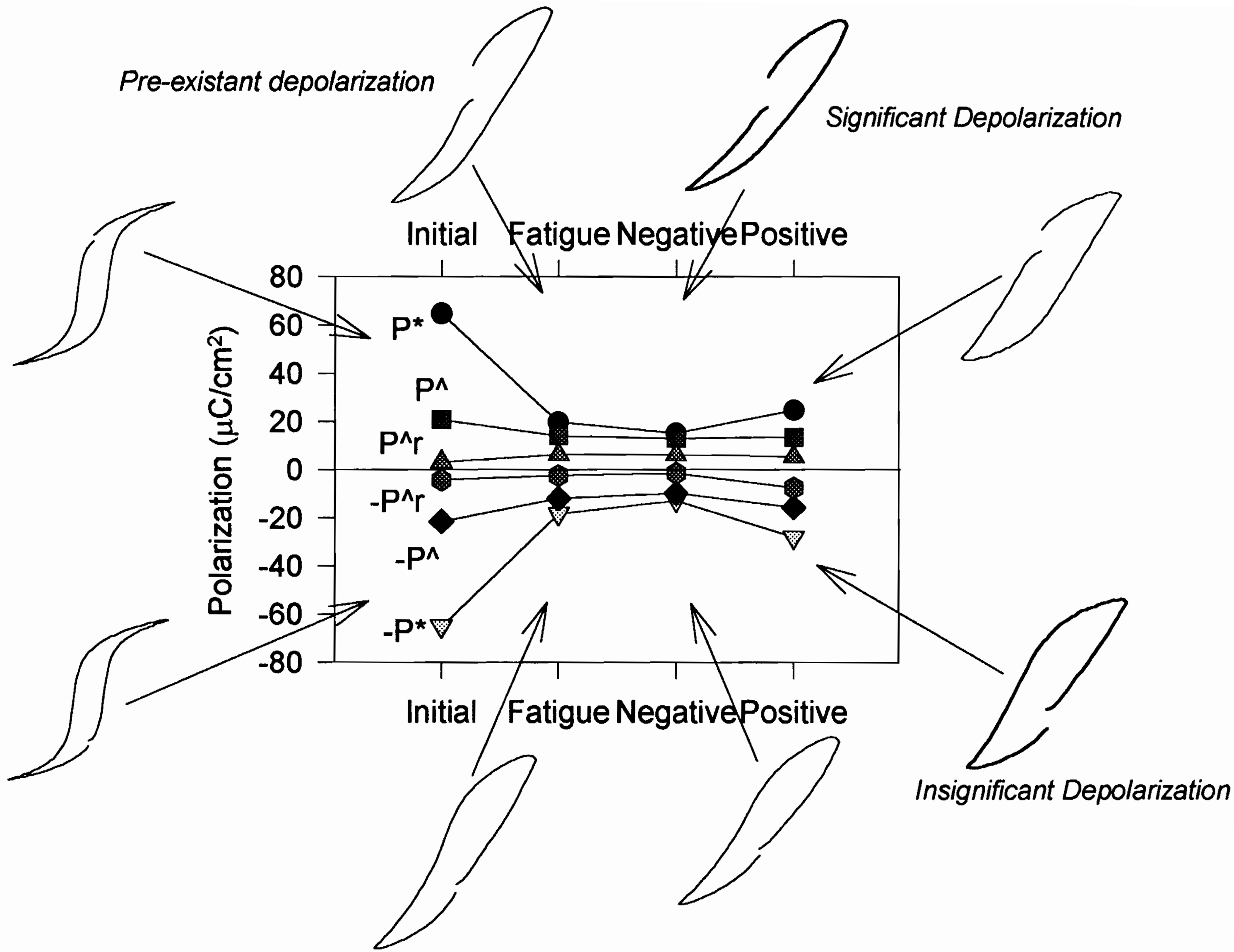


Fig A-1 Imprint in Sputtered Pt/PZT/Pt (0.3μm) at 25°C

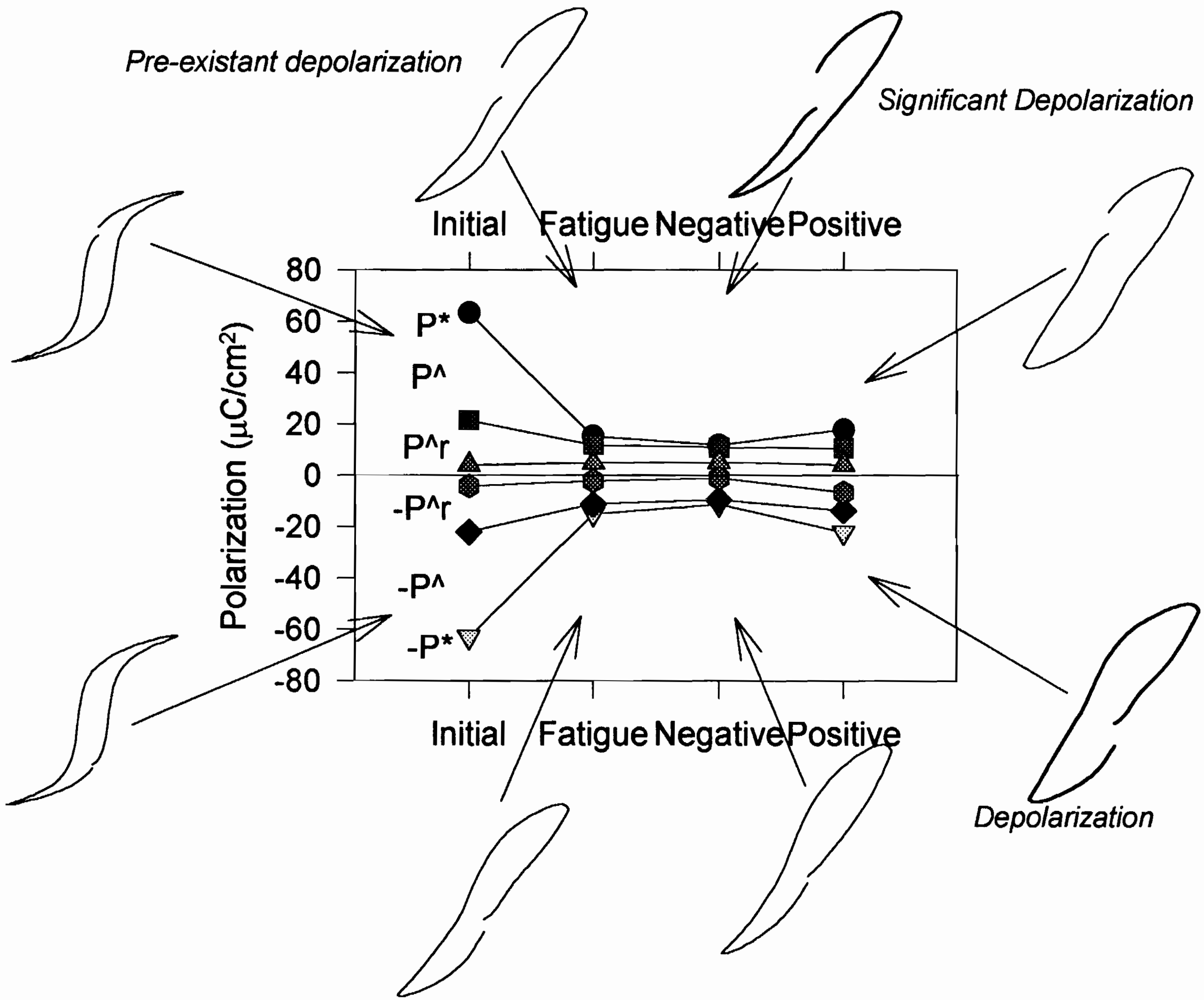


Fig A-2 Imprint in Sputtered Pt/PZT/Pt (0.3μm) at 50^{o}C

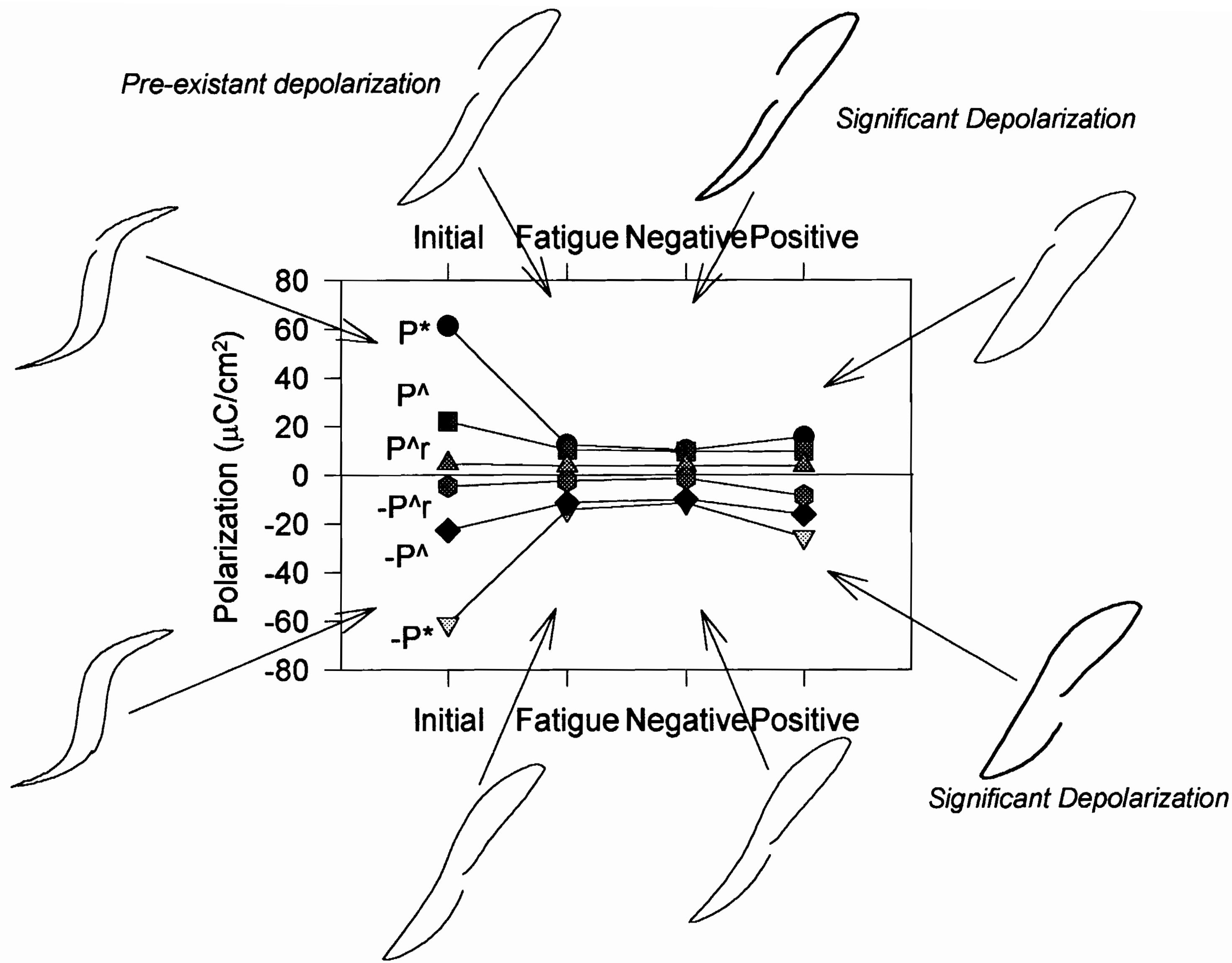


Fig A-3 Imprint in Sputtered Pt/PZT/Pt (0.3μm) at 75°C

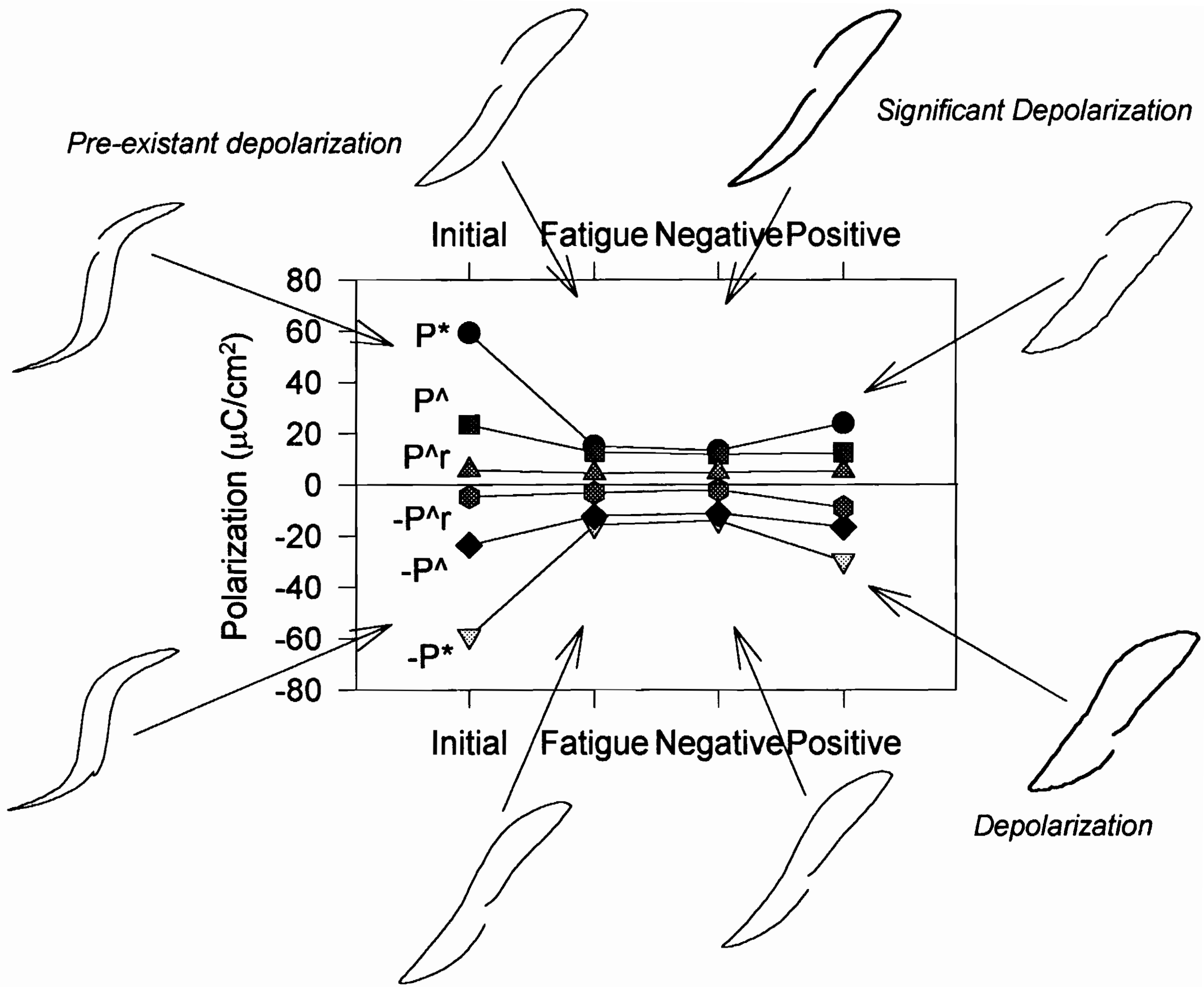


Fig A-4 Imprint in Sputtered Pt/PZT/Pt (0.3μm) at 100°C

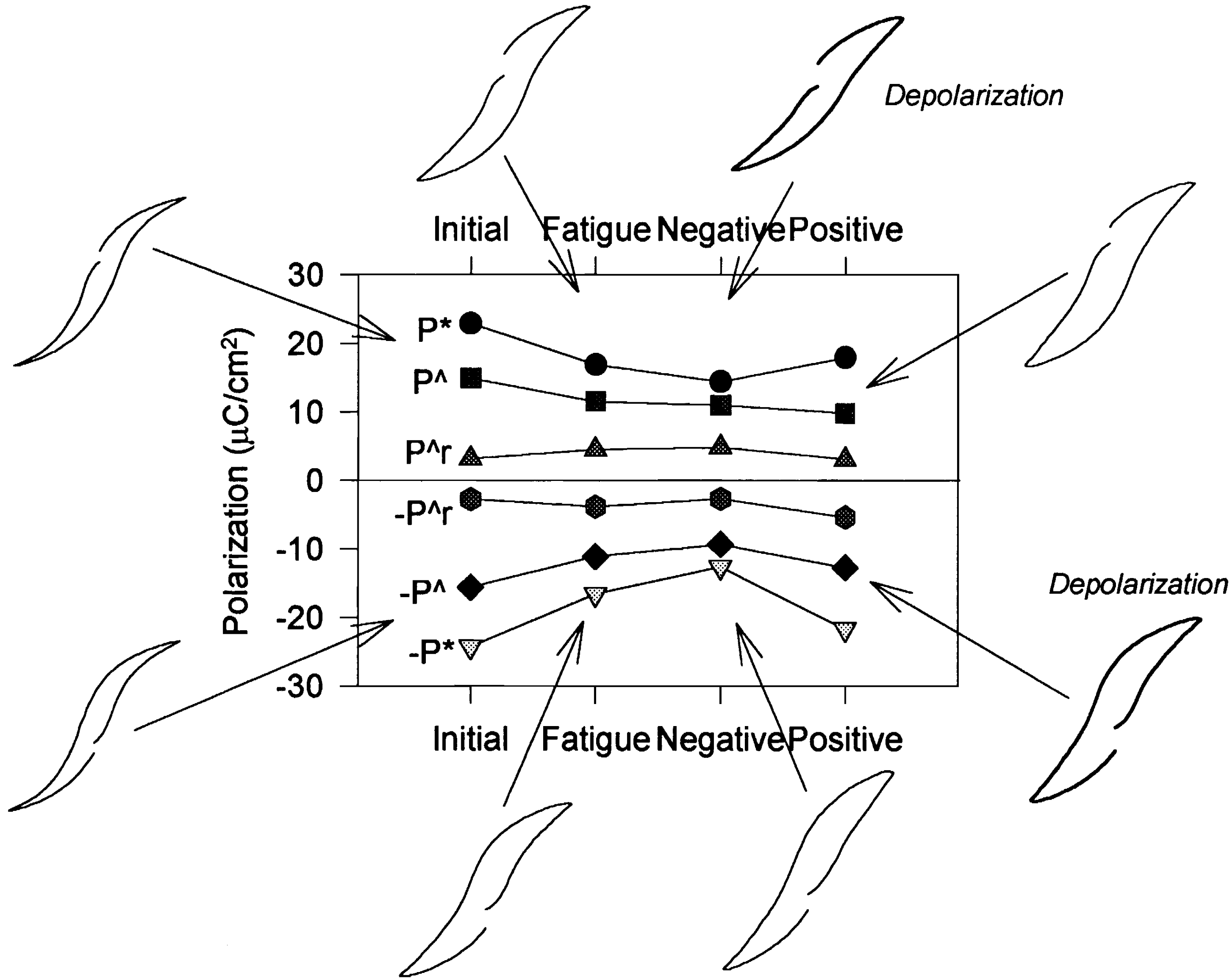


Fig A-5 Imprint in MOD Pt/PZT/Pt (0.239μm) at 25^{o}C

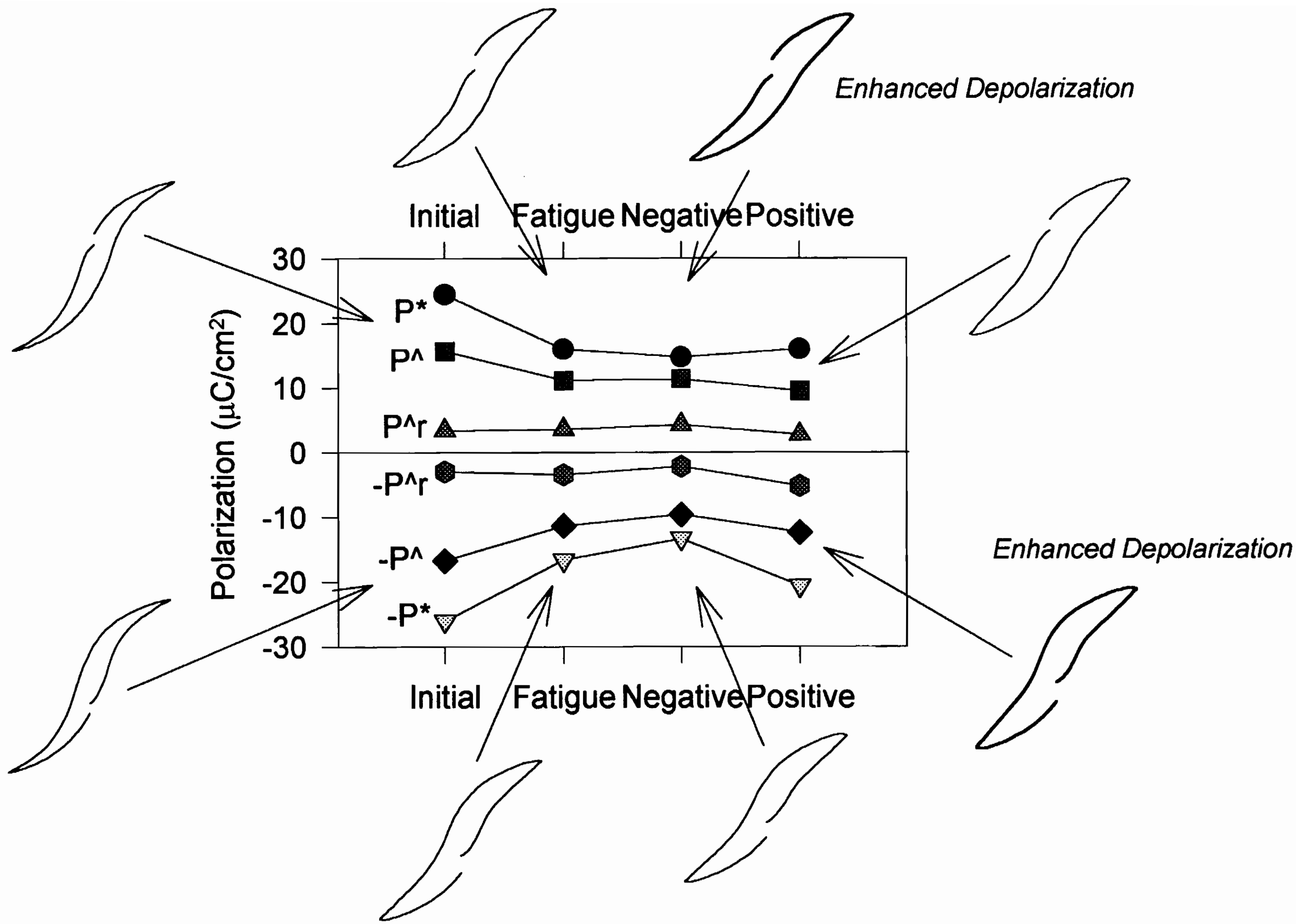


Fig A-6 Imprint in MOD Pt/PZT/Pt (0.239µm) at 50°C

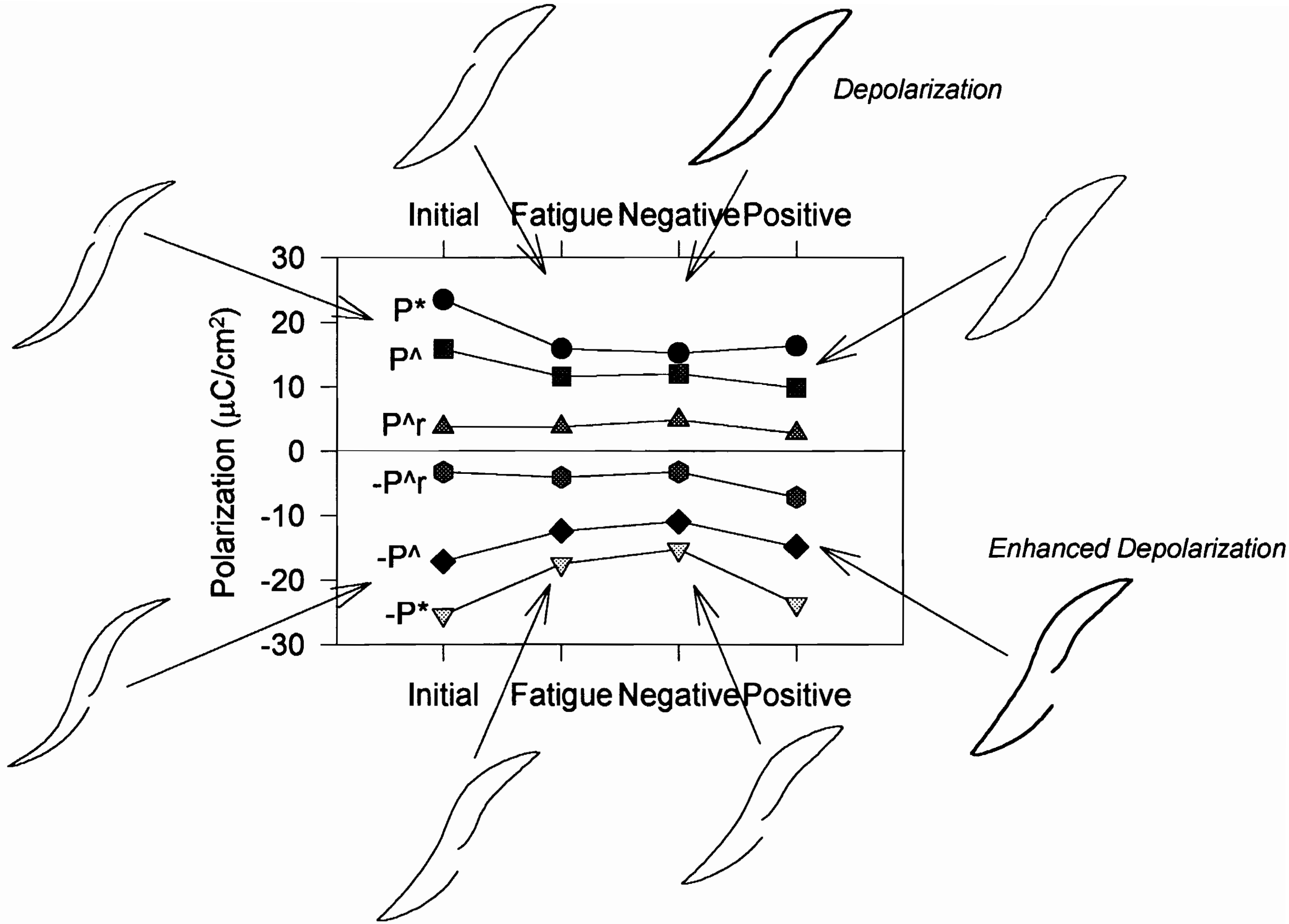


Fig A-7 Imprint in MOD Pt/PZT/Pt (0.239μm) at 75°C

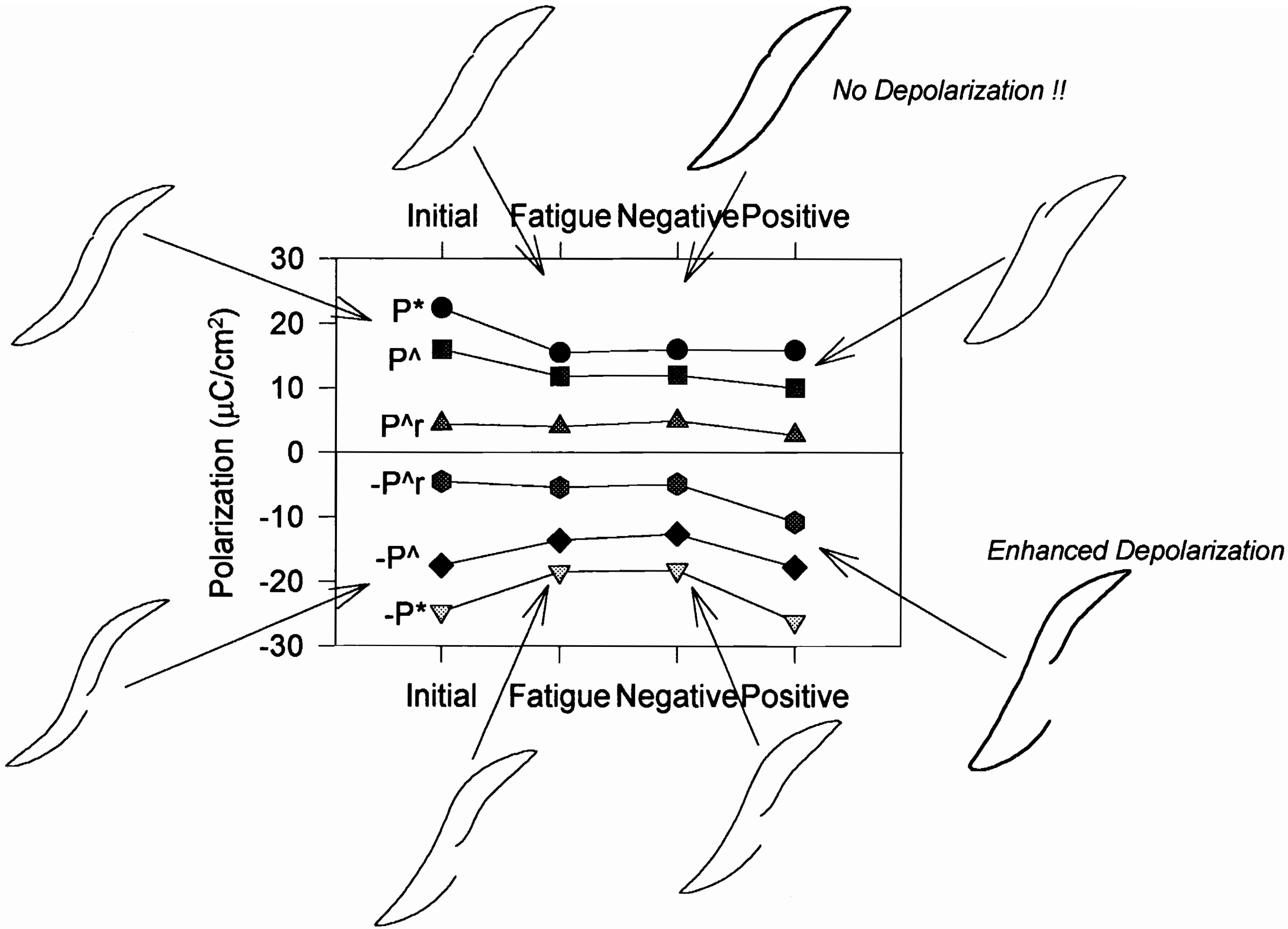


Fig A-8 Imprint in MOD Pt/PZT/Pt (0.239μm) at 100°C

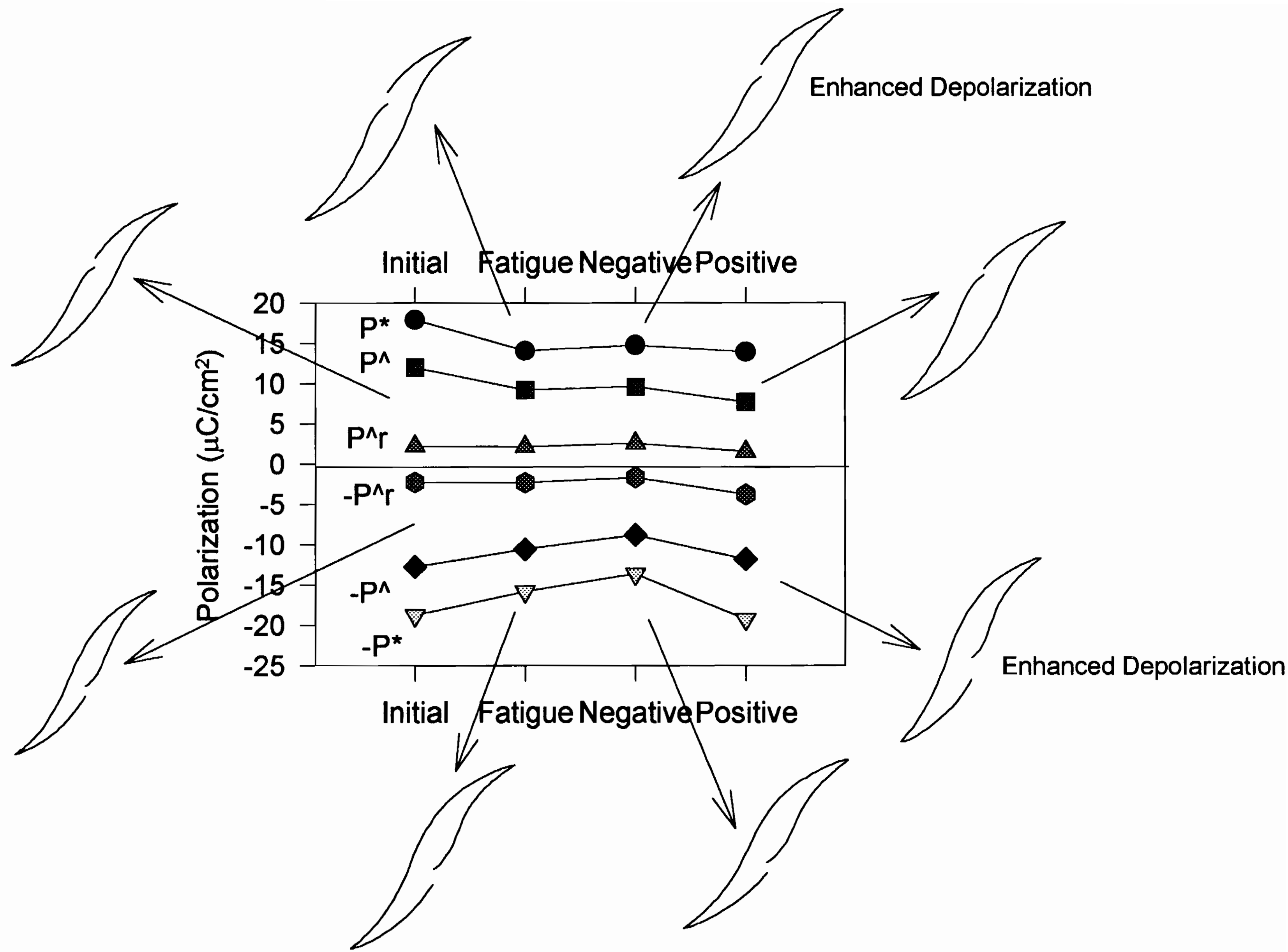


Fig A-9 Imprint in Pt/PZT/Pt (0.239μm) at 25^{o}C

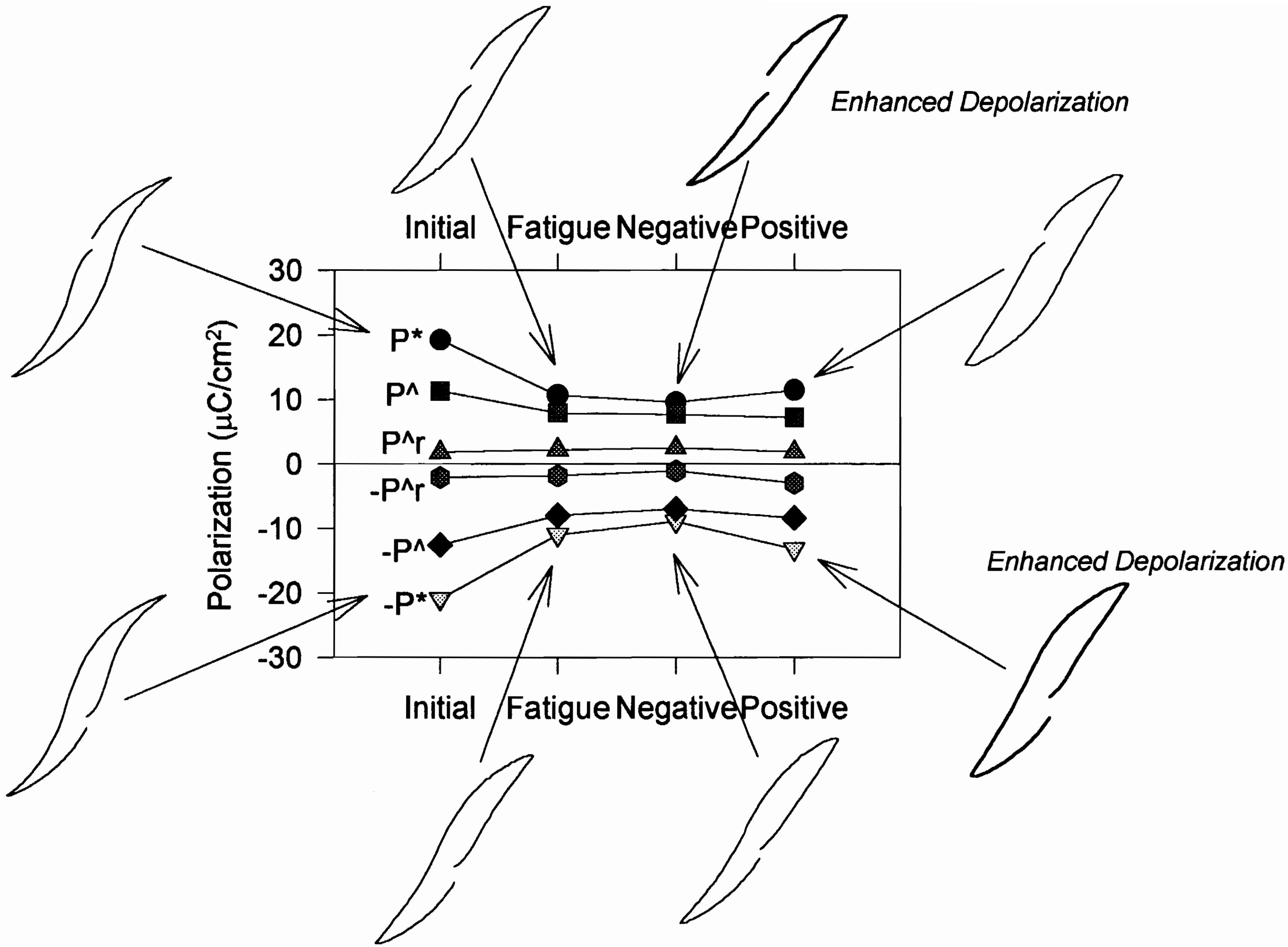


Fig A-10 Imprint in Pt/PZT/Pt (0.359μm) at 25°C

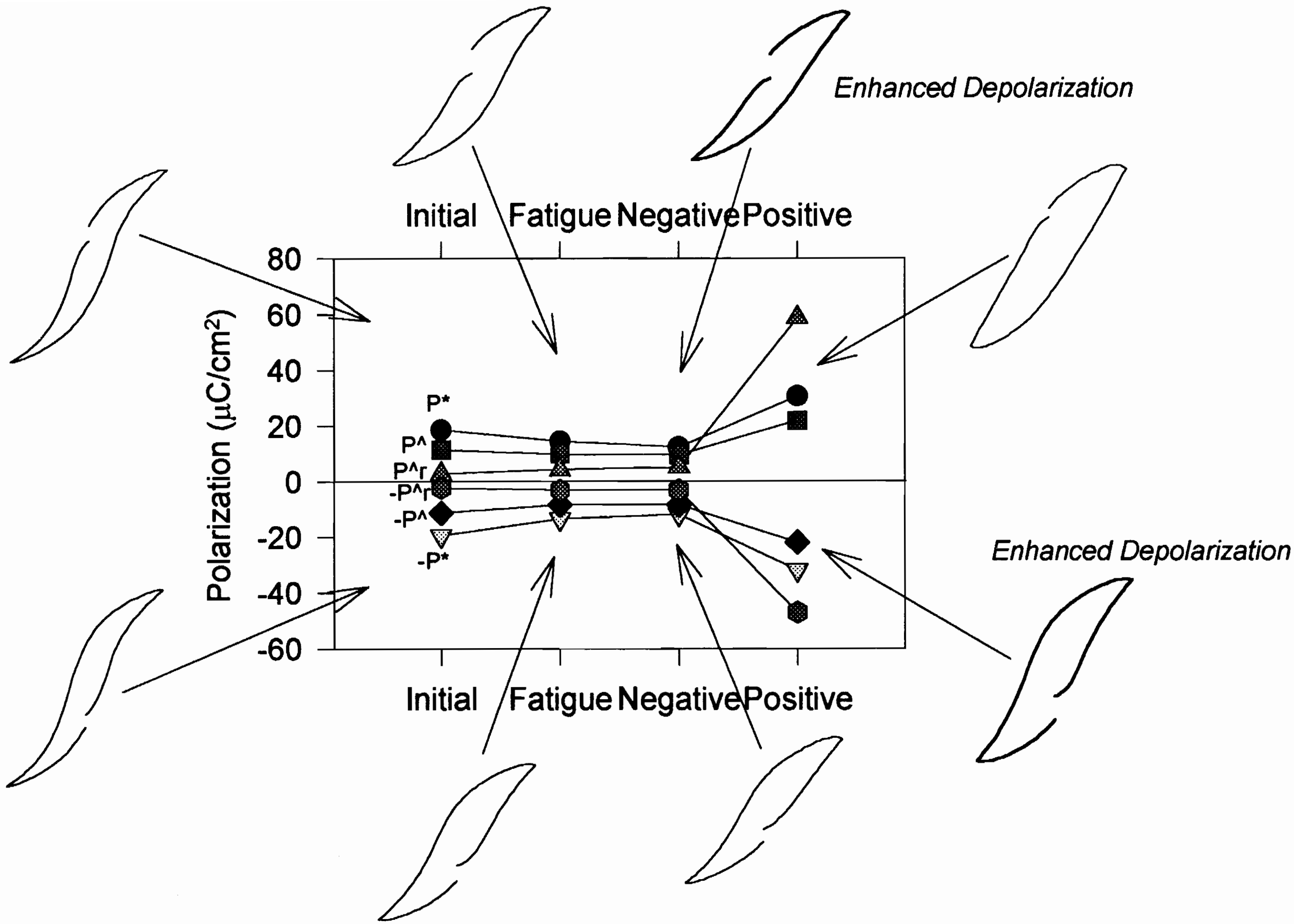


Fig A-11 Imprint in Pt/PZT/Pt (0.473μm) at 25°C

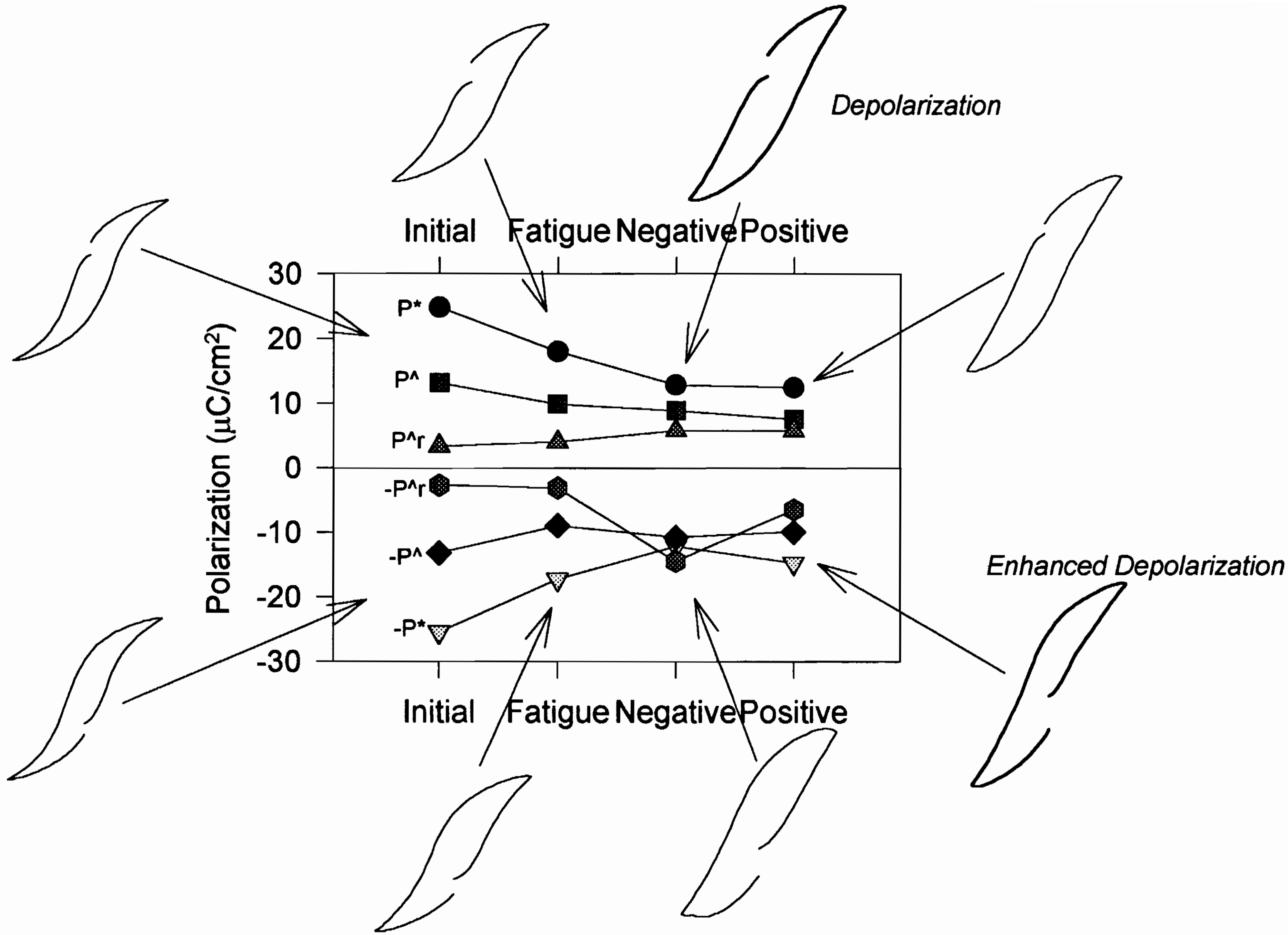


Fig A-12 Imprint in Pt/PZT/Pt (0.588μm) at 25°C

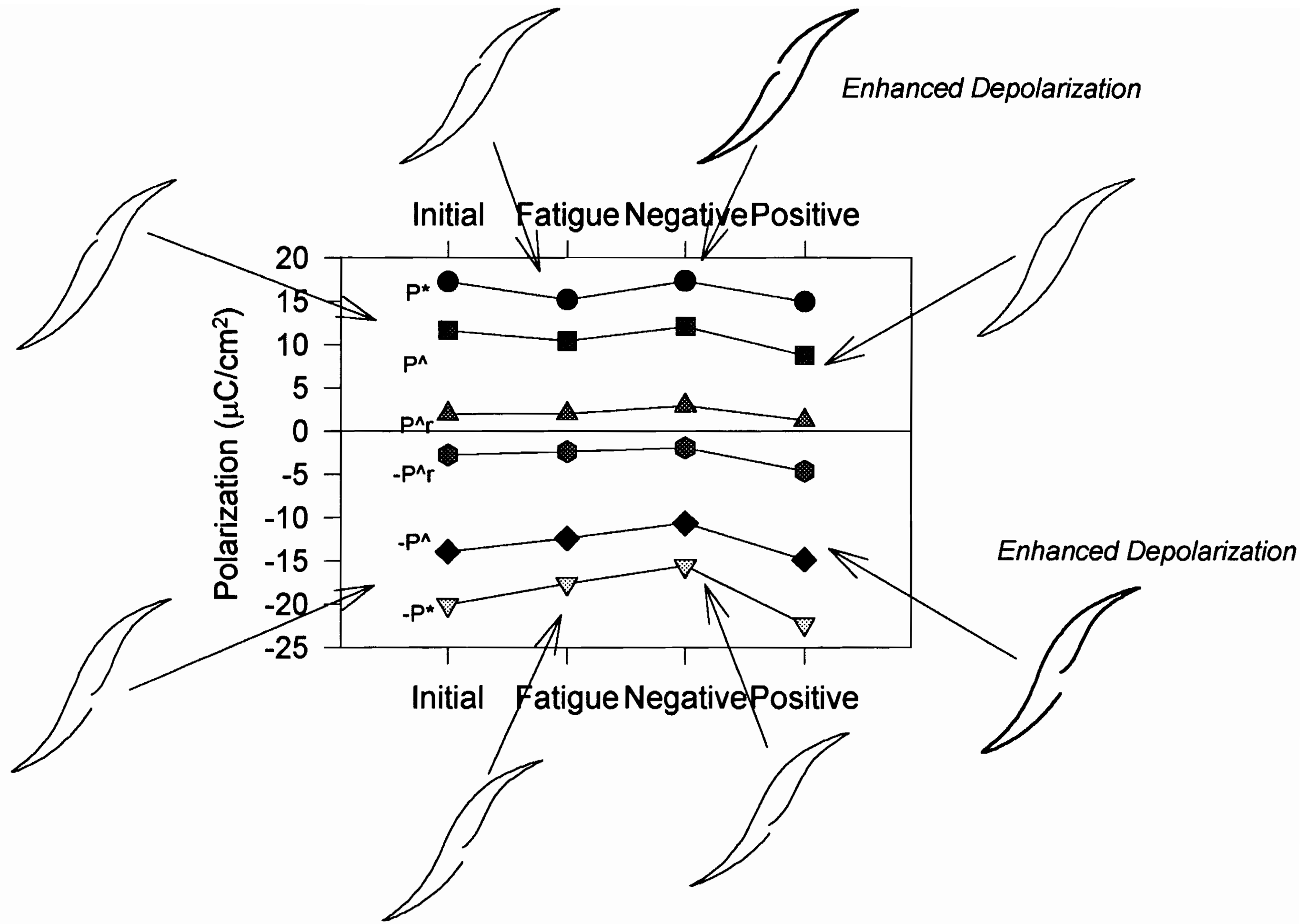


Fig A-13 Imprint in Pt/PZT/Pt (0.239μm) at 85^{O}C

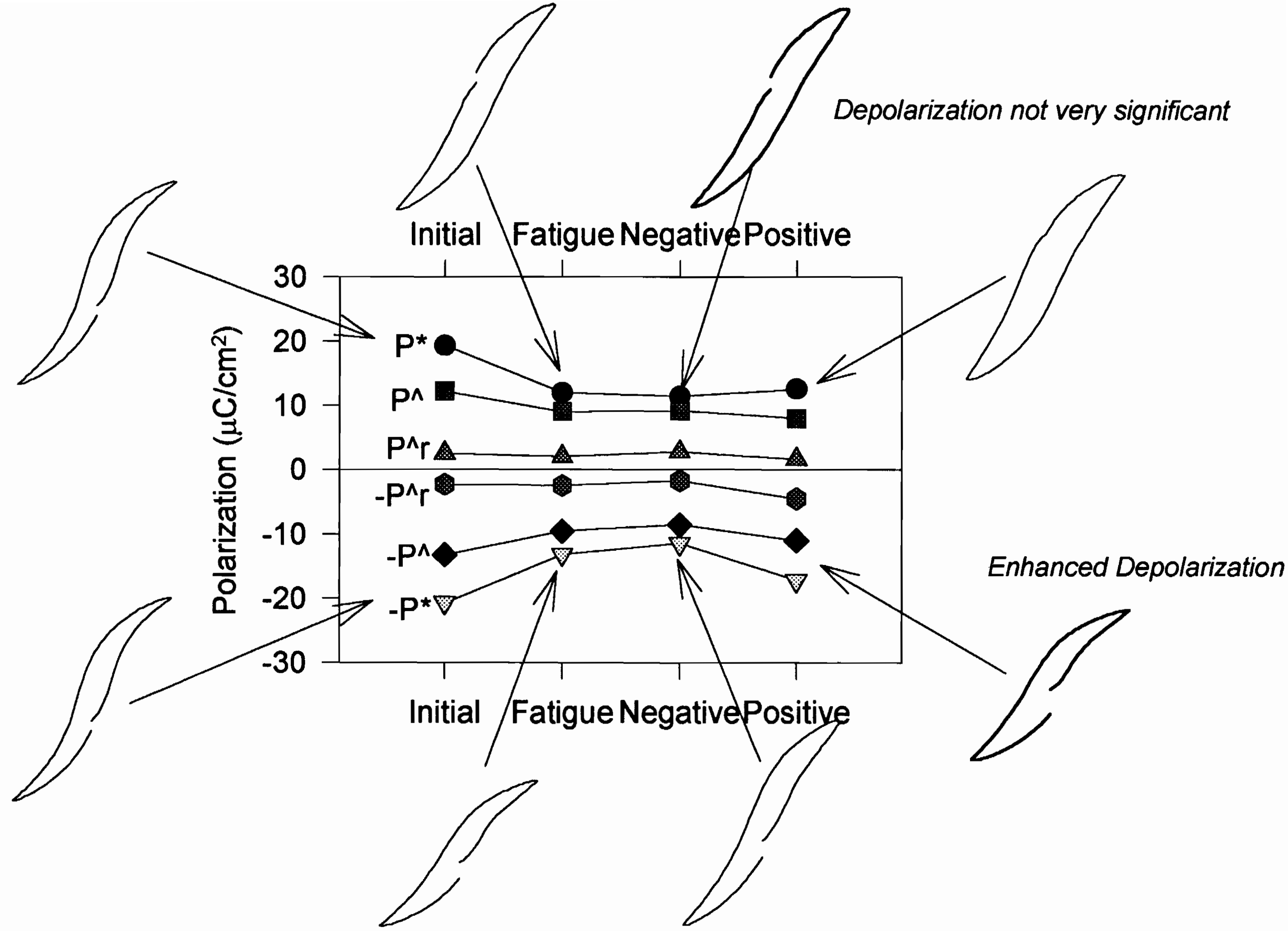


Fig A-14 Imprint in Pt/PZT/Pt (0.359μm) at 85°C

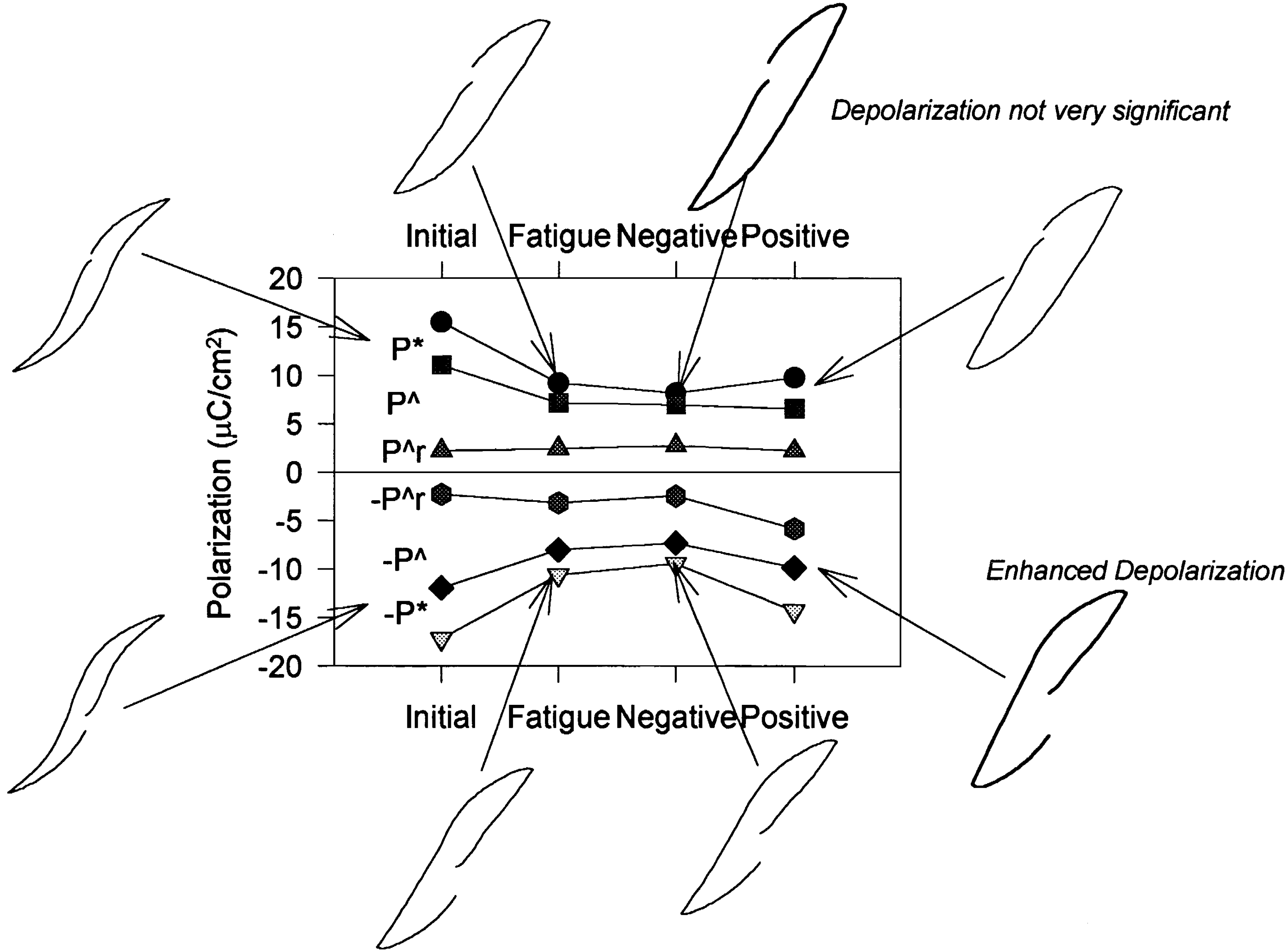


Fig A-15 Imprint in Pt/PZT/Pt (0.473μm) at 85^{o}C

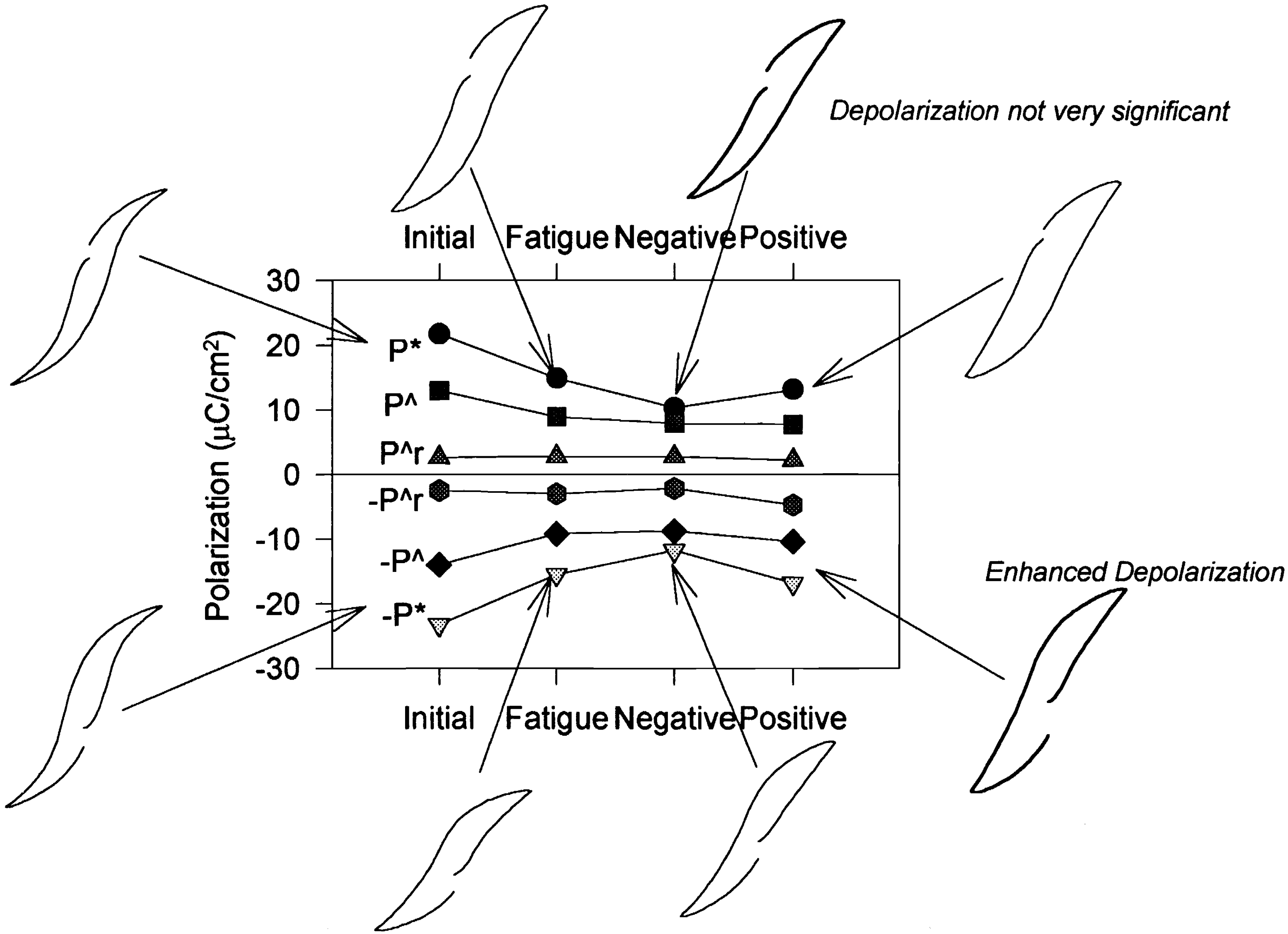


Fig A-16 Imprint in Pt/PZT/Pt (0.588μm) at 85^{o}C

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VITA

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Mayukh Bhattacharya

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