

ELECTRICAL CHARACTERIZATION
OF A MULTILAYER LOW TEMPERATURE CO-FIREABLE CERAMIC
MULTICHIP MODULE

by
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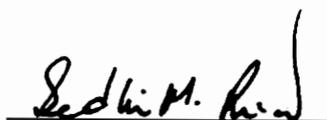
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ELECTRICAL CHARACTERIZATION
OF MULTILAYER LOW TEMPERATURE CO-FIREABLE CERAMIC
MULTICHIP MODULES

by
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(ABSTRACT)

The purpose of this research is to develop an understanding of Multichip Modules, (MCMs), more specifically those fabricated with a Low Temperature Co-fireable Ceramic (LTCC) tape systems. The study will consist of designing, processing, and testing two generic MCM test patterns. The effects on signal propagation caused by vias and wire bonds, crosstalk for surface and embedded transmission lines, crosstalk between vias, effects of bends in transmission lines are studied and discussed in this work. Time Domain and Frequency Domain measurements are performed and presented in this thesis work for electrical characterization of MCM structures using LTCC systems.

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CHAPTER 1

INTRODUCTION

1.1--Overview

The objective of this research is to perform an electrical characterization of a Multichip Module (MCM) fabricated from a multilayer, Low Temperature Co-Fireable Ceramic (LTCC) tape system. Two generic test modules are produced using DuPont's LTCC material, Green Tape™ 851AT. The modules consist of conductor patterns typically found in MCM applications. Among the conductor lines studied are crosstalk lines, wirebond lines, tee lines, and lines passing under and near ground planes. The effects of different types of bends and via patterns are also considered in this work.

Chapter 1 is a general introduction to MCM technology. Chapter 2 presents a literature survey of various published work in the MCM field, and more specifically, the ceramic MCM (MCM-C) field. Chapter 3 is a description of the two test packages, referred to as Generic Circuits I and II, performed in this work. Chapter 4 presents analysis of these sample modules from a Time and Frequency Domain perspective. Chapter 5 provides the summary, conclusions, and future work proposed in this area.

1.2--The Need for MCM Packaging

Today's packaging and interconnection technology is not consistent with the advances being made in the Integrated Circuit, more specifically, the trend towards higher pincount is demanding new forms of IC packaging which result in larger chip footprints^[1].

As digital circuit speeds increase, the need for a low propagation delay package continues to grow. The limiting factor in many high speed data processing units is the packaging technology used. A major source of delay in today's computers is the time required for a signal to pass from one chip to another.^[2] One of the most important merits of an effective package, is the delay time associated with it. Delay is controlled by distance between components and the speed at which the signal propagates. Propagation speed is directly proportional to the dielectric constant of the package used.^[3] The MCM packaging scheme eliminates 60% to 80% of the size of an equivalent printed circuit board layout. This redistribution results in a significant increase in system speed^[4]. Since parasitic capacitance and inductance along the length of the trace is reduced, circuit bandwidth is improved. A typical MCM system may include the following:^[5]

- Digital Signal processing circuits
- Memory arrays
- Mixed analog/digital circuits
- Multiple VLSI (Very Large Scale Integration) and ASIC (Application Specific Integrated Circuit) die packaging
- Analog to Digital and Digital to Analog data converters
- Microwave signal and power amplifiers
- Voltage regulators

1.3--An Overview of MCM-C's

The IPC defines an MCM-C as a multichip package or substrate in which the dielectric layer is a ceramic material.^[6] Multichip Modules (MCM) have been around for over 25 years. Ceramic Multichip Modules (MCM-C) were first used in the late 70's. Since then, more improved ceramic materials have been developed. These improved ceramic materials include Low Temperature Co-Fireable Ceramics (LTCCs). Before with High Temperature Cofired Ceramics (HTCCs), packages had to be fired at much higher temperatures, around 1600°C. Using these high firing temperatures required the use of special metals, such as molybdenum or tungsten. These metals do not have the high conductivity that copper, silver, and gold have. However with LTCCs, being fired at around 850-950°C, these high conductivity metals can now be used^[7].

1.4--The Need for LTCC's in MCM-C Packaging

Each MCM interconnect technology provides unique characteristics. Using LTCCs for MCM-Cs offer two main advantages. Being ceramic, they provide a hermetic seal. This gives MCM-Cs the opportunity to be used under higher humidity conditions. Secondly, because this is a multilayer technology, it allows the distribution of different interconnects to various layers. This distribution reduces the surface area required as compared to single layer techniques. Low Temperature Co-Fired Ceramics, (LTCC) provide a low dielectric constant, and allow these circuits to operate at much higher frequencies than allowed by conventional printed circuit boards^[8]. As discussed earlier, we know that with a lower dielectric constant, the propagation time will be much faster.

Allowing the use of gold, copper, aluminum, and silver, LTCCs provide for better transmission line conductivity.

This thesis is structured into five chapters; Chapter I is a general introduction. Chapter II is a literature review of published work related to Multichip Modules. Chapter III is a description of the two generic test packages. Chapter IV gives an analysis of the Time Domain and Frequency Domain measurements made of the two generic test packages. Finally, Chapter V provides conclusions of this research work.

CHAPTER 2

LITERATURE REVIEW

2.1--Introduction

The intent in this chapter is to highlight other studies related to this research work. There are several areas discussed in this project. Section 2.2 discusses the different types of multichip modules (MCMs). Section 2.3 discusses the use of Low Temperature Co-fireable Ceramics (LTCCs) in MCM applications. Section 2.4 discusses research conducted in the area of bends in transmission lines. Finally, section 2.5 discusses electrical crosstalk between conducting lines using LTCC systems.

2.2--Different Types of MCMs

MCMs are designated according to the technology incorporated within the substrate^[9]. Numerous references discuss the different types of MCMs used in today's market. The three main technologies used for MCM realization are:

- MCM-L, high-density, laminated printed-circuit boards.
- MCM-C, ceramic substrates, including High Temperature Co-Fireable Ceramic (HTCC), LTCC, and Aluminum Nitride.
- MCM-D, deposited metallization, including thin-film deposited substrates.

Blood and Carey^[10] discuss the three main types of MCMs, however they also designate MCM-Si, (substrates constructed with silicon wafers). Usually this type of MCM would be classified as MCM-D because of the deposited metallization on the silicon substrate. The authors make comparisons between each technology indicating the advantages and disadvantages of each. MCM-Si has the smallest trace pitch, although

MCM-D with the next lowest trace pitch, uses conductors with lower resistances.

MCM-L has been around the longest, and costs the least to produce. MCM-L products are very suitable for consumer electronics where low cost and low-to-medium power dissipation is desired. The authors discuss MCM-C technology as applied to high temperature co-fired ceramics, (HTCC), not to LTCCs. Many of the disadvantages encountered using HTCC systems are not present with the LTCC systems. HTCCs require the use of high resistance metals such as tungsten and molybdenum, whereas LTCCs use silver, copper, and gold, therefore firing occurs at much lower temperature with LTCC systems. The authors mention that HTCCs are very strong and relatively inert to handling and environmental exposure. Although LTCCs are more fragile, they are hermetically sealed, making them less susceptible to environmental conditions. In this regard, the authors seem to indicate that there is no single technology best suited for all applications, but that each technology is well suited for different applications.

Blood and Dixon^[11] state that MCM-L is capable of meeting cost requirements for high volume, cost sensitive systems. The authors state MCM-L technology will continue to move multichip modules into mainstream applications. The key advantage of MCM-L technology is low cost. There already exists an infrastructure for high volume production. MCM-L technology also has some disadvantages that need to be discussed, such as low routing density, poor thermal conductivity, a high coefficient of thermal expansion, and typically high electrical crosstalk.

Hargis^[12] discusses MCM-C technology. Materials used for MCM-Cs include alumina, the most mature and cost-effective material followed by LTCCs. LTCCs are the

most versatile of the materials. LTCC materials and procedures are compatible with standard or conventional thick-film processing. LTCC MCM-Cs possess an electrical conductivity over four times greater than thin-film MCM. LTCCs have the potential for low dielectric constants. The material systems in LTCC are not as well developed as alumina, but the potential for variable properties makes LTCCs very appealing.

The newest material for MCM-Cs is aluminum nitride. Aluminum nitride is an excellent thermal conductor, has a thermal expansion coefficient matching silicon, and performs well in high-frequency applications. Often, LTCCs are combined with aluminum nitride in order to take advantage of the best properties of each.

Sigliano^[13] discusses thin-film/deposited MCMs, (MCM-D). Dielectric constants run between 2-4 at about 10 MHz when using organic insulators such as polyquinoline, teflons, triazine, and BCB (bisbenzocyclobutenes). These materials have excellent dielectric constant, good adhesion and good mechanical properties, and are chemically resistant and some are photo-etchable. MCM-Ds possess the highest line densities, which result in short line lengths, thus improving delay times. MCM-D technology is usually an expensive technology that is only found addressing high-end niche market packaging solutions. MCM-D advantages include the use of high conductivity metals--gold, copper, and aluminum, and very fine outer lead bond pitch.

Based upon the previous references, along with others^[14], I have constructed this table in order to assist the reader to the characteristics of each technology possesses which characteristics, and how each technology compares to the others.

	MCM-L	MCM-C (HTCC)	MCM-C (LTCC)	MCM-D
Line/Space Density	0.005"	0.002"	0.002"	0.001"
Dielectric Coefficient	4.5 -- 5.0	9	5	2.4 -- 4.0
Structural Integrity	strong	strong	fragile	strong
Ability to Transfer Heat	fair	good	fair	good
Relative Cost	low	medium	medium	high
Maturity	excellent	good	good	good
High Volume Productivity	excellent	poor	poor	poor

2.3--The Use of LTCCs in MCMs

Amey^[15,16] points out that, "Packaging and interconnection has and will continue to limit electronic system performance." He goes on to point out that MCM-Cs can meet most of today's multichip packaging needs at a relatively lower cost, and lower risk. One reason that MCM-Cs contribute so much is due to the low dielectric constants of their materials. He also discusses applications which demonstrate the use of MCM-Cs produced by industry during the past 25 years. He mentions a stackable memory module developed by Harris GASD Corporation, Melbourne, FL. This memory module uses an LTCC from DuPont, known as Green Tape™. He also discusses a 32 x 32 bit switch, switching 310 Mb/s. Using the Green Tape™ system, consisting of a low dielectric

constant ceramic, and high conductivity conductors, this package was able to perform well, meeting the system delay requirements.

Schroeder^[17] begins his paper by making a case for multichip packaging, then goes on to make a case for using LTCCs in multichip packaging. He first states that MCM packaging eliminates 60% to 80% of the size of an equivalent printed circuit board layout, and this redistribution allows for improved speed and bandwidth of the package. He then goes on to compare materials used in multichip packaging. He contrasts LTCCs against high temperature co-fireable ceramics (HTCC), multilayer thin-film, and thick-film. One advantage of LTCC over HTCC is that LTCC allows the use of gold, silver, and copper, instead of molybdenum and tungsten which is required for HTCC. Using these high performance metals as conductors allows for better signal trace conductivity resulting in optimum electrical performance. LTCCs do not expose the package to as high of a thermal shock as HTCCs. He also mentions the two main disadvantages of LTCC. First, that LTCC has a lower thermal conductivity than HTCC, and second, LTCC is very brittle. LTCC has a flexural strength of 38K psi whereas alumina's flexural strength is 48K psi, and HTCC is 60K psi. Schroeder performed the following four tests on a 1.8" x 1.8" hermetic LTCC MCM with 0.025" pitch leads with no failures. The four tests were:

- 10,000 G acceleration per MIL-STD-883, Test Method 2001.
- -65°C to 150°C temperature cycle per MIL-STD-883, Test Method 1010, Condition C.
- 1500g .5ms shock 6 axis per MIL-STD-883, Test Method 2002, Condition B.
- 20g logarithmic 20-2000 Hz vibration 3 axis per MIL-STD-883, Test Method 2007, Condition A.

2.4--The Effects of Transmission Line Bends

Rainal^[18] discusses the effects of bends in transmission lines. He tests 45, 90, and 180 degree bends, and provides formulas for each. He shows that "...the magnitude of a reflected wave from a 90 degree bend is comparable to the magnitude of the reflection associated with an equivalent capacitive discontinuity of a few tenths of a picofarad." He also discusses that zero reflection conditions are approached when the bend is gradual, such as a rounded corner to avoid discontinuities. A 45 degree mitered bend reduces maximum reflection from 4.743% to 4.518%. Reflections from the bends are capacitive in character. He measures the signal reflections from these bends and records their equivalent capacitances. The 45, 90 and 180 degree bends are 0.181, 0.190, and 0.192 pF, respectively. He concludes for bit rates near a few gigabits per second and common dielectrics, that 90 degree bends will suffice, however for higher bit rates, more gradual bends are needed.

2.5--Crosstalk within LTCCs

Francomacaro, et. al.^[19] discuss a Gallium Arsenide-based, high-speed direct digital synthesizer packaged on a LTCC, more specifically, Green Tape™. He discusses the criteria that were needed to be met in order to successfully package this GaAs chip.

- multiple conductor levels for signal layers and distributed power and ground planes
- lines and spaces narrow enough to wire high lead count chips
- high conductivity conductors
- low dielectric constant for high-speed pulse propagation

- dielectric layers thick enough to allow construction of 50 ohm transmission line interconnects with readily achievable line widths
- capability to remove heat directly from the GaAs die

LTCCs meet all of the previous requirements which make this an ideal packaging material for this and other high-speed applications. He then discusses the electrical considerations in designing this package. He performed crosstalk analysis on parallel coupled dual striplines. He concludes that line-to-line spacing should be approximately 2 linewidths. He simulated these lines with SPICE[®], using 600 Mhz trapezoidal pulse with 150 picosecond rise and fall times. The crosstalk was estimated to be less than 5% of the voltage swing. Upon fabrication, measurements were made, and he states that the measured values are with 2% of those values which were predicted.

2.6--Conclusion

In this chapter we have reviewed different studies related to the work in this thesis. MCM-L, MCM-C, and MCM-D have been defined and discussed. Next, LTCCs, as applied to MCM-C, were discussed. Transmission line bend effects were reviewed. Finally, crosstalk within LTCCs was discussed.

CHAPTER 3

DESCRIPTION OF THE TEST PACKAGES

3.1--Introduction to Generic Circuit I

The purpose of this chapter is to give the reader a detailed description of the two test packages used to conduct this research work. The dimensions given are post-fired, unless otherwise specified. Shown in figure 3-1 is the first of two test modules, referred to as Generic Circuit I. Generic Circuit I has a substrate with a thickness near 0.025" (0.635 mm). The outer dimensions of the substrate are 2.05" x 2.05" (52.07 mm x 52.07 mm). The height of the wall is also 0.025" (0.635 mm). The inside dimensions of the cavity are 1.340" x 1.340" (34.04 mm x 34.04 mm). The outside dimensions of the wall are 1.696" x 1.696" (43.08 mm x 43.08 mm). The bottom ground plane was sputter deposited with Aluminum, and has a thickness of 0.0136 μm . The perimeter measurement pads all have the same dimensions of 0.0400" x 0.0400" (1.016 mm x 1.016 mm).

3.1.1--Serpentine Via Pattern

The serpentine via pattern, shown in figure 3-2, consists of ten vias in a snake-like pattern. The conductor lines alternate, through the ten vias, between the top and middle layers. The spacing, starting from the left, is 0.202" (5.13 mm) center-to-center for the first four vias, and 0.101" (2.57 mm) center-to-center for the last six vias. The distance separating the two conductors, that is the height of the connecting vias, is 0.007" (0.18 mm).

3.1.2--Staggered Via Pattern

The staggered via pattern, shown in figure 3-3, consists of vias organized similar to the serpentine via pattern, however, it is a step-like structure. Beginning at the top, there is a conductor line, then a via steps down to the middle conductor, then a via steps down to the bottom conductor layer. This continues back up to the top, and then continues again with a different distance separating the vias. The via spacing is 0.202" (5.13 mm) for the first section, and 0.101" (2.57 mm) for the second section, respectively.

3.1.3--Wire Bond Line

The wire bond line pattern, shown in figure 3-4, consists of a line broken in the middle, terminated by two bonding pads having dimensions of 0.025" x 0.025" (0.635 mm x 0.635 mm). The spacing between the two bonding pads is 0.100" (2.54 mm). There is a conductor pattern next to the actual wire bond line used for reference purpose. This wire bond reference is identical to the wire bond line, except the reference line has a conductor line connecting the two pads, whereas the wire bond line has a 0.001" (25.4 μ m) diameter gold wire bond connecting the two pads.

3.1.4--High Frequency Signal Line

The high frequency signal line, shown in figure 3-5, is a dual ground-plane, constant strip-width signal line which is used to reduce the effects of the wall regions on signal propagation. This line has a width of 0.009" (0.229 mm). The middle ground planes has the same dimensions as the signal strip itself, and is located 0.0075" (0.1905 mm) below the high frequency signal strip. The stripline portion is designed as unequal

dielectric height stripline and the dielectric heights for the upper and the lower dielectrics are 0.0011" (27.94 μm) and 0.0025" (63.5 μm), respectively. The middle ground planes are connected to the bottom ground planes through five vias. Three vias connect the middle ground plane inside the cavity and have a via spacing of 0.4331" (11.00 mm), while two vias connect the two middle ground planes outside the cavity and their vias are located 0.1126" (2.860 mm) from the edge of the substrate.

The high frequency signal strip has slightly different designs at the two ends. On one end, the middle ground planes end right at the interfaces, while at the other end the middle ground planes end 0.0433" (1.100 mm) away from the interfaces.

3.1.5--5 and 10 mil Embedded and Surface Crosstalk Lines

The 5 and 10 mil embedded and surface crosstalk lines, shown in figure 3-6, are dependent upon the dielectric surrounding the two signal lines, therefore the crosstalk for embedded lines is different for surface lines. The 5 mil lines have 0.005" (0.127 mm) line width, and 0.005" (0.127 mm) separation between the two lines. The 10 mil lines likewise have 0.010" (0.254 mm) line width, and 0.010" (0.254 mm) spacing respectively.

3.1.6--Ground Plane Proximity Line

The ground plane proximity line, shown in figure 3-7, is used to determine the effects of a ground plane on a signal line when the line passes close to the ground plane. This line is 0.0090" (0.2286 mm) wide. It passes near the ground plane at a separation distance of 0.0224" (0.5690 mm).

3.1.7--Ground Plane Underpass Line

The ground plane underpass line is also shown in figure 3-7. This line is used to determine the effects of a ground plane when the signal line passes under it. The underpass line is 0.0090" (0.2286 mm) wide and passes 0.0109" (0.2769 mm) under the ground plane.

3.2--Introduction to Generic Circuit II

Shown in figure 3-8 is the second of the two test patterns, referred to as Generic Circuit II. The dimensions given are post-fired, unless otherwise specified. Generic Circuit II has a substrate thickness of 0.0250" (0.6350 mm). The outer dimensions of the substrate are 2.05" x 2.05" (52.07 mm x 52.07 mm). The inside dimensions of the cavity are 1.340" x 1.340" (34.04 mm x 34.04 mm). The outside dimensions of the wall are 1.696" x 1.696" (43.08 mm x 43.08 mm). The height of the wall is also 0.0250" (0.6350 mm). The bottom ground plane was sputter deposited with Aluminum, has a thickness of 1.1 μm .

3.2.1--90 Degree Bend and 90 Degree Tee

The purpose of the 90 degree bend line, shown in figure 3-9, is to study the effects of different types of bends in conductor lines. The length of this line along the horizontal direction is 0.8960" (22.76 mm) and 0.7110" (18.06 mm) along the vertical direction, respectively. The line thickness is 0.009" (0.2286 mm). The 90 degree tee, also shown in figure 3-9, is identical to the 90 degree bend, with the exception that the end of the lines

being split off into two endpoints. The two tee lines are separated by a distance of 0.1200" (3.048 mm).

3.2.2--45 Degree Bend and 45 Degree Tee

The 45 degree bend line, shown in figure 3-10, is similar to the 90, with the exception of the horizontal and vertical lengths of the line. The lengths are 0.6310" (16.03 mm) and 0.5660" (14.38 mm), along the horizontal and vertical directions, respectively. The 45 degree tee is shown in figure 3-10. It has identical dimensions to the 45 degree bend line.

3.2.3--Rounded Bend and Rounded Tee

The rounded bend, shown in figure 3-11, was designed by taking a 90 degree bend, and rounding the corner. A radius of 0.0250" (0.635 mm) was used. The horizontal and vertical lengths of the line, excluding the radius, are 0.3910" (9.931 mm) and 0.4460" (11.33 mm), respectively. The rounded tee is shown in figure 3-11. It has identical dimensions to the rounded bend line.

3.2.4--Wire Bond Lines

The wire bond lines for Generic Circuit II were devised in order to obtain a comparison of different length bonds. Bonding pads are identical to those in Generic Circuit I, 0.030" x 0.030" (0.762 mm x 0.762 mm). Separation distances of 0.030" (0.762 mm) and 0.100" (2.54 mm) are included in Generic Circuit II.

3.2.5--Via Crosstalk Lines

Via crosstalk lines, shown in figure 3-12, are used to measure the crosstalk between vias. Two lines go towards each other, meet near the middle, then vias carry the signal to the ground plane at the bottom. The vias, like all others in this package, are 0.005" (0.127 mm) in diameter. The edge-edge separation distances are 0.005" (0.127 mm), 0.010" (0.254 mm), and 0.015" (0.381 mm), respectively.

3.2.6--Staggered Via Pattern Revisited

The staggered via pattern in Generic Circuit II is identical to that included in Generic Circuit I. The purpose of duplicating this portion was to obtain the frequency/time domain measurements not made on Generic Circuit I.

3.2.7--Ground Plane Underpass Line Revisited

The ground plane underpass line in Generic Circuit II is identical to that included in Generic Circuit I. The purpose of repeating this portion was to obtain the frequency/time domain measurements not performed on Generic Circuit I.

3.3--Conclusion

This chapter has provided the reader with a description of the two test modules fabricated for this work. Dimensions (lines, ground planes, etc...) for Generic Circuit I and II were kept as close as possible to each other in order to maintain consistency between the two measurements. Figures 3-1 through 3-12 show the geometry of each pattern. Both test modules consist of 14 layers of tape each. The bottom seven composed the active portion, and the top seven were used to build up the wall structure. Processing steps of these two modules are explained with more detail in Appendix A, Green Tape™ Processing.

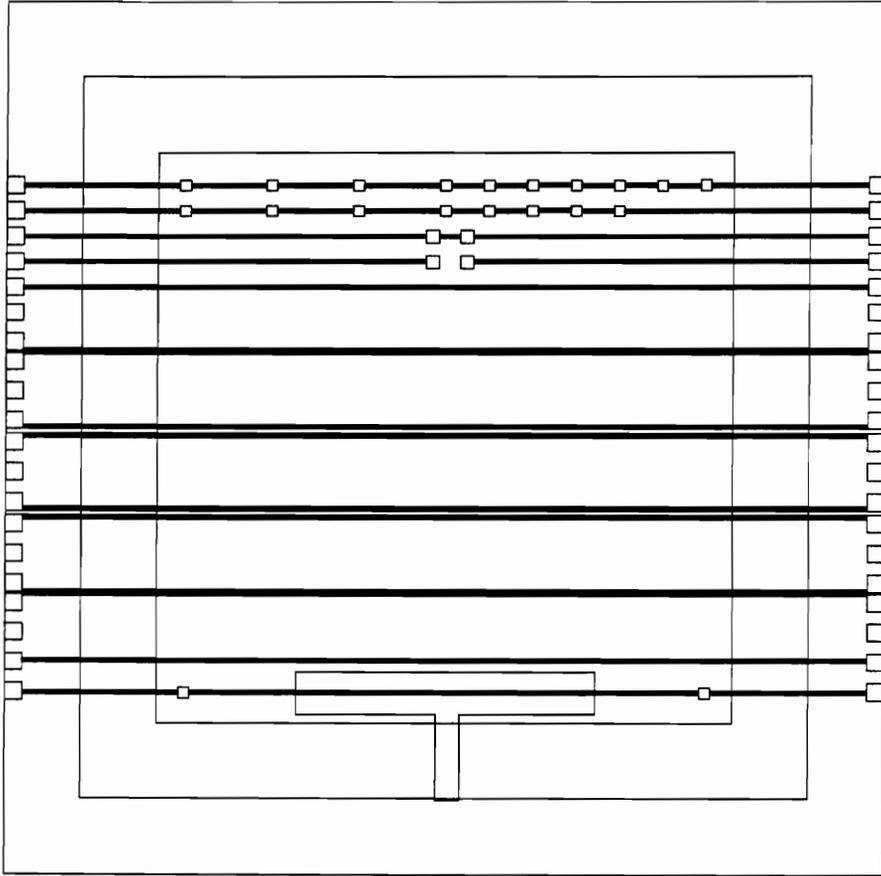


Figure 3-1
Generic Circuit I

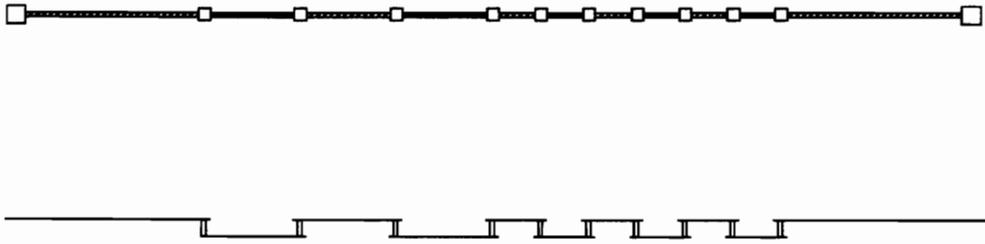


Figure 3-2
Serpentine Via Pattern
(Top and Side Views)

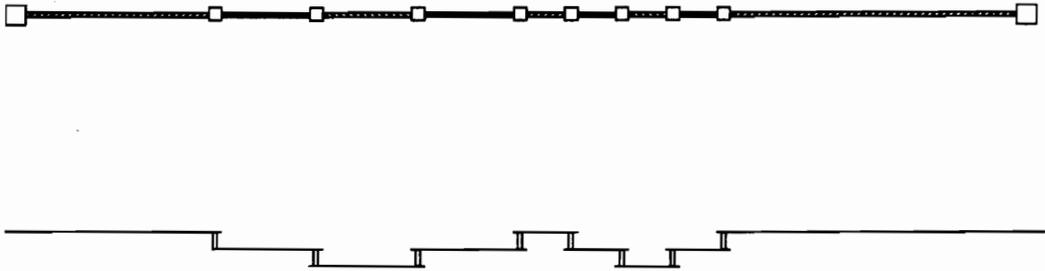


Figure 3-3
Staggered Via Pattern
(Top and Side Views)

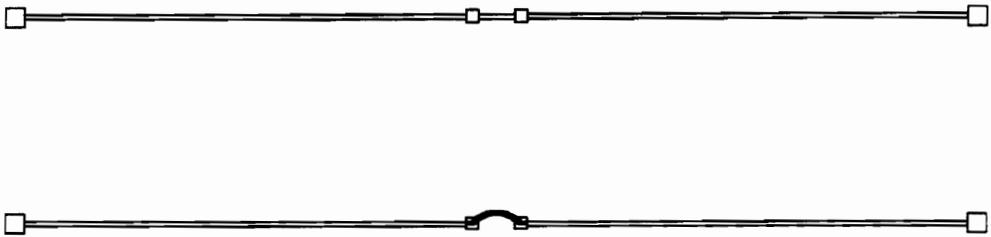


Figure 3-4

Wire Bond Reference Line and Wire Bond Line

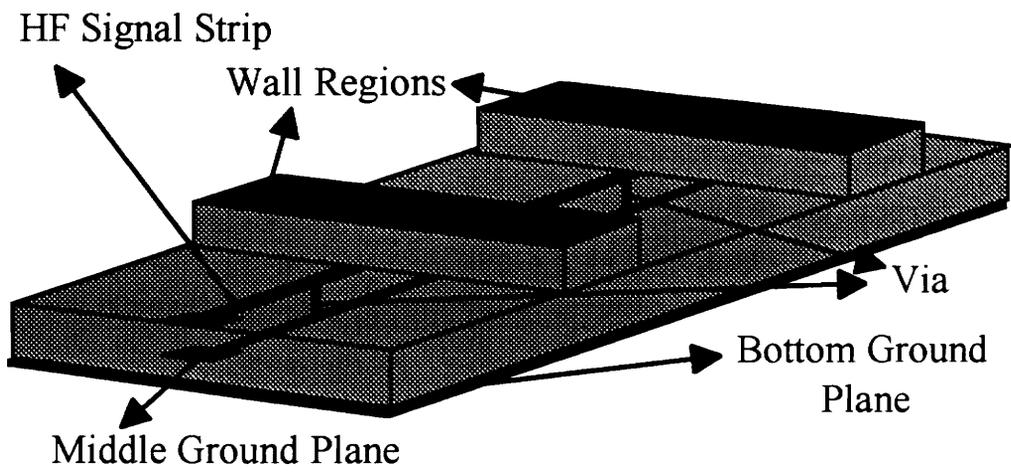


Figure 3-5

High Frequency Signal Line

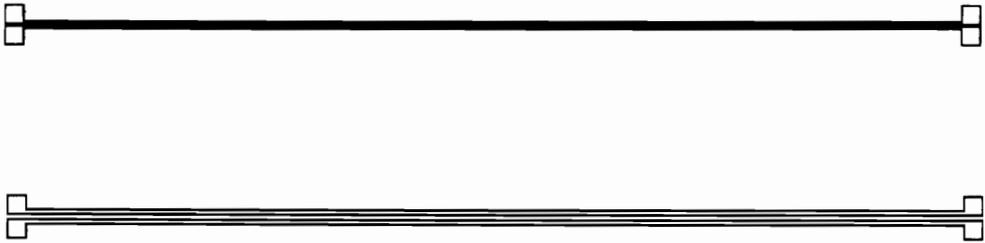


Figure 3-6

5 and 10 mil Crosstalk Lines

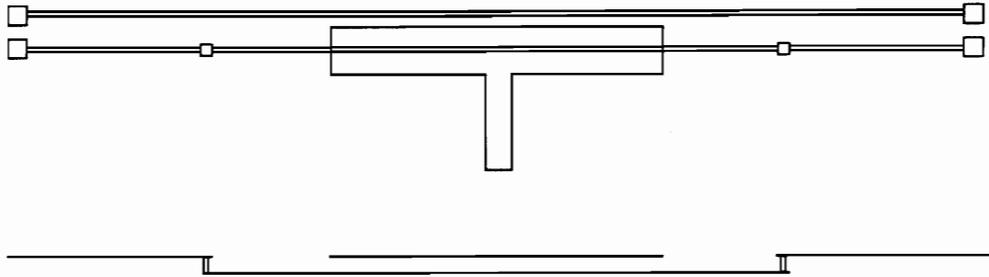


Figure 3-7

Ground Plane Proximity Line and Ground Plane Underpass Line

(Top and Side Views)

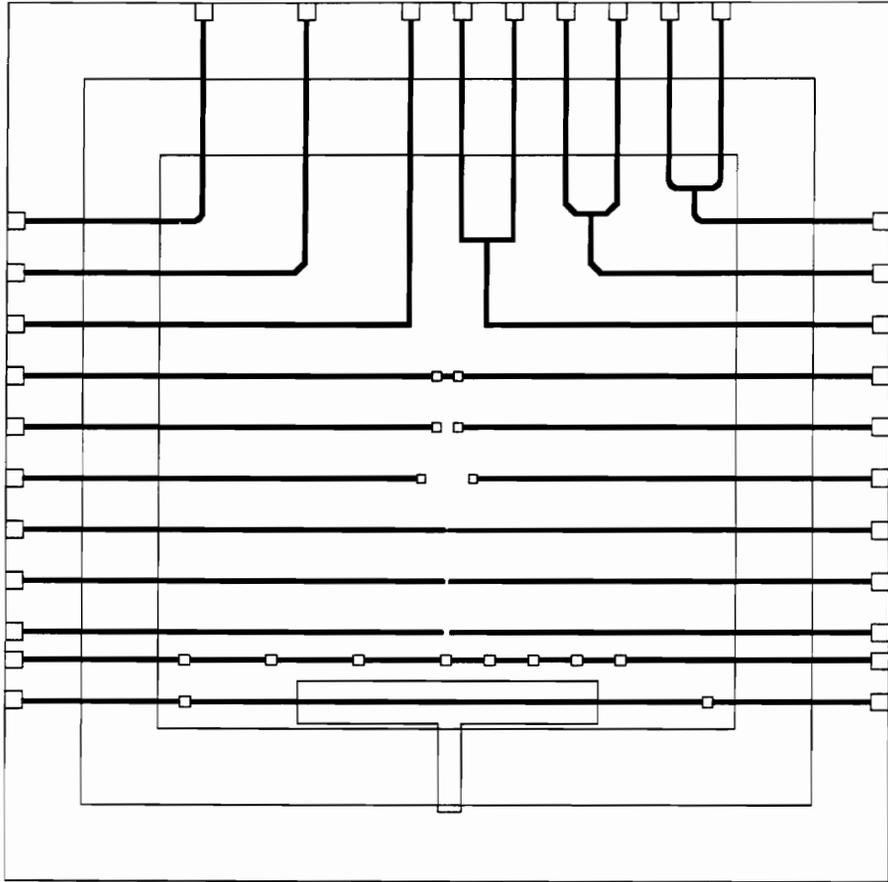


Figure 3-8
Generic Circuit II

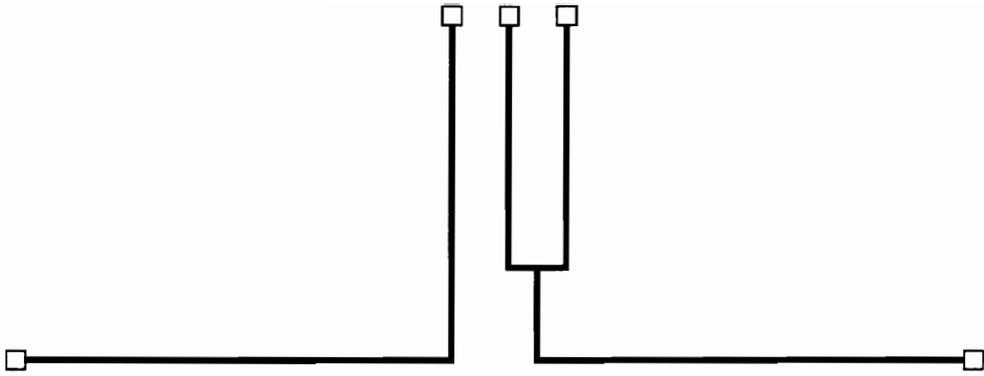


Figure 3-9

90 Degree Bend and 90 Degree Tee

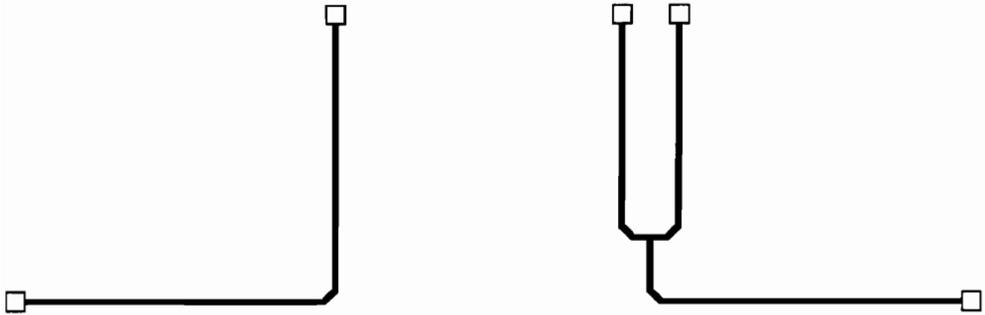


Figure 3-10

45 Degree Bend and 45 Degree Tee



Figure 3-11

Rounded Bend and Rounded Tee

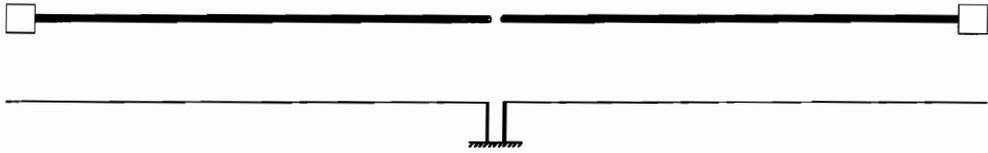


Figure 3-12
Via Crosstalk Lines
(Top and Side Views)

CHAPTER 4

ANALYSIS OF TIME AND FREQUENCY DOMAIN

MEASUREMENTS OF THE TEST PACKAGES

4.1--Introduction

The purpose of this chapter is to give the reader an analysis of the Time Domain and Frequency Domain measurements performed on the two test packages used during this research. The test setup for the Time Domain measurements, and the Frequency Domain measurements will be described. Both Time and Frequency Domain measurements from the various patterns of both Generic Circuit I and II, will be illustrated and discussed.

4.2--Tests Setup

Time Domain Measurement Setup. The Time Domain test setup consists of a Hewlett-Packard 54124A Four Channel Test Set connected to a Hewlett-Packard 84120A Digitizing Oscilloscope Mainframe. The Test Set generates a pulse of <45 ps rise time with a magnitude of 0.0 Volts \rightarrow 0.2 Volts. The Digitizing Oscilloscope displays the waveform and sends the waveform to a computer for storage and data processing.

The Time Domain Measurement results show the signal distortion, due to the different discontinuities, as the pulse propagates along the length of the conductor.

Frequency Domain Measurement Setup. The Frequency Domain Measurement setup consists of a Hewlett-Packard 8510B Vector Network Analyzer. The Network Analyzer is capable of performing measurements from 45 MHz to 40 GHz.

The Frequency Domain Measurement results show the bandwidth limitations and the expected signal loss due to the different discontinuities.

4.3--Generic Circuit I

Time and Frequency Domain measurements of the different lines of Generic Circuit I are illustrated and discussed. The TDR reference waveform for Generic Circuit I is illustrated in Figure 4-1.

4.3.1--Serpentine Via Pattern

Shown in Figure 4-2 is the TDR waveform of the serpentine via pattern. The reflections from the two wall regions can be clearly seen. Due to the dielectric height under the conductor changing with each via transition, the characteristic impedance of each segment also changes. The variation in the characteristic impedance results in discontinuities and their effect is visible in the TDR waveform. Shown in fig. 4-3 is the s_{11} measurement of the serpentine via pattern. This measurement shows that this type of via pattern can be used if the frequency of operation is below 2 GHz. Generic Circuit I shows a resonance at 1 GHz.

4.3.2--Staggered Via Pattern

Shown in Figure 4-4 is the TDR waveform of the staggered via pattern. In this pattern, the variation in the dielectric heights is significantly greater. This results in the discontinuities in the TDR waveform being much more pronounced than in the Serpentine Via pattern. It was impossible for Frequency Domain measurements to be made on the Staggered Via pattern, however the pattern will be revisited with Generic Circuit II.

4.3.3--Wire Bond Line

Shown in Figure 4-5 is the TDR waveform of the wirebond reference line. The reflection due to the bonding pads can be observed. Shown in Figure 4-6 is the TDR waveform of the actual wirebonded line. By comparing this waveform with the reference line, it is noted that the wire bond does not incorporate significant discontinuity in the path of the signal if the frequency of operation is below 2 GHz.

4.3.4--High Frequency Signal Line

Shown in Figure 4-7 is the TDR waveform of the High Frequency (HF) Signal line. It is observed that the presence of the middle ground plane vias result in the incorporation of some discontinuities in the signal propagation path. Since there is a finite resistance associated with the middle ground plane and the bottom ground plane therefore a potential and hence a capacitance exists between the two. This capacitance vanishes whenever there is a ground plane connecting via. Since this capacitance is very low, it is

this capacitance that determines the characteristic impedance of the HF Signal Strip. At the via locations, the only capacitance left is the HF Signal Strip to middle ground plane capacitance. As this capacitance is higher in value it results in a lower characteristic impedance for the portion of the HF Signal Strip. Shown in Figure 4-8 is the TDR waveform of Port 2 of the high frequency line. In this case the middle ground plane ends at a distance of 1.1 mm from the walls. This case results in the reflection from the discontinuity at the wall region being slightly less pronounced. Shown in Figure 4-9 is the s_{11} measurement of the high frequency line. The s_{11} plot shows that below 1 GHz the HF Signal Strip has lower than -10 dB reflection. The s_{11} plot also shows the package resonance at 1 GHz.

4.3.5--5 and 10 mil Embedded and Surface Crosstalk Lines

Shown in Figure 4-10 is the crosstalk data for the embedded 5 mil crosstalk lines. Shown in Figure 4-11 is the crosstalk data for the embedded 10 mil crosstalk lines. Shown in Figure 4-12 is the crosstalk data for the surface 10 mil crosstalk lines. The launcher used for these measurements provides valid data up to only 2 GHz. It is observed that the crosstalk is below -20 dB for frequencies below 1 GHz. As the signal propagates along the length of the line it is degraded by the resistance of the line, therefore the measured crosstalk for the far end is less than the measured crosstalk for the near end. Comparing the embedded and surface 10 mil lines, it is observed that the embedded lines have less crosstalk than the surface lines for the far end measured data. This is the result of the embedded lines being more lossy than the surface lines. During the firing cycle the

glass from the ceramic gets embedded in the co-fireable conductor paste, and thus increases the conductor loss.

4.3.6--Ground Plane Proximity Line

Shown in Figure 4-13 is the TDR waveform of the ground plane proximity line. In the portion where this line runs close to the ground plane, its characteristic impedance changes and results in a discontinuity. This change in the characteristic impedance is also attributed to the secondary capacitance between the line and the ground plane. This capacitance is lower in value than the capacitance between the line and the bottom ground plane and hence reduces the overall capacitance and thus increases the characteristic impedance of the line. Shown in Figure 4-14 is the s_{11} measurement for the ground plane proximity line. The measured s_{11} data for this line shows higher reflection than the HF Signal Strip. This data also shows the package resonance at 1 GHz.

4.3.7--Ground Plane Underpass Line

Shown in Figure 4-15 is the TDR waveform of the ground plane underpass line. Since in this portion the line is very similar to an unequal dielectric height stripline, its capacitance increases. The increased capacitance, in turn, decreases the characteristic impedance, as observed in the TDR waveform.

4.4--Generic Circuit II

Shown in Figure 4-16 is the TDR reference waveform for Generic Circuit II. This waveform was acquired by using the Hewlett Packard open circuit standard. The small step in front of the main transition indicates that the impedance of the system does not exactly match that of the reference standard.

4.4.1--90 Degree Bend and 90 Degree Tee

The TDR and TDT measurements of the 90 Degree Bend and the 90 Degree Tee Lines are presented in Figures 4-17 and 4-18, respectively. From the TDR waveforms we observe that the line impedance is slightly greater than 50 ohms. The 90 Degree Bend Line has a much more uniform impedance than the 90 Degree Tee Line. The 90 Degree Tee Line shows a capacitive load at the intersection. The TDT measurement of the tee line shows a much slower rise time than what was measured in the bend line, due to the capacitive nature of the intersection at the tee. The Frequency Domain measurements of these two lines are illustrated in Figures 4-19 and 4-20. These measurements show that the 90 Degree Tee Line is affected by capacitive loading at slightly lower frequencies as compared to the frequencies achieved by the 90 Degree Bend Line.

4.4.2--45 Degree Bend and 45 Degree Tee

The TDR and TDT measurements of the 45 Degree Bend and the 45 Degree Tee Lines are presented in Figures 4-21 and 4-22, respectively. From the TDR waveforms we

observe that these lines have an impedance slightly greater than 50 ohms. Like the 90 Degree Bend Line, the 45 Degree Bend Line has a much more uniform impedance than the 45 Degree Tee Line. The 45 Degree Tee Line shows a capacitive load at the intersection. The TDT measurements show that the larger capacitance of the tee line results in a much slower rise time than what was measured in the 45 Degree Bend Line. The Frequency Domain measurements of the 45 Degree Bend Line and the 45 Degree Tee Line are shown in Figures 4-23 and 4-24, respectively. These measurements show that the 45 Degree Tee Line is more affected by capacitive loading at slightly lower frequencies than the 45 Degree Bend Line.

4.4.3--Rounded Bend and Rounded Tee

The TDR and TDT measurements of the Rounded Bend and Rounded Tee Lines are presented in Figures 4-25 and 4-26, respectively. The Rounded Bend and Tee Lines show the slowest rise time, as compared to the 90 and 45 Degree Lines. This is due mainly to the length of the rounded lines being shorter than the 90 and 45 Degree Lines. The Frequency Domain measurements of the Rounded Bend and Rounded Tee Lines are presented in Figures 4-27 and 4-28, respectively. Due to the rounded bends being less capacitive than the 90 Degree Bends, the capacitive loading does not affect the Tee Line as much, explaining the similarity of the frequency measurements of the Rounded Bend Lines and Rounded Tee Lines.

4.4.4--Wire Bond Lines

The TDR and TDT measurements of the Wire Bond lines are shown in Figure 4-29 and 4-30, respectively. From a TDR and TDT perspective, the different length wire bonds do not show much effect on the electrical performance due to the short length of the wirebond (100 mils and 30 mils). The Frequency Domain measurements of the Wire Bond Reference Line, 30 mil Line, and the 100 mil Line are shown in Figures 4-31, 4-32, and 4-33, respectively. The different length bonds seem to have only a small effect on electrical performance from a Frequency Domain perspective, also.

4.4.5--Via Crosstalk Lines

Crosstalk measurements of the 5 mil, 10 mil, and 15 mil coupled vias are illustrated in Figures 4-34, 4-35, and 4-36, respectively. Changing the spacing between the coupled vias shows little difference due to the small length of the coupling portion of the vias (25 mils) and coupling between the measurement probes.

4.4.6--Staggered Via Pattern (*Revisited*)

The TDR and TDT measurements for the Staggered Via Line, Generic Circuit II, are illustrated in Figures 4-37 and 4-38. The staggered via line has a significant variation in dielectric heights, thus changing the characteristic impedance of the line. This mismatch limits the performance of the staggered via pattern at the higher frequencies as shown from the Frequency Domain measurements given in Figure 4-39.

4.4.7--Ground Plane Underpass Line (*Revisited*)

The TDR measurement of the Ground Plane Underpass Line is illustrated in Figure 4-40. Similar to the staggered via line, the Ground Plane Underpass Line has unequal dielectric height, causing an increase in capacitance, resulting in a lower characteristic impedance, as observed in the TDR waveform. Unfortunately, TDT and s_{11} measurements were not possible due to fracture of the part during the clamping and mounting in the test fixture.

4.5--Conclusion

Time Domain and Frequency Domain measurements have been performed and presented. The test setup for these measurements has been described. Analysis of these measurements has been given. MCM capabilities of LTCC tape systems have been demonstrated. The two MCM test packages have been shown to provide adequate performance for frequencies of operation below 1 GHz, compatible with the requirements of today's digital circuits.

The via pattern lines demonstrate that if the characteristic impedance of the different segments are matched then the discontinuities associated with these lines can be reduced. Signal lines passing close to the ground planes must be designed such that the change in the overall capacitance is small. We have seen from Generic Circuit I that embedded lines have less crosstalk when compared to surface lines. Referring to the 90, 45 and rounded bend/tee lines, we observe the line impedance is slightly greater than 50 ohms. Also observed, the bend lines have a much more uniform impedance than the tee

lines. The tee lines show a capacitive load at the intersection. Observing the TDT measurements of the 90, 45, and rounded bend/tee lines, we see that the larger capacitance of the tee lines results in a much slower rise time than what was measured in the bend lines. The s_{11} measurements of the 90 degree bend line and tee line are relatively similar. There seems to be little improvement when going to the 45 degree bend and tee lines as opposed to using a 90 degree bend. The tee lines, at lower frequencies, appear to behave similarly to the bend lines. However at higher frequencies, capacitive loading starts to take effect in the tee lines, before doing so in the bend lines. As seen from both test packages, the different lengths of wirebonds do not show much effect on the electrical performance, due mainly to the short length itself (100 mils) from a TDR and TDT perspective. This is also true for the Frequency Domain measurements (s_{11}). Changing the spacing between the coupled vias shows little difference due to the small length of the coupling portion of the vias (only 25 mils) and coupling between the measurement probes. The staggered via line has a significant variation in dielectric heights, thus changing the characteristic impedance of the line. This mismatch limits the performance of the staggered via pattern at the higher frequencies.

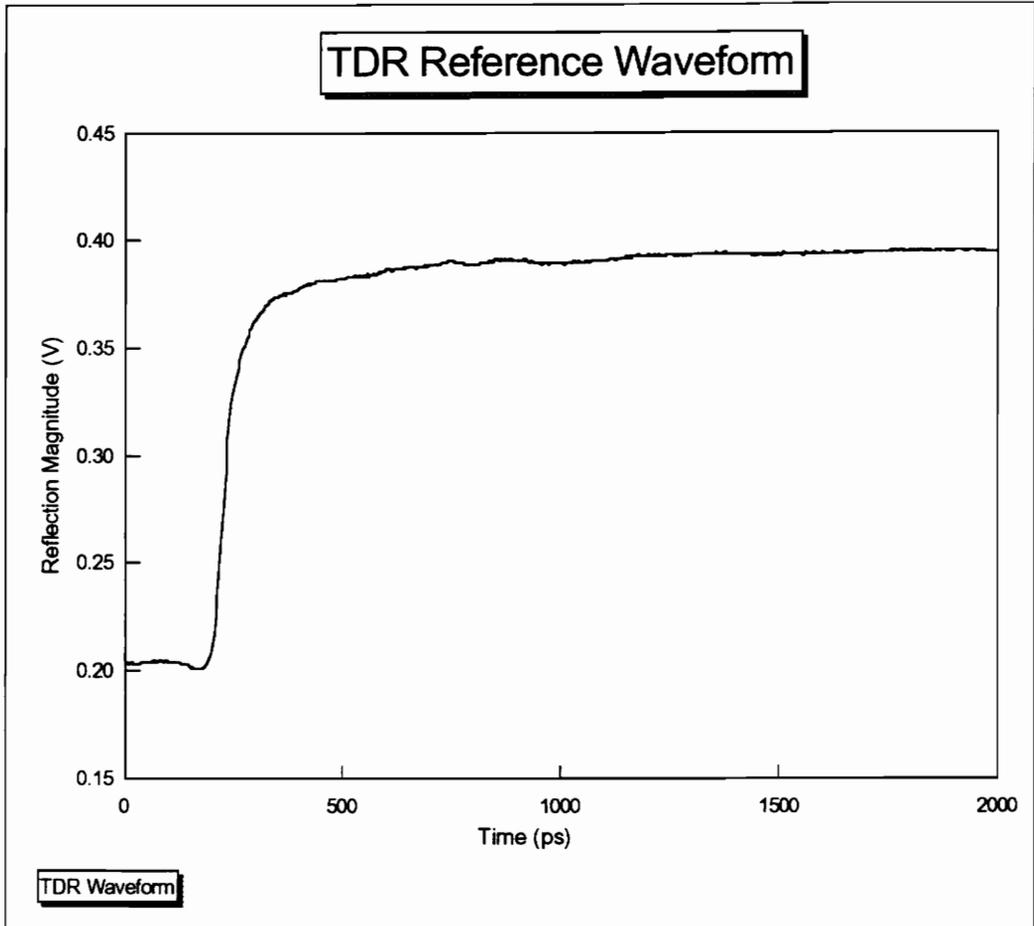


Figure 4-1

TDR Reference Waveform

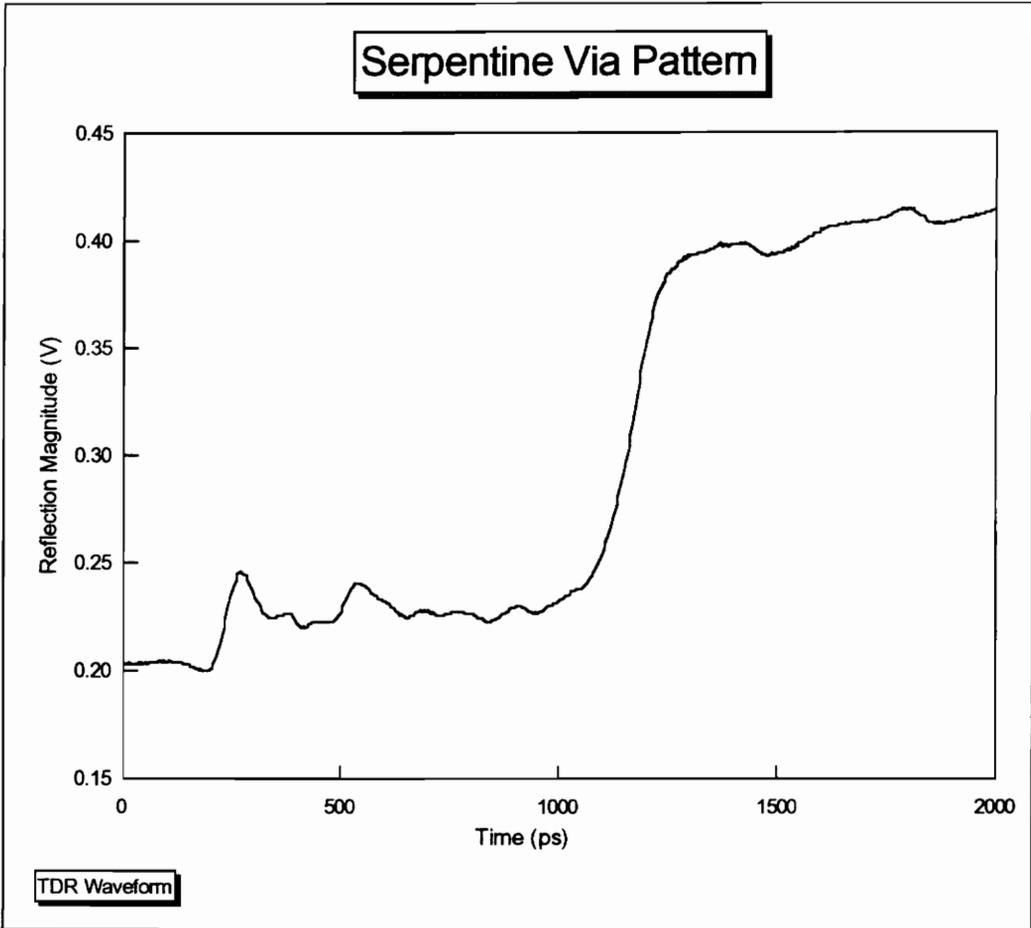


Figure 4-2
Serpentine Via Pattern
TDR Waveform

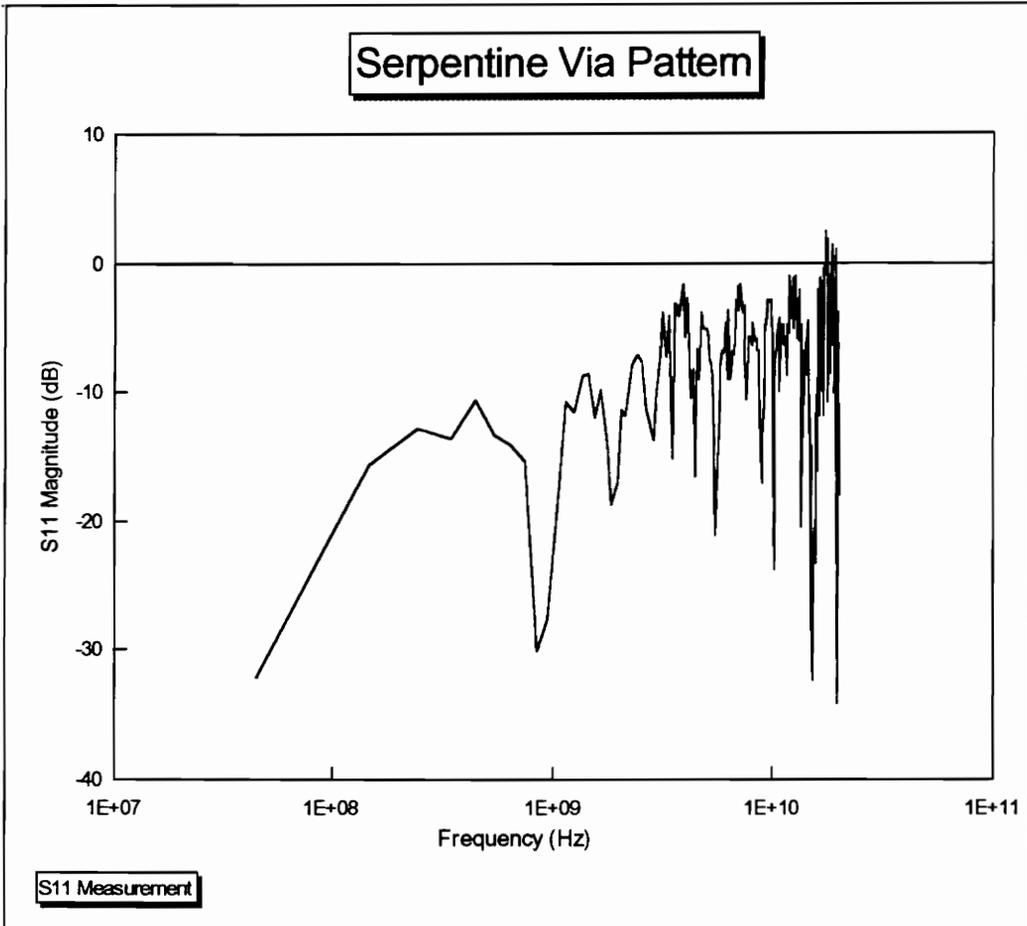


Figure 4-3
Serpentine Via Pattern
 s_{11} Measurement

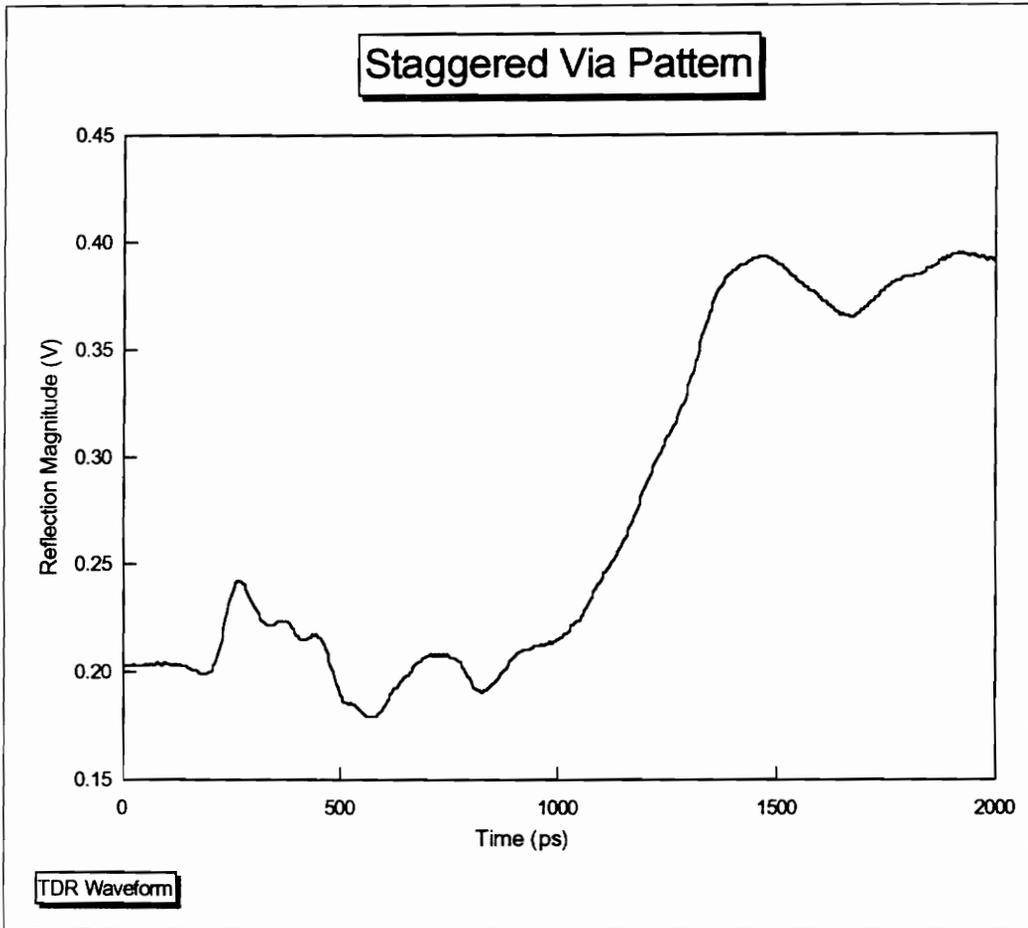


Figure 4-4
Staggered Via Pattern
TDR Measurement

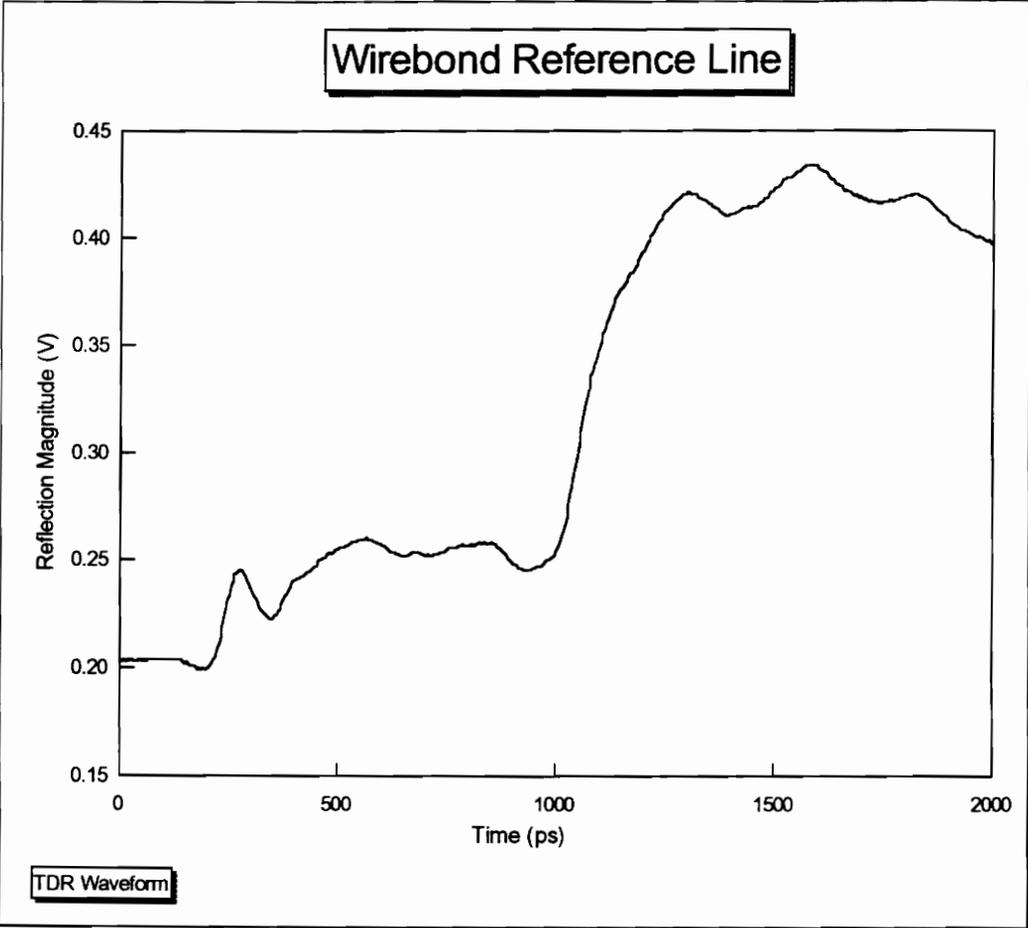


Figure 4-5

Wirebond Reference Line

TDR Measurement

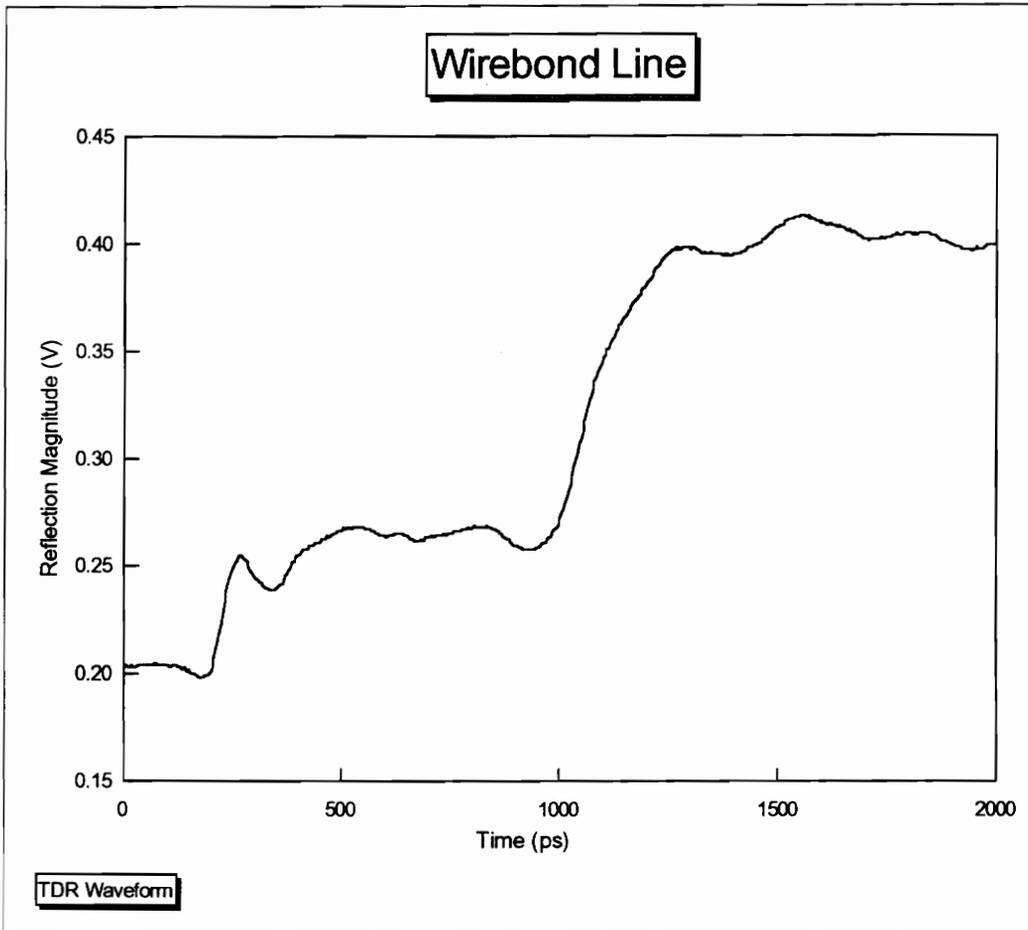


Figure 4-6
Wirebond Line
TDR Measurement

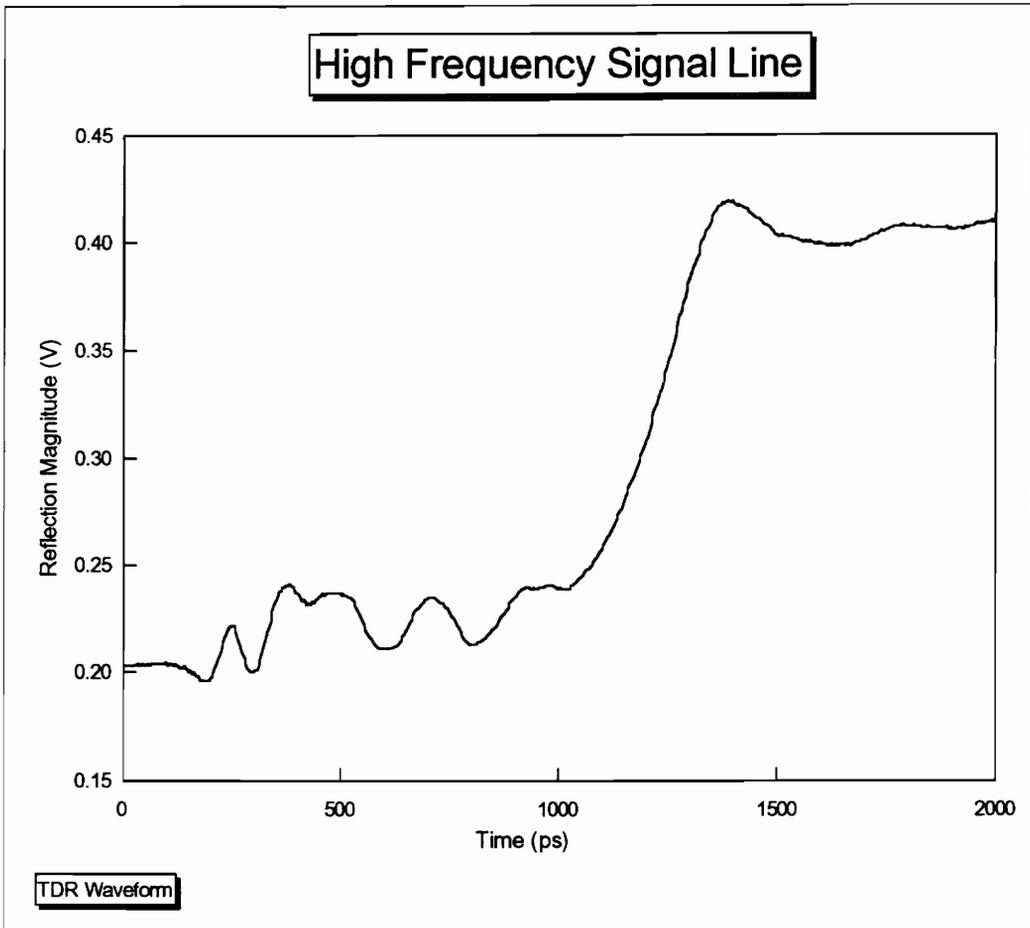


Figure 4-7

High Frequency Signal Line

TDR Measurement

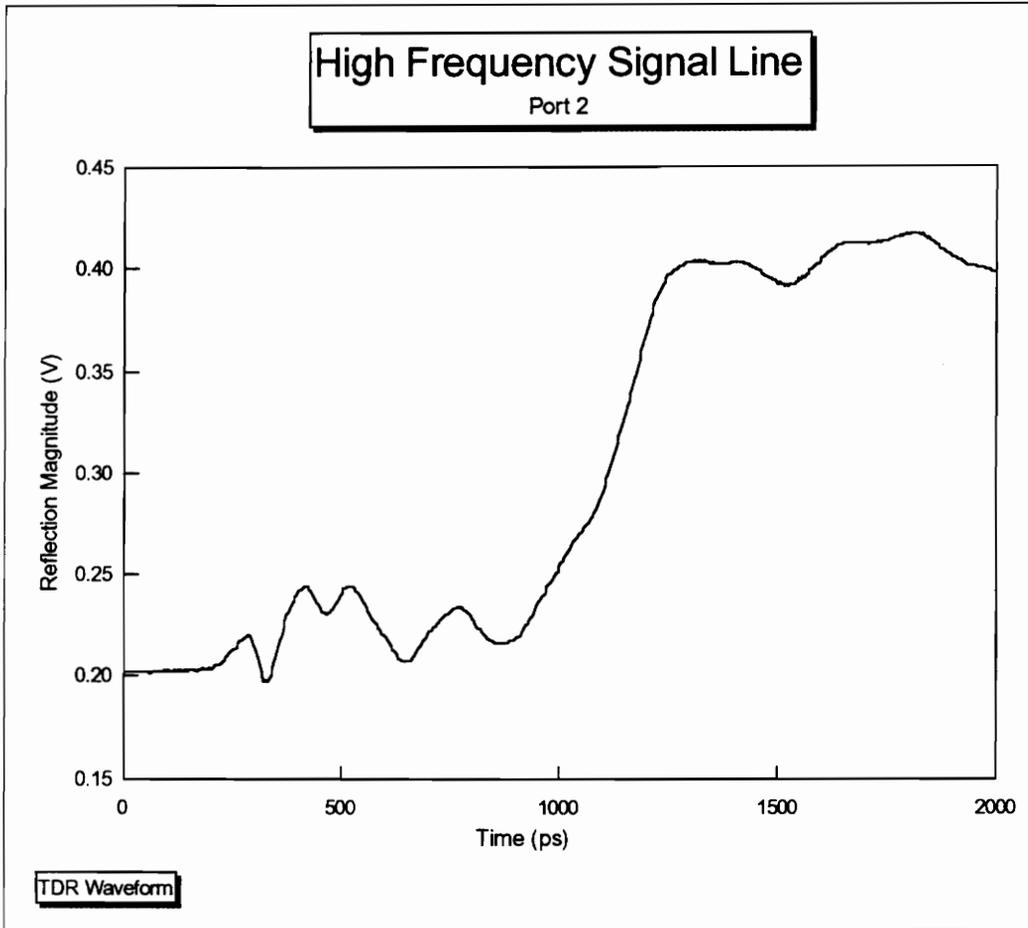


Figure 4-8
High Frequency Signal Line--Port 2
TDR Measurement

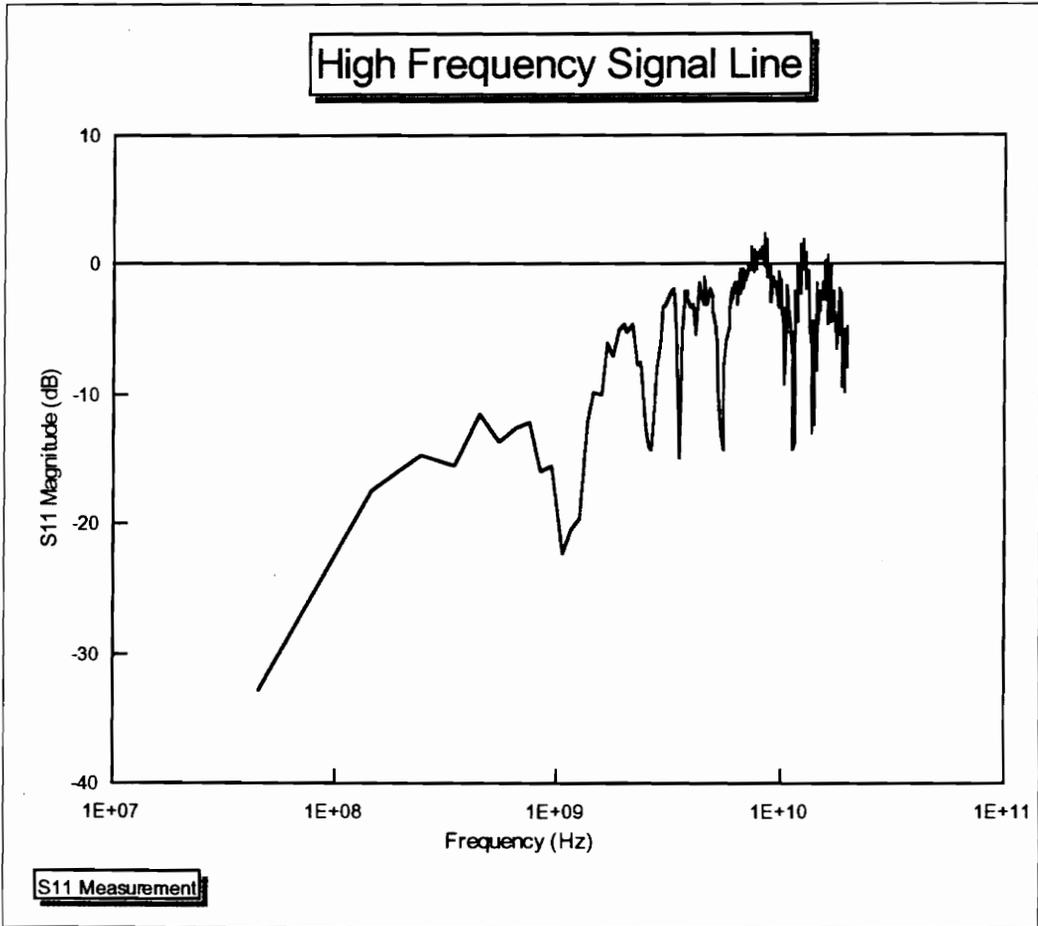


Figure 4-9

High Frequency Signal Line

s_{11} Measurement

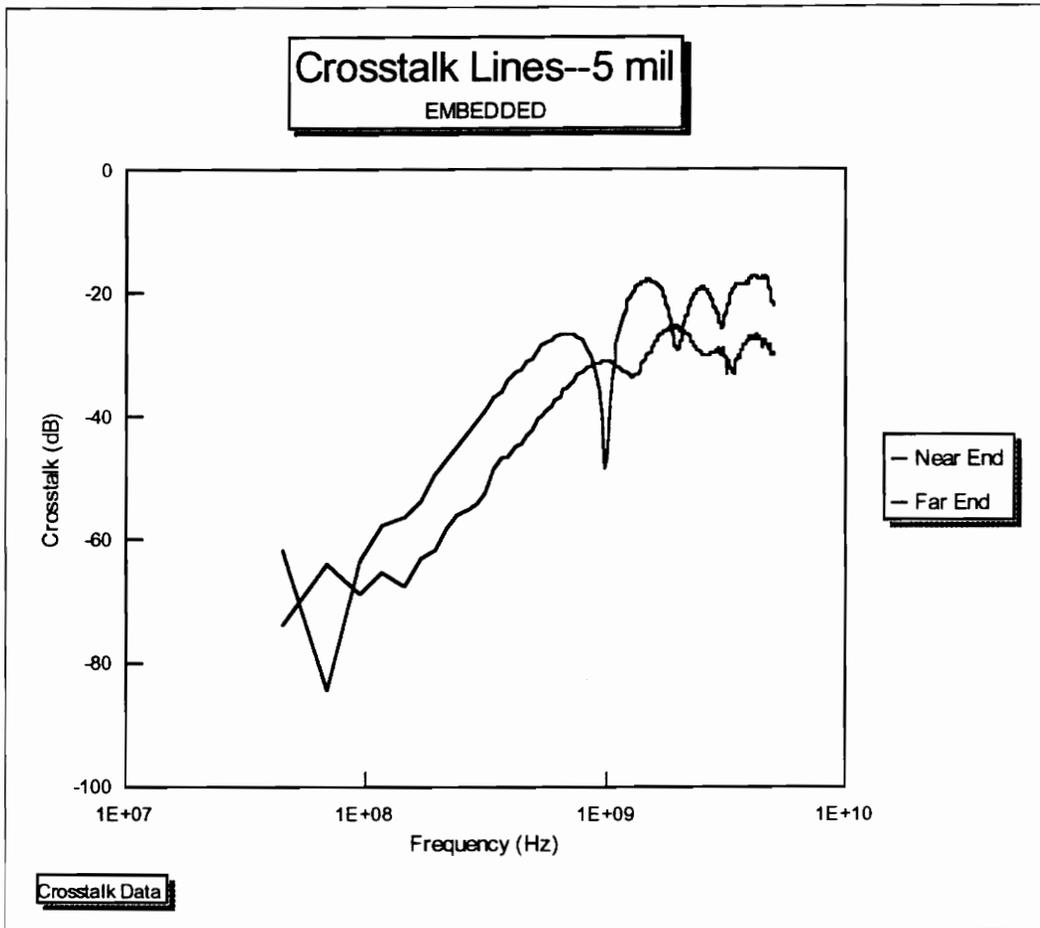


Figure 4-10

Embedded 5 mil Crosstalk Lines

Near and Far End Crosstalk Data

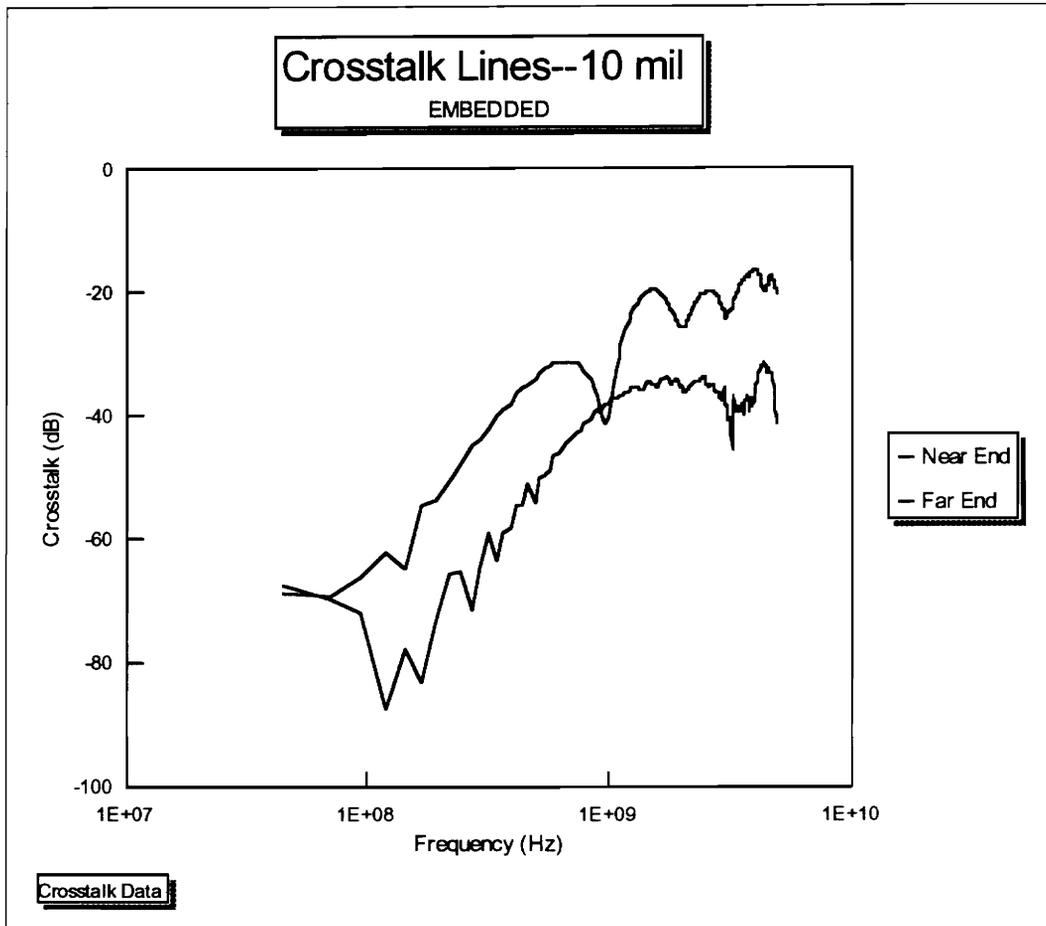


Figure 4-11

Embedded 10 mil Crosstalk Lines

Near and Far End Crosstalk Data

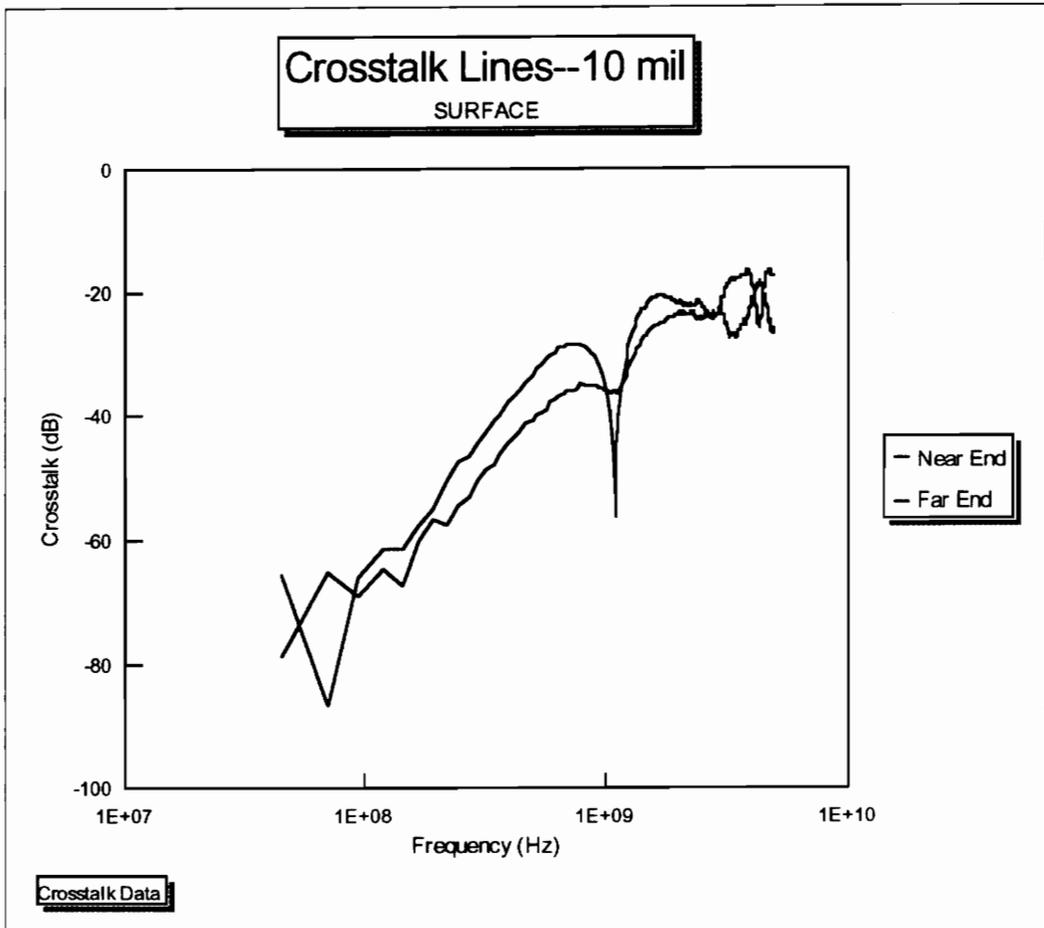


Figure 4-12

Surface 10 mil Crosstalk Lines

Near and Far End Crosstalk Data

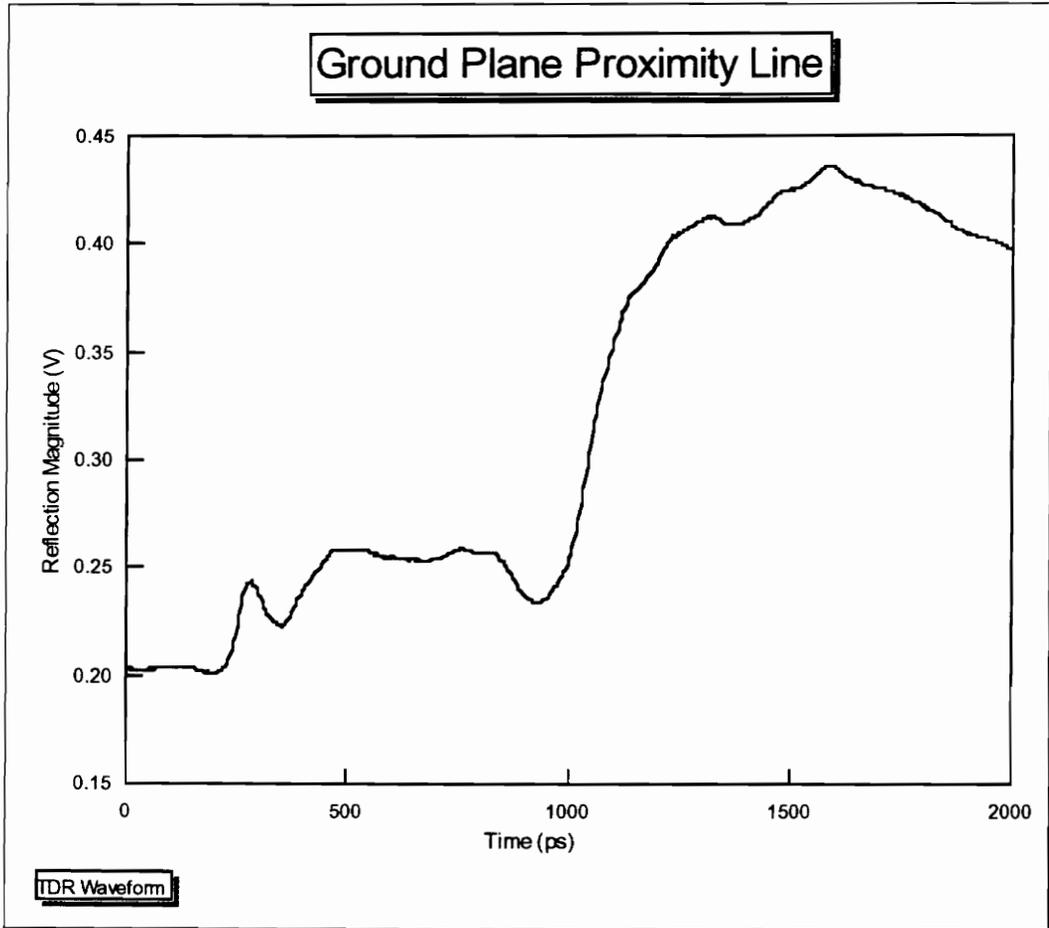


Figure 4-13

Ground Plane Proximity Line

TDR Waveform

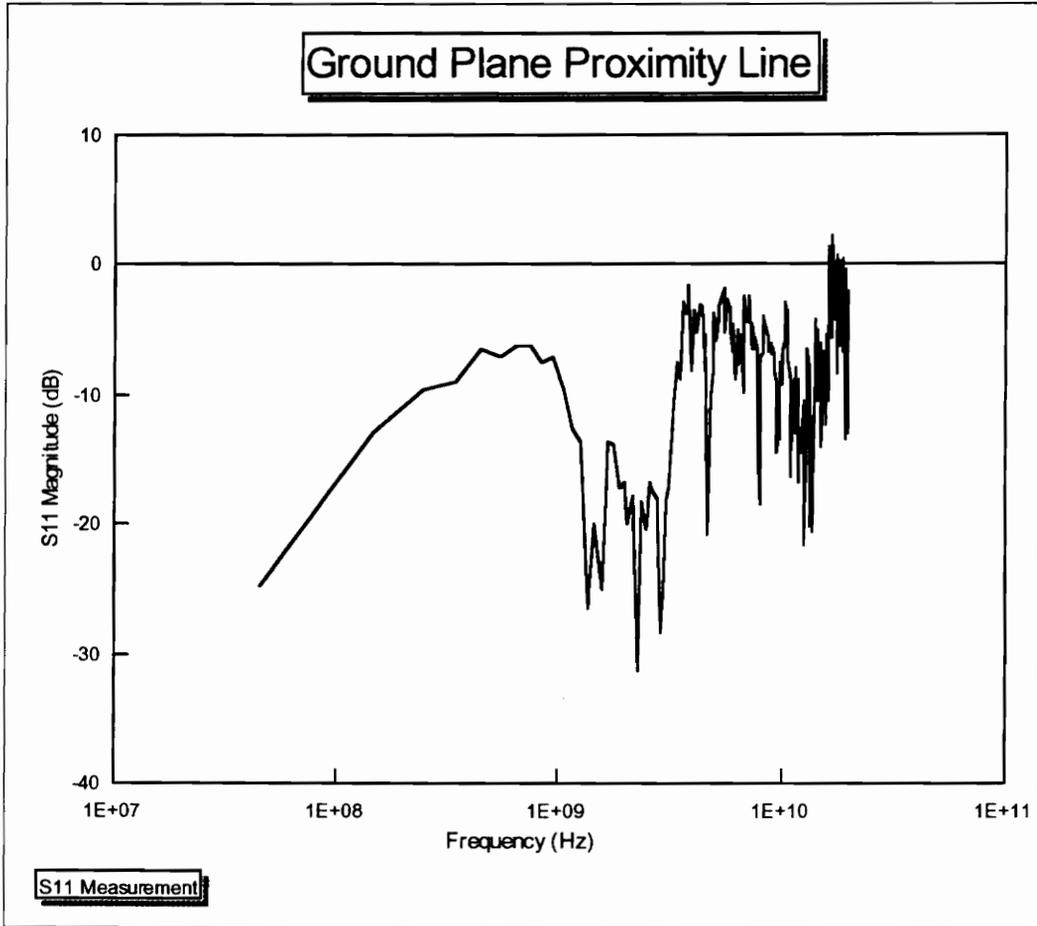


Figure 4-14

Ground Plane Proximity Line

s_{11} Measurement

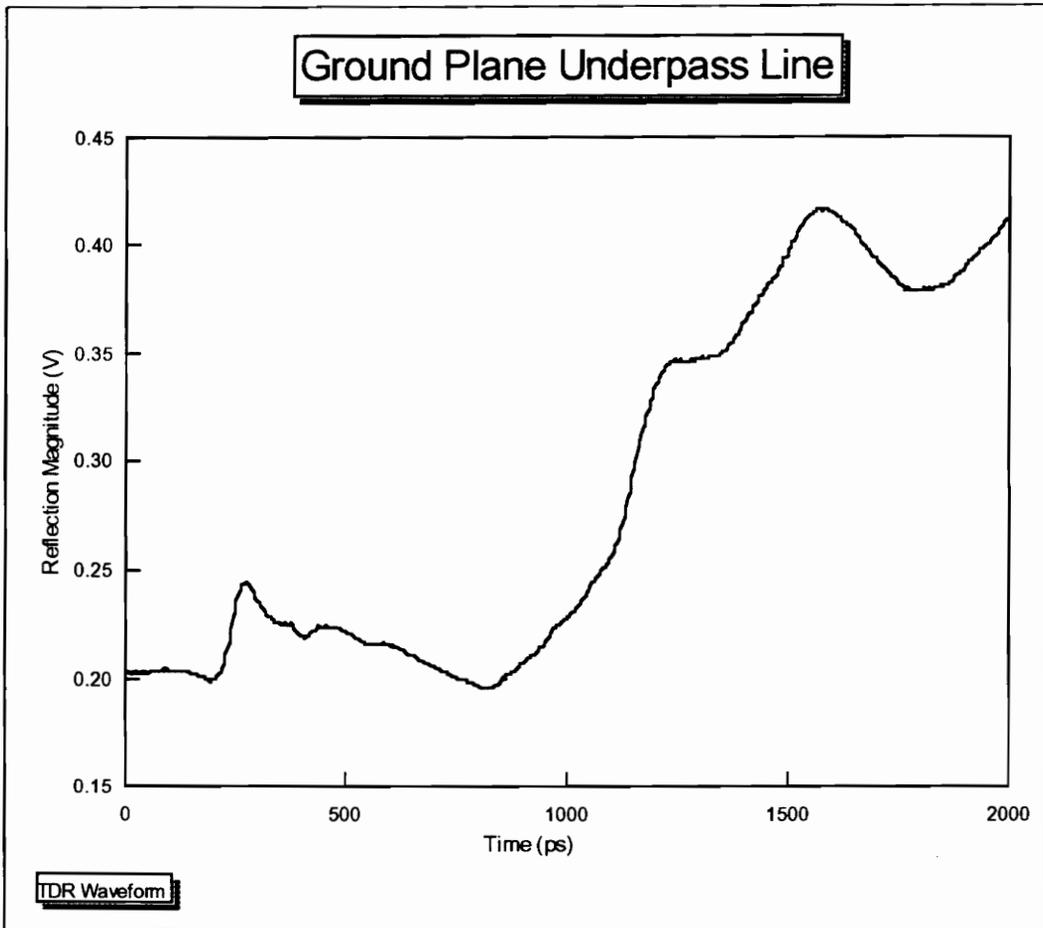


Figure 4-15
Ground Plane Underpass Line
TDR Response

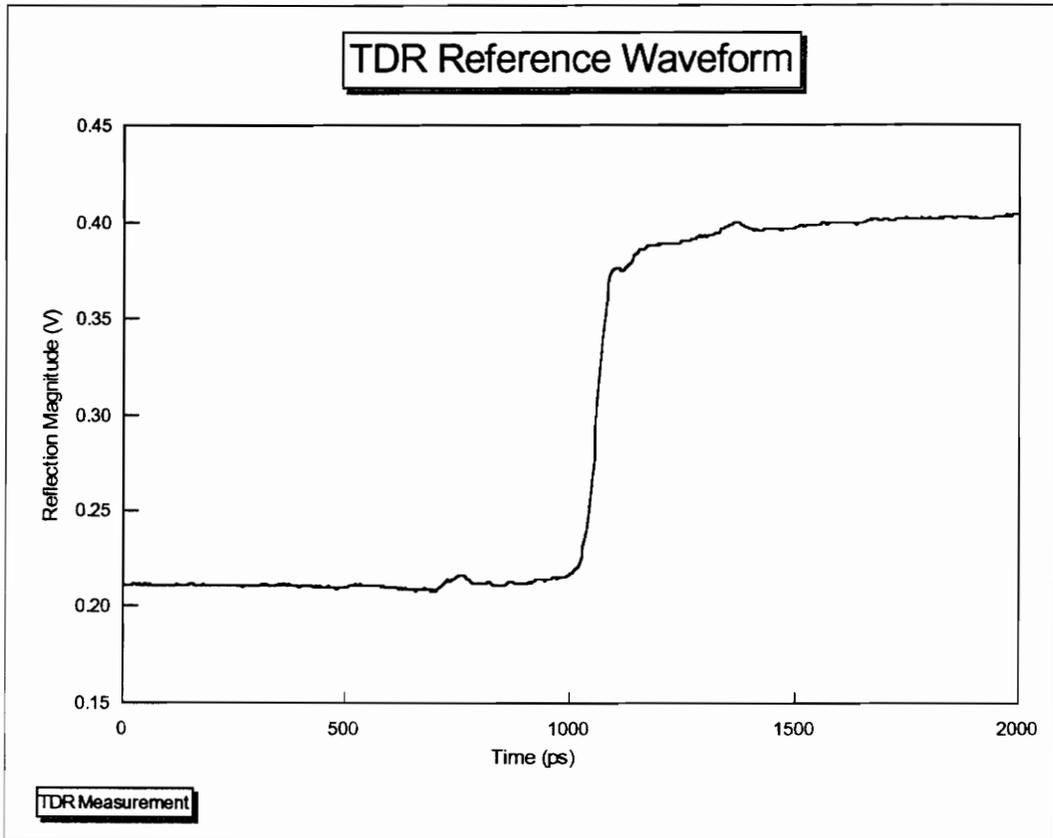


Figure 4-16

TDR Reference Waveform

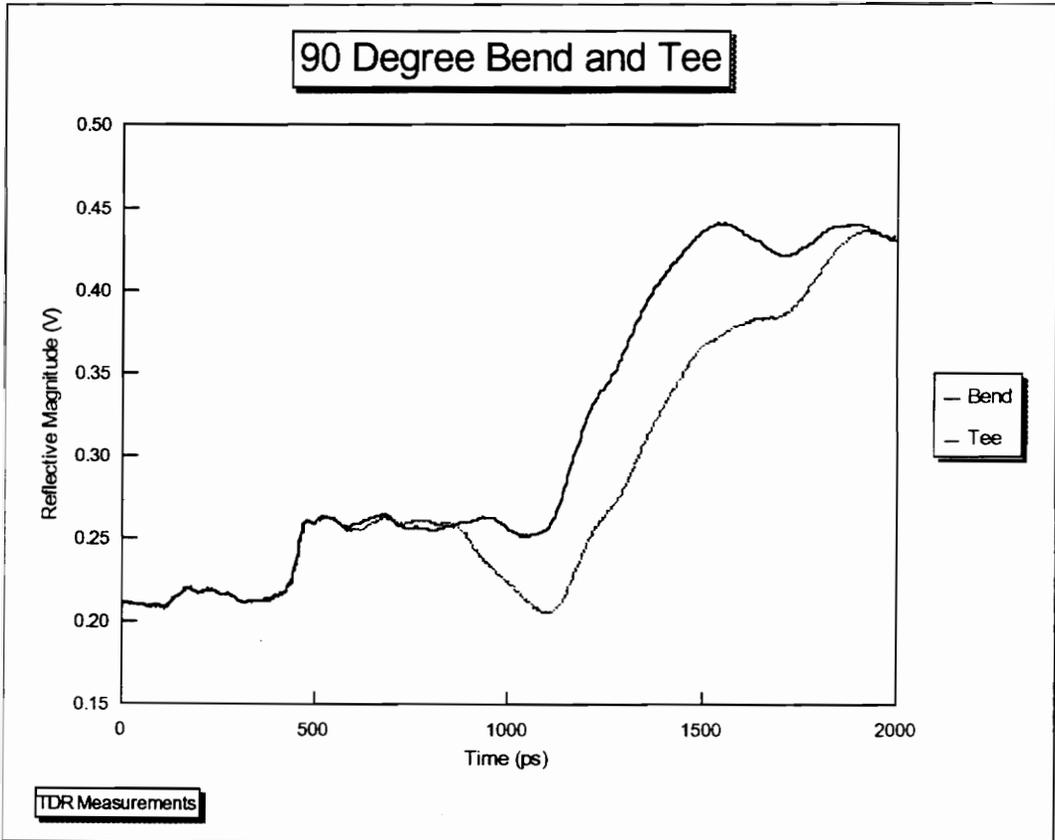


Figure 4-17
90 Degree Bend Line and 90 Degree Tee Line
TDR Measurement

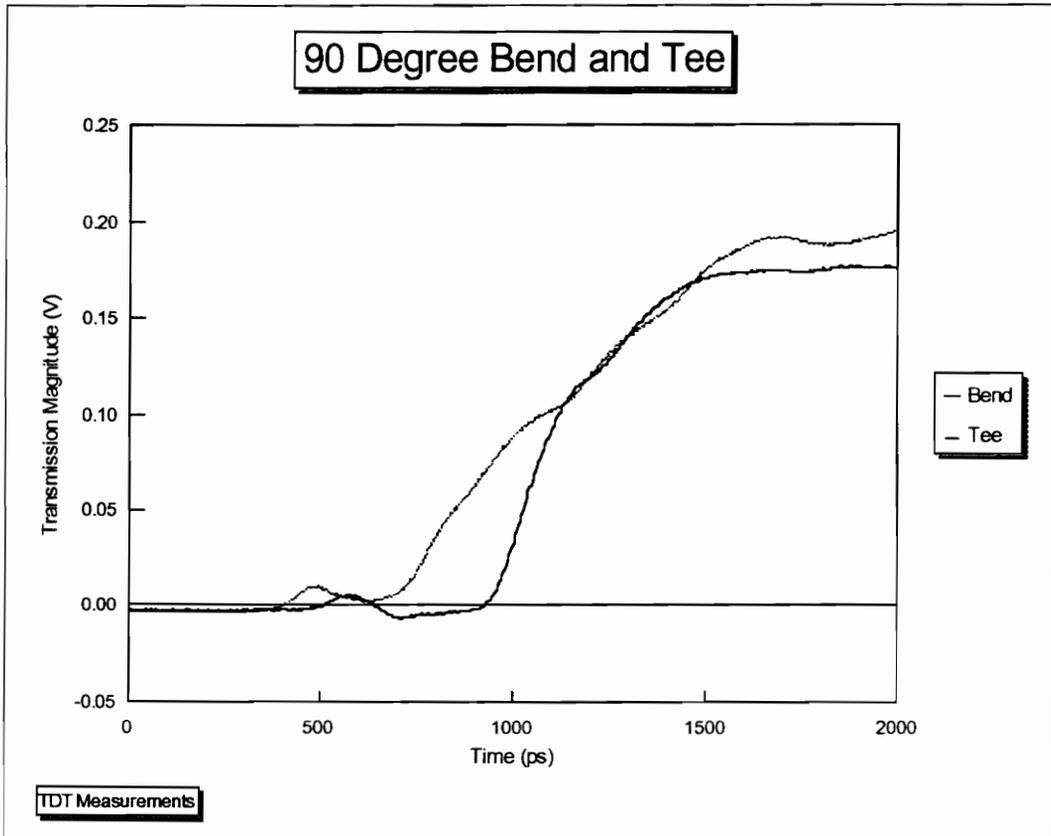


Figure 4-18

90 Degree Bend and 90 Degree Tee Lines

TDT Measurement

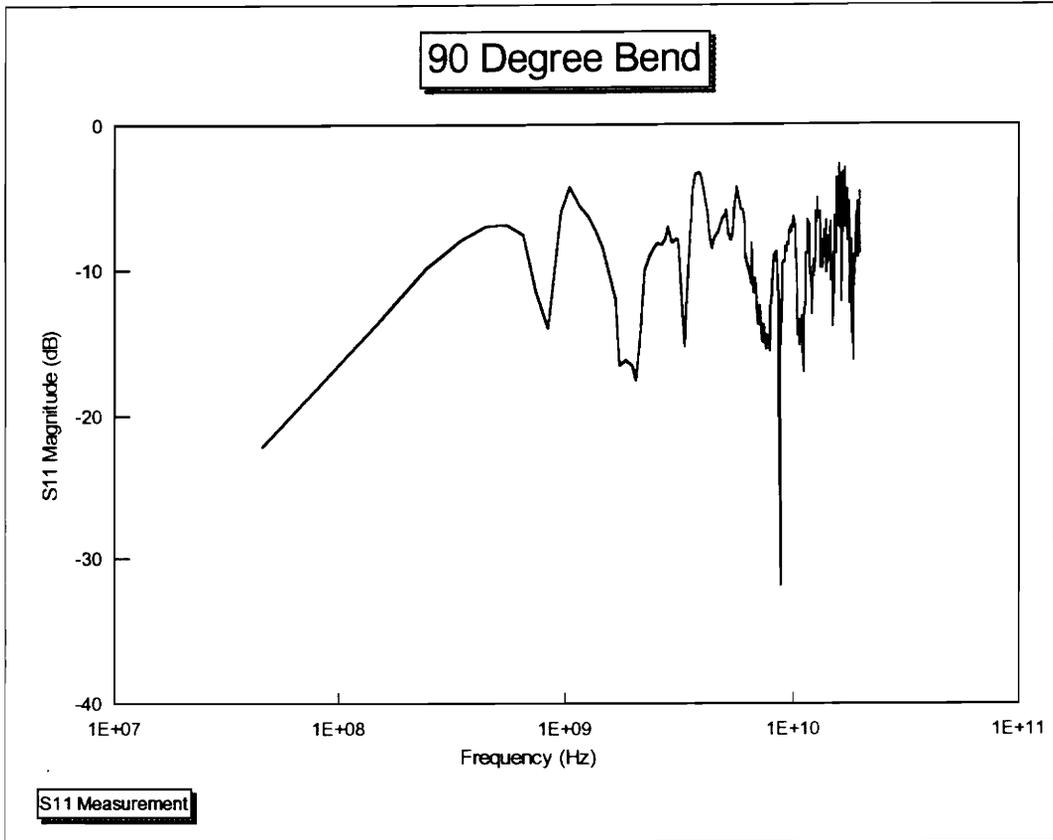


Figure 4-19
90 Degree Bend
S₁₁ Measurement

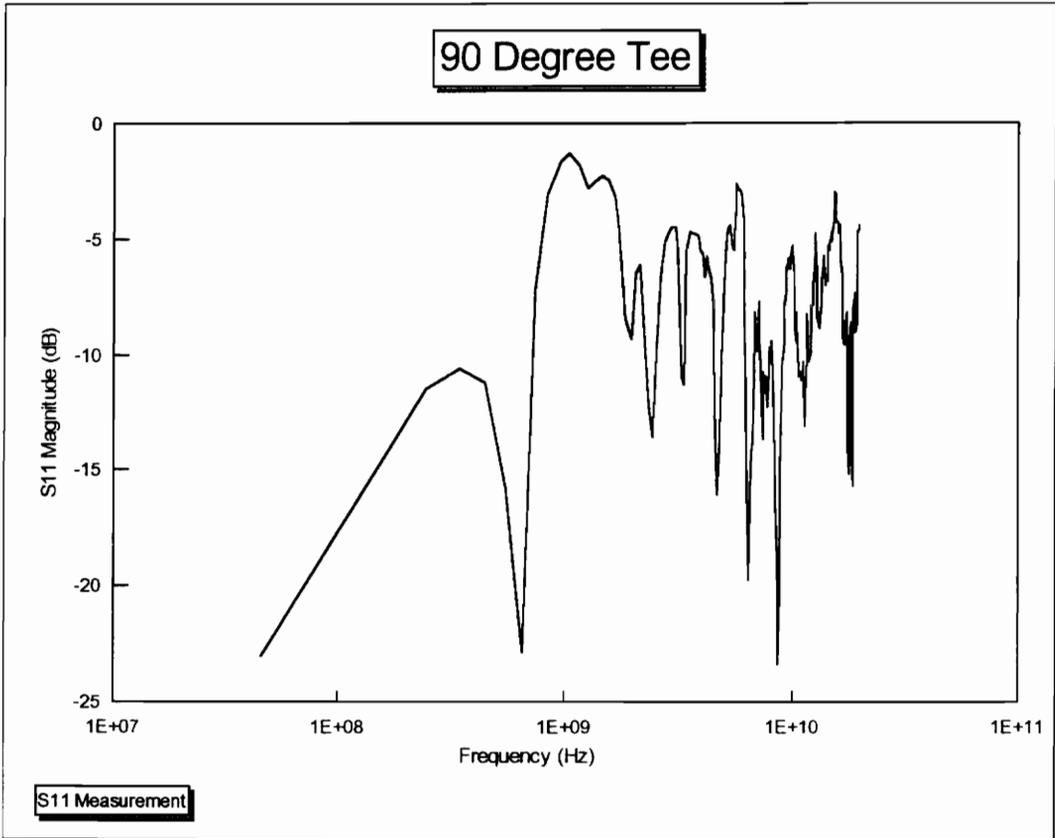


Figure 4-20
90 Degree Tee
 S_{11} Measurement

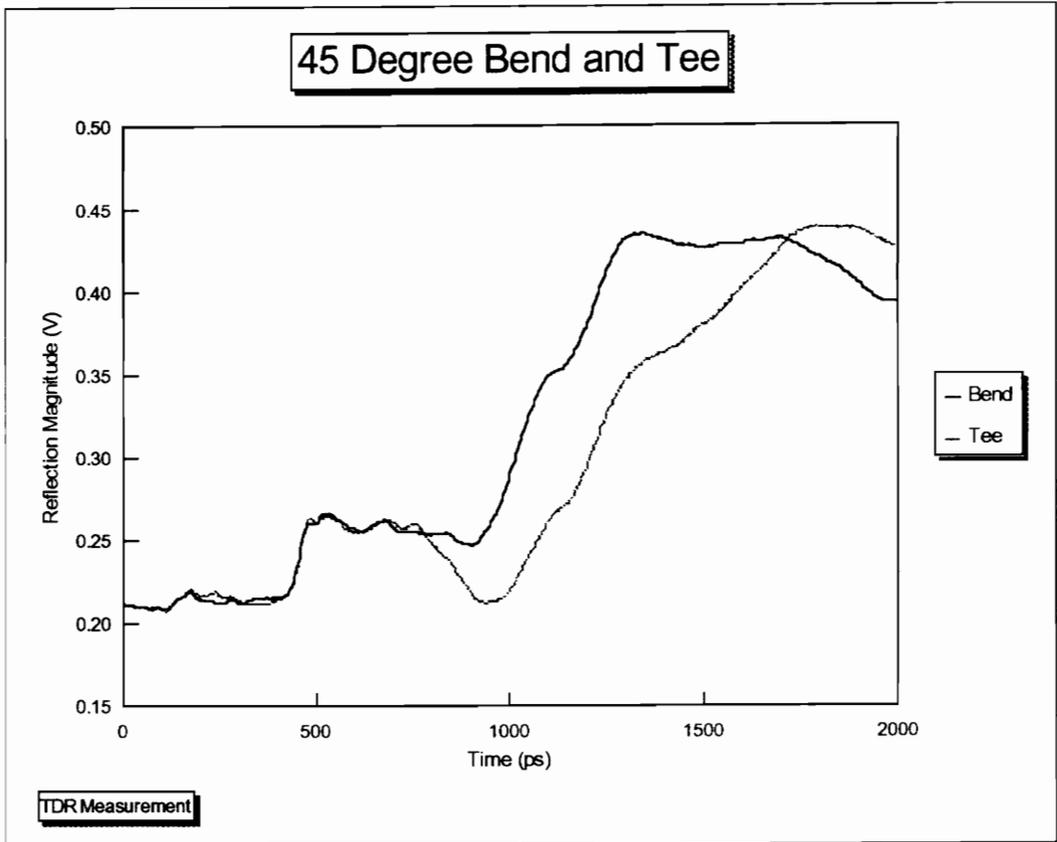


Figure 4-21
45 Degree Bend Line and 45 Degree Tee Line
TDR Measurement

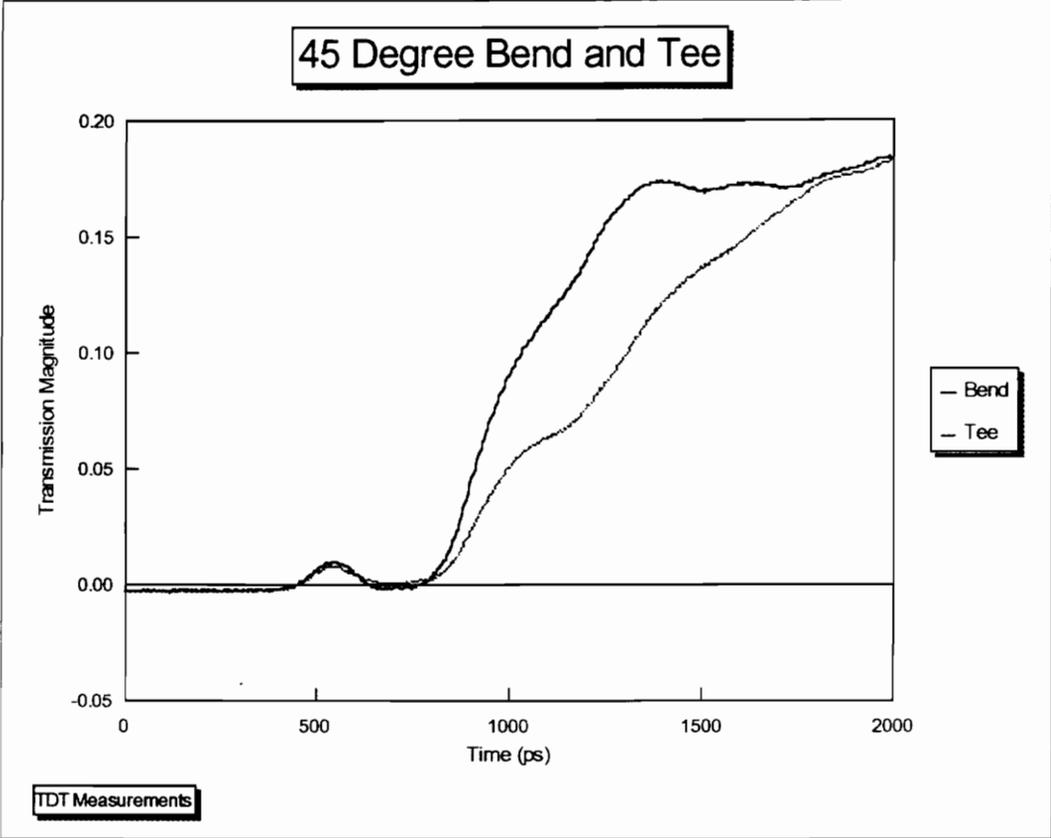


Figure 4-22
45 Degree Bend Line and 45 Degree Tee Line
TDT Response

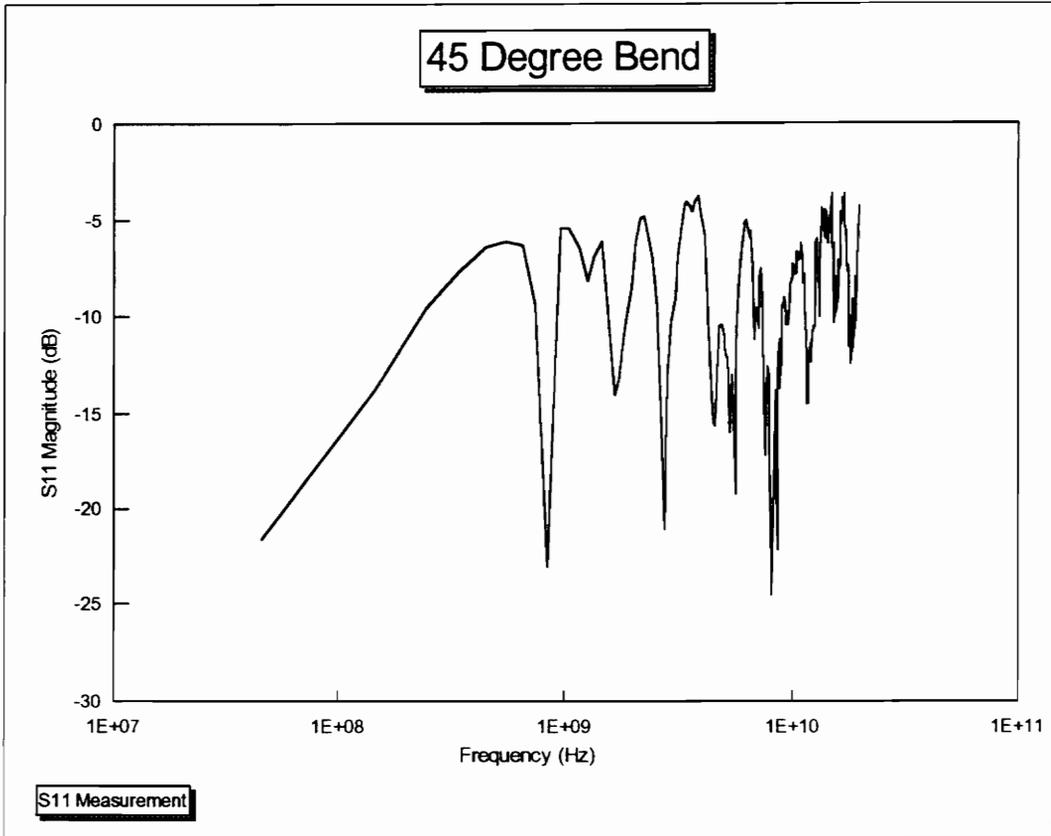


Figure 4-23
45 Degree Bend
 S_{11} Measurement

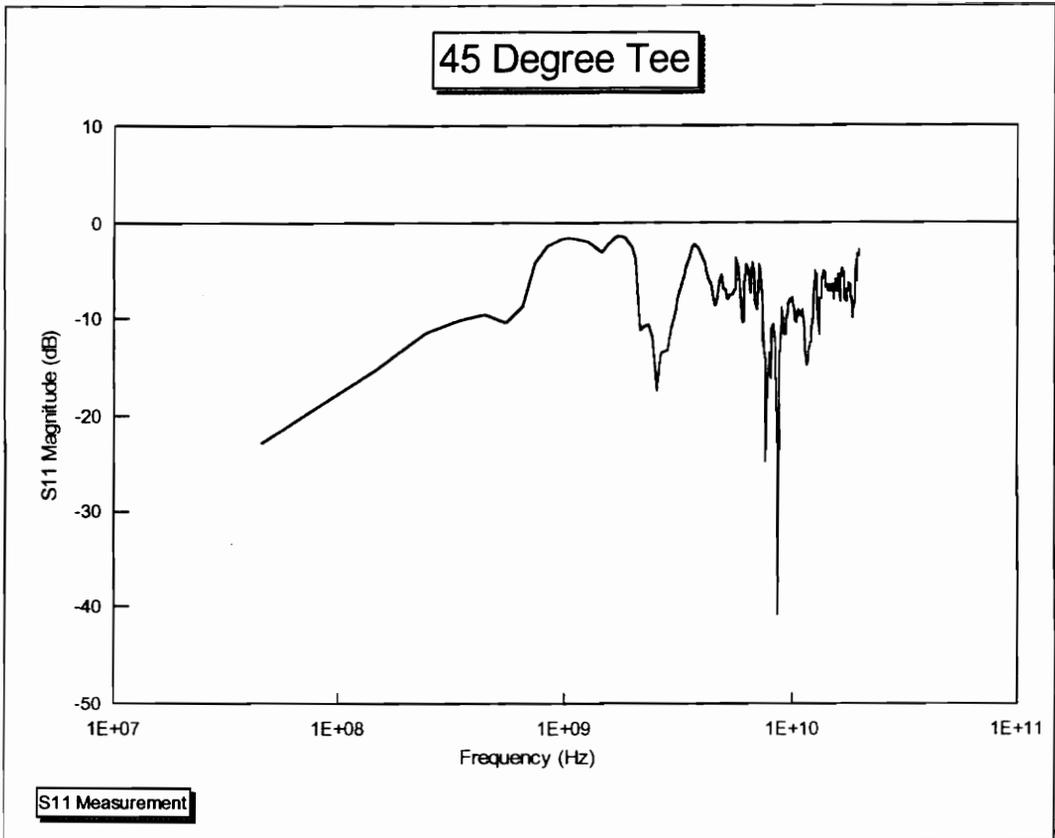


Figure 4-24
45 Degree Tee Line
S₁₁ Measurement

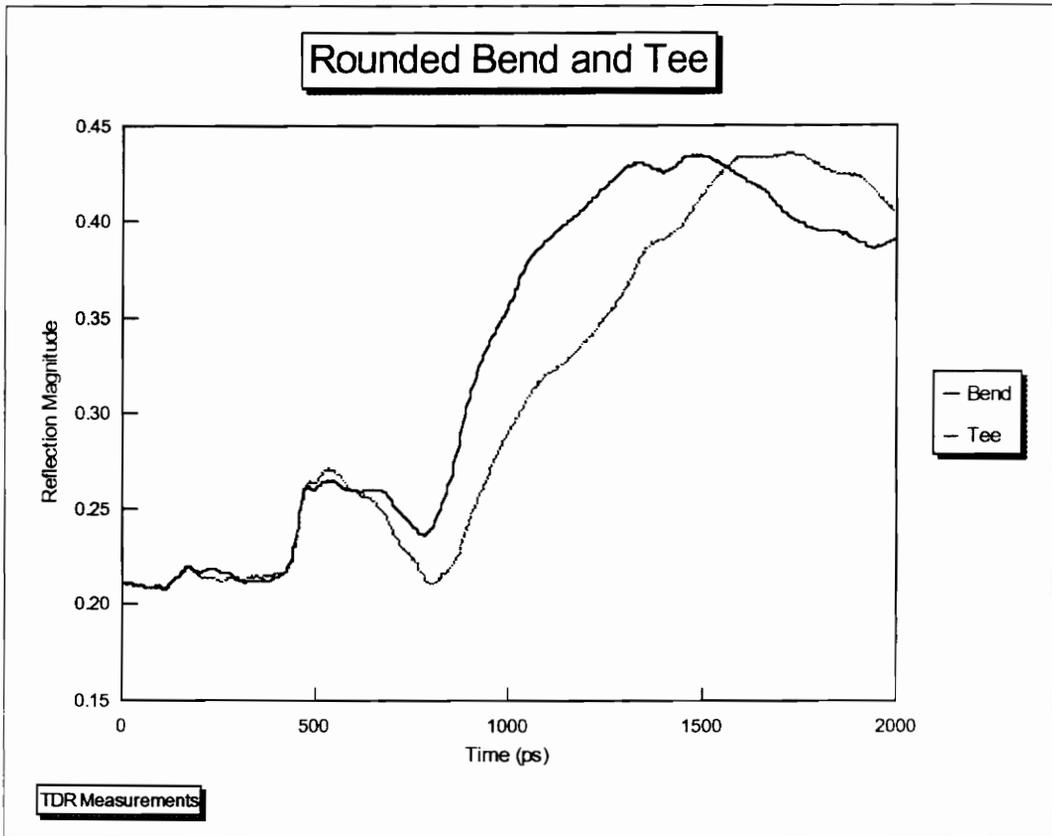


Figure 4-25
Rounded Bend Line and Rounded Tee Line
TDR Measurement

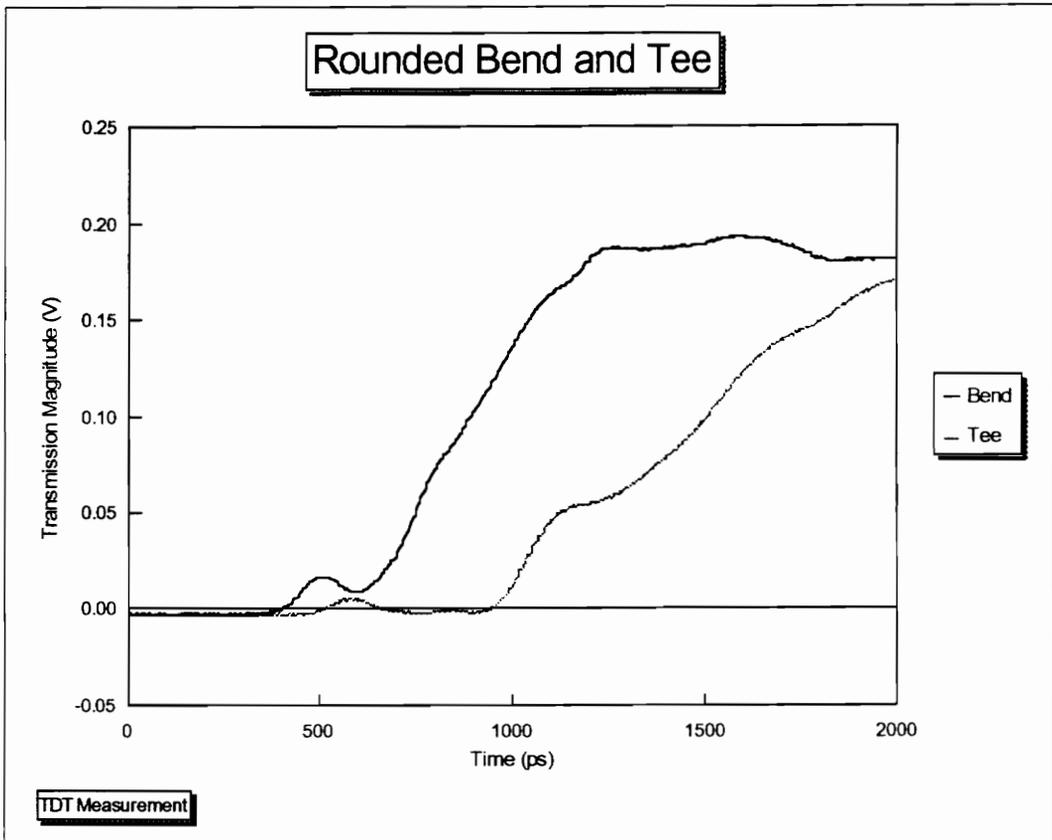


Figure 4-26

Rounded Bend Line and Rounded Tee Line

TDT Response

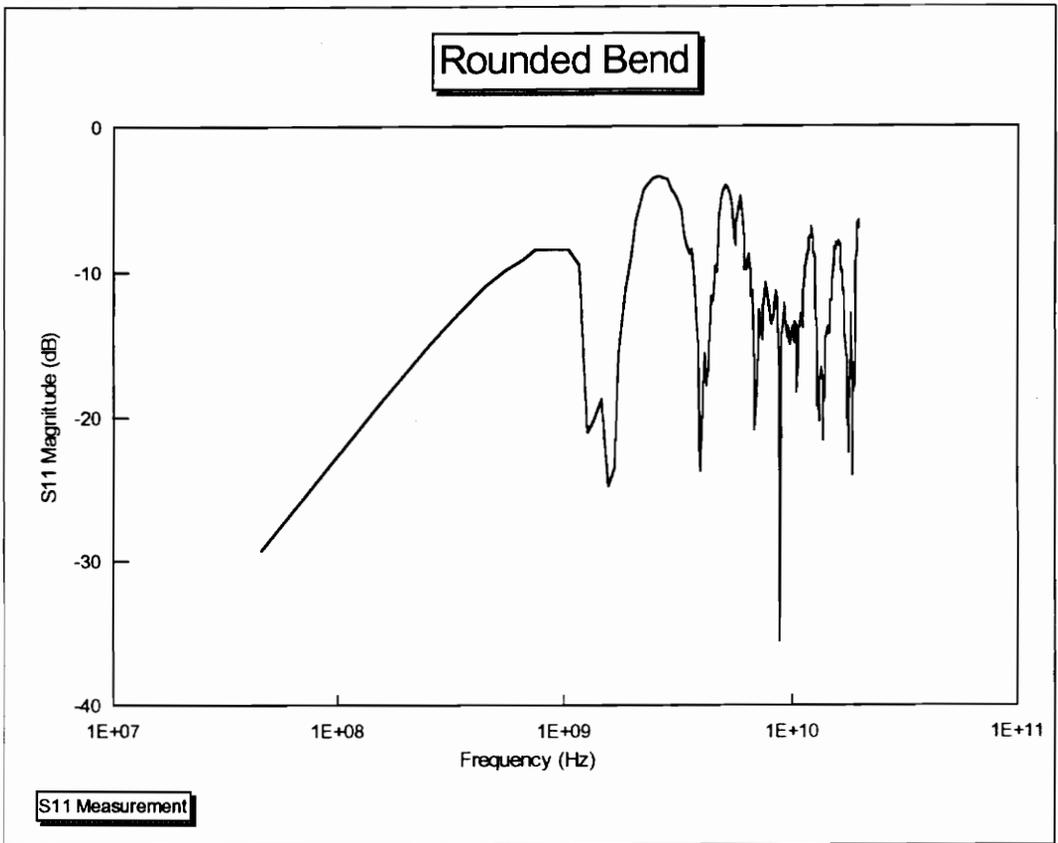


Figure 4-27
Rounded Bend Line
S₁₁ Measurement

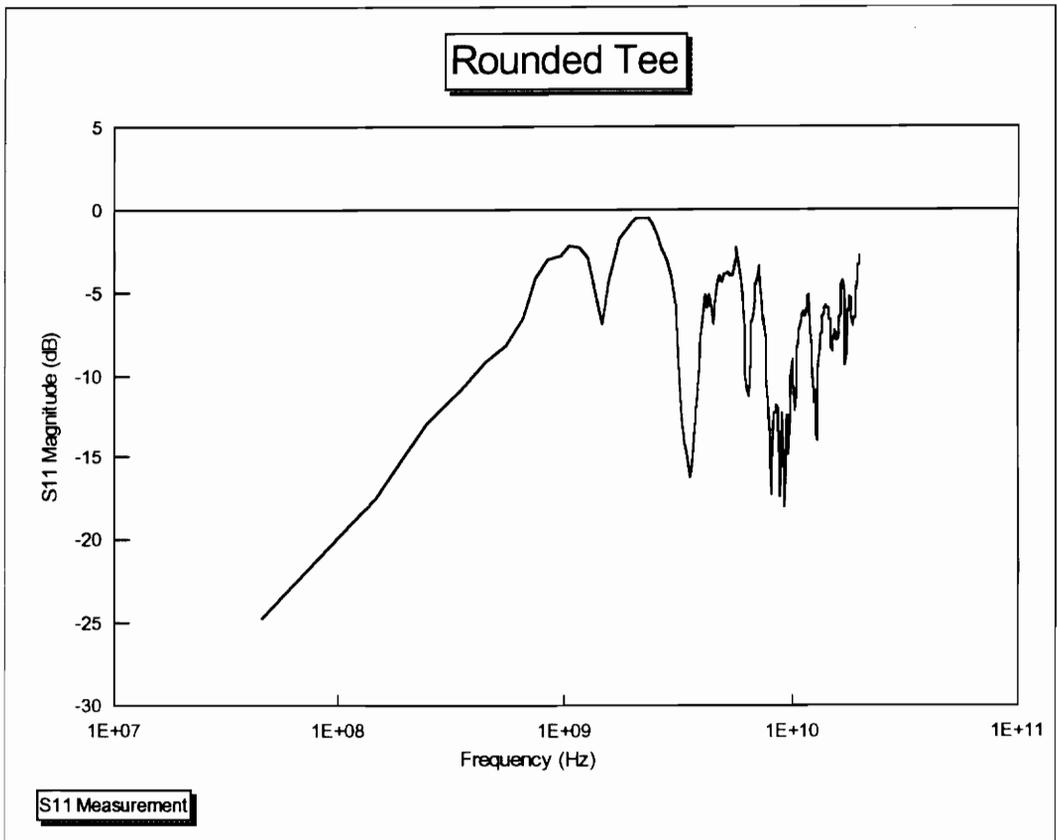


Figure 4-28

Rounded Tee

S₁₁ Measurement

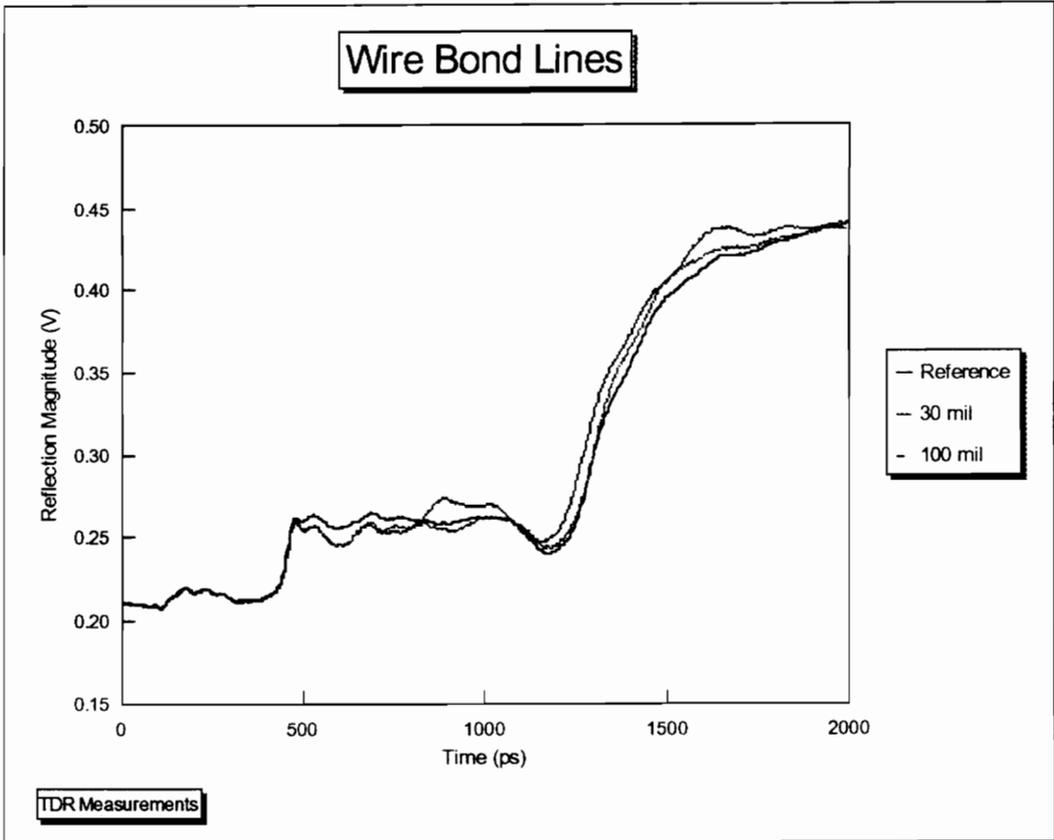


Figure 4-29

Wirebond Lines

TDR Measurements

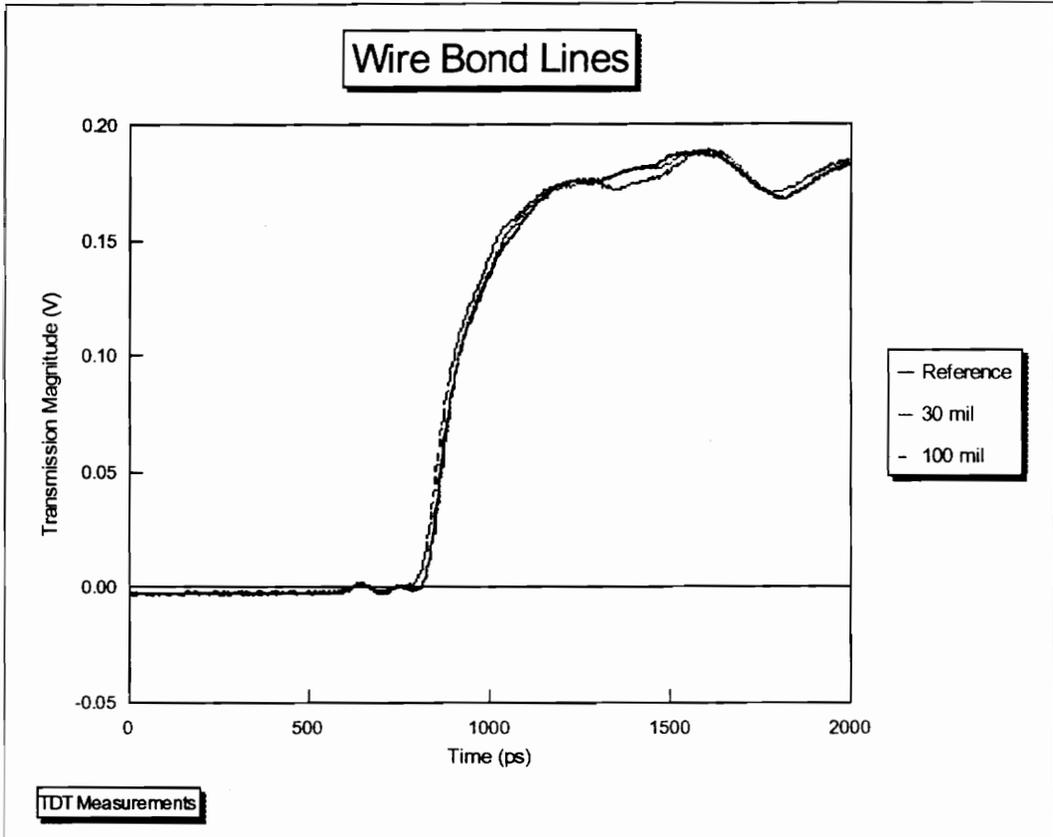


Figure 4-30

Wirebond Lines

TDT Measurements

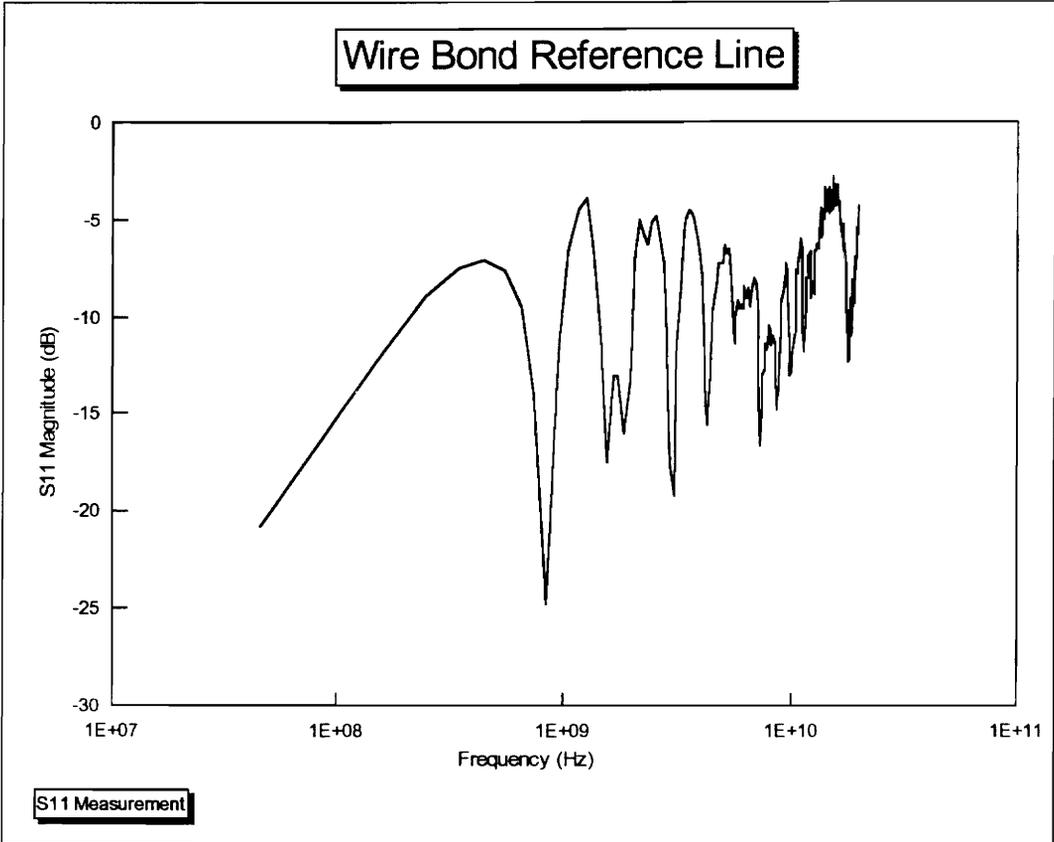


Figure 4-31

Wirebond Reference Line

S_{11} Measurement

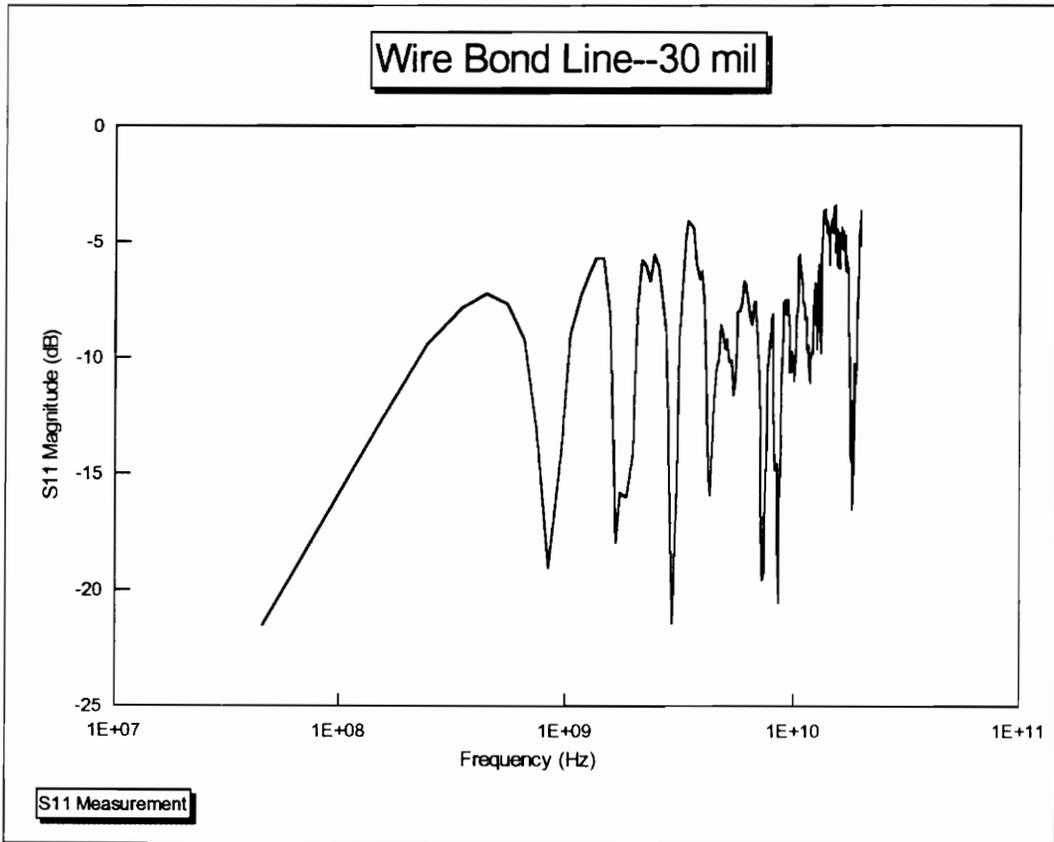


Figure 4-32
Wirebond Line--30 mil
 S_{11} Measurement

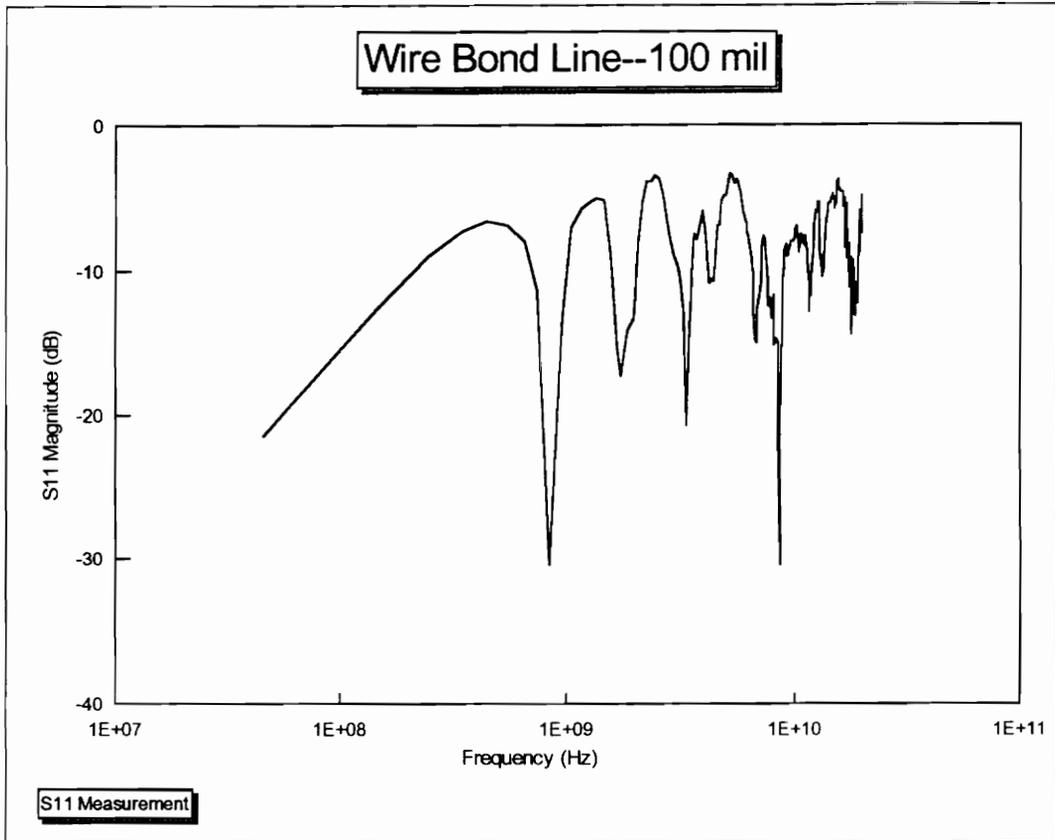


Figure 4-33
Wirebond Line--100 mil
 S_{11} Measurement

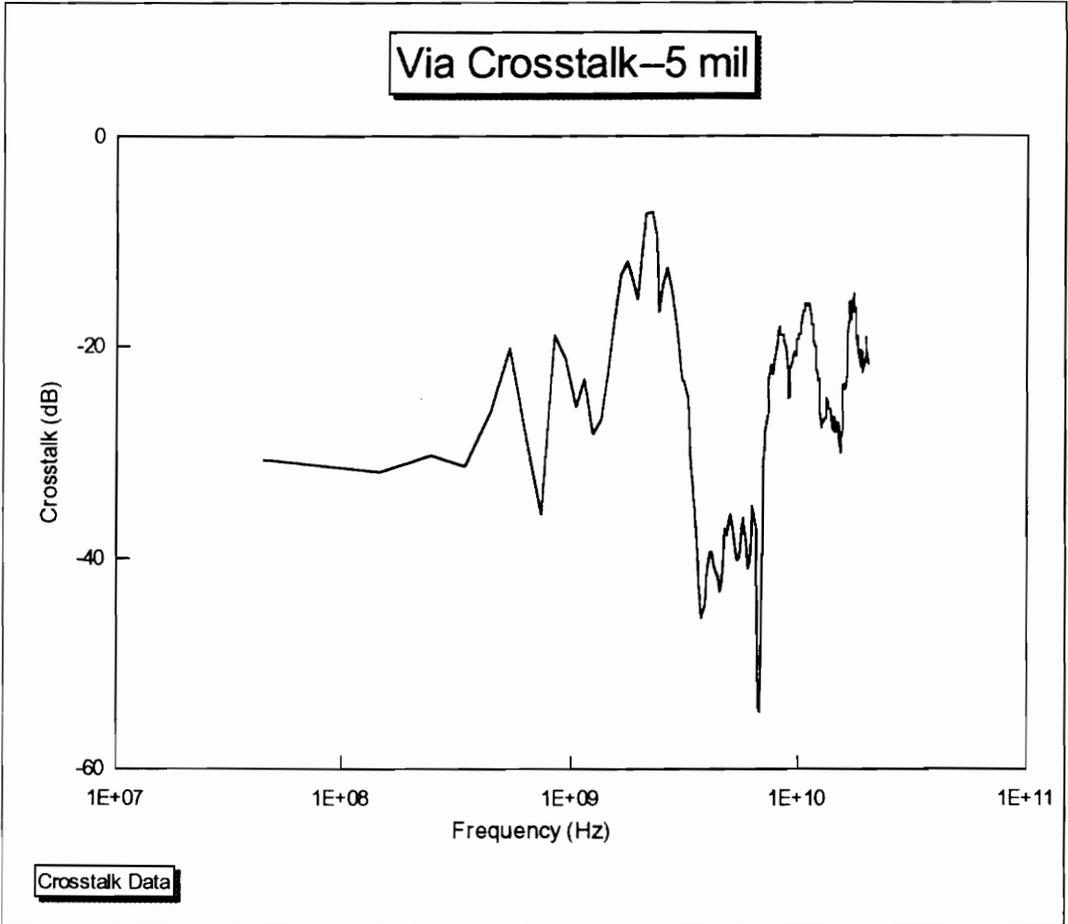


Figure 4-34
5 mil Coupled Vias
Crosstalk Data

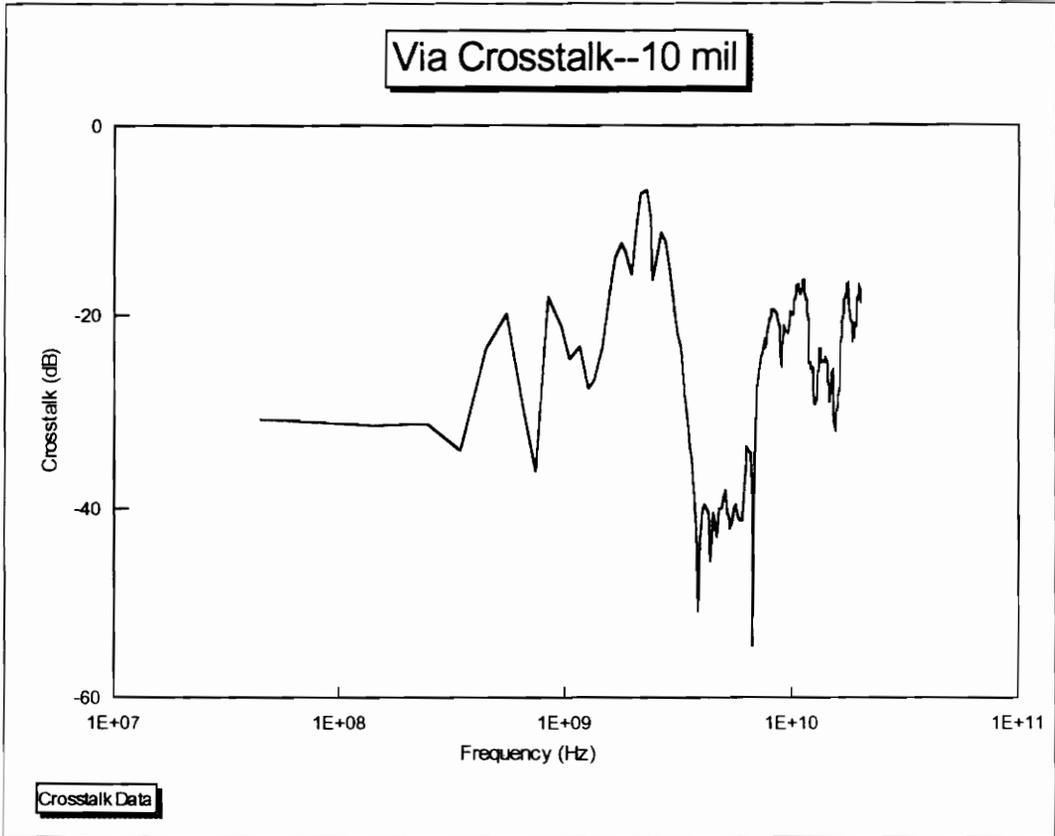


Figure 4-35
10 mil Coupled Vias
Crosstalk Measurement

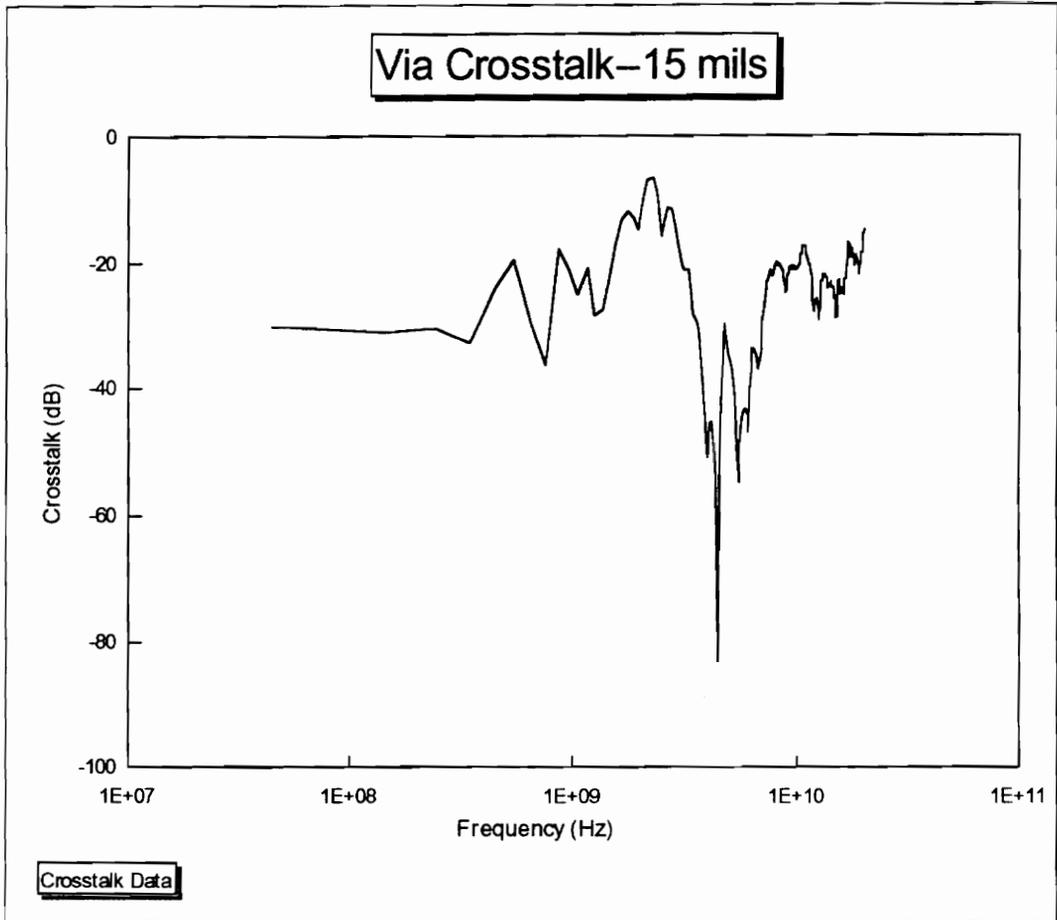


Figure 4-36
15 mil Coupled Vias
Crosstalk Measurement

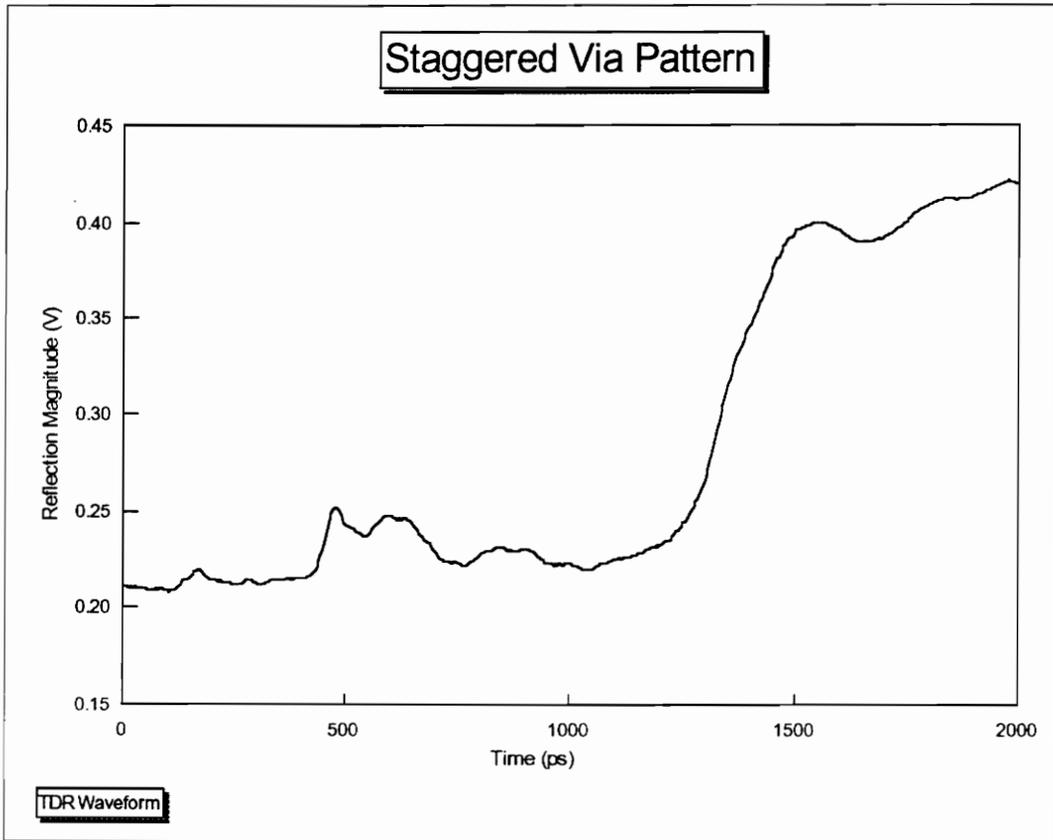


Figure 4-37
Staggered Via Pattern
TDR Measurement

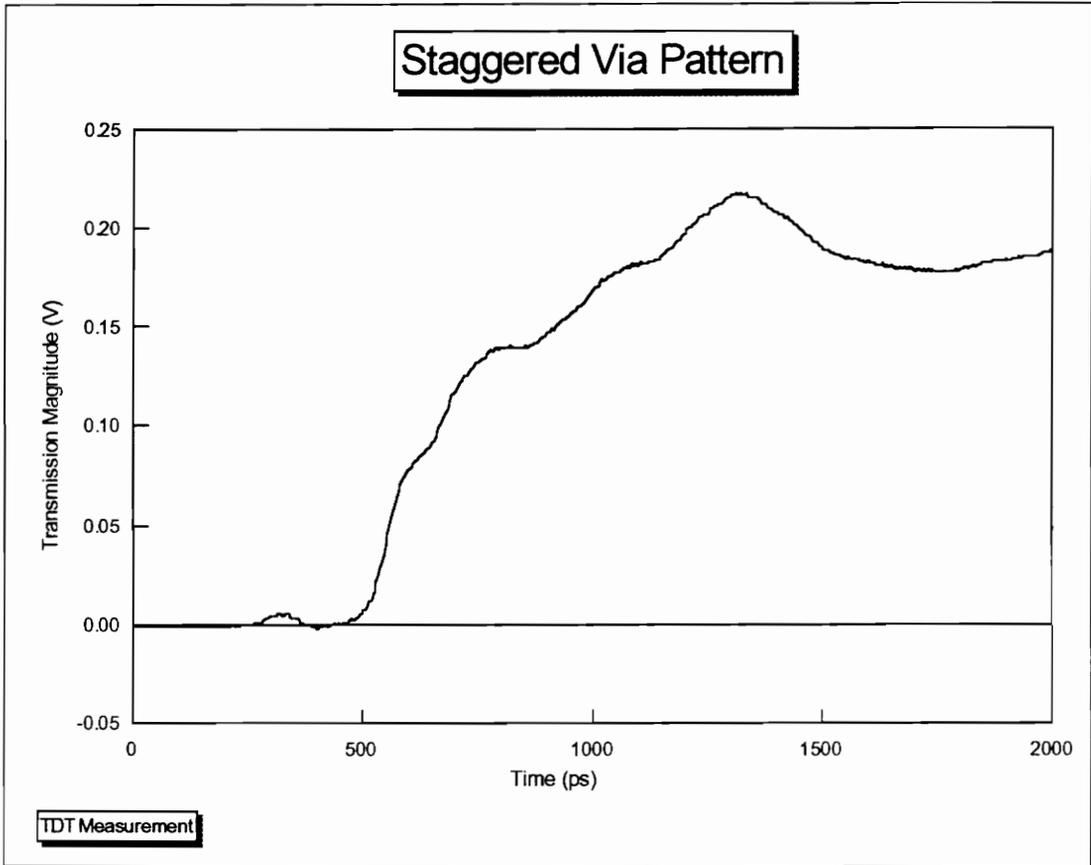


Figure 4-38
Staggered Via Pattern
TDT Measurement

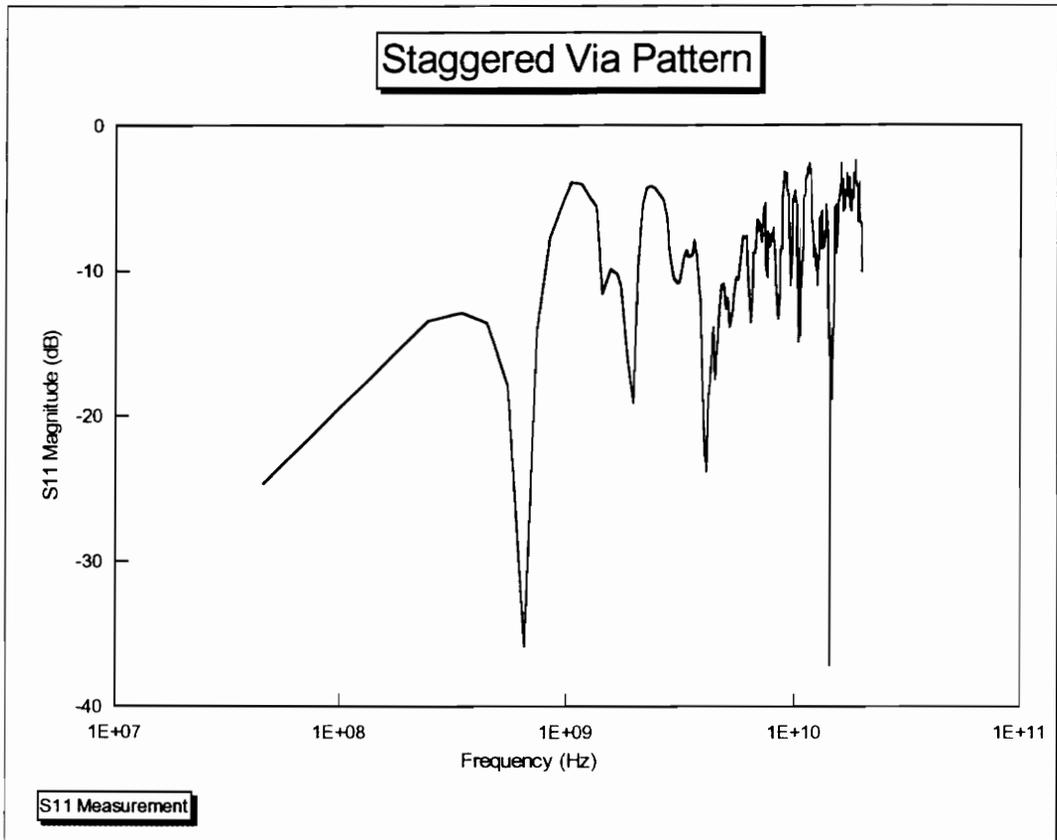


Figure 4-39
Staggered Via Pattern
S₁₁ Measurement

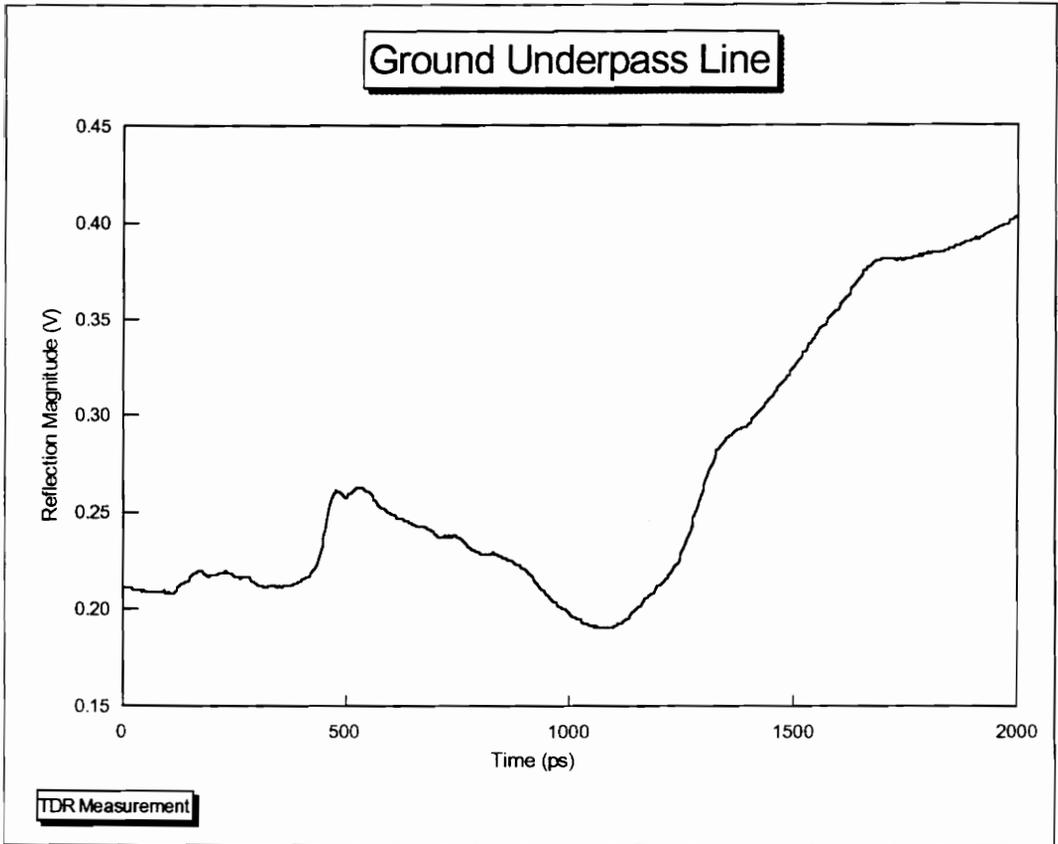


Figure 4-40
Ground Plane Underpass Line
TDR Measurement

CHAPTER 5

CONCLUSIONS

5.1--Conclusions

Two generic circuits have been fabricated and electrically evaluated. The MCM capabilities of Low Temperature Co-fireable Ceramics (LTCCs) have been demonstrated in this work. From these packages we have observed the effects of different via patterns, lines underpassing and bypassing ground planes, right angle bends, rounded bends, obtuse angle bends, tee lines of similar fashions, and effects of wire bonds. Time Domain and Frequency Domain measurements have been performed and presented.

MCM capabilities of LTCC tape systems have been demonstrated. The two MCM test packages have been shown to provide adequate performance for frequencies of operation below 1 GHz, compatible with today's digital circuits. The via pattern lines demonstrate that if the characteristic impedance of the different segments are matched then the discontinuities associated with these lines can be reduced. Signal lines passing close to the ground planes must be designed so that the change in the overall capacitance is small. We have observed from Generic Circuit II that the line impedance is slightly greater than 50 ohms. The bend lines have a much more uniform impedance than the tee lines, the tee lines showing a capacitive load at the intersection. We have observed the TDT measurements of the 90, 45, and rounded bend/tee lines, seeing the larger capacitance of the tee lines resulting in a much slower rise time than what was measured in the bend lines. The s_{11} measurements of the bend lines and tee lines have been observed as

being relatively similar. There seemed to be little improvement when using the 45 degree bend and tee lines as opposed to using a 90 degree bend. The tee lines, at lower frequencies, behaved similarly to the bend lines. However at higher frequencies, capacitive loading started to take effect in the tee lines, before doing so in the bend lines. The different lengths of wirebonds did not show much effect on the electrical performance due to the short length itself (100 mils) from a TDR and TDT perspective. This was also true for the Frequency Domain measurements (s_{11}). Changing the spacing between the coupled vias showed almost no difference due to the small length of the coupling portion of the vias (only 25 mils) and coupling between the measurement probes. The staggered via line, having a significant variation in dielectric heights, has shown a change in the characteristic impedance of the line. This mismatch limits the performance of the staggered via pattern at the higher frequencies.

From both Generic Circuit I and II, we see that LTCC tape systems lend adequate performance for today's digital circuits operating at frequencies below 1 GHz. The multilayer nature of tape systems provide many advantages when used to fabricate MCMs.

5.2--Future Work

Future research work related to this area may consist of superconducting MCM packages. LTCC tape systems that have 0% shrinkage already exist and would be ideal for using with superconductive pastes. This would allow the superconductor to be free of any additives to make the superconductor shrink with the ceramic, as with previous tape systems. One obstacle to overcome would be the chemical reaction between the

superconductor and the ceramic materials. A silver buffer layer can be used. This is easier on the surface, more difficult when embedding the superconductor between layers.

Another area of related work would be a comparison of equal length lines with different bends and lines with multiple bends. Due to the limited space, only the bend and tee lines could be kept equal length. Future packages may include bend lines, 90 degree, 45 degree, and rounded bends, all of equal length, and tee lines of equal length.

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APPENDIX A

GREEN TAPE™ PROCESSING

1. Design generic circuit packages with respective layers using AutoCad®.
2. Remembering the shrinkage factor, plot the patterns on rubylith.
3. Photoreduce the rubylith patterns.
4. Using the films from the photoreduction, make the necessary screens for printing.
5. Blank out the required number of Green Tape™ sheets, wearing gloves to prevent finger oil contamination.
6. Form vias in each layer using the YAg laser, with laser files for each layer.
7. Set the drying oven temperature to 120° C.
8. Use the YAg laser to make stainless steel masks in order to fill vias. Use the same laser files as for the green sheets, except change the radius to be approximately 10% larger.
9. Prepare the printing equipment for Green Tape™ printing using the porous stone stage.
10. Using the stainless steel masks, fill the vias with the appropriate via-fill paste.
11. Dry the filled layers in the drying oven for 5 minutes at 120° C.
12. Remove the filled layers from the oven and inspect by using a microscope.
13. Repair any improperly filled vias.
14. After all vias have been properly filled, set up the printing equipment to print the first conductor pattern, using the appropriate conductor paste.
15. After all patterns have been printed, place in the drying oven for 5 minutes at 120°C.
16. Remove the printed layers from the oven and examine with a microscope.
17. Correct or redo any defective layers.
18. After all layers have been printed with the appropriate conductor pattern, stack the layers, remembering the order, in the lamination die.
19. After the layers are correctly placed in the lamination die, turn on the laminating press, setting the temperature to 70° C.
20. Place the die in the 170°F press and add 7000 psi of pressure.
21. Maintain both heat and pressure for 10 minutes.
22. Release the pressure slowly to prevent warping of the sample and remove die from the press.
23. Remove laminated sample from the die
24. Cut away registration holes using the hydraulic hot knife.
25. Using acetone and compressed air, clean a setter for the module to be placed on.
26. Place the setter and module in the ashing furnace.
27. Set the ashing furnace profile as follows:
 - Ramp 1: 11°C/min.
 - Temp 1: 130°C
 - Hold 1: 0 min.
 - Ramp 2: 11°C/min.

Temp 2: 240°C
Hold 2: 0 min.
Ramp 3: 11°C/min.
Temp 3: 350°C
Hold 3: 60 min.
Ramp 4: 3°C/min.
Temp 4: 300°C
Hold 4: 0 min.
Ramp 5: 2°C/min.
Temp 5: 200°C
Hold 5: 0 min.
Ramp 6: 1°C/min.
Temp 6: 20°C
Hold 6: 60 min.
Fan: ON

28. During the ashing furnace profile, bring up the belt furnace using the following settings:
 - Zone 1: 700° C
 - Zone 2: 860° C
 - Zone 3: 860° C
 - Zone 4: 855° CBelt Speed: 2.0 inches/minute
29. After cycle is complete, carefully remove setter and sample from the ashing furnace, and place it on the belt furnace.
30. After firing, remove setter and sample from belt and proceed with post-fired processing and measurements.

VITA

Cecil Edward Barton was born in Princeton, West Virginia, July of 1969. A year later, he and his family relocated near Athens, West Virginia; where he later attended high-school. While holding part-time/full-time employment, he attended Bluefield State College. Later, in May of 1991 he received a Bachelor's Degree in Electrical Engineering Technology. In the Fall of 1991, he began working towards a Master's Degree at the Bradley Department of Electrical Engineering at Virginia Polytechnic Institute and State University. There, he became familiar with the Microelectronics Laboratories and began working in the Microelectronics facilities there. Under the direction of Dr. Aicha Elshabini-Riad, he served as both a Graduate Teaching Assistant, teaching the Hybrid Microelectronics Laboratory Course, and a Graduate Research Assistant.