A High Power Density Three-level Parallel Resonant Converter for Capacitor Charging

by

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Electrical Engineering

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ABSTRACT

This dissertation proposes a high-power, high-frequency and high-density three-level parallel resonant converter for capacitor charging. DC-DC pulsed power converters are widely used in military and medical systems, where the power density requirement is often stringent. The primary means for reducing the power converter size has been to reduce loss for reduced cooling systems and to increase the frequency for reduced passive components. Three-level resonant converters, which combine the merits of the three-level structure and resonant converters, are an attractive topology for these applications. The three-level configuration allows for the use of lower-voltage-rating and faster devices, while the resonant converter reduces switching loss and enhances switching capability.

This dissertation begins with an analysis of the influence of variations in the structure of the resonant tank on the transformer volume, with the aim of achieving a high power density three-level DC-DC converter. As one of the most bulky and expensive components in the power converter, the different positions of the transformer within the resonant tank cause significant differences in the transformer's volume and the voltage and current stress on the resonant elements. While it does not change the resonant converter design or performance, the improper selection of the resonant tank structure in regard to the transformer will offset the benefits gained by increasing the switching

frequency, sometimes even making the power density even worse than the power density when using a low switching frequency. A methodology based on different structural variations is proposed for a high-density design, as well as an optimized charging profile for transformer volume reduction.

The optimal charging profile cannot be perfectly achieved by a traditional output-voltage based variable switching frequency control, which either needs excess margin to guarantee ZVS, or delivers maximum power with the danger of losing ZVS. Moreover, it cannot work for widely varied input voltages. The PLL is introduced to overcome these issues. With PLL charging control, the power can be improved by 10% with a narrow frequency range.

The three-level structure in particular suffers unbalanced voltage stress in some abnormal conditions, and a fault could easily destroy the system due to minimized margin. Based on thoroughly analysis on the three-level behaviors for unbalanced voltage stress phenomena and fault conditions, a novel protection scheme based on monitoring the flying capacitor voltage is proposed for the three-level structure, as well as solutions to some abnormal conditions for unbalanced voltage stresses. A protection circuit is designed to achieve the protection scheme.

A final prototype, built with a custom-packed MOSFET module, a SiC Schottky diode, a nanocrystalline core transformer with an integrated resonant inductor, and a custom-designed oil-cooled mica capacitor, achieves a breakthrough power density of 140W/in^3 far beyond the highest-end power density reported (<100 W/in^3) in power converter applications.

In memory of my grandfather

Yongshou Sheng

1915-1991

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Table of Contents

Table of Figures

List of Tables

Chapter 1 Introduction

1.1. Background

Pulsed power is a unique technology that can compress energy into a short but intense burst to create extreme conditions without the demand for a very large energetic power source or to create power bursts that cannot be sustained continuously by a conventional converter.

Figure 1-1 shows a basic concept of pulsed power. With traditional power sources, such as batteries, solar cells, fuel cells, or utility electric power, a pulsed power supply is used to pump the energy into the energy storage component. The high-power short pulse is used to generate the active load using lasers, RF, X-rays, particle beams, etc. Energy is typically stored within electrostatic fields via capacitors, magnetic fields via inductors, as mechanical energy using large flywheels connected to special purpose high-current alternators, or as chemical energy using high-current lead-acid batteries, or explosives. The capacitor-charging power supply is a typical application of pulsed power, which is purposed with charging the load capacitor, so the electrical energy is stored in the capacitor and discharged in a short time for varied applications.

The history of the pulsed power generators can be traced back to World War II. Compelling national security needs for radars, accelerators, nuclear weapons effects simulators have resulted in the development of pulsed power and the military application of the pulse generator. As a result of fundamental changes in the world geo-political and strategic military environment, the overall funding base for R&D and procurement in the aggregate shrunk. Fortunately, the commercialization of technology offers significant

promise for providing a significant long-term source of support to keep the pulsed generator moving forward. In a much quoted paper [A-1], Steve Levy et al. described 66 different possible applications of pulsed power technology in 1992. Their list now apparently approaches 100 items [A-2]-[A-8]. Besides being continuously applied on military applications, such as electro-magnetic (EM) guns and armor and the electro-thermal chemical (ETC) gun, pulsed power can be found in industry, medical equipment, and even in our everyday life, e.g. miniature pulsed power make the flash possible in our cameras.

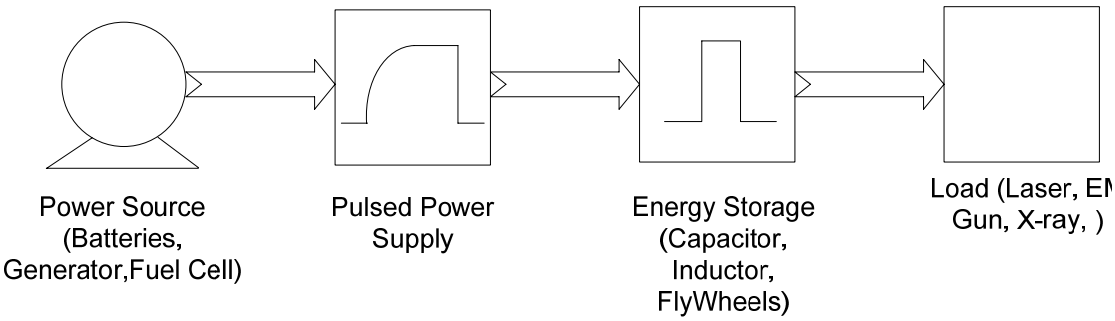


Figure 1-1. What is pulsed power?

The development of the pulsed power technology has been promoted by the emergence and evolution of semiconductor power devices [A-9]-[A-16]. The primitive switches that were developed before the semiconductor power device, such as thyratrons and spark gaps, are commonly used in pulsed-power applications. However, their lifetime and reliability are severely affected by electrode erosion, flashover, reaction products, etc. The power semiconductor devices involved, such as insulated-gate bipolar transistors (IGBTs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and static-induction thyristors (SITs), not only improve the performance of the pulsed power generator in terms of improving the lifetime and providing compactness and mobility, but

semiconductor devices also make the extension of pulsed power applications possible by their unmatched switching performance.

Capacitor charging power supply (CCPS) is a special type of power supply for charging load capacitor. The capacitive energy is used to generate electric or magnetic fields, which can be used for X-ray, laser beam, plasma-source implantation, particle accelerator, EM-gun, etc. The output voltage of the CCPS is normally very high, typically from several kV to several tens of kV, for high energy stored in capacitor. The charge cycle of a CCPS consists of a charging mode during which the capacitor charges to its preset value and the trickle charging mode, also called refresh mode, during which the voltage across the capacitor is maintained stable within a specified tolerance.

In contrast to a conventional high-voltage DC power supply that delivers constant voltage or power to its load, the output power and voltage of the CCPS varies over a wide range during charging process, almost like changing from short circuit initially to open circuit at the end. The instantaneous output power is almost zero at the beginning of the charging mode, and, if the charging current is constant, the peak instantaneous output power occurs at the end of the charging mode. The refresh mode is typically a low-power mode because the currents are small compared to those in the charging mode. The average output power for a CCPS depends on the repetition rate and its maximum stored energy and charging time.

When the CCPS starts to charging the load capacitor, it is important to limit the output (charging) current for safe operation to avoid in-rush current. The CCPS operates in constant-current (CC) mode initially. In refresh mode, the capacitor voltage is maintained constant and CCPS is required to operate in constant-voltage (CV) mode.

Typical durations of the power pulses of CCPS are in the range between nanoseconds and seconds. Some literatures hence propose to fully utilize the "Thermal Inertia" of the semiconductors and the heat sink for the CCPS design. Operation in "Thermal Inertia" mode means that the transient thermal impedance is used for thermal design. In other words, the power loss can be absorbed by the circuit elements themselves, or thermal capacitance. Operation in "Thermal Inertia" mode always means that cooling fins, plumbing, heat exchangers etc. can be eliminated [F-17][F-19].

Now more than ever, the demand for high power is growing while the converter volume is keeping shrinking, which results in a sustained trend toward a challenging requirement of high power density. The research topic of this dissertation focuses on developing a high-density DC/DC converter for capacitor charging. Table 1-I shows the main specifications.

TABLE 1-I. THE SYSTEM SPECIFICATIONS

Parameters	**Specification**
Input voltage	600 V
Output voltage	10 kV
Load capacitance	0.3 mF
Average output power	30 kW
Ambient temperature	65 ^{o}C
Power density	Greatest possible

In order to meet the challenging power density goal and performance requirements, innovative solutions in many areas of the converter system design can be sought, developed and applied. These areas include: topology and control, semiconductor devices, passive components, insulation systems, thermal management systems, and packaging. Figure 1-2 illustrates the basic strategy for high-power-density converter design. Topology and control are the main topics covered in this dissertation.

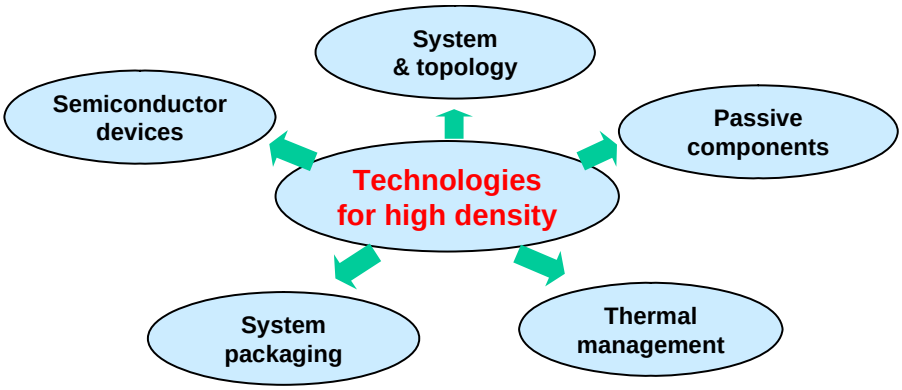


Figure 1-2. Basic technical strategy for high density.

1.2.Research scopes and challenges

The greatest power density possible is desired for the capacitor-charging power supply. A thorough literature review is conducted in order to understand the status of the state-of-the-art power density of pulsed power supply.

Reference [A-17] shows a high-power-density PWM converter design for CCPS through application of MOSFET and new magnetic material. A full-bridge PWM converter is used for its modular design. The system is achieved by 6 200 kW units in parallel. Reference [A-18] introduces a CCPS with series resonant converter (SRC). The converter is operated at 33 kHz with IGBT. High output voltage and voltage sharing on the rectifier diodes are achieved by multiple secondary transformer windings in series. Reference [A-20] focuses on a high-power-density CCPS design. Three-level series-parallel resonant converter (SPRC, also called LCC) is proposed with 200 kHz switching frequency. The 3 kW system achieves 35 W/in^3. The power density is further improved to 72 W/in^3 with a three-level parallel resonant converter at 700 kHz. Based on a thorough survey [A-17]-[A-40], the available power densities are summarized in Table 1-II.

TABLE 1-II. Survey summary on pulsed power charger converter systems

Topology	Semi. Device	Fs Range	Power & Vo	Thermal Method	Power Density	Reference
Full-bridge PWM Hard switch	MOSFET	24 kHz	200 kW 16 kV	Liquid cooling	16 W/in^3	[A-17] 1993
SRC ZCS mode	IGBT	33 kHz	38 kW 40 kV	Water cooling	2 W/in^3	[A-18] 1999
Half bridge PRC	IGBT	30-50 kHz	70 kW 24 kV	Water cooling	16 W/in^3	[A-19] 2001
Three-Level LCC	MOSFET	Up to 200kHz	3 kW 10 kV	Natural Cooling	35 W/in^3	[A-20] 2004
Full bridge SRC	IGBT	Up to 61kHz	20 kW 50 kV		39 W/in^3	[A-21] 2006
Three-Level PRC	MOSFET	Up to 700kHz	3.7 kW 10 kV	Natural Cooling	72 W/in^3	[A-22] 2007

These references reveal that power density is closely associated with detailed specifications and operation conditions. It is hard to make a fair comparison between the power densities of the reported state-of-the-art pulsed converters. In addition, most literature doesn't provide the power density value. Nevertheless, as illustrated in table, power density continually increases with successive pulsed-power converters. IGBTs and MOSFETs are the primary switches applied in the literature surveyed. IGBTs are capable of operating in the range of 10 kHz – 70 kHz. The relatively low conduction loss and high power handling capability are the major advantages of the state-of-the-art IGBTs. However, the relatively low switching frequency of the IGBT limits the further improvement on power density. On the other hand, MOSFETs are adopted to overcome the drawbacks of IGBTs. However the relatively low blocking voltage of the MOSFET as compared with the IGBT constrains its applications. Though the state-of-the-art

commercial MOSFETs have up to a 1.2 kV voltage rating, the performances of the MOSFETs are dramatically decreased as the blocking voltage increases. For the conventional power MOSFET, the drift resistance is proportional to the square of the blocking voltage [F-20]. When the MOSFET blocking voltage increases, the on-resistance will be dominated by the drift resistance, and will dramatically increase. While considering the principal objective of high power density, MOSFET is necessary due to its superior high switching frequency capability.

In order to use a low-voltage-rating power MOSFET, a three-level structure is selected, shown in Figure 1-3 [B-1]-[B-7]. The main advantage of a three-level structure is that the main switch only withstands half of the input voltage.

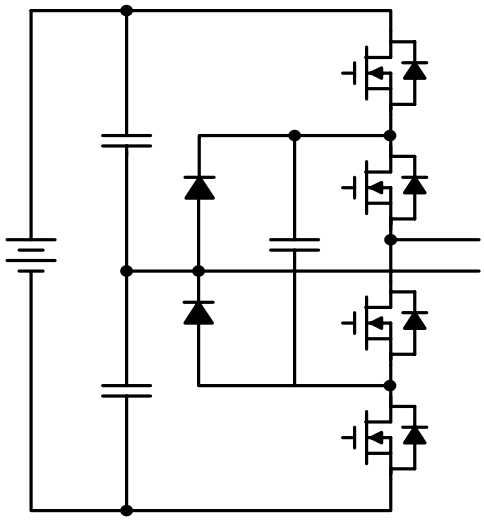


Figure 1-3. Three-level converter

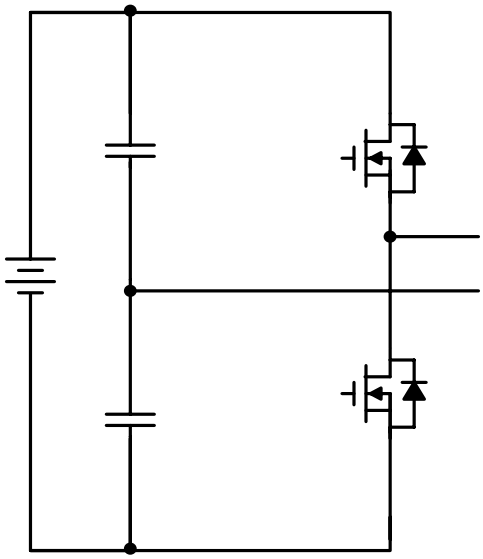


Figure 1-4. Half-bridge converter

The three-level structure can be derived from a half-bridge structure shown in Figure 1-4. If two converters are used to deliver the same power with the same conditions, the main difference between the two converters is the device selection for the main switches of each converter, which can be briefly illustrated by the following comparison. Table 1-III shows two MOSFETs, 1200V/30A for the half-bridge converter and 600V/31A for the

three-level converter. With the same operating conditions, the two converters have the same voltage margin. Typically, the industry benchmark figure-of-merit (FOM) product Rdson*Qgd is used here to represent the performance of different devices. It is obvious that the FOM of the 600 V MOSFET is much lower than the FOM of the 1200 V MOSFET. Even considering the two 600V MOSFETs in series needed in a three-level converter, the on-resistance and gate charging energy are still much less than the half-bridge converter with a 1200V MOSFET, which also means high efficiency with a three-level converter. Furthermore, the current rating is limited as the device voltage rating increases due to the available large die size. Hence more high-voltage-rating devices are needed in parallel due to low current rating, which means a complex layout and worsened paralleling issues.

TABLE 1-III. MAIN MOSFET CHARACTERISTICS FOR HALF-BRIDGE AND THREE-LEVEL

Structure	Device	Rating	Rdson (Ω)	Qgd (nC)	FOM (Ω*nC)
Half-Bridge	APT12040L2FLLG	1200 V 30 A	0.40	179	71.6
Three-level	APT6017JFLL	600 V 31 A	0.17	55	9.35

Regarding the topologies applied in a pulsed power supply, these topologies can be categorized generally into two types: PWM converters and resonant converters. The PWM converters include the conventional boost [A-25], flyback [A-26], Ward [A-27] and full-bridge PWM converters [A-17], [A-28]-[A-30]. Like PWM converters, resonant converter topologies have been introduced and used widely for pulsed power supplies, including the series resonant converter (SRC) [A-18], [A-21], [A-31]-[A-34], parallel resonant converter (PRC) [A-22], [A-36], series-parallel resonant converter (SPRC) [A-37], [A-38] and LCL-T resonant converter, [A-39], [A-40]. The topologies can be divided into isolated topologies and non-isolated topologies depending on whether there is a

transformer.

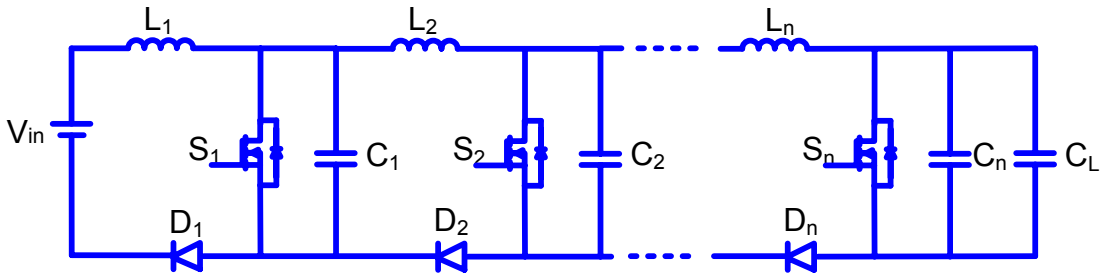


Figure 1-5. Cascade Boost converter, also called Marx converter.

Based on the literature survey, non-isolation topologies, such as the boost converter, are seldom found in pulsed power supplies. This is partially due to the barriers of the performance of high-voltage devices. Operation duty cycle could be another practical reason to restrict the application of the simpler non-isolation topologies. A boost converter array shown in Figure 1-5 has been introduced to reduce the device voltage stress and optimize duty cycle control, but the system will be very expensive, bulky and inefficient [A-41][A-42].

With the presence of a transformer, we can utilize low-voltage, high-current switches on the primary side and low-current, high-voltage devices for the secondary side. However, for isolation topologies in high–power, high-frequency operations, attention must be paid to the influence of parasitics, which induces high voltage stress, and can even change the converter behavior. Resonant converters are preferred to solve these issues. In order to shrink the passive components' volume, high-frequency operation is preferable. ZVS and ZCS soft-switching can effectively reduce the switching loss and therefore these soft-switching technologies are widely applied for the capacitor-charging systems. Due to the special properties of capacitor load, the load condition varies widely, even from short circuit to open load during the charging process. Conventional phase-shift PWM

converter suffers ZVS loss of lagging switches at light load. Many literatures introduce improved topologies to achieve ZVS for whole load conditions [F-21]-[F-23]. However, compared with phase-shift PWM converter, the resonant tank circuit can help to achieve ZVS operation much more easily for whole charging period without any auxiliary circuit.

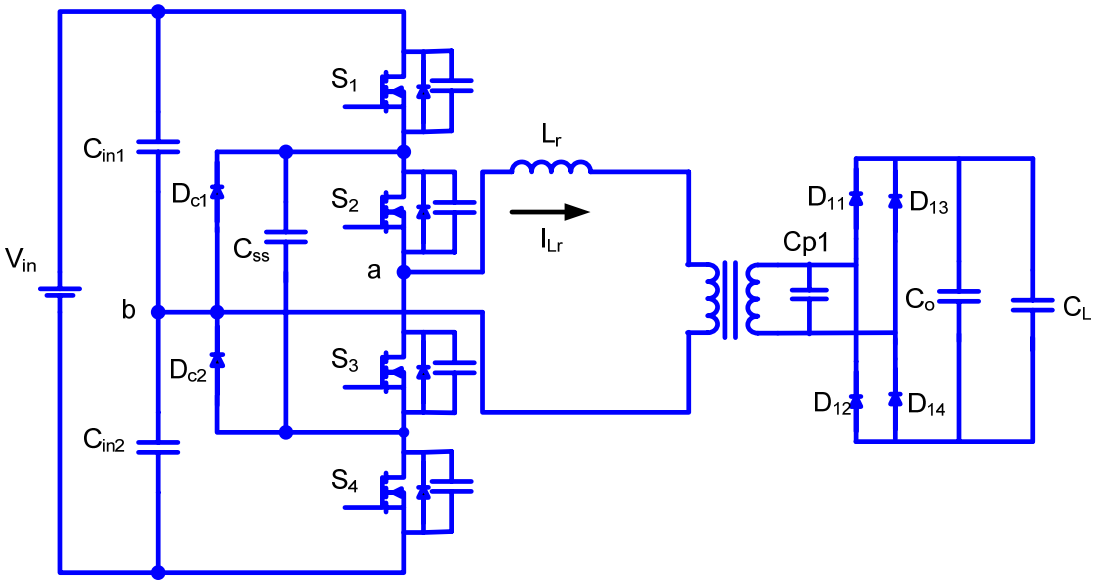


Figure 1-6. The thee-level parallel resonant converter.

Regarding the varied types of resonant converter, obviously the parasitics of the transformer cannot be absorbed fully by the SRC, and they will distort the behavior of the SRC. Furthermore, the necessary extremely high turns-ratio will exacerbate the parasitics of the transformer because of its non-step-up property. SPRC and LCL converters have been introduced as appropriate solutions to these problems. In terms of power density, the introduced external resonant component will impact the power density. In addition, the LCL also cannot completely absorb the transformer's parasitics. Considering the critical requirements of high power density and a high-voltage boost, after a thorough comparison a PRC topology was chosen as the prototype converter design for capacitor-charging applications because of its desirable features, minimal resonant components,

high-voltage boost property and full absorption of the transformer's parasitics. The transformer leakage inductor can be utilized as a resonant inductor with proper design to make a further improvement on the power density. Therefore, a three-level parallel resonant converter is proposed as the main topology, shown in Figure 1-6.

Though the topology is proposed for high-power-density capacitor-charging power supply design, the following question still exists: What are the challenges for a high-power-density three-level parallel resonant converter design?

First, normalization method is commonly used in traditional resonant tank design. With this method, the resonant tank can be treated as a black-box for one type of resonant tank, such as the SRC or PRC. Therefore, the influence of structural variations of the resonant tank on the volume of the transformer and resonant components is neglected. However, the voltage and current of the resonant tank components, including the transformer, are closely related to the transformer positions, which will finally influence the components' design and volume, thereby having an impact on the system's power density. Particularly as one of the most bulky and expensive components in the power converter, the influences of different resonant converters' configurations on the transformer are never analyzed. A methodology for high-power-density resonant tank design is needed. A proper resonant tank can not only improve the converter performance, but also increase the system power density.

Secondly, when the main topology is determined, the main component count is fixed. How to reduce the components' volume by reducing the components' stresses, including the voltage stress, current stress and thermal stress, is equally important for the high-power-density objective. On the other hand, reducing the current stress and thermal stress

also helps to improve the efficiency, and then improves the power density due to increased power delivery capability. The three-level parallel resonant converter can employ the better performance MOSFET and make the soft-switching operation possible during the whole charging period; however, it depends on a control scheme to exert the benefits of the topology. A desired control scheme is required to achieve soft-switching, reduce the components' stresses and maximize the power delivery capability.

Thirdly, three-level structure is selected for low voltage rating MOSFET application. The problem of unbalanced voltage stresses of the main switches in three-level structure has also been reported in literatures. However, the reasons are not fully analyzed, as well the system's failure phenomena. Furthermore, as all of our efforts are focused on high power density design, a reduction in reliability is the penalty paid for the high-power-density converter, which can be caused by the following reasons. a) Noise interference should be the first concern, as it can significantly interfere with the controller behavior and even other equipment. The noise is worsen due to large parasitics caused by the bulky components and the distance needed for high-voltage isolation and high dv/dt and di/dt in a high-power converter. b) In order to minimize component volume and achieve high power density, the least margins are left in component selection and design. The voltage and current spike will increase for high-switching–frequency, high-power applications, which will result in system failure or shorten the system's lifetime. c) Though the three-level structure reduce the main switches' voltage stress and makes the application of the power MOSFET possible, it is subject to unbalanced voltage stresses for the two switches in series. Furthermore, as opposed to other DC-DC converters, the converter always works at wide load conditions during the capacitor charging, which

requires a very reliable design and control. Even with a very reliable design, failure cannot be completely eliminated. Effective detections and protections against multiple failures without bulky and lossy components are expected.

Moreover, all of the concepts have to be verified with hardware implementation. Besides achieving the required performance and functions, a compact system design will finally impact the system volume. Finding how to integrate all of the components into a high power density converter while delivering the performance as expected is challenging and critical.

To address these issues, the objective of dissertation is to investigate different solutions to achieve a breakthrough in high-power-density of a capacitor-charging power supply at high-power, high-frequency operation.

1.3.Organization of dissertation

The background and status of the development of capacitor charging power supplies have been provided in the Introduction. The development barriers and challenges have been identified. In order to meet the challenging power density goal and performance requirements, the issues are be investigated and solved with the proposed methods. The following chapters are arranged as follows:

In Chapter II, a methodology of high-power-density resonant tank selection is detailed. Though the preliminary three-level parallel resonant converter is chosen, a high-power-density parallel resonant tank is selected after thorough analysis and comparison. The concept of high-power-density resonant tank selection can be extended to the other resonant tanks, such as the SRC and SPRC. A prototype with two different PRC resonant tanks is built and tested for verification.

In Chapter III, two control schemes are presented for three-level control and resonant converter charging control, respectively. Phase-shift (PS) control is widely used in three-level DC-DC converters for soft switching. Compared with PS, non-phase-shift control can not only reduce the power loss, but also reduce the parasitic influence and component stress. While the proposed schemes are for capacitor charging control, a constant-power-factor control scheme has been proved to have advantages over conventional charging schemes, like constant power charging and constant current charging, for high efficiency. Phase-locked loop (PLL) is first introduced for capacitor charging control, which can not only guarantee ZVS operation during the whole charging period, but also maximizes the output power delivery with minimized circulating energy. The design procedure and boundaries are discussed. The analysis and design are verified by simulation and experimental results.

In Chapter IV, a novel protection circuit is proposed to prevent failures from unbalanced voltage stresses and protect the system against cases of multiple failures. Most failures come from the unbalanced voltage stresses across the main switches. Due to the feature of the three-level structure, a failure of one of the switches will cause all of the rest of the switches to fail. The mechanism of the possible failure is analyzed and the reasons are classified. A novel protection circuit based on flying capacitor voltage monitoring is proposed. With the help of simulation, this protection method is sensitive to multiple failure cases. The effect of the protection for different failure cases is summarized and validated by experimental results.

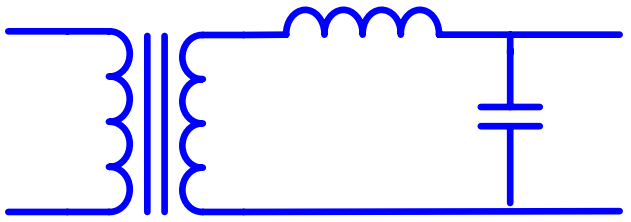
In Chapter V, the hardware implementation and experimental results are addressed, including component design and selection, system design and assembly, and functional

verification. A prototype with a breakthrough power density, 140W/in^3, is successfully achieved.

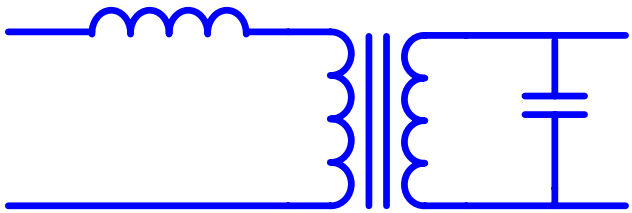
Finally, Chapter VI summarizes the entire dissertation. Future work is discussed based on the achievements of this study and the insights gained on the topic.

Chapter 2 High Power Density Resonant Tank Design

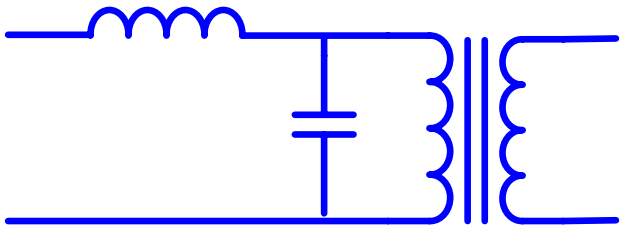
To meet the extreme demand for high power density, the passive component size should be reduced using a high switching frequency. The conventional PWM converter suffers from excessive power loss as the switching frequency is increased, and parasitics significantly distort the converter's operation. Resonant converters are preferred because of their desirable properties for high switching frequency operation, such as soft-switching operation, parasitics absorption and/or utilization, and low EMI.



(a) Structure I



(b) Structure II



(c) Structure III

Figure 2-1. Three PRC structural variations with different transformer position.

When transformer is used in resonant converter, the resonant converter can have different structural variations associated with different transformer position. With

different transformer positions in the resonant tank, all of the structural variations of the PRC are shown in Figure 2-1.

The different structural variations can be found in a variety of applications [C-1]-[C-4]. [C-5] and [C-6] compare the resonant converter behavior when the resonant capacitor is moved from the transformer primary side to secondary side, or the PRC structure I or structure II shown in Figure 2-1. The comparison focuses on the influence of transformer leakage inductance and stray capacitance on resonant tank. Due to the non-ideality of high frequency transformer, transformer design and its influence on resonant converters are thoroughly discussed in the discussion of converter design [C-7]-[C-10].

Even though it is one of the most bulky and expensive components in the power converter, the influences of different resonant converters' configurations on the transformer are never analyzed. The size of the transformer is limited by the maximum temperature rise and the saturation flux density of the core material. The transformer power handling capability is significantly related to its volume. While it does not change the resonant converter design and performance, different positions of the transformer in the resonant tank cause serious differences in the transformer's volume, as well as the voltage and current stress on resonant elements. The improper selection of the resonant tank structure with the transformer can offset the benefits of increasing switching frequency operation, making the situation even worse.

This chapter explains the concept derived from the parallel resonant converter (PRC). Two example designs and experimental results are provided for verification. A methodology for a high-power-density resonant tank design is proposed. This concept can be extended to other isolated resonant converters.

2.1. Structural variations and volumetric formula

If these structural variations meet the following assumptions, these structural variations can deliver same performance as a PRC converter.

1. The transformer is an ideal transformer and has the same turns-ratio for all structures.
2. The converters work under the same conditions, including the same input voltage, output voltage, load resistance, switching frequency, etc.
3. The resonant tanks have the same normalized resonant frequency and resonant impedance.

The resonant tank design is independent of the structural variations under the above assumptions. Thus, in essence, the converter performs the same with different structures; the only change is the resonant tank structure, which affects the resonant inductance and capacitance.

If the transformer turns-ratio is N (secondary turns over primary turns), the inductance will be $L_p \cdot N^2$, and the capacitance will be C_p / N^2 when they are moved from the transformer's primary side to the secondary side. L_p and C_p are the inductance and capacitance, respectively, when they are on the transformer's primary side. Though the converter has the same performance based on the assumed operating conditions, each component has distinct effects on the voltage and current stresses in different variations. In order to evaluate the influence on the components volume, and then the power density, a series of volumetric functions are used, as described below [F-1]-[F-4].

2.1.1. Volumetric formula

A. Transformer volume estimation

The transformer volume estimation is very complex, encompassing the dependence of

winding loss [F-24]-[F-28], core loss and permeability [F-27]-[F-34], and heat transfer [F-34]-[F-36]. In order to keep with the objective of the analysis, comparing the influence of different transformer positions in resonant tank for same application, the variables of voltage and current of the transformer are focused for transformer volume comparison. Therefore, the following assumptions are made:

- core material
- core geometry
- the current density in the conductors
- the maximum flux density allowed in the magnetic material.

The transformer design has a set of constraints, such as the saturation flux density and power handling capability. The area product (AP) is widely used transformer design, obtained by multiplying the core magnetic cross-section area by the window area.

The required cross-sectional core area of the transformer (A_c) is given by:

$$A_c = \frac{\int_0^{\frac{T_s}{2}} V_p dt}{2 \cdot B_m \cdot N_p} \tag{2-1}$$

where V_p is the transformer primary side input voltage, T_s is the switching period, B_m is the achieved maximum flux density, N_p is the primary winding turns.

If using λ to express the volt-sec,

$$\lambda = \int_0^{\frac{T_s}{2}} V_p dt \tag{2-2}$$

The equation (2-1) can be simplified as

$$A_c = \frac{\lambda}{2 \cdot B_m \cdot N_p} \tag{2-3}$$

If the voltage waveform is a regular waveform, the equation (2-1) can be expressed again

by

$$A_c = \frac{V_p}{B_m \cdot N_p \cdot f_s \cdot K_f} \tag{2-4}$$

where V_p is the transformer primary side input voltage, f_s is the switching frequency and K_f is the waveform coefficient. For square waveform, K_f is equal to 4; for sinusoidal waveform, K_f is equal to 4.44.

The window area is occupied by primary winding and secondary winding.

$$A_w = \frac{N_p \cdot A_{wp}}{K_u} + \frac{N_s \cdot A_{ws}}{K_u} \tag{2-5}$$

where K_u is the window utilization factor, N_s is the secondary winding turns, A_{wp} is the primary winding wire area and A_{ws} is the secondary winding wire area.

It is reasonable to assume that the primary winding and secondary winding have the same current density J , it can be expressed by:

$$J = \frac{I_{prms}}{A_{wp}} = \frac{I_{srms}}{A_{ws}} \tag{2-6}$$

While the winding current keeps the following relationship:

$$\frac{I_{prms}}{I_{srms}} = \frac{N_s}{N_p} \tag{2-7}$$

Inserting the equation (2-6) and (2-7) into (2-5) yields

$$A_w = \frac{2 \cdot N_p \cdot I_p}{K_u \cdot J} \tag{2-8}$$

The needed area product (AP) can be obtained by combining the equation (2-3) and (2-8)

$$AP = A_w \cdot A_c = \frac{\lambda \cdot I_{prms}}{B_m \cdot J \cdot K_u} \tag{2-9}$$

Though the formula includes many variables, the volt-sec and current are the only two variables for each of the structures and the fixed core material. Some literatures use the area product (AP) for volume estimation [F-3][F-37]. But it is rough and can not be explained with a physical meaning. [F-2][F-4][F-38] derive a function which indicates that the transformer volume is approximately proportional to its VA to the power of ¾, given by

$$Vol_T \propto (A_w \cdot A_c)^{0.75} \propto (\lambda \cdot I_{rms})^{0.75} \tag{2-10}$$

Transformer volume is hard to obtain accurately with a derived function. It needs a case by case study. However, the above equation is sufficient for transformer volume comparison.

Because the sinusoidal approximation method will be used for the analysis and comparison in the next section, the influence of the waveform coefficient, K_f, will be automatically considered. Therefore, the waveform coefficient can be removed from the volumetric expression, and the rms value of voltage can be used. Transformer volume is approximately proportional to its VA to the power of ¾, which is also called "VA size", as expressed by (2-11).

$$Vol_T \propto (A_w \cdot A_c)^{0.75} \propto (V_{rms} \cdot I_{rms})^{0.75} \tag{2-11}$$

B. Inductor volume estimation

The resonant inductor is an ac inductor. The design is similar to that of a transformer. The assumptions made for transformer still work for inductor. The same maximum flux

density for inductor design also indicates the same core loss density. In addition, the inductor currents in different structural variations have the same shapes. Only the magnitudes vary with the different transformer positions. Usually the inductor current is the sinusoidal waveform in the resonant converter. So the waveform effect can be ignored. Inductor design can also use the area product method.

The needed core window area is expressed by:

$$A_w = \frac{I_{rms} \cdot N}{J \cdot K_u} \tag{2-12}$$

And the desired core cross-section area can be obtained by the following equation:

$$A_c = \frac{L \cdot I_{\max}}{N \cdot B_m} \tag{2-13}$$

where $I_{\max}$ is the peak winding current. For a simple comparison, the peak current is replaced by the rms current.

and then the area product can be expressed by:

$$AP = A_c \cdot A_w = \frac{L \cdot I_{rms} \cdot I_{\max}}{k_u \cdot J \cdot B_m} \propto L \cdot {I_{rms}}^2 \tag{2-14}$$

Using the same assumptions as we used with the transformer, the inductor volume can be proportional to its stored energy [F-38][F-39]:

$$Vol_L \propto (A_w \cdot A_c)^{0.75} \propto (L \cdot I_{rms}^2)^{0.75} \tag{2-15}$$

Obviously, the product of $L \cdot I_{rms}^2$ is constant for the resonant inductor on either side of the transformer, which means there is a constant inductor volume. When the inductor located on one transformer side with low inductance and high current is moved to other side with high inductance and low current, in essence, the inductor just trades its copper

loss to iron loss. It should be noted that energy storage method is not accurate enough to inductor volume optimization in a particular applications. It needs a case by case design.

C. Capacitor volume estimation

The relationship between the electrical properties of the capacitor and the volume of the capacitor isn't as clear as the magnetics.

Voltage and capacitance are the key contributors to the volume. The volume of the capacitor is considered to be proportional to its stored energy [F-39][F-40].

$$Vol_c \propto C \cdot V^2 \tag{2-16}$$

Like the resonant inductor, the products of CV^2 stay constant, as further explained by the following example. For instance, N discrete capacitors in parallel are needed to meet the requirements for capacitance, voltage rating and current rating when the transformer turns-ratio is N and the resonant capacitors are located on the primary side. They can meet the requirements of capacitance, voltage rating and current rating automatically when they are moved to secondary side by simply changing the connection from paralleling to series, and vice versa. Obviously, the volumes of resonant capacitors stay the same for either side. This example can also explain the influence of the resonant inductor. Again, it should be noted that the volumetric function is not accurate enough for volume optimization for a particular application. In addition, the commercial capacitors' parameters vary into discrete steps not in a continuous way. Thus, once the designer obtains the calculated values for the required capacitor and checks the commercial datasheets, the closed upper values could be quite far. Reference [F-41][F-42] provide a curve about the relationship of capacitor volume, energy and voltage based on commercial electrolytic capacitors. [F-43] even provides an equation to describe the

relationship of volume and voltage rating for electrolytic capacitor. Though Mica or ceramic capacitors commonly are used for resonant capacitors instead of electrolytic capacitor, a more accurate volumetric function for these capacitors need further study.

2.2.Transformer volume comparison

Based on the aforementioned assumptions and analysis, the volume of the inductor and capacitor stay the same, no matter where the transformer is. So only the impact on transformer size is discussed in this section.

In order to simplify the analysis, the voltage and current of the transformer are described by normalized data. The base quantities are given below:

$$V_b = V_{inrms}, I_b = I_{inrms}, f_b = f_o \tag{2-17}$$

where V_{inrms} is input voltage to the resonant tank, I_{inrms} is the input current to the resonant tank and f_o is the resonant frequency of the resonant tank.

The transformer's voltage and current of Structure I are the same as the base quantities. According to the transformer volumetric function (2-10), the volume of the transformer in Structure I is used as the base quantity.

$$Vol_{Tr\_b} = Vol_{Tr\_strI} \propto (V_b \cdot I_b)^{0.75} \tag{2-18}$$

Compared with the transformer in Structure I, the current of the transformer of Structure II is the same as the input current, while the voltage is different while the transformer in Structure III suffers different voltage and current.

$$Vol_{Tr\_strII} \propto (V_{rms\_2} \cdot I_{rms\_2})^{0.75} \tag{2-19}$$

$$\frac{Vol_{Tr\_strII}}{Vol_{Tr\_b}} \propto \left(\frac{V_{rms\_2}}{V_b}\right)^{0.75} = (M_v)^{0.75} \tag{2-20}$$

where $M_v = \frac{V_{rms\_2}}{V_b}$.

$$Vol_{Tr\_strIII} \propto (V_{rms\_3} \cdot I_{rms\_3})^{0.75} \tag{2-21}$$

$$\frac{Vol_{Tr\_strII}}{Vol_{Tr\_b}} \propto \left(\frac{V_{rms\_3} \cdot I_{rms\_3}}{V_b \cdot I_b}\right)^{0.75} = (M_v \cdot M_i)^{0.75} \tag{2-22}$$

where $M_i = \frac{I_{rms\_3}}{I_b}$.

There are plenty of papers on resonant converter analysis. Sinusoidal approximation [C-12] and the state plane [C-13]-[C-16] are two important methods for fundamental analysis. The sinusoidal approximations have a particular problem when the converter is in discontinuous conduction modes, because the harmonics cannot be ignored, or at low quality factor, due to non-sinusoidal waveforms. However, it has a closed-form solution and is good enough to illustrate the differences between the component stresses of the structural variations. For the design, many papers have detailed analysis and design guidelines based on particular topologies and operation modes. In any case, simulation is the best way to obtain the exact component stresses.

The transformer voltage of structure II and structure III, M_v, is given by the equation (2-23)

$$M_v = \left| \frac{Q}{\frac{\pi^2}{8} \cdot Q - \frac{\pi^2}{8} \cdot Q \cdot \omega_n^2 + j \cdot \omega_n} \right| \cdot \frac{\pi}{2\sqrt{2}} \tag{2-23}$$

where $Q = \frac{R_L}{N \cdot Z_o}$, R_L is equivalent load resistance, N is transformer turns-ratio, Z_o is

the resonant impedance; $\omega_n = \frac{\omega_s}{\omega_o}$, $\omega_s = 2\pi f_s$, ω_o is the resonant frequency.

The current of the transformer in structure II is the same as the structure II. The current of the transformer in structure III, M_i, is given by the equation (2-24).

$$M_i = \left| \frac{Q}{\frac{\pi^2}{8} \cdot Q - \frac{\pi^2}{8} \cdot Q \cdot \omega_n^2 + j \cdot \omega_n} \right| \cdot \left| \frac{j \cdot \omega_n}{Q} + \frac{\frac{\pi^2}{8}}{1 + j \cdot \omega_n \cdot Q \cdot \frac{\pi^2}{8}} \right| \tag{2-24}$$

TABLE 2-I. TRANSFORMER'S VOLAGE, CURRENT AND RELATED VOLUME IN ALL VARIATIONS OF PRC

Structural variation	Voltage	Current	Volume Index	Normalized Volume
Transformer of Structure I	1	1	1	1
Transformer of Structure II	M_1	1	M_1	M_1
Transformer of Structure III	M_1	M_2	$M_1 \cdot M_2$	$M_1 \cdot M_2$

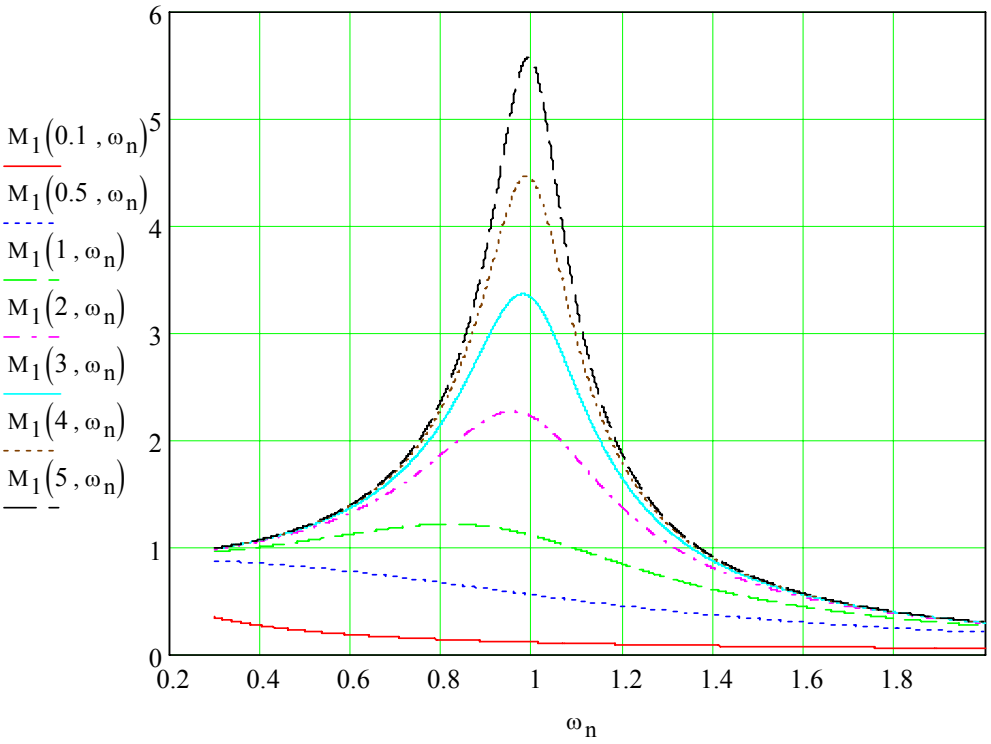


Figure 2-2. PRC output voltage gain (M_v) after waveform adjustment.

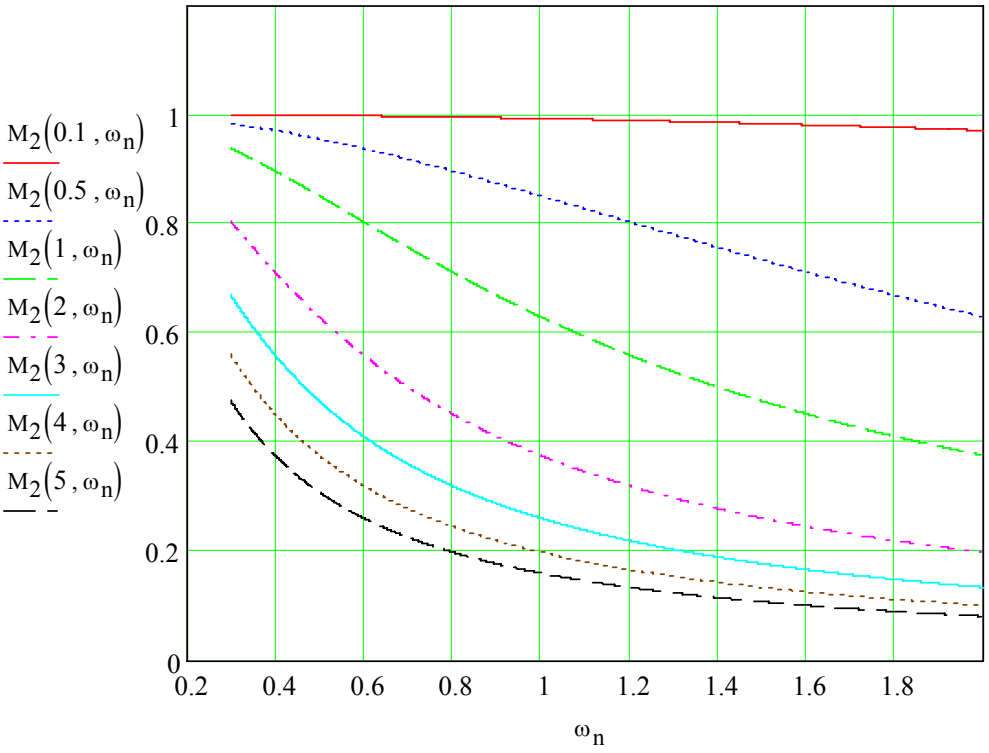


Figure 2-3. PRC output current gain (M_i).

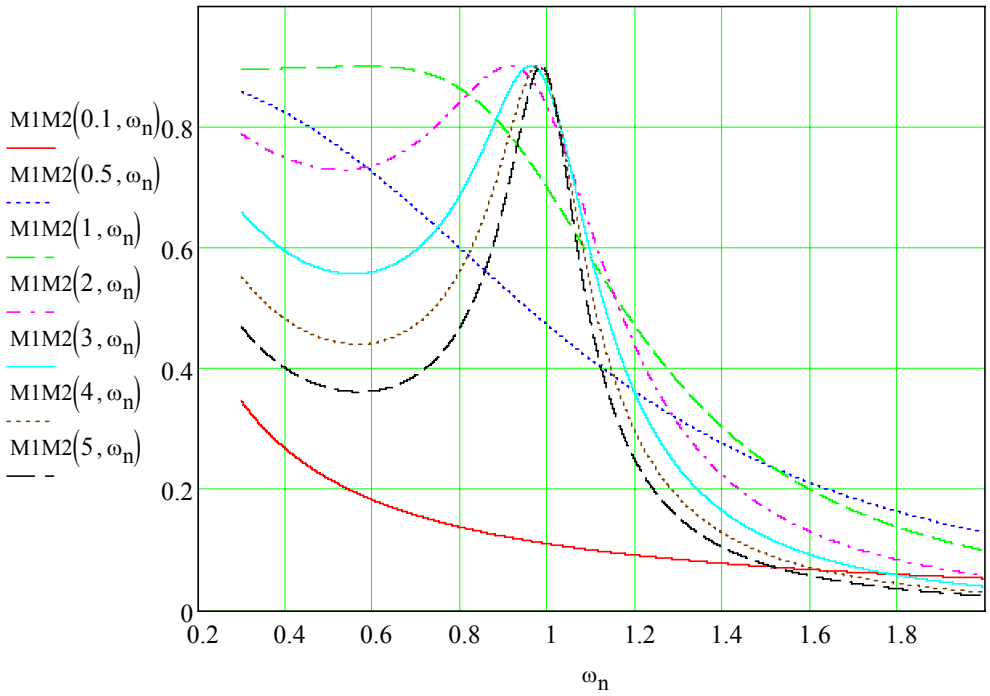


Figure 2-4. The product of M_i and M_v ($M_i \cdot M_v$)

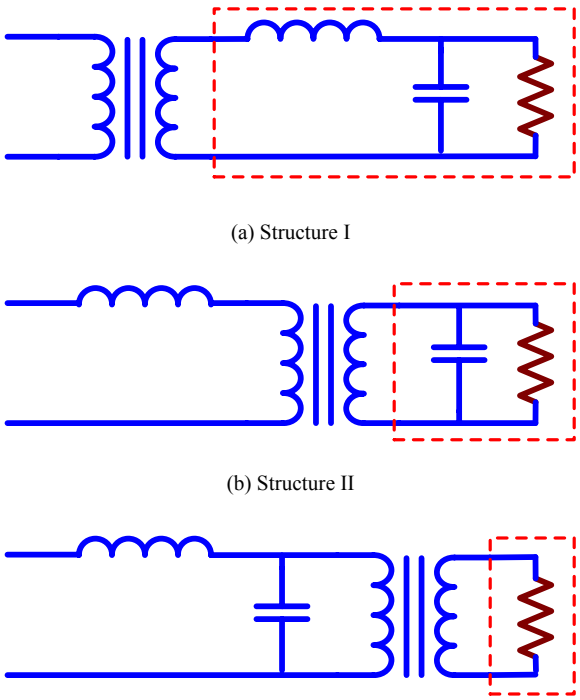
Table 2-I lists the transformer normalized voltage, current, volume index and normalized volume. Figures 2-2, 2-3 and 2-4 show the relationships of M_i versus normalized frequency, M_v versus normalized frequency, and $M_i \cdot M_v$ versus normalized frequency (ω_n) with varied quality factor Q, respectively.

The current is the same for the transformers in Structure I and Structure II. Therefore the volume of the transformer in these two structures is only influenced by the voltage and its waveform. The resonant tank input voltage is the same as the voltage on the transformer in Structure I. Consequently, the voltage ratio M_v is equal to the VA product ratio of the transformers in Structure I and Structure II. As Fig.2-2 shows, the transformer in Structure II is much larger than the transformer in Structure I when the converter is operated at high Q and the switching frequency is near the resonant frequency. Though the transformer in Structure II has low voltage at low Q, or the switching frequency is very different from the resonant frequency, this operation mode is undesired due to the weak voltage regulation capability and the fact that it loses the resonant converter's advantages.

Unlike Structure II, Structure III has different voltage and current on the transformer than Structure I. The ratio of the output current to the input current, M_i, is shown in Figure 2-3, which is usually less than one. Based on the curves of the product of $M_i \cdot M_v$ shown in Fig. 2-4, the advantages of Structure III over Structure I in the transformer is noticeable. The maximum achievable value of $M_i \cdot M_v$ is around 0.9, which is caused by different waveforms. Obviously, Structure III is preferred in terms of power density.

2.3.Theoretical explanation and summary

From Fig. 2-2, we see that M_v can be either much larger than one or less than one with different quality factors (Q) and switching frequencies (ω_n). In order words, the volume of the transformer in Structure II can be larger than or less than the transformer volume in Structure I. As shown by Fig. 2-4, the product of $M_i \cdot M_v$ is always less than one, which means the transformer volume in Structure III can be always smaller than the one in Structure I .



(a) Structure I

(b) Structure II

(c) Structure III

Figure 2-5.The equivalent load of the transformer in PRC structural variations.

Significant changes to the transformer's volt-amps (VA) can be explained by the power factor concept. Figure 2-5 shows the transformer equivalent load in three PRC structural variations. To simplify the analysis, the structures are classified into two types: Type A and Type B.

A. Transformer withstands real power

The transformer in Structure III is directly connected to the load. Therefore, the transformer always has in-phase voltage and current, or only withstands real power, shown in Figure 2-6. For the same application, the converter delivers the same output power to load. Thus the transformer design in Structure III is determined by only the converter power level and switching frequency. This kind of structure is desired for the high-power-density resonant tank due to the minimal transformer size.

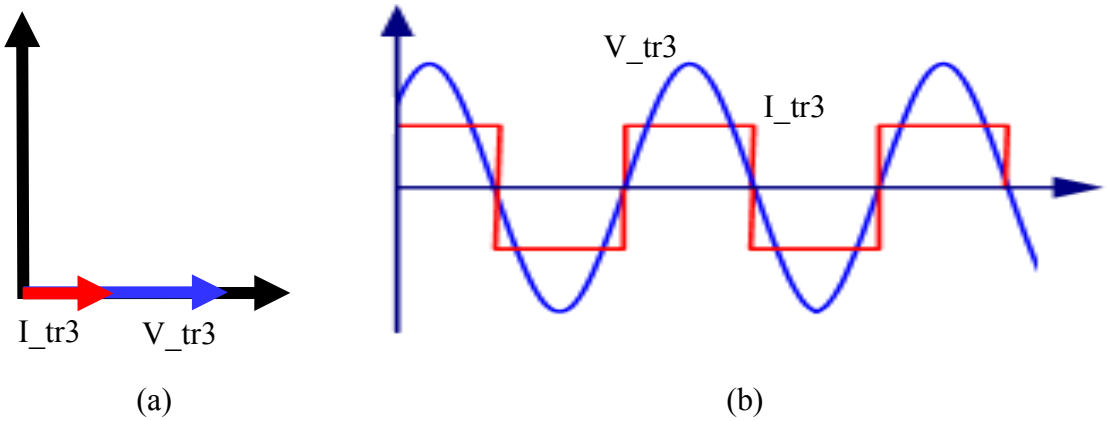


Figure 2-6. Current (I_tr3) and voltage (V_tr3) of the transformer in PRC structure III. (a) voltage and current vectors (b) current and voltage waveforms

B. Transformer withstands real power and reactive power.

In contrast with Type A, the transformer in Type B, which is both Structure I and Structure II, has to endure high reactive power in addition to the real power, shown in Figure 2-7 and Figure 2-8. Even for the same application, the transformer in Type B may need several times higher VA product than the VA product of Type A due to the low power factor.

When the switching frequency is close to the resonant frequency, the reactive power is minimized, and the VA product of the transformer in Structure I approaches the VA product of the transformer in Structure III. The voltage vector and current vector can be in phase when the switching frequency is equal to the resonant frequency. However,

compared to the VA product of transformer in structure III, it still suffers a slightly larger VA product due to the square waveform of voltage while the voltage across the transformer in structure III is sinusoidal waveform.

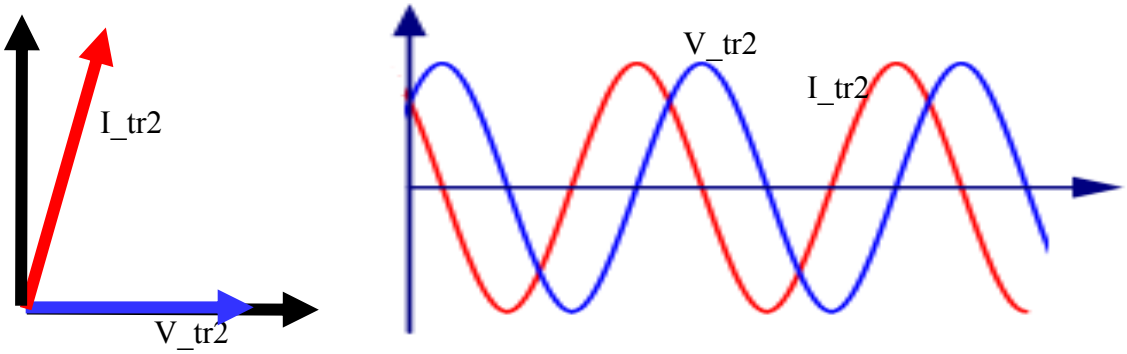


Figure 2-7. Current (I_tr2) and voltage (V_tr2) of the transformer in PRC structure II. (a) voltage and current vectors (b) current and voltage waveforms

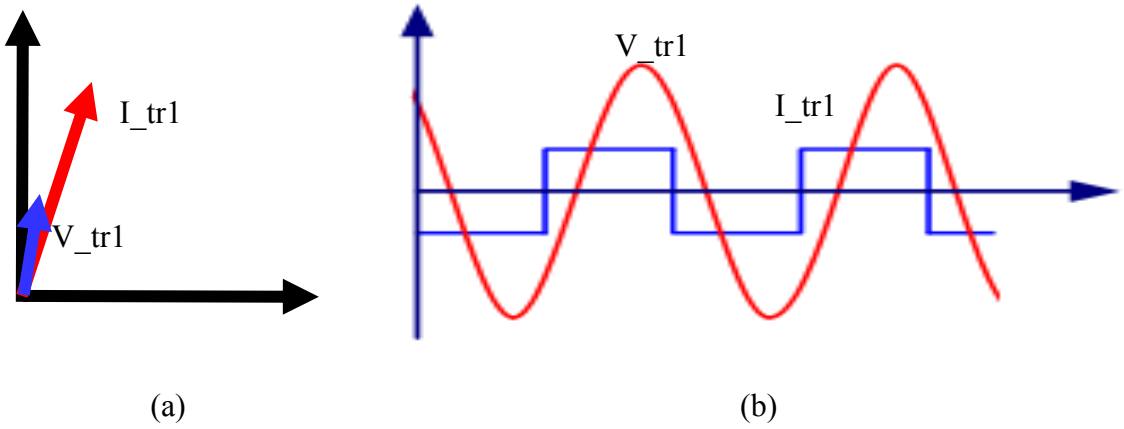


Figure 2-8. Current (I_tr1) and voltage (V_tr1) of the transformer in PRC structure I. (a) voltage and current vectors (b) current and voltage waveforms

When the transformer is incorporated into the resonant tank, like in Structure II, however, the transformer will suffer high reactive power when the switching frequency is near the resonant frequency. When the switching frequency is far beyond the resonant frequency, the resonant inductor plays a dominant role, so that the transformer in Structure II has lower voltage than in Structure I. When the switching frequency is far below the resonant frequency, the resonant capacitor plays a dominant role, so that the

voltage of the transformer in Structure II moves closer to the voltage of the transformer in Structure I. In essence, the behavior of the PRC at a low quality factor is similar to its behavior at a high switching frequency. The PRC at low quality factor works like a PWM converter, and the resonant inductor is dominant.

Based on this analysis, the following points can be made.

1) In terms of power density, it is desirable to leave the transformer with the output load to achieve unity power factor, like in Structure I. The transformer volume can be determined by the converter power level and the lowest switching frequency.
2) When the resonant converter operates around the resonant frequency, the transformer connected with the input source also has a high power factor and low VA, like in Structure II. This operation area is normally desired by the designer for a resonant converter. Though its VA could be larger than the VA of Type B in some conditions, such as when the switching frequency is far beyond the resonant frequency, it still can be an option, because the worst case will determine the transformer design for varied switching frequency control.
3) For high-power-density resonant converter design, it is not recommended to have the transformer in the middle of the resonant tank unless there are some special considerations or operation modes.

2.4.Example design and experimental verification

The topology shown in Figure 2-9 is chosen to verify the impact of structure variations on the transformer volume. The input and output keep the same conditions. The only variable is the black box, which will be replaced by Structure I and Structure II of the

PRC. The detailed component design and experimental results are provided below for comparison and verification.

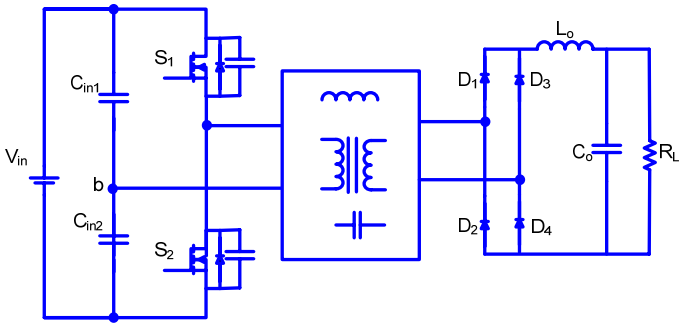


Figure 2-9. Half-bridge PRC.

2.4.1. Example design

The PRC is commonly used at a high quality factor. At a low quality factor, the current of the PRC is a triangle that induces a large turn-off loss and EMI noise. The converter boosts 100V input voltage to a 300V output voltage. Since the magnitude of the AC voltage is half that of the input voltage, the six-fold voltage gain is achieved by twice the turns ratio of the transformer and three times the voltage gain of the PRC. Two converters running at the same frequency with the same normalized frequency point are expected to perform the same, even though they employ two different structures. The design requirements and the resonant component values of each structure are summarized in Table 2-II and 2-III. The voltages and currents of the transformers and resonant inductors are listed in Table 2-IV for Structure I and Structure II. The voltages and currents of the resonant capacitors are not provided because they are identical in these two structures.

TABLE 2-II. SUMMARY OF CONVERTER SPECIFICATION

Parameters	Value	Parameters	Values
Input voltage	100 V	Output Voltage	300 V
R_Load	100 Ω	Io	3 A

Switching frequency	100 kHz	Resonant Frequency	95 kHz
Turns Ratio	2	Resonant Impedance	7.2 Ω
Q	4	M	3

TABLE 2-III. DETAILED RESONANT TANK PARAMETERS

Structure I		Structure II	
L	48uH	L	12uH
C	58nF	C	58nf

The VA of Structure I is a little bit larger than the output power due to the inductive current needed for ZVS operation, as shown by Table 2_IV. However, it is only about one-third of the VA of Structure II. Though the transformer leakage inductance is absorbed by the resonant inductor in both converters and doesn't impact the converter behavior, the large leakage inductance will impact the comparison results. The interleaving techniques of the primary and secondary layer are employed to minimize the leakage inductance. Litz wire is used for the transformer and inductor design. The inductances of the resonant inductors are slightly tuned based on the measured leakage inductances.

TABLE 2-IV. VOLTAGE AND CURRENT STRESSES OF RESONANT COMPONENTS AND TRANSFORMER

		Structure I	Structure II
Transformer	Irms	26	26
	Ipeak	36	36
	Vrms	172	50
	Vpeak	248	52
	Volt-second	714 uVs	250 uVs
Inductor	Inductance	12 uH	48 uH
	Irms	26	13
	Ipeak	36	18
	Vrms	197	394
	Vpeak	300	600
Capacitor	Capacitance	58 nF	58 nF

	Irms	12.7	12.7
	Ipeak	20.4	20.4
	Vrms	345	345
	Vpeak	496	497

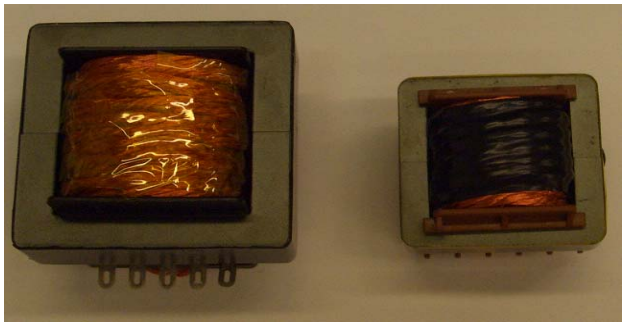
TABLE 2-V. SUMMARY OF TRANSFORMER DESIGN

	Structure I	Structure II
wire size(P)	0.033 (cm^2)	0.037 (cm^2)
Number of turns(P)	9	14
wire size(S)	0.016 (cm2)	0.018 (cm2)
Number of turns(S)	18	28
Core	EE32/16/9	EE42/21/15
Volume	25 (cm^3)	64 (cm^3)
Peak flux density	0.139 (T)	0.145 (T)
Lm	289 (uH)	953 (uH)
Pcu	3.3 (W)	6.4 (W)
Pcore	3.2 (W)	6.4 (W)
Tr	87 ^oC	90 ^oC

TABLE 2-VI. SUMMARY OF INDUCTOR DESIGN

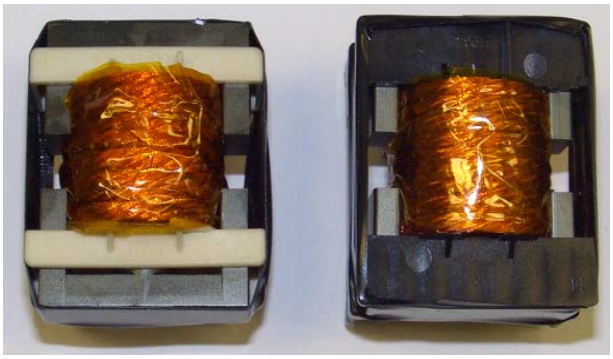
	Structure I	Structure II
wire size	0.019 (cm^2)	0.038 (cm^2)
Number of turns	36	18
Core	ETD34/17/11	ETD34/17/11
Volume	31 (cm^3)	31 (cm^3)
Gap length	1.1 (cm)	1.1 (cm)
L	46.5 (uH)	11.4 (uH)
Bmax	0.139 (T)	0.139 (T)
Pcu	3.24 (W)	3.24 (W)
Pcore	3.29 (W)	3.29 (W)
Tr	80 (^oC)	80 (^oC)

The final magnetic components, transformers and inductors for the two structural variations are given in Tables 2-V and 2-VI. Accordingly Figs. 2-10 and 2-11 show the physical components. The sizes of the inductors are almost the same, while the volume of the transformer in Structure II is about 2.5 times larger than the transformer in Structure I.



a b

Figure 2-10. Relative size of transformers for PRC.
(a)Transformer for Structure II. (b) Transformer for Structure I.



a b

Figure 2-11. Relative size of inductors for PRC. (a) Inductor for Structure II (b) Inductor for Structure I.

2.4.2. Experimental verification

The two converters operate under the conditions shown in Table 2-II. The performances of the converters are almost identical, as shown in Figs. 2-12 and 2-13. The two converters deliver the same power to the load with the same output voltage. Having almost the same input currents and turn-off currents means the two converters have the same conduction losses and switching losses on the main switches. The Vds waveforms of the main switch are also very close, which indicates the same amount of noise and voltage stresses on the main switches. The voltage and current stresses of the transformer and inductor of Structure II are shown in Figs. 2-14 and 2-15, and the voltage and current stresses of the transformer and the inductor of Structure I are shown in Figs. 2-16 and 2-17.

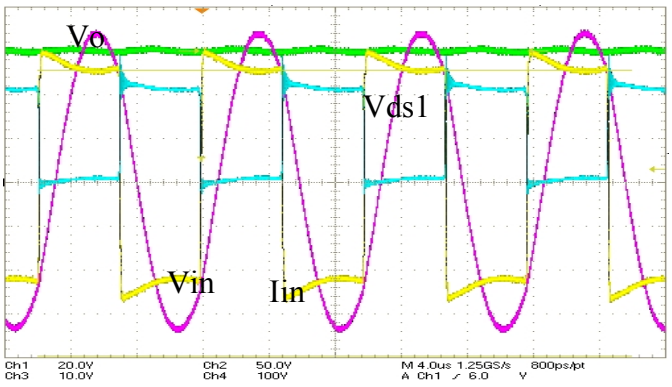


Figure 2-12. System performance of Structure II: Input voltage (Vin), Switch 1 voltage (Vds1), input current (Iin) and output voltage (Vo).

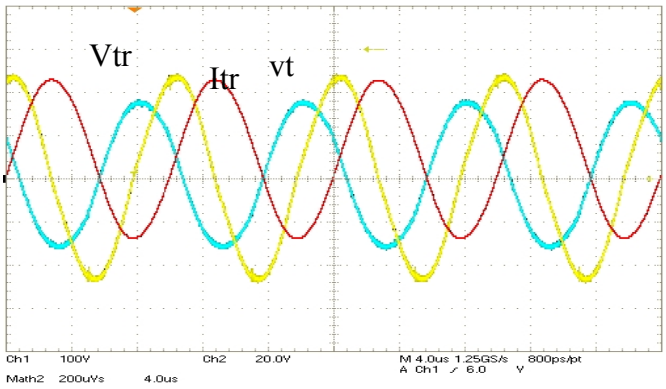


Figure 2-13. Transformer stresses of Structure II: transformer voltage (Vtr), transformer current (Itr) and the product of volt-second (vt).

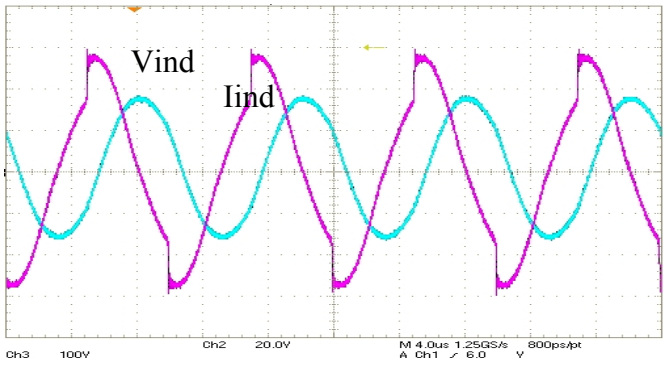


Figure 2-14. Inductor stresses of Structure II: inductor voltage (Vind) and current (Iind).

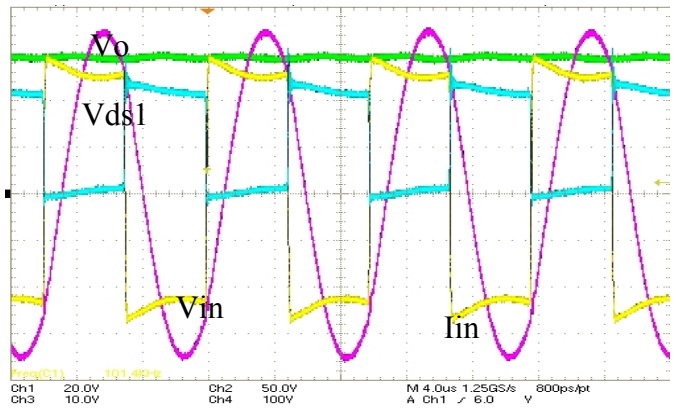


Figure 2-15. System performance of Structure I: Input voltage (Vin), Switch 1 voltage (Vds1), input current (Iin) and output voltage (Vo).

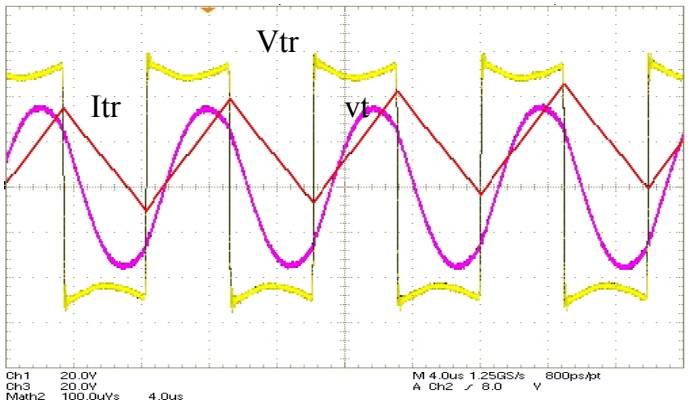


Figure 2-16. Transformer stresses of Structure I: Transformer voltage (Vtr), transformer current (Itr) and the product of volt-second (vt)

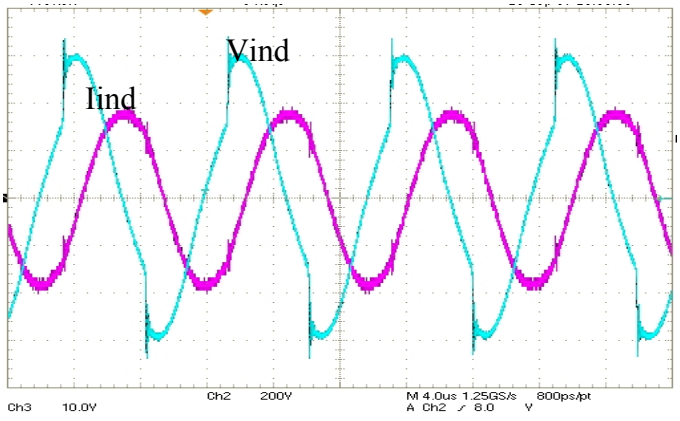


Figure 2-17. Inductor stresses of Structure I: inductor voltage (Vind) and current (Iind)

The shape of the inductor current and voltage waveforms are very similar, aside from the different magnitudes. The ratio of the magnitudes is the same as the transformer turns

ratio. The voltage stresses of the transformers in the two structures are different, even though the transformer current stress is the same for both structures. Therefore, the products of voltage and second are calculated for comparison. Due to the different shapes of the voltage waveforms, the product of the voltage and second is sinusoidal in Fig. 2-13, while it is triangular in Fig. 2-16. The peak-to-peak values of the curves are related to the volt-second values. The experimental results match the analysis and design very well. The two converters can achieve the same performance with the same resonant tank design, while Structure I of the PRC has a transformer two times smaller than the one used in Structure II of the PRC. Furthermore, the efficiency can be improved by the low power loss on the smaller transformer.

2.5.Design methodology for a high power density resonant tank

The example design and experimental results show the influence of structural variations on the transformer size and the system power density. However, the purpose of the example is only to verify the theoretical analysis. The converters are designed to operate at certain point, Q=4 and M=3. In practice, the resonant converter is supposed to run with an operation area in which the different line voltages and different load conditions are considered.

The resonant converter operation differs significantly from the PWM converter. The resonant tank design is complex. A methodology is introduced to guide the structural variations selection and to determine how to reduce the transformer volume for a high-power-density design. The design methodology is divided into two parts, which depend on whether the resonant tank parameters are determined. The key difference between the

two conditions is the transformer turns ratio. After the resonant tank parameters are selected, the turns-ratio should be constant with varied structural variations. During the resonant tank design, the turns-ratio is one of the variables.

2.5.1. Structure selection with given resonant tank parameters

When the resonant tank parameters are determined, the resonant inductance and capacitance for each structural variation is fixed in order to keep the same resonant tank design and converter performance.

Obviously, Structure III is always the best because it is directly connected with a resistive load and always has unity power factor. But it is hard to tell whether Structure I or Structure II is better for low transformer volume. Because the transformer design is based on the worst operating conditions, the key of structure selection is to determine the worst case for the transformer design. Due to the different line voltages and load conditions, the worst case varies with different conditions.

A design example is provided to explain how to find the worst conditions for transformer design. The half-bridge PRC shown in Fig. 2-9 can again be used as an example. In order to make the example as a more general one, the specifications shown in table 2-VII includes varied input line voltages and load conditions. Table 2-VIII summarizes the main resonant tank parameters calculated by the specifications and operating parameters. Figure 2-18 shows the operation area in the normalized voltage gain curves according to the typical design in Table 2-VIII.

TABLE 2-VII. DESIGN SPEFICATIONS

Vin	300-400V
Vo	48V
Po	200-2000W
Fsw_min	200kHz

TABLE 2-VIII. RESONANT TANK PARAMETERS AND OPERATION AREA

Q range	Lr (uH)	Cr (nF)	Transform Turns Ratio (n)	Freq. Range (kHz)	Max. ILrms (A)
2-20	17.9	35.4	0.16	200-248	20.4

With the aforementioned method, the resonant tank parameters shown in Table 2-VIII can be implemented by three PRC resonant tank structural variations. For a transformer design, the worst case determines the minimum requirement of the transformer volume. Compared to light load which operates at even higher switching frequencies, the worst case should be under a heavy load condition. It should be noted that the current through the resonant tank at light load is not substantially less than the current at heavy load due to the inherent low voltage regulation capability of PRC at light load. More current is circulated in the resonant tank other than to load at light load.

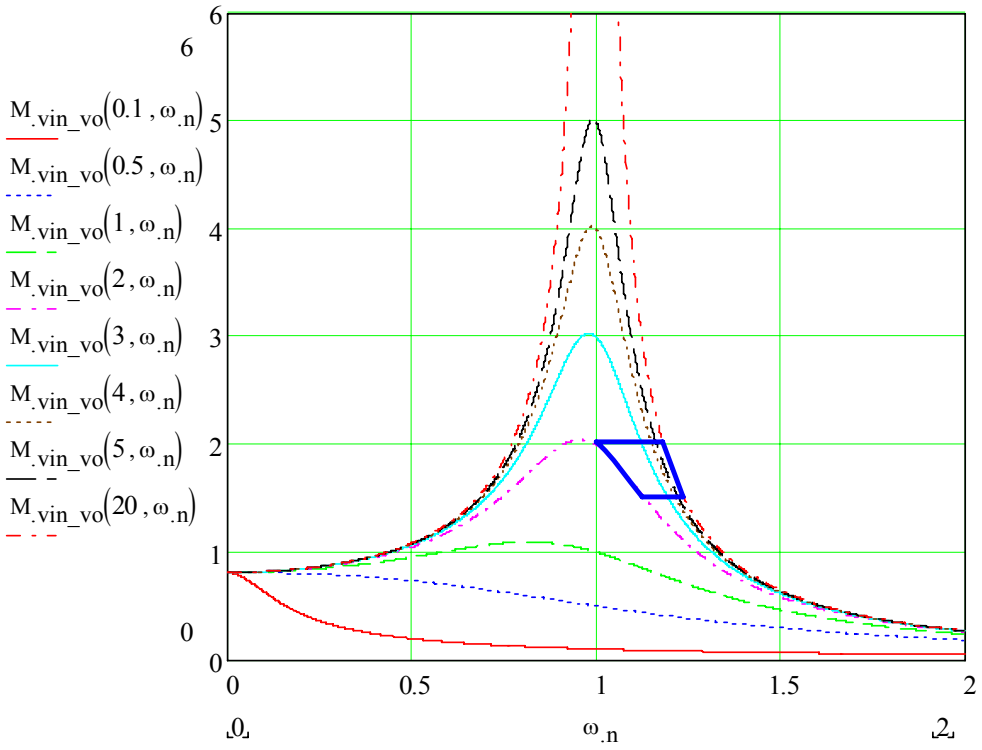


Figure 2-18. PRC operation area in gain curves.

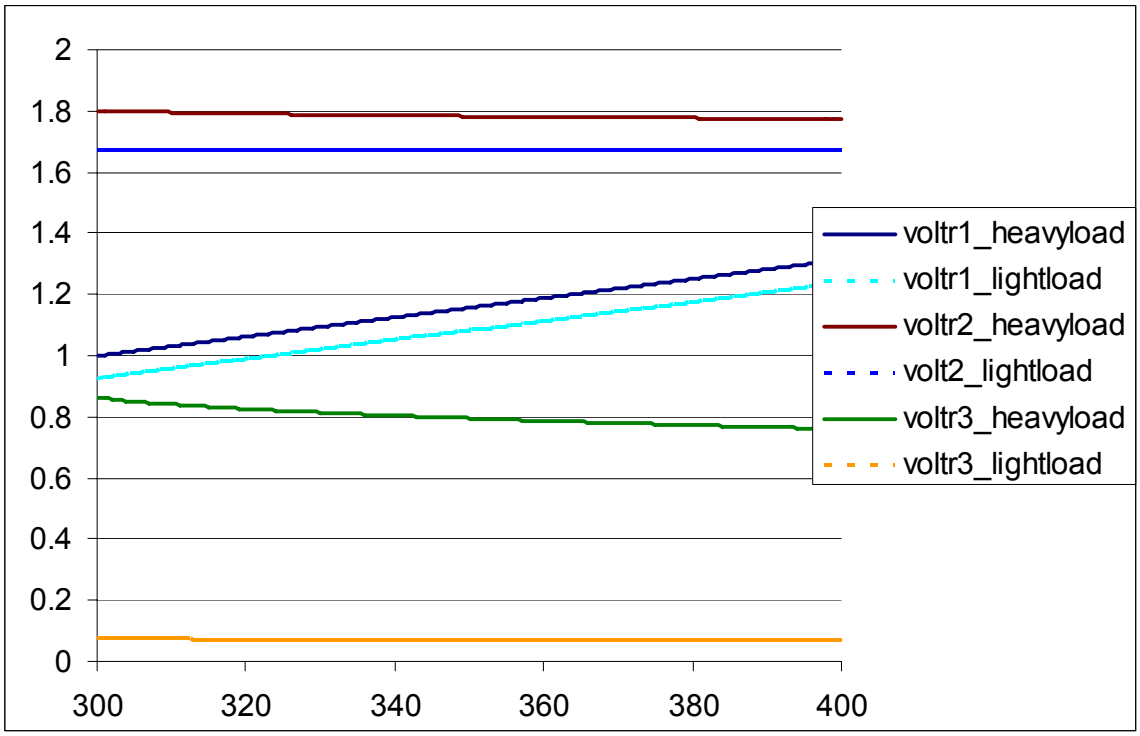


Figure 2-19. Transformer volume vs. input voltages for three structures.

With the help of the derived transformer volumetric function, the worst condition for transformer can be found with the volumetric values associated with the three structural variations shown Fig. 2-19. The X-axis is the input line voltage varied from low line to high line. Table 2-VIII summarizes parameters for transformer at each conditions, low line and heavy load, low line and light load, high line and heavy load, high line and light load. The volumetric values in the Table 2-VIII is a normalized value. The volumetric data at low line heavy load of structure I is used as a base value.

For structure I to structure III, the worst case happens at high line and heavy load, low line and heavy load, low line heavy load respectively, which matches the calculation values very well. It can be concluded that the heavy load is the worst case for transformer design, though the differences between volumetric values of Structure I at light load and heavy load are not obvious when it is compared with the 10 times difference between the

light load and heavy load, as well as the volumetric values of Structure II.

TABLE 2-IX. EACH TRANSFORMER STRESSES IN THREE PRC STRUCTURAL VARIATIONS WITH HIGH LINE AND LOW LINE CONDITIONS

	Structure I	Structure II	Structure III
Low line heavy load			
V_tr (V)	150	347	347
Kf	4	4.44	4.44
I_tr (A)	16.7	16.7	6.7
Fs (kHz)	200	200	200
Normalized Vol_tr	1	2.1	0.84
High Line heavy load			
V_tr (V)	200	344	344
Kf	4	4.44	4.44
I_tr (A)	18.32	18.32	6.6
Fs (kHz)	227	227	227
Normalized Vol_tr	1.29	2	0.72
Low line light load			
V_tr (V)	150	345	345
Kf	4	4.44	4.44
I_tr (A)	17.92	17.92	0.8
Fs (kHz)	238	238	238
Normalized Vol_tr	0.9	1.87	0.083
High line light load			
V_tr (V)	200	344	344
Kf	4	4.44	4.44
I_tr (A)	18.63	18.63	0.78
Fs (kHz)	249	249	249
Normalized Vol_tr	0.9	1.85	0.078

According to the Table 2-IX, the transformer in Structure III has the lowest volume. Since the transformer only transfers real power to the load, the power is constant from low line to high line. But due to the variable frequencies, the worst case for structure III always happens at the lowest frequency at low line and heavy load.

However, the transformer in Structure II and Structure III suffers high reactive power in addition to real power. The worst condition for these two structures will vary from low line to high line depends on different design areas. According to Table 2-IX, the transformer in structure I has the second lowest transformer volume. The VA product is in the middle of Structure II and Structure III. The transformer in Structure II has the largest voltage volume with the given design specifications.

B. Structure selection with undermined resonant tank parameters

In order to design the high-power-density resonant tank more effectively, we should consider the structural variations during the resonant tank design. There are many trade-offs in the PRC design. Due to the significant influence of structural variations on transformer volume, it is desired to consider the particular structural variation during the operation area selection instead of a concept of PRC.

TABLE 2-X. FOUR RESONANT TANK DESIGNS FOR THE SAME APPLICATION.

Case No	Q range	Lr (uH)	Cr (nF)	Transform Turn Ratio (n)	Freq. Range (kHz)
I	0.5-5	5	29	0.436	200-626
II	1-10	9.8	50	0.293	200-331
III	2-20	17.9	35.4	0.16	200-248
IV	3-30	25.8	26	0.107	200-233

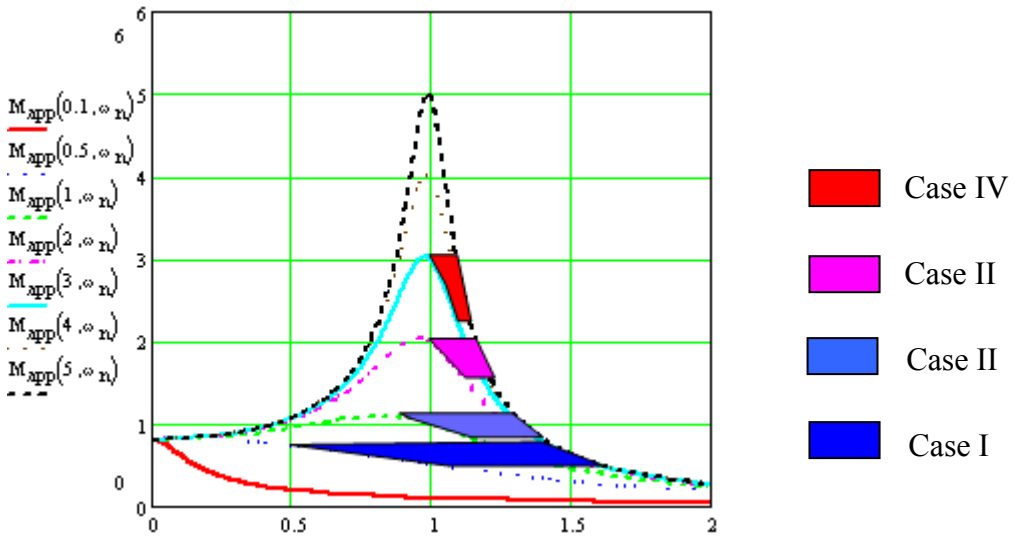


Figure 2-20. Operation areas with different designs.

With the same circuit and design requirement used in the previous section, Table 2-X lists the main resonant tank parameters and operation switching frequency for four different possible operation areas with different Q ranges. The operation areas can also be illustrated in Fig.2-20.

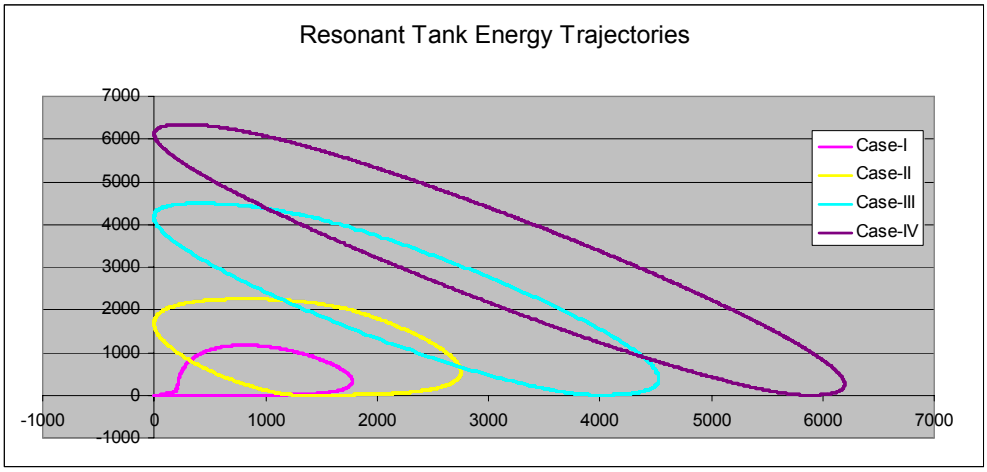
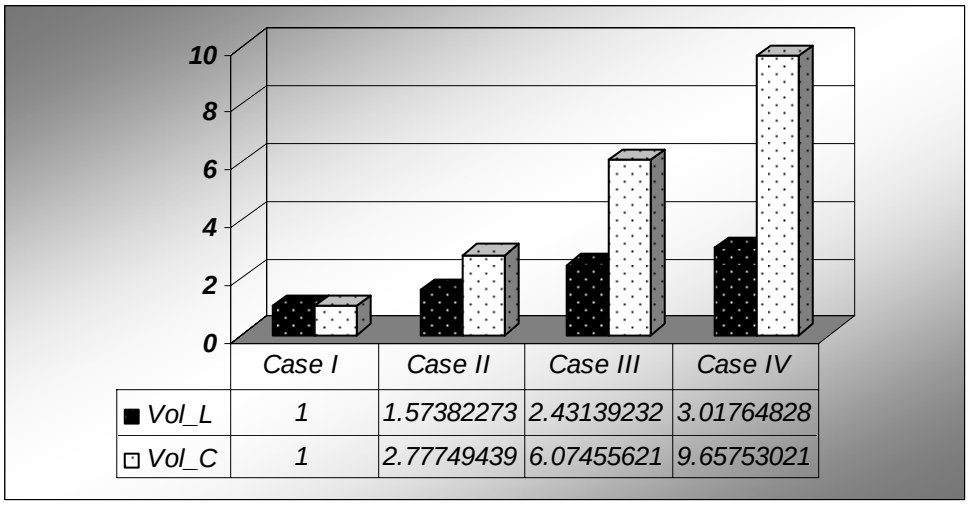


Figure 2-21. Resonant tank energy at different design cases.



	Case I	Case II	Case III	Case IV
■ Vol_L	1	1.57382273	2.43139232	3.01764828
⊡ Vol_C	1	2.77749439	6.07455621	9.65753021

Figure 2-22. Normalized resonant inductor and capacitor volumes at different design cases.

As aforementioned analysis, the resonant inductor and capacitor volume won't be influenced for the same resonant design at different structural variations. However, while the structural variations are involved into the pre-stage of resonant converter design, the volume variation of resonant inductor and capacitor has to be considered. The resonant tank energy trajectories are shown in Fig. 2-21. Since the resonant inductor and capacitor volume is proportional to their stored energy, the normalized resonant inductor and capacitor volume are shown in Fig.2-22, where the inductor volume and capacitor volume of design case I are used as base quantities for normalization.

The influence of resonant tank design on resonant inductor and capacitor volume is very

straightforward, i.e., the resonant inductor and capacitor volume independent from structural variation is monotonically increases as the targeted operation area of quality factors increases.

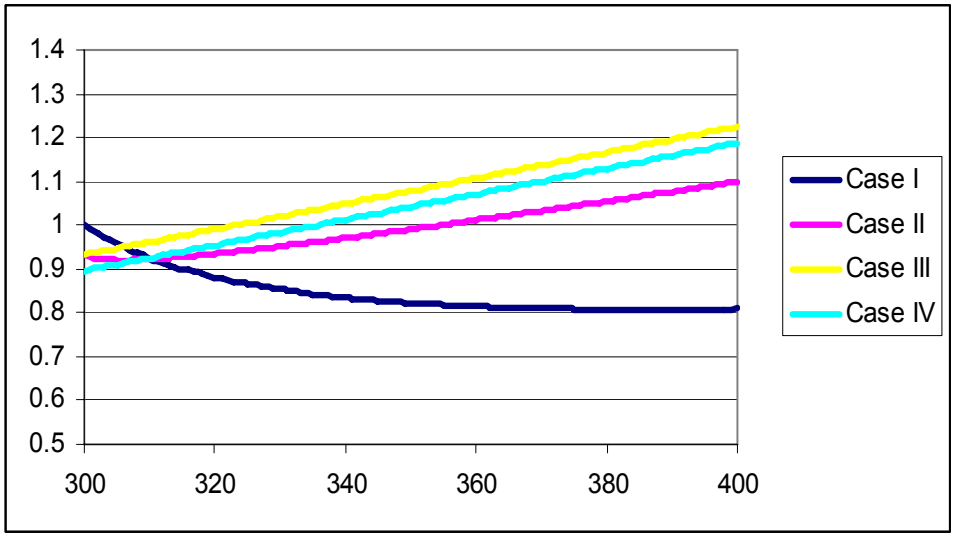


Figure 2-23. Transformer volume vs. input voltages for Structure I with four design Cases

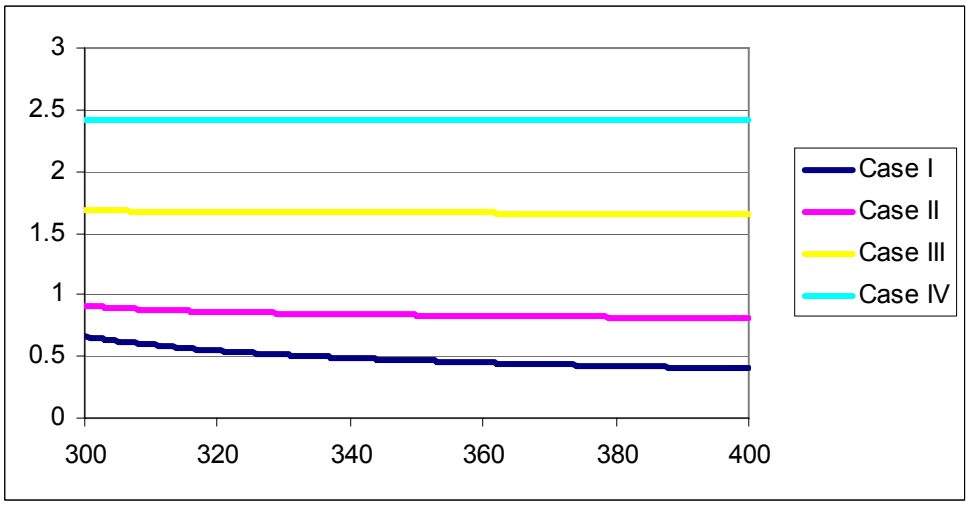


Figure 2-24. Transformer volume vs. input voltages for Structure II with four design Cases

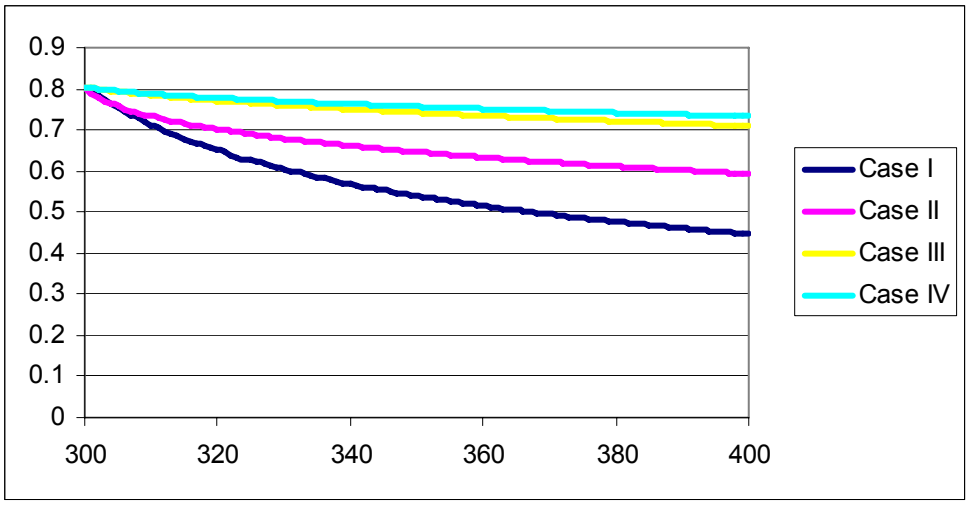


Figure 2-25. Transformer volume vs. input voltages for Structure III with four design Cases

Compared with resonant inductor and capacitor, the influence on transformer volume is more complex, which is related to the structure variations and detailed design cases. Figs 2-23 -2-25 show the normalized transformer volume at heavy load with different design cases for structure I ,structure II and structure III respectively.

The detailed transformer parameters at two terminals, low line and high line, are summarized in table 2-XII, where the base quantity for volume normalization is the volumetric volume at low line and heavy load of structure I. It can be seen from the table, the structure II and structure III always has the worst case for transformer design at low line heavy load, while the structure I has the worst case at low line heavy load and high line heavy load depended on the targeted operation area.

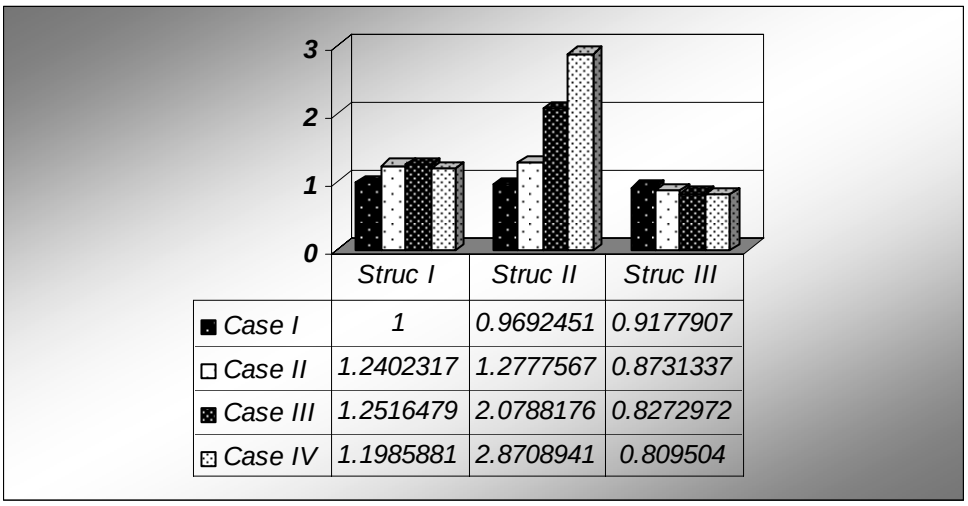
TABLE 2-XI. TRANSFORMER HEAVY LOAD VOLTAGES AND CURRENTS AT LOW LINE AND HIGH LINE WITH DIFFERENT DESIGN CASES.

	Structure I	Structure II	Structure III
Case I			
Low line heavy load			
V_tr (V)	145	156	156
Kf	4	4.44	4.44
I_tr (A)	17.33	17.33	16.41
Fs (kHz)	200	200	200

Normalized Vol_tr	1	0.969	0.918
High Line heavy load			
V_tr (V)	194	148	148
Kf	4	4.44	4.44
I_tr (A)	22.23	22.23	17.94
Fs (kHz)	385	385	385
Vol_tr (V.A/kHz)	0.892	0.612	0.494
Case II			
Low line heavy load			
V_tr (V)	145	198	198
Kf	4	4.44	4.44
I_tr (A)	18	18	12.3
Fs (kHz)	200	200	200
Normalized Vol_tr	1.04	1.278	0.873
High Line heavy load			
V_tr (V)	194	192	192
Kf	4	4.44	4.44
I_tr (A)	19.92	19.92	12.54
Fs (kHz)	248	248	248
Vol_tr (V.A/kHz)	1.24	1.11	0.696
Case III			
Low line heavy load			
V_tr (V)	145	347	347
Kf	4	4.44	4.44
I_tr (A)	16.71	16.71	6.65
Fs (kHz)	200	200	200
Normalized Vol_tr	0.964	2.079	0.827
High Line heavy load			
V_tr (V)	194	348	348
Kf			
I_tr (A)	18.32	18.32	6.63
Fs (kHz)	226	226	226
Vol_tr (V.A/kHz)	1.252	2.023	0.732
Case IV			
Low line heavy load			
V_tr (V)	145	512	512
Kf			
I_tr (A)	15.64	15.64	4.41
Fs (kHz)	200	200	200
Normalized Vol_tr	0.902	2.87	0.81
High Line heavy load			
V_tr (V)	194	511	511
Kf			
I_tr (A)	17	17	4.4
Fs (kHz)	219	219	219
Vol_tr (V.A/kHz)	1.1986	2.844	0.736

If the volumetric value of structure I at worst case with Case design I is used as base quantity, the normalized transformer volumetric values for different structures and design areas at worst condition are summarized in Fig. 2-26.

First, as expected, Structure III is always the best structure for high power density. The transformer volumetric values of structure III keep the lowest value compared with other structures at different design areas. It should be noted that the gain from low Q design doesn't help for transformer volume reduction in structure III. The value even goes down as the design area covers high quality factor Q because the current is discontinuous at low quality factor Q and then has high harmonics.



	Struc I	Struc II	Struc III
Case I	1	0.9692451	0.9177907
Case II	1.2402317	1.2777567	0.8731337
Case III	1.2516479	2.0788176	0.8272972
Case IV	1.1985881	2.8708941	0.809504

Figure 2-26. Normalized transformer volume comparison at different design areas and structures.

On other contrary, the transformer volumetric values of structure II keep increasing as the design area goes high quality factor Q because of more reactive power when the resonant converter operates a high quality factor. The transformer volume of structure II will be substantially influenced by the quality factor Q. Therefore more attention needs to be paid to the resonant tank design for Structure II. When the resonant converter is designed at very low quality factor, such as case I, the transformer volumetric value of structure II is even lower than the one of structure I because of the PRC doesn't boost the input voltage. In fact, this area is not desired for resonant converter operation. The PRC lost the advantages of resonant converter and works more like a PWM converter at low

quality factor.

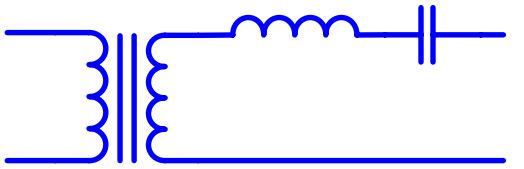
The lowest transformer volumetric value of structure I happens at design case I. When the design area is located to high quality factor, the worst case of transformer volumetric value of structure I happens at high line heavy load instead low line heavy load because of the increased current. In order to regulate the output voltage, the resonant converter has to operate at high switching frequency far away the resonant frequency. The increased current and voltage outweighs the increased switching frequency. But transformer volumetric values almost keep the same with varied design areas.

In summary, considering the structural variation in the resonant tank design is important for a transformer design. The resonant tank that can be designed with a low Q value has less effect on the transformer volume for different structural variations and normally results in low transformer volume. If high Q is desired, Structure II should be avoided; otherwise a compromise between the transformer volume and other considerations is needed.

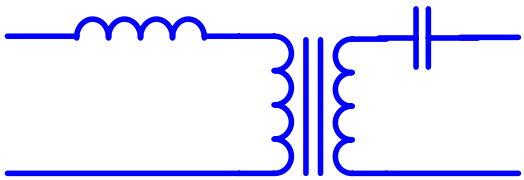
2.6. Concept extension

The influence of structure variation on the transformer driven from a PRC can be extended to other resonant converters. Figures 2-27 and 2-28 show the structural variations of the other two basic resonant converters, the series resonant converter (SRC) and the series parallel resonant converter (SPRC), or LCC. It should be noted that the position of the resonant inductor and the position of the series capacitor in the SRC and SPRC can be exchanged if they are located on the same transformer side. Hence, a total of three structural variations of the SRC and four structural variations of the SPRC are

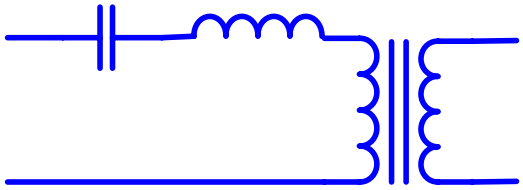
provided. These structural variations can also be found in a wide variety of applications [C-17]-[C-25].



(a) Structure I

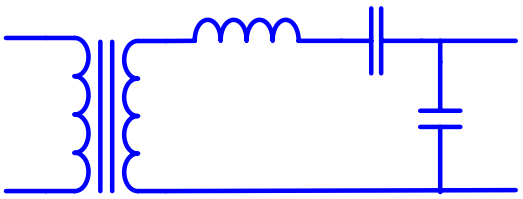


(b) Structure II

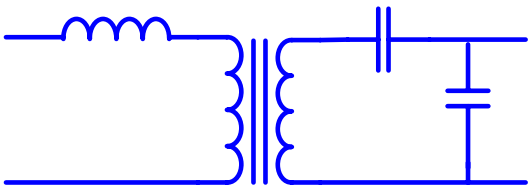


(c) Structure III

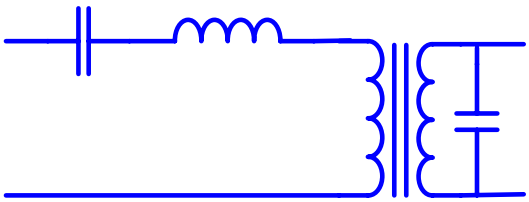
Figure 2-27. SRC structural variations



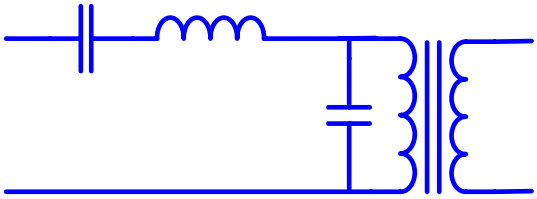
(a) Structure I



(b) Structure II



(c) Structure III



(d) Structure IV

Figure 2-28. SPRC structural variations.

It is interesting that all of the transformer currents in all three SRC structural variations are same. This means the voltage stress is the only variable for the transformer design when the structural variations are considered. Figure 2-29 shows the transformer voltage stress ratio of Structure II to Structure I, and Fig. 2-30 shows the transformer voltage stress ratio of Structure III to Structure I. The transformer in Structure II suffers extremely high voltage stress when the switching frequency is near the resonant frequency, which is always aimed for in SRC operation by the designer, while the voltage stress of Structure III is generally lower than that of Structure I. The voltage stress of Structure III approaches the value of the transformer in Structure I only when the switching frequency is close to the resonant frequency. At low quality factor or under light load conditions, the transformers in the three structural variations have similar voltage stress. However, the SRC will behave like a PWM converter at low quality factor, similar to a PRC.

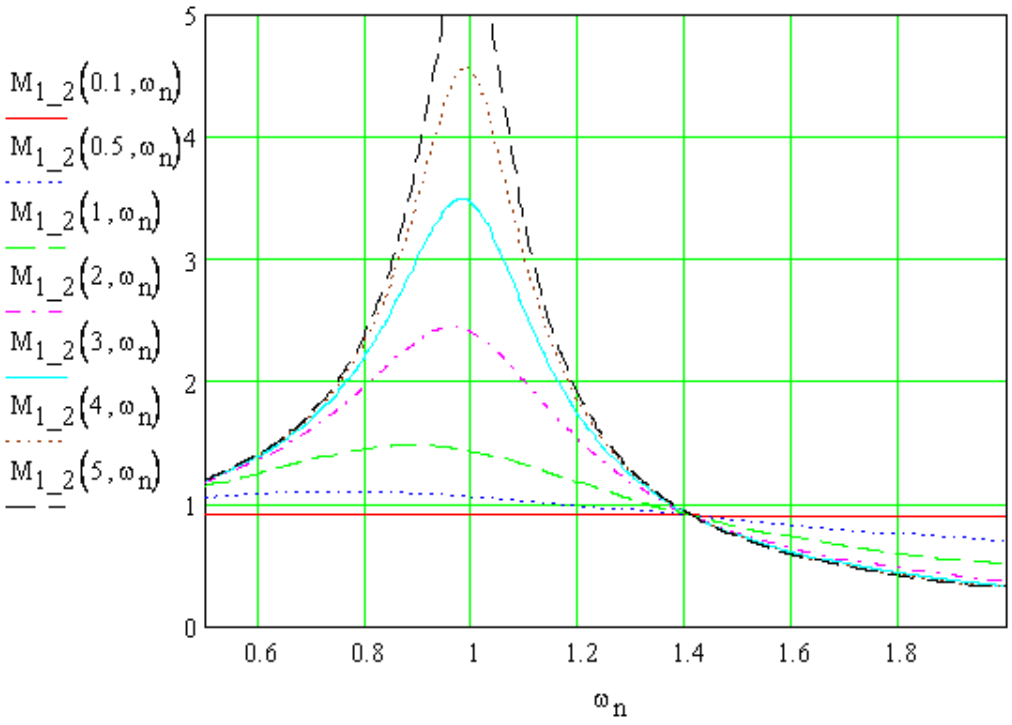


Figure 2-29. SRC voltage gain of Structure II voltage stress over Structure I voltage stress.

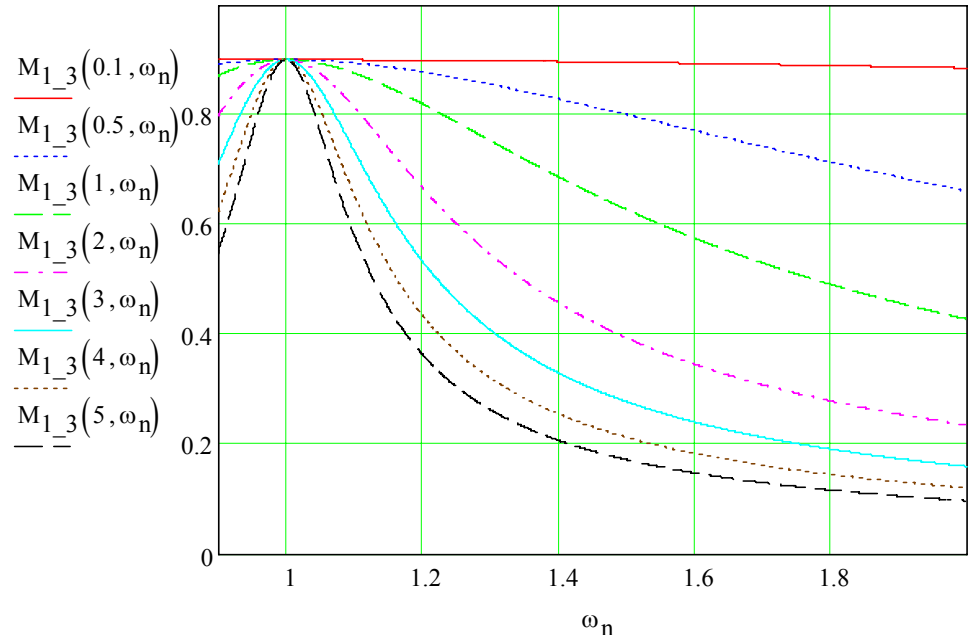


Figure 2-30. SRC voltage gain of Structure III voltage stress over Structure I voltage stress.

The voltage and current stresses of the SPRC are not illustrated by graphs. The performance of the SPRC can be treated as the combination of the SRC and PRC.

Depending on the ratio of series capacitance to parallel capacitance, the SPRC will tend to work like either the SRC or PRC, and then the conclusions from the SRC or PRC will apply to the SPRC.

2.7. Other considerations with structure variations

In practice, the structural variations have to be considered from a system point of view. Thus the main impacts, other than the transformer volume, are presented before the high-power-density design is discussed. Otherwise, the intended resonant tank behavior may be distorted or a penalty of system power density will be paid.

A. Transformer parasitics' influence

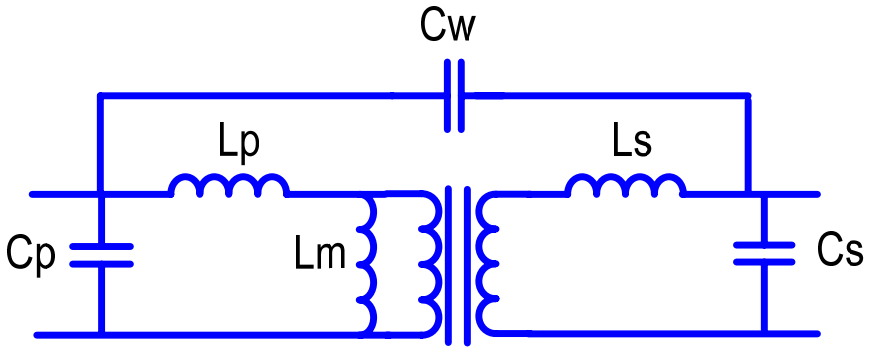


Figure 2-31. High-frequency transformer model.

The transformer parasitics cannot be neglected in a real transformer. Operation of transformers at high switching frequencies increases the importance of the parasitics, leakage inductance and stray capacitance. Figure 2-31 shows an equivalent circuit of practical high frequency transformer. The winding-to-winding capacitance is important in eliminating common-mode signals. The stray capacitance is typically induced at a high resonant frequency in the transformer impedance plot, normally several MHz beyond the operating frequency, unless the intent is to design a large capacitor with a large dielectric

constant material for integration. Magnetizing inductance is normally two or three orders higher than the leakage inductance unless it is reduced on purpose. The typical simplified transformer mode can be expressed by Fig. 2-32. Only the leakage inductance is of concern.

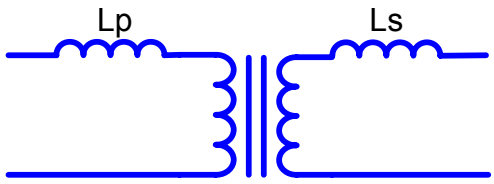


Figure 2-32. Simplified transformer model.

Nowadays more and more applications integrate the resonant component into transformer with leakage inductance control or package technologies [F-5]-[F-10]. Structure I and Structure II of PRC are attractive this applications because the resonant inductor is always in series with the leakage inductance in these structures, or it absorbs the leakage inductance of the transformer. However, for the PRC Structure III, the resonant inductor is connected with the resonant capacitor and leakage inductor. The resonant tank will behave like an LCL instead of a PRC if the leakage inductance is comparable with the resonant inductance. Therefore, if the transformer parasitics are comparable with the resonant components' value, the behaviors of different structural variations may be distorted by the transformer parasitics. By contrast, absorbing or utilizing the transformer leakage inductance as resonant inductor is one of the advantages of the resonant converter. Though the resonant inductor integrated into transformer can not move freely as an external inductor, a proper resonant structural variation still can be achieved by controlling the leakage inductance distribution, on transformer primary side or secondary side.

[F-11] has introduced a leakage inductance distribution control method with the use of

coaxial windings. However, this method makes the transformer fabrication special. The method presented by [F-3] is commonly used for leakage inductance control. If the transformer winding layout is illustrated as Figure 2-33, Equation (2-16) is usually used for total leakage inductance calculation.

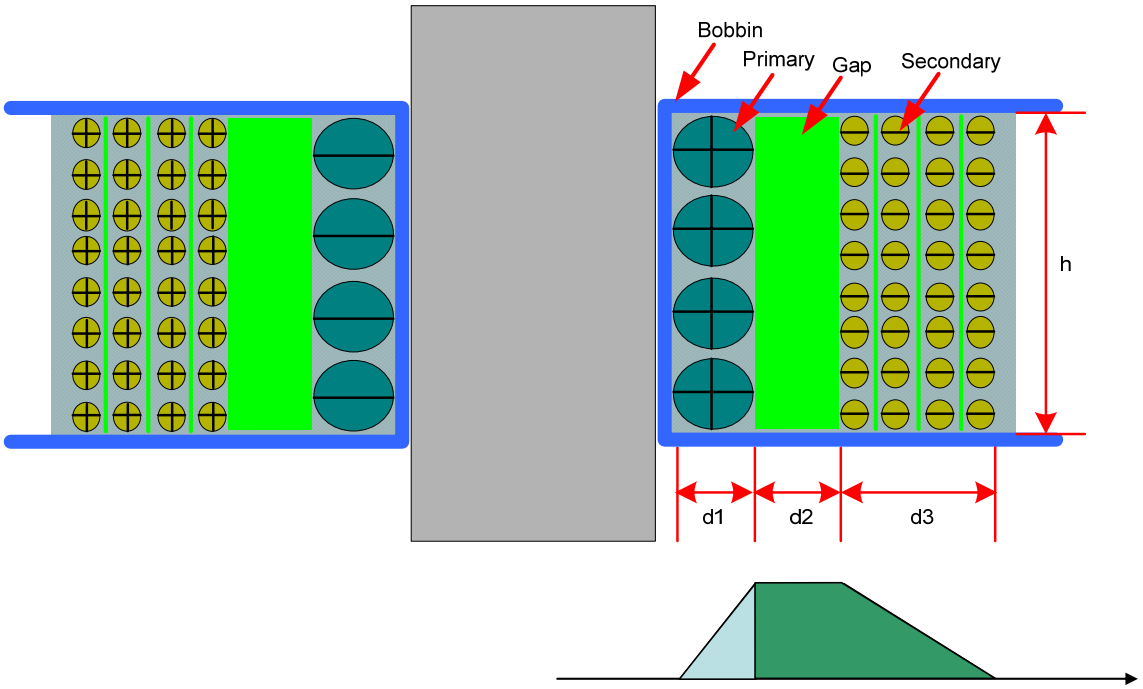


Figure 2-33. Leakage inductance calculation.

$$L\_lk\_tot = \frac{\mu_o \cdot N_p^2 \cdot l_w}{h_w} \cdot \left(\frac{d_1 + d_3}{3} + d_2 \right) \tag{2-25}$$

Where μ_o is the absolute permeability, N_p is the primary winding turns if the leakage inductance refers to transformer primary side, l_w is the mean perimeter of windings. h_w is the winding height, d_1 and d_3 are the primary winding width and secondary winding width respective, d_2 is the distance between primary winding and secondary winding.

The leakage flux consists of the internal flux of the outer winding and the flux within the inter-winding space which is only linked by the outer winding. Hence, the leakage

inductance for outer winding can be easily be derived as

$$L\_lk\_out = \frac{\mu_o \cdot N_p \cdot l_w}{h_w} \cdot \left(\frac{d_3}{3} + d_2 \right) \tag{2-26}$$

The internal flux of inner winding can be treated as primary side leakage inductance.

$$L\_lk\_out = \frac{\mu_o \cdot N_p \cdot l_w}{h_w} \cdot \left(\frac{d_2}{3} \right) \tag{2-27}$$

It should be noted that the assumption for above three equations is that coupling coefficient won't be influenced by the varied inter-winding space. Hence, the calculation value is usually less than the real value due to the decreased coupling coefficient.

B. DC blocking function

In a half-bridge or full-bridge circuit, the unbalanced charge in each half cycle will cause an asymmetrical volt-second on the transformer's primary side. A DC blocking capacitor in series with the transformer's primary winding is required to prevent core saturation. It should be noted that the unbalanced charge can be adjusted by the shifting of the neutral point voltage in a half-bridge converter or in other words, the two input capacitors can serve as a DC blocking capacitor. In this case a blocking capacitor may not be needed. Since a PRC does not have capacitors in series with the transformer winding, the structural variations are independent of this issue. However, if a SRC or other resonant tank has a resonant capacitor in series with transformer winding, the series resonant capacitor will also work as a DC blocking capacitor if it is located on the transformer's primary side. When the series resonant capacitor is moved to the secondary side in different structural variations, an additional DC blocking capacitor will be required, which is detrimental to the power density.

2.8. Summary

In this chapter, the influence of structure variations is analyzed. Without any impact on the system performance, the structure variations with different transformer positions result in significant changes on the transformer's voltage and current, which in turn influence the transformer volume and system power density.

Based on the derived volumetric functions for the inductor, capacitor and transformer, the impacts on the PRC resonant tank are thoroughly analyzed and summarized. The reason for the huge impact on transformer volume by the different structural variations for the same application can be explained by the power factor concept. The different structural variations result in substantially different apparent powers even for the same application, delivering the same real power to the load. This concept is verified by an example design with two PRC structural variations. These two converters deliver almost identical performance, but the one with Structure I of the PRC has around twice as small a transformer than the one with Structure II.

In order to fully utilize the benefits of power density with different structural variations, the methodology is introduced according to different design stages. Though the concept is initiated by a PRC converter, it can be extended to other isolated resonant converters. The other two basic resonant converters, SRC and SPRC, are used as examples for the introduction of concept extension. The concept is designed with power density in mind; other considerations associated with the structural variations have to be included for each particular application. Two main additional considerations, the transformer parasitics absorption and the DC blocking function of the series capacitors, are explained as well.

Chapter 3 Control Scheme and Design

The proposed control scheme not only achieves the design objectives, but also can reduce the component stresses and needed values so that low voltage rating devices with less volume can be used and high system efficiency can be obtained. The control scheme of the three-level parallel resonant converter can be divided into two parts: three-level structure control and parallel resonant converter charging control.

3.1.Three-level control scheme

Three-level configuration can reduce the main switches' voltage stress to half of the input voltage, so that a lower voltage rating device with better performance can be used. In a three-level converter like that shown in Fig. 2-2, the top pair of switches, S_1 and S_2, and the bottom pair of switches, S_3 and S_4, switch on and off alternately to generate a high-frequency AC quasi-square voltage input to the resonant tank. With phase-shift control, which was first proposed by Francisco [B-8], the outer switches should be turned off before the inner switches are tuned off, and the switches in the two legs are turned off and on alternatively.

However, variable frequency control is popular in resonant converters. In variable frequency control, the power is regulated by the varied switching frequency instead of by the varied duty cycle. Then, the outer switch S_1 and inner switch S_2 (or S_3 and S_4) can be switched simultaneously, thus there is no phase shift in variable switching frequency control. Both phase-shift (PS) and non-phase-shift (NPS) operation modes have been used for three-level resonant converters [B-3]-[B-5]. In both cases, the voltage control is

realized through frequency control while maintaining nearly 50% duty cycles. The typical waveforms for PS and NPS operation modes are illustrated in Figure 3-1 and Figure 3-2, respectively.

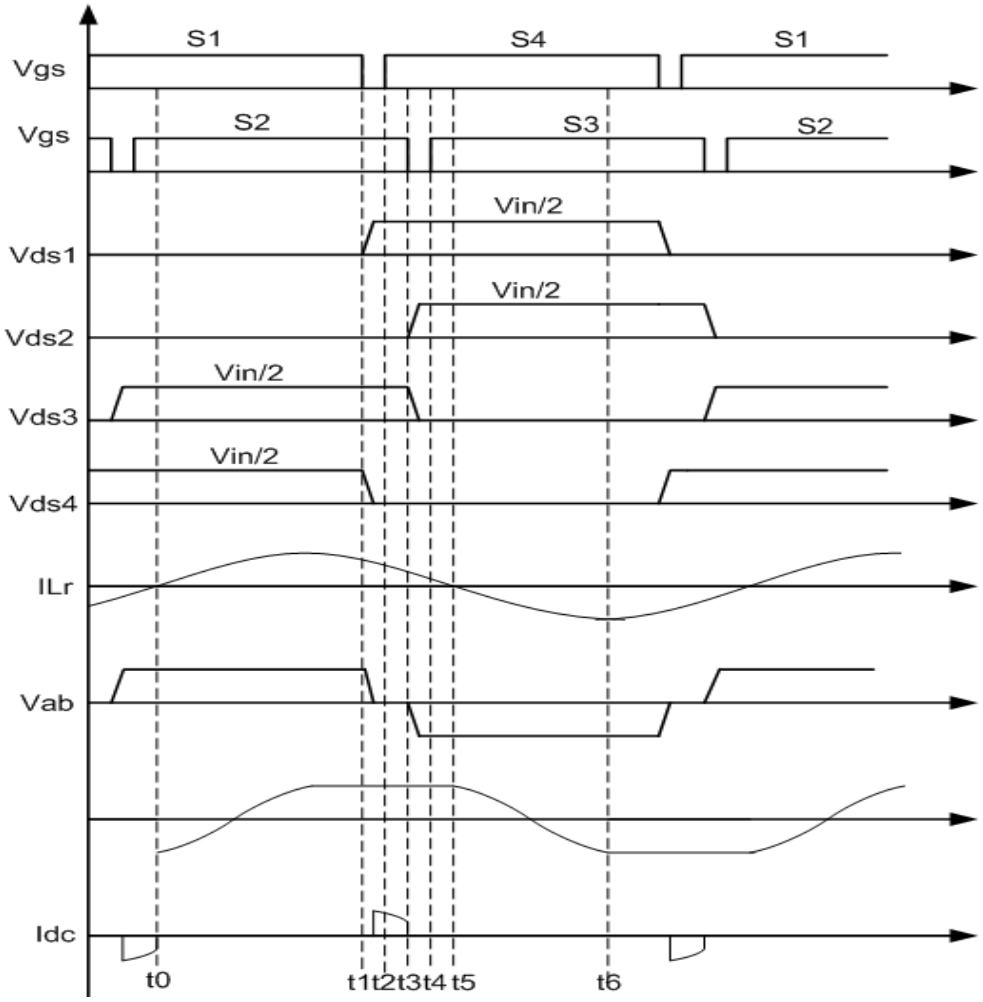


Figure 3-1. Principal waveforms of three-level PRC with PS ZVS operation

For the converter using PS mode in Figure 3-1, the deadtime and phase shift need to be set. In order to achieve ZVS operation, the phase shift has to be larger than the deadtime. The details of the operation analysis can be found in [B-3]. In essence, NPS mode can be considered to be a special case of PS operation mode.

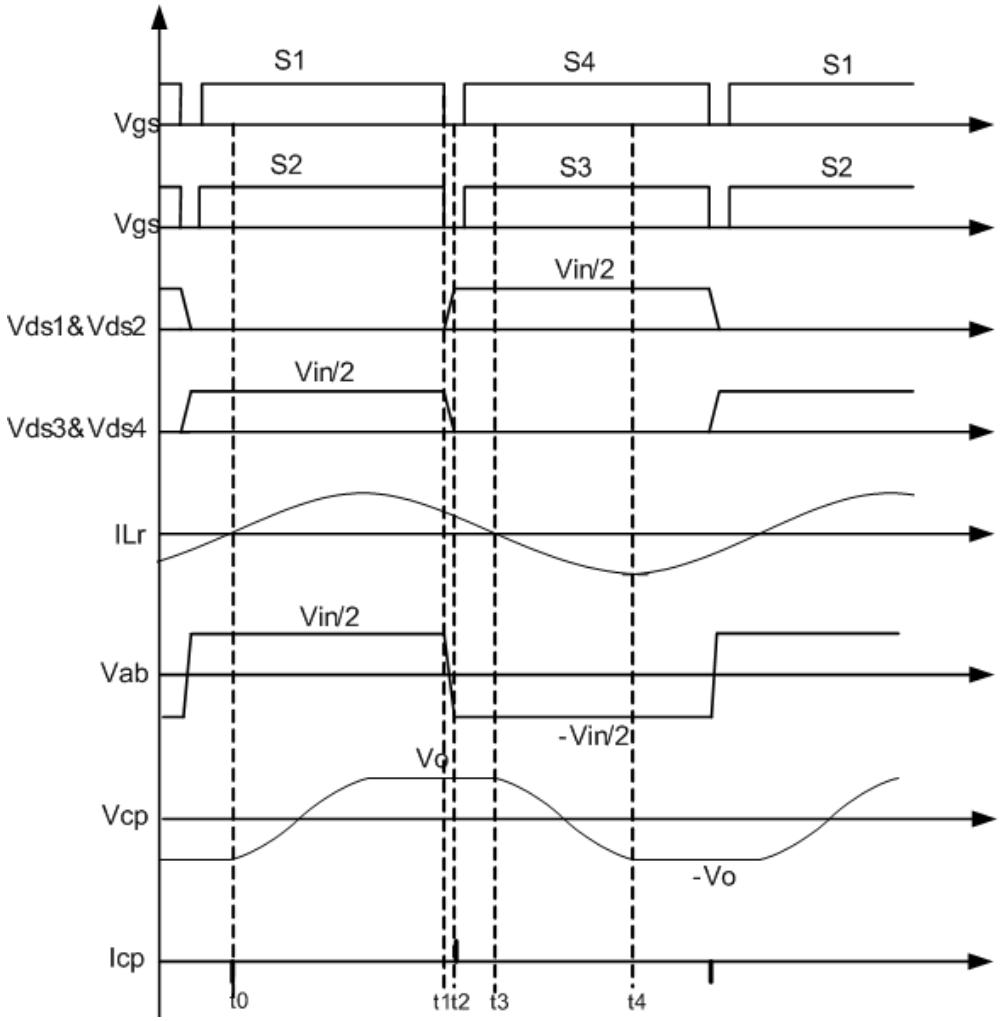


Figure 3-2. Principal waveforms of three-level PRC NPS ZVS operation

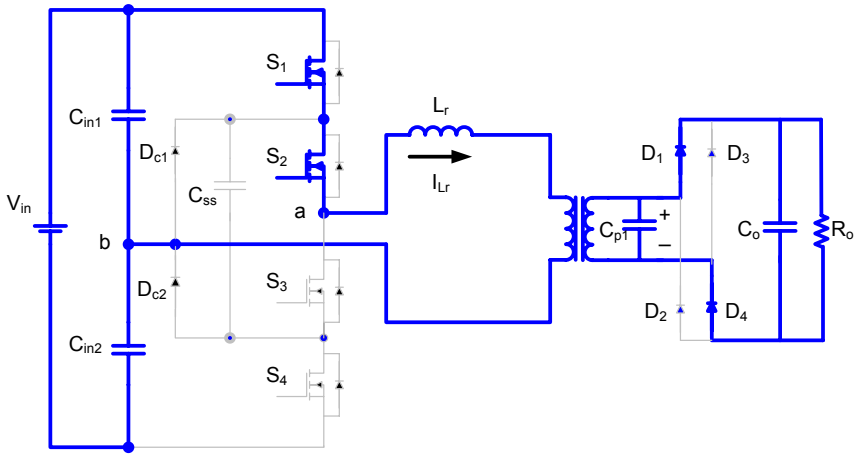
However, the flying capacitor (C_{ss}) is connected in parallel to the input capacitors during the freewheeling stage of the converter which is illustrated in detailed in Chapter 4. Therefore, the input capacitors have the opportunity to balance their charge through C_{ss} in every half of a switching cycle [B-8]. When the C_{ss} is connected with the input capacitor, it is like two voltage sources in parallel. These two component voltages can be charged/discharged to the same voltage instantaneously. In practice, the time for voltage balance is associated with the parasitic inductance. In order to keep the self-balance

capability in NPS operation, the snubber capacitors across the drain and source of inner switches, S2 & S3, have larger capacitance to generate a delay time to the outer switches, S1 & S4. The delay time should be large than the voltage balance time. Therefore, the analysis is focused on effect of phase-shift on the converter performance, including power loss, clamping circuit voltage and current stress and parasitic influence.

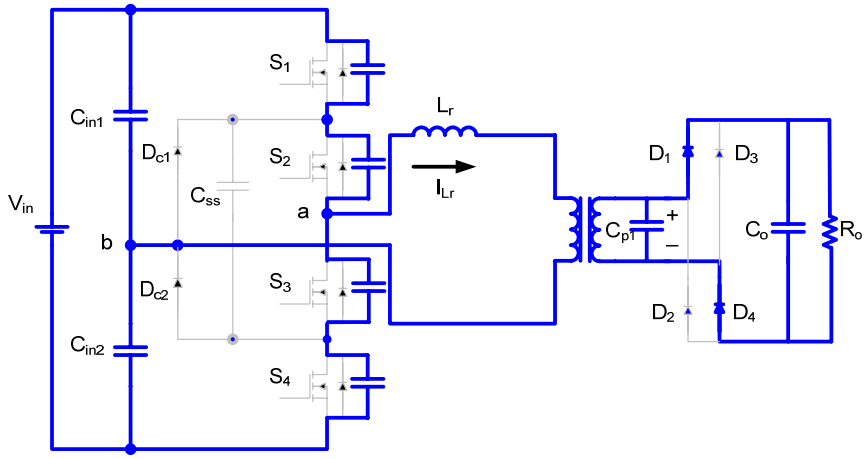
3.2.Operation mode of NPS and comparison between PS and NPS

3.2.1. Operation mode of NPS

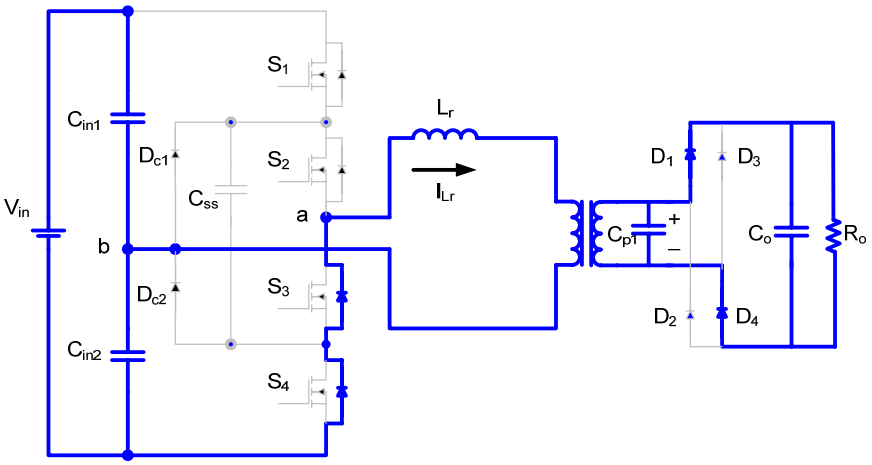
Figure 3-2 shows the principal waveforms of three-level PRC NPS operation. There are six stages of operation during each half of a switching cycle. In order to simplify the analysis of the converter, it is assumed that the circuit operates in steady state; the output filter capacitor is large enough to be considered as a voltage source; all the devices are ideal, and the transformer magnetizing current is ignored.



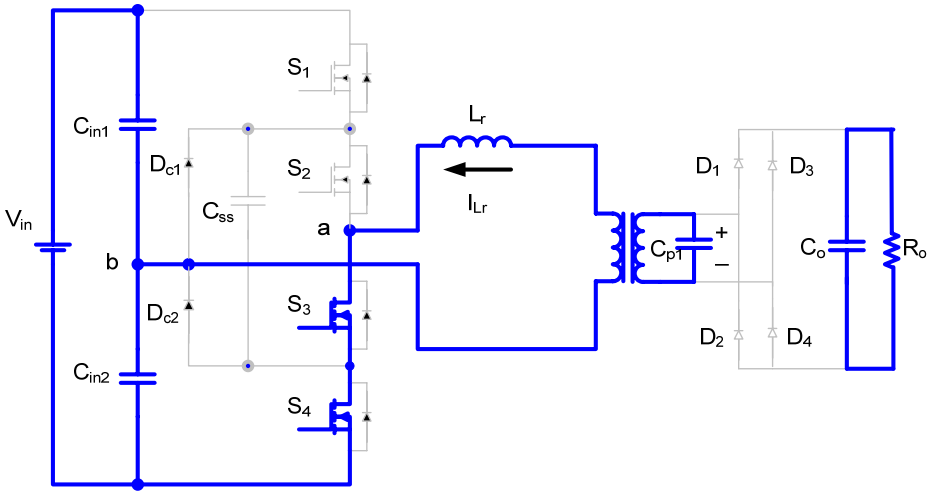
a. (t0-t1)



b. (t1-t2)



c. (t2-t3)



d. (t3-t4)

Figure 3-3. Equivalent circuit for each stage

As mentioned above, all switches in the circuit operate with nearly 50% duty cycles.

The power is regulated by a varied switching frequency. There is no phase shift between S_1 and S_2 or between S_3 and S_4. The equivalent circuit for each stage of operation is shown in Fig. 3-3. These stages are described below.

[t_0-t_1]: During this stage, switches S_1 and S_2 conduct, and the input power is delivered to the output.

[t_1-t_2]: At t_1, switches S_1 and S_2 are turned off, and the current through the resonant inductor continues in the same direction and charges and discharges the parasitic capacitance of S_1, S_2, S_3 and S_4. This stage ends when the voltages across the parasitic capacitor of S_1 and the parasitic capacitor of S_2 reach $V_{in}/2$. At the same time, the voltage across the parasitic capacitance of S_4 reaches zero, and the anti-parallel diode D_4 begins to conduct.

[t_2-t_3]: After t_2 and D_4 start conducting, switches S_3 and S_4 can be turned on with ZVS. When they are turned on, the primary current freewheels through switches S_3 and S_4 instead of the body diodes. The converter continues transferring power to the load. This stage ends when the inductor current changes its direction, and the rectifier bridge starts to block the voltage as the resonant capacitor voltage starts to drop.

[t_3-t_4]: At t_3, the inductor current starts to increase in the reverse direction. The resonant capacitor voltage starts to reduce and change its polarity. This interval ends when switch S_2 is turned off, and leakage inductance L_{lk} resonates with parasitic capacitances C_2 and C_3. The voltage across C_2 rises to half the level of input voltage V_{in}, and the resonant capacitor voltage is equal to the output voltage and starts to deliver power to the load again, and a new half of a switching cycle begins.

3.2.2. Comparison between PS and NPS

This section compares the PS and NPS operation modes in detail in this section. The analysis is based on the PS and NPS without any delay between the switches in the same leg. Because the operation modes influence the performance of the converter and thus the device selection, the analysis focuses on the power loss, component stress and parasitic impacts. During the comparison, the main concern is the power loss, which is related to not only the system efficiency, but also the volume of the heatsink. Because of the system's ZVS operation and the negligible difference of conduction loss between the two ZVS operation modes, the analysis of the power losses will be focused on the turn-off current and switching frequency.

The second aspect of comparison is component stress. The analysis is focused on the current stress on the clamping diodes and flying capacitors, which also lead to serious thermal stress.

In addition, the impacts of the parasitic inductance on the over-voltage of the drain-to-source V_{ds} are studied. The ring of V_{ds} is one of the main reasons of MOSFET failure. A clean V_{ds} waveform also contributes to reducing the EMI noise.

a. Power Losses

Conduction Loss:

The mathematical derivations below are based on the sinusoidal analysis with the first fundamental frequency. Though each operation mode is expected to have nearly 50% constant duty cycles, it needs enough deadtime for ZVS operation, which results in a high duty cycle loss. Furthermore, PS operation mode will obviously cause additional duty cycle loss due to phase shifting. The duty cycle is used to indicate the influences on power loss for the following analysis. With Fourier analysis, the peak fundamental

frequency voltage value V_{ab} can be expressed as:

$$V_{ab1} = \frac{4}{\pi}\frac{V_{in}}{2}\sin(\frac{D\pi}{2}) \quad 0 \le D \le 1 \tag{3-1}$$

where D is the duty cycle and V_{in} is the input voltage.

Even if the operating duty cycle of the converter is as small as 90%, the fundamental harmonics of voltage V_{ab} is only reduced by 1.2%. Thus the tiny phase shift has almost no influence on the fundamental harmonic voltage. Therefore, it is reasonable to assume the conduction loss is practically the same for the two operation modes.

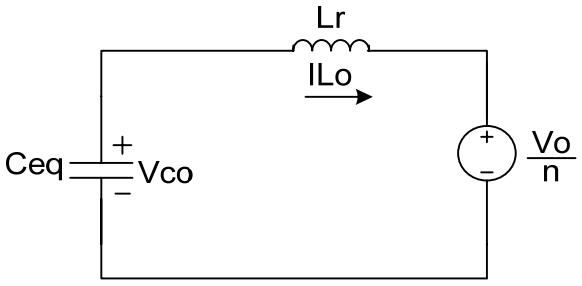


Figure 3-4. Equivalent circuit for ZVS operation

Switching Loss:

Because of the ZVS operation, the turn-on loss is negligible, and only the turn-off loss is included in the switching loss. The turn-off current and switching frequency determine the turn-off loss if the turn-off voltage is assumed to be constant. Based on the properties of the PRC, the converter will continue transferring the energy to the load during the switching of each leg's turning on and off alternately. The ZVS equivalent circuit is shown in Fig. 3-4.

The energy in the resonant inductor L_r is:

$$E = \frac{1}{2}L_r I_{Lr}^2 > \frac{1}{2}C_{sw}\left(\frac{V_{in}}{2}\right)^2 + \frac{V_o}{n}I_{Lr}t \tag{3-2}$$

where C_{sw} can be approximated as the output capacitance of the switch, and t is the time duration for the resonant inductor current from turn-off to zero. Usually, the energy transferred to the load will be much larger than the energy stored in the capacitors.

Here, the resonant inductor current can be approximated by

$$I_{Lr} = I_{Lm} \sin\theta \tag{3-3}$$

where I_{Lm} is the peak value, $\theta = 2\pi \cdot f_s \cdot t$ with zero value at θ_0 when resonant inductor current starts to increase, and f_s is the switching frequency.

Since the energy transferred to the load is the integration of power with time, the equation (3-2) can be rewritten with inserting equation (3-3)

$$\frac{1}{2} \cdot L_r \cdot I_{Lr}^2 \geq \frac{1}{2} \cdot C_{sw} \cdot \left(\frac{V_{in}}{2}\right)^2 + \int_0^{\frac{\alpha}{\omega}} \frac{V_o}{n} \cdot I_{Lr} \cdot Sin(\omega \cdot t) dt \tag{3-4}$$

where $\omega = 2\pi f$, α is the current angle when switching turns off.

Simplifying the equation (3-4), the minimum resonant inductor current which is expressed by angle α can be obtained:

$$\frac{1}{2} L_r \left(I_{lr} \sin\alpha\right)^2 \geq \frac{1}{2} C_{sw} \left(\frac{V.in}{2}\right)^2 + \frac{V_o}{n} I_{lr} \frac{1-\cos\alpha}{\omega} \tag{3-5}$$

where $\omega = 2\pi \cdot f$.

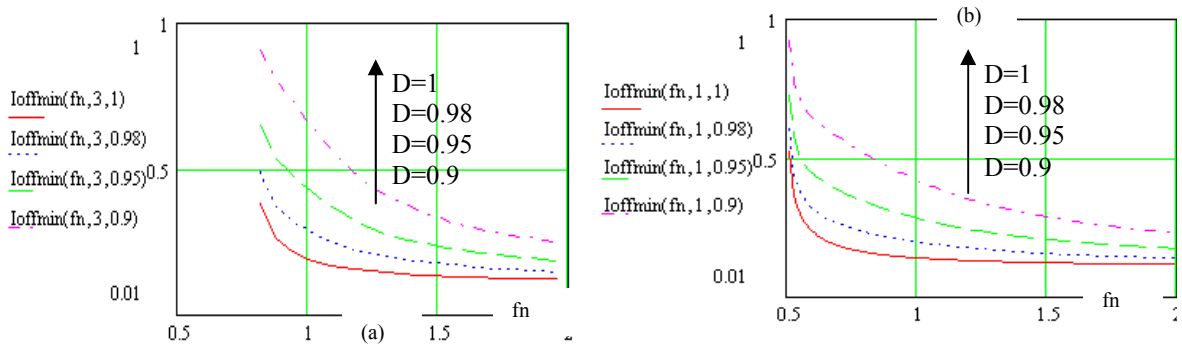


Figure 3-5. Normalized minimum turn off current with different duty cycle (a) Q=3 (b) Q=1

In Equation (3-1), when D is equal to 1, V_{ab1} is the peak value of the first harmonics of the square waveform when it is PS operation mode. When D is less than 1, this kind of waveform still can be treated as a square wave with the reduced magnitude $\frac{V_{in}}{2}\sin\left(\frac{D\pi}{2}\right)$ when it is in NPS operation mode.

Finally, the function of the minimum resonant inductor current for ZVS related to α is obtained with the variables of normalized frequency (fn), quality factor (Q) and duty cycle (D). Therefore, the minimum angle of the inductor current can be solved with the help of the above equations. Bunch curves of minimum normalized turn-off current for ZVS can be obtained and are shown in Figure 3-5. For PS operation, the minimum turn-off current is determined by the inner switches. Its minimum turn-off current for ZVS operation is:

$$I_{off\ \min PS} = I_{Lr}\sin(\alpha - \frac{1}{2}(1-D)\pi) \tag{3-6}$$

For NPS, the minimum current turn-off current for ZVS is:

$$I_{off\ \min NPS} = I_{Lr}\sin\alpha \tag{3-7}$$

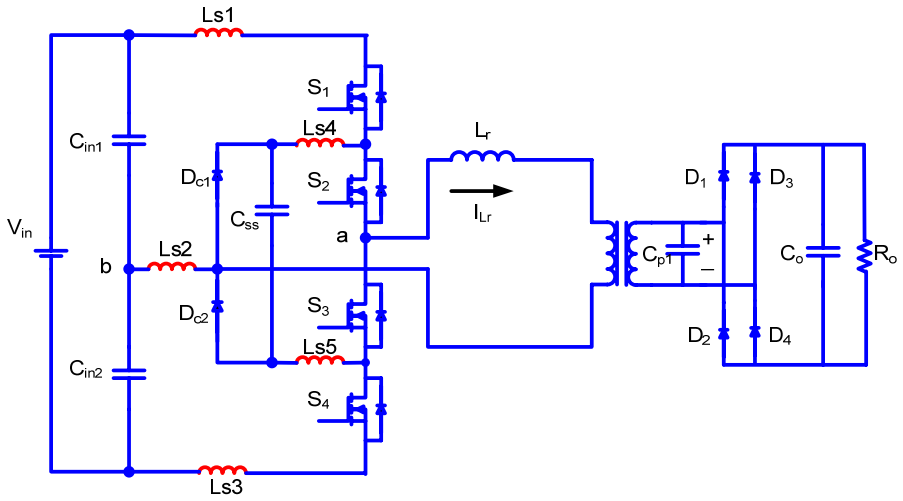
Usually α is very large, close to 180°. Therefore even the phase shift is pretty small,

and $I_{off\ \min PS}$ will be much larger than $I_{off\ \min NPS}$. Alternatively, if the minimum currents are kept the same for the two operation modes, the switching frequency has to be increased for PS operation mode; otherwise, the ZVS operation will be lost for PS operation mode. As a result, PS operation mode will make the switching loss worse than NPS operation mode.

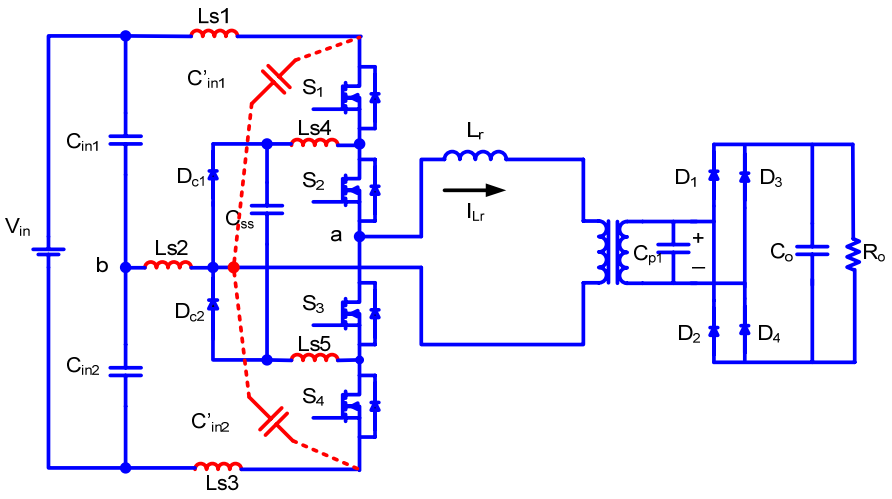
b. Component Stress of Clamping Diode and Flying Cap

For PS ZVS operation, clamping diodes and a flying capacitor will operate when the switches turn on and off. In high-power applications, the clamping diode has to withstand high current and temperature stresses. High current rating diodes and a relatively large heatsink are necessary. Meanwhile, the flying capacitor also must be selected carefully.

Without the phase shift, the clamping diode and flying capacitor have no current during the transition of the switches. The current rating of the clamping diodes and flying capacitor could be greatly reduced. The reduced thermal stress means it is not necessary to put the clamping diodes in the same heatsink as the MOSFETs, which will provide more flexibility for layout.

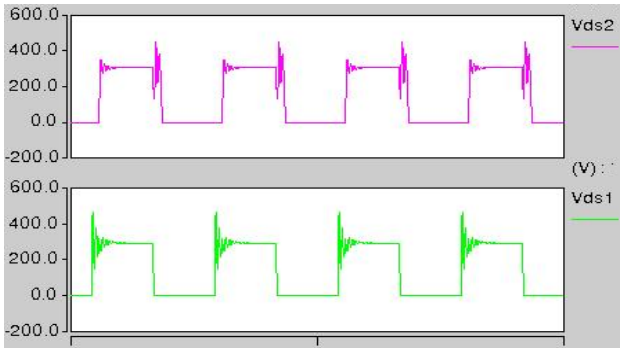


(a)

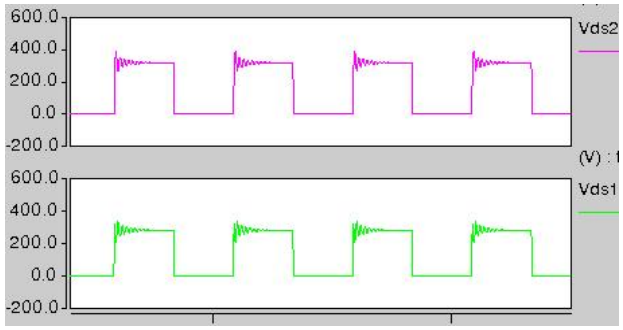


(b)

Figure 3-6. Parasitic inductances in three-level parallel resonant converter. (a) Practical topology (b) Practical topology with decoupling capacitor.



(a)



(b)

Figure 3-7. The simulation results of Vds1 and Vds2 (a) Phase shift operation (b) Non-phase-shift operation.

c. Parasitic Inductance Impacts

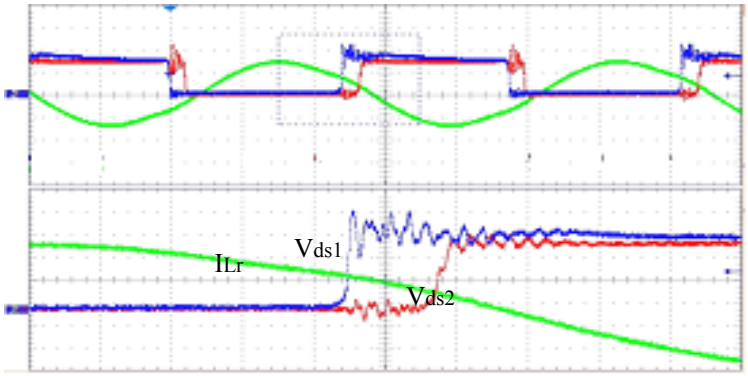
In practice, some stray inductances are included in the power stage, which will cause over-voltage and unbalanced blocking voltage sharing between the switches at turn-off. Particularly in high-power applications where devices with larger size are used, the parasitic influences in the power stage become the main concern. Figure 3-6 shows the three-level converter topology with parasitic inductances. Compact layout and decoupling capacitors can effectively alleviate the parasitic influence. If the input capacitors are tightly connected with the switches, as Figure 3-6 (b) shows, the influences of L_{s1}, L_{s2} and L_{s3} can be mostly eliminated. However, in practice, it is not easy to completely remove L_{s4} and L_{s5} by layout. These two parasitic inductors still cause large over-voltage rings when the switches turn off during PS operation, because the energy of the parasitic inductors have to be released while the switches turn on and off alternately. However, NPS operation mode can avoid this problem. The simulation demonstrates that NPS operation can effectively eliminate L_{s4} and L_{s5}'s impact on the turn-off over-voltage. Because of the symmetric structure, the simulation result shown in Figure 3-7 only includes the V_{ds} of S_1 and S_2.

3.2.3. Experiment verification for NPS operation

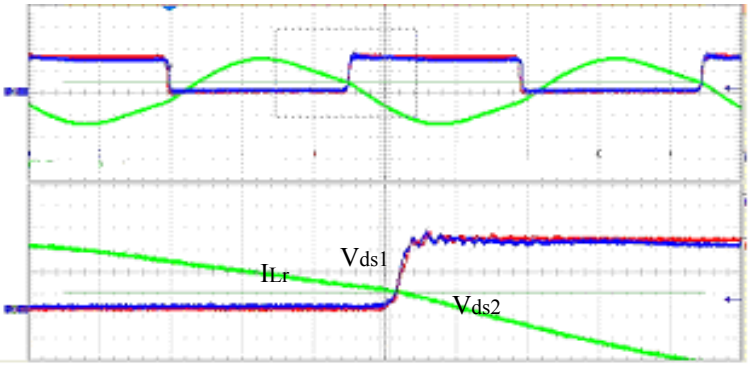
Figure 3-8. Version I Prototype of the 30kW three-level parallel resonant with 64W/in^3

A prototype of a 30kW, 500-700V dc input to 10kV dc output converter was used for

testing, with APT60M75L2LL as the main switches, resonant inductor L=3.63μH, resonant capacitor C=1.24nF, and a high-voltage transformer with a turns ratio of 11 and four output windings, shown in Fig. 3-8.



(a) PS operation mode at 210kHz



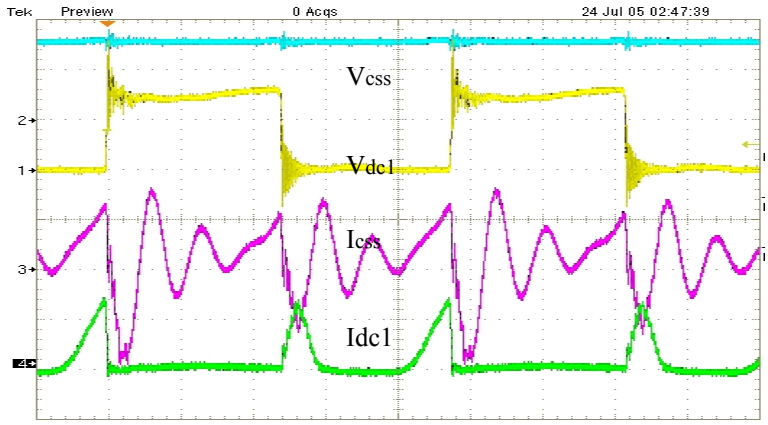
(b) NPS operation mode at 202kHz

Figure 3-9. Waveforms of V_{ds1},V_{ds2} and resonant inductor current Ilr (200 V/div, 200 V/div, 80 A/div, 1 us/div)

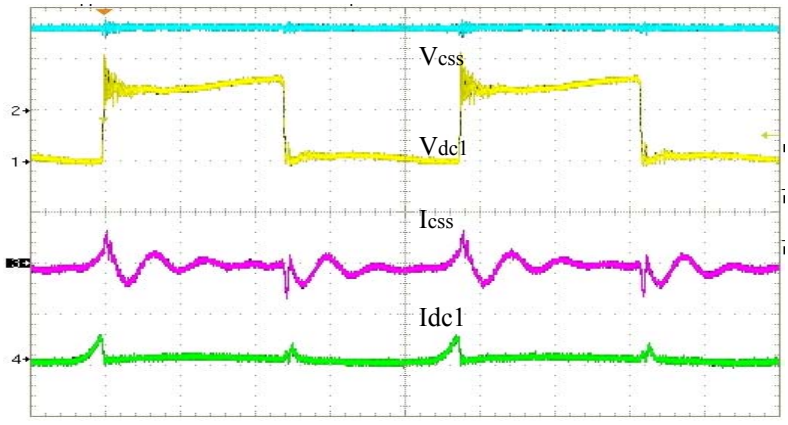
The experimental results are in good agreement with our theoretical analysis. First, as Fig. 3-9 shows, there is significant improvement on the turn-off overvoltage clamping for NPS. The V_{ds} waveforms of Fig. 3-9(b) is quite clean compared to Fig. 3-9(a). In order to keep the same minimum turn-off current, with about 8% duty cycle loss, the converter has to increase the switching frequency from 202 kHz to 210 kHz; otherwise the converter will lose ZVS. During PS operation, the turn-off current of the leading switch is

about twice that of the lagging switch.

Figure 3-10 shows the voltage and current of the up-clamping diode (Dc1) and flying capacitor (Css). It should be noted that there is a small turn-off delay time between the switches in the same leg for the NPS operation mode in order to guarantee that the turn-off time of the outer switches is no later than the turn-off time of the inner switches. Therefore, the flying capacitor and clamping diode still have current with NPS operation. Compared with the PS operation, the current with NPS operation is reduced greatly.



(a) PS operation mode



(b) NPS operation mode

Figure 3-10. Waveforms of flying capacitor voltage (V_{css}), up-clamp diode voltage (V_{dc1}), flying capacitor current (I_{css}) and clamping diode current (I_{dc1}) (200 V/div, 200 V/div, 80 A/div, 80 A/div, 1 us/div)

3.3. Charging profile

3.3.1. Traditional PRC capacitor charging control

The most common capacitor charging techniques are constant current and constant power. The constant-current charging method provides a constant current during the charge period. The selection of the constant-current charge is determined by the required time and targeted load energy.

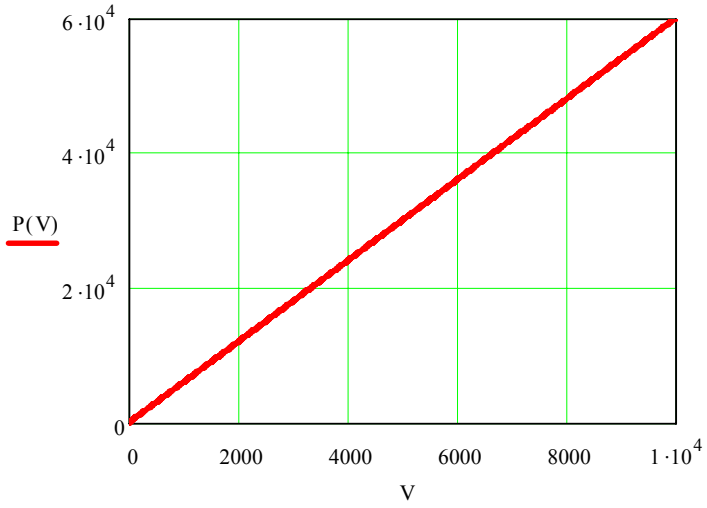


Figure 3-11. Output power as a function of the output voltage for a 6A constant-current charge

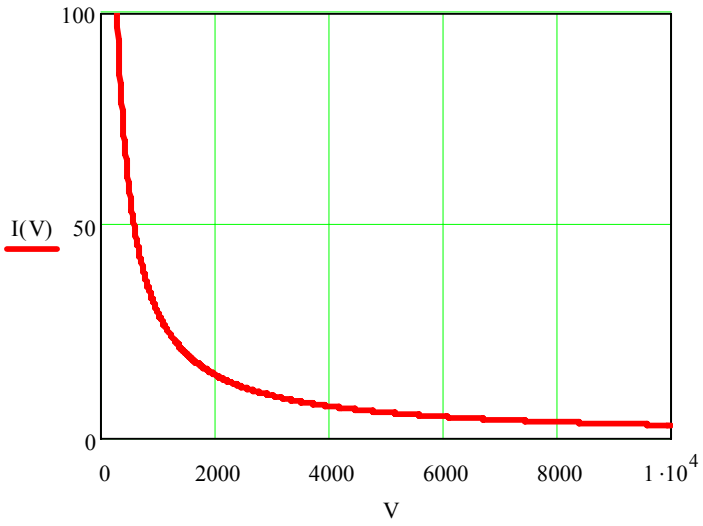


Figure 3-12. Charging current as a function of the output voltage for a 30kW constant-power charge

A constant-current charge higher than 6A is necessary to charge the equivalent capacitance of 0.3 mF within 0.5 seconds. Figure 3-11 shows the curve of the output power vs. the load capacitor voltage. One of the problems presented by this method of charging is that the output peak power of the converter exceeds 60kW at the end of the charge period. This peak power imposes extra stress on the converter design.

Constant-output power charge is another possible method for charging the equivalent capacitance without exceeding the output peak power. In this way, it is guaranteed that during the charge process, the peak power never exceeds the capabilities of the high-voltage converter. For the same charging requirement, a 30kW constant-output power is needed. As shown in Fig. 3-12, one of the disadvantages for this charging mode is that the charge current is very high at a low output voltage. In order to overcome the problems presented by these two methods of charge, a hybrid capacitor charging (HCC) method is proposed for this application [D-1]. The main idea of the HCC method is to start the charge process using a constant-current charge mode. In this way, the current stress in the primary and secondary devices is limited. When the output power reaches the allowed output peak power, the process of charging is changed from a constant current charge to a constant power charge. A power density of 25 W/in^3 is achieved for 3kW capacitor charger in lab. The main drawback of this charging method is the high circulating energy during the constant power charge period. The output power of the resonant converter is limited by a higher switching frequency. However the total input power won't be limited due to the high circulating energy in the resonant tank.

The power factor is used to indicate circulating energy [C-11]. For a resonant converter, if the switching frequency is equal to the resonant frequency, the input voltage

and current are in phase. This means there is no circulating energy when all of the input power is delivered to the load. On the other hand, ZVS operation cannot be achieved if the input voltage and current are in phase. Inductive current is needed to charge and discharge the switch capacitors. Therefore, the switching frequency is preferred to be higher than the resonant frequency. Figure 3-13 shows PRC voltage gain curves. The dashed red curve indicates the resonant frequencies varied with quality factor Q. In order to overcome the high circulating energy during constant power charge, a constant power factor capacitor charging (CPFCC) method is proposed by Dianbo Fu [D-2]. For ZVS operation, the switching frequency must be kept on the right side of curve *a* during the capacitor charging. Meanwhile, the switching frequency should be as close to curve *a* as possible to minimize the circulating energy, like curve *b* in Fig. 3-13.

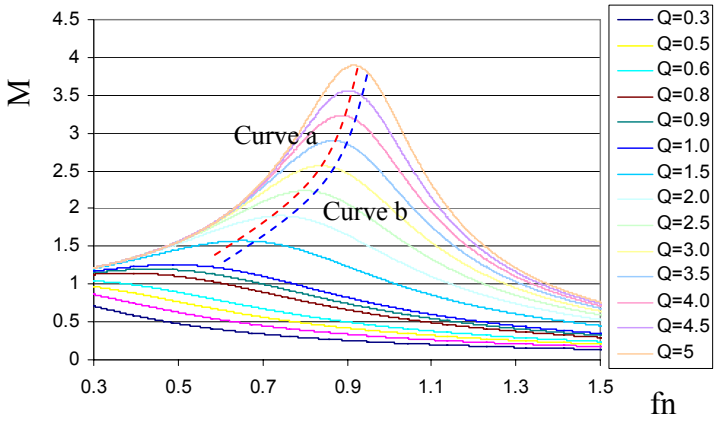


Figure 3-13. Voltage gain curves of parallel resonant converter (PRC)

The comparison of the charging trajectories between the CPFCC and HCC is illustrated in Fig. 3-14. Comparing the CPFCC with the HCC method, we can conclude that the converter will reduce a lot of circulating energy and therefore higher efficiency can be achieved by using the HCC method.

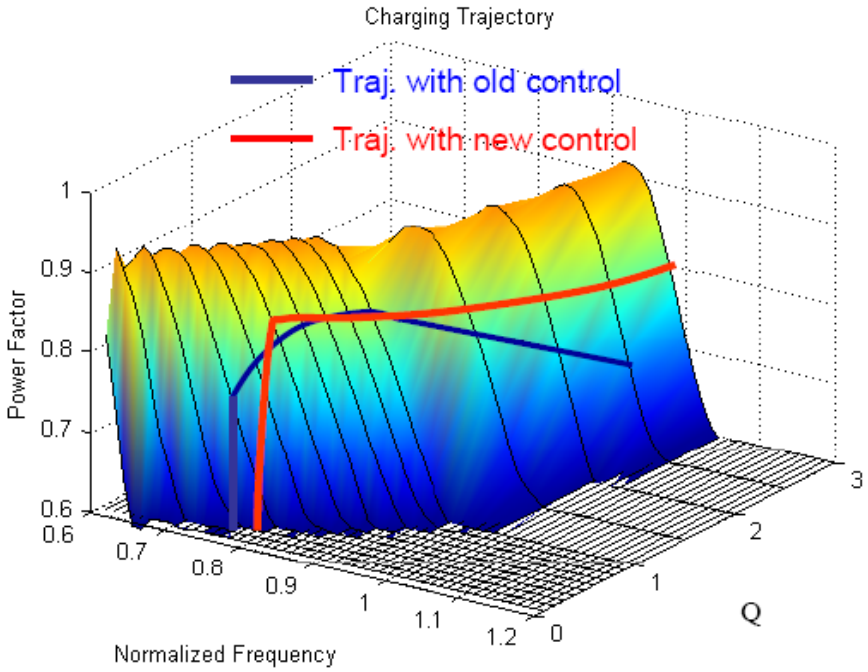


Figure 3-14. Charging trajectories comparison between CPFCC and HCC [D-2].

However, this cannot be accomplished during the entire charging period. At the beginning of the charging process, the voltage of the load capacitor is very low. This leads to a very low Q and a very low switching frequency. As a result, a combined charge method is adopted for this application. The principle is to start the charging process by applying a constant-current charge mode. When the load capacitor is charged, the output voltage will increase. The power factor of the converter will also increase. Once the power factor reaches the predetermined value, the converter will change to constant power factor charge mode. Since the switching frequency doesn't vary too much during the constant-current charge mode, constant switching frequency is used practically for a simple control implementation.

3.3.2. Proposed new PRC capacitor charging profile

It actually doesn't matter what the charging method is, as long as the load capacitor can be charged to 10kV. The constant-current charging method, the constant-power

method, and the constant power factor are limited by the converter itself.

Due to the extremely high transformer turns-ratio, which results in a high stay capacitance on the transformer's secondary side and a relative high leakage inductance, PRC structure II is the only suitable structure for this application when discrete resonant inductor and capacitor are used. . Figure 3-15 shows the volt-second for transformer design during whole charging period with CPFCC control. The peak value is around 2.09mVs, which occurs at the end of the charging cycle.

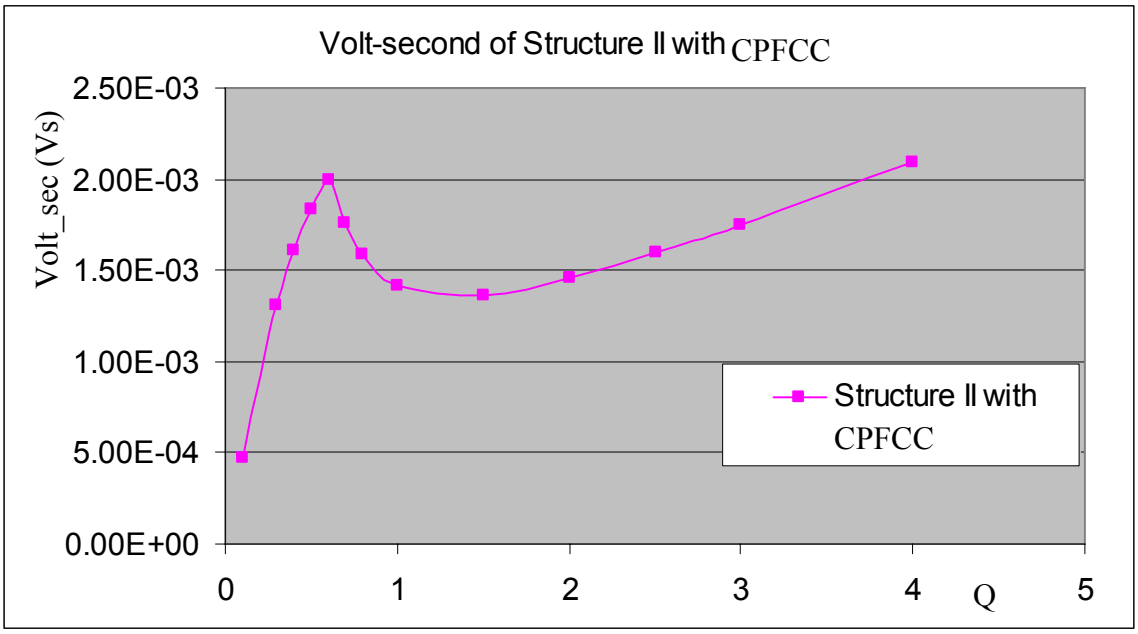


Figure 3-15 Volt-second of structure II with CPFCC

In order to further reduce the resonant tank size, the leakage inductance is used as the resonant inductance. Therefore, the practical structure can be PRC structure I or structure II. By wrapping the secondary winding on the primary winding, the leakage inductance distribution is shown in Fig. 3-16, which is a median structure between Structure I and Structure III.

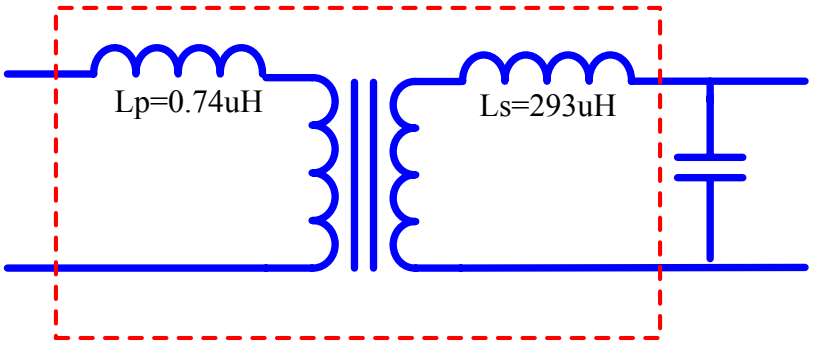


Figure 3-16. Practical structure as leakage inductor utilized as resonant inductor

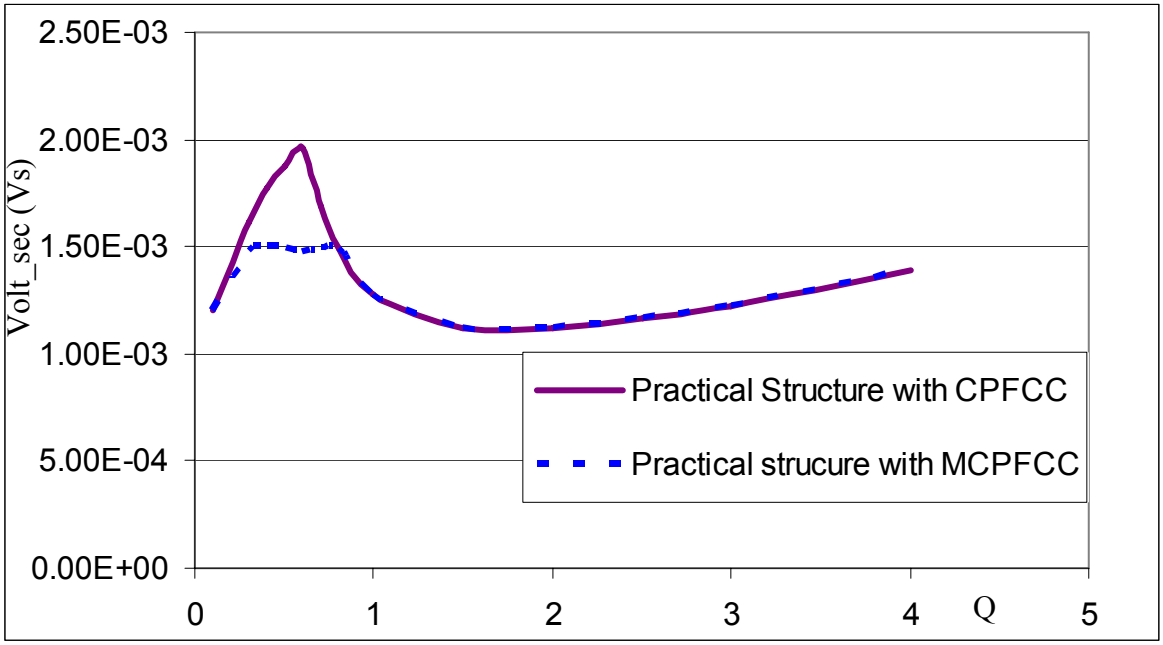


Figure 3-17. Transformer volt-second with different charging schemes

Figure 3-17 shows the volt-second curve when the practical structure is considered. The peak volt-second value is about 2 mVs during the initial charging period. The peak value is caused by the constant-current charging method. It is not necessary to maintain the constant-output current as long as the rectifier diode can handle the change in current. In fact, when a SiC Schottky diode is used as the output rectifier bridge, the power loss on the rectifier is significantly reduced due to the SiC Schottky diode's virtual zero reverse recovery loss property. In order to minimize the transformer volume, a modified constant power factor charging (MCPFCC) method is desired.

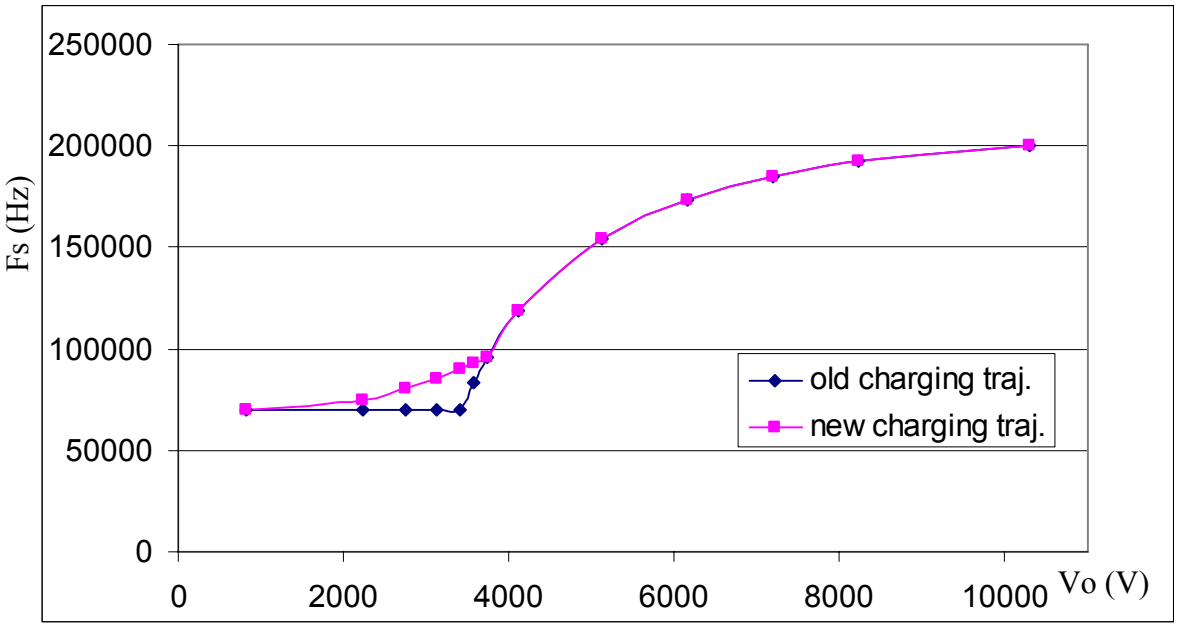


Figure 3-18. Charging profiles with different charging schemes.

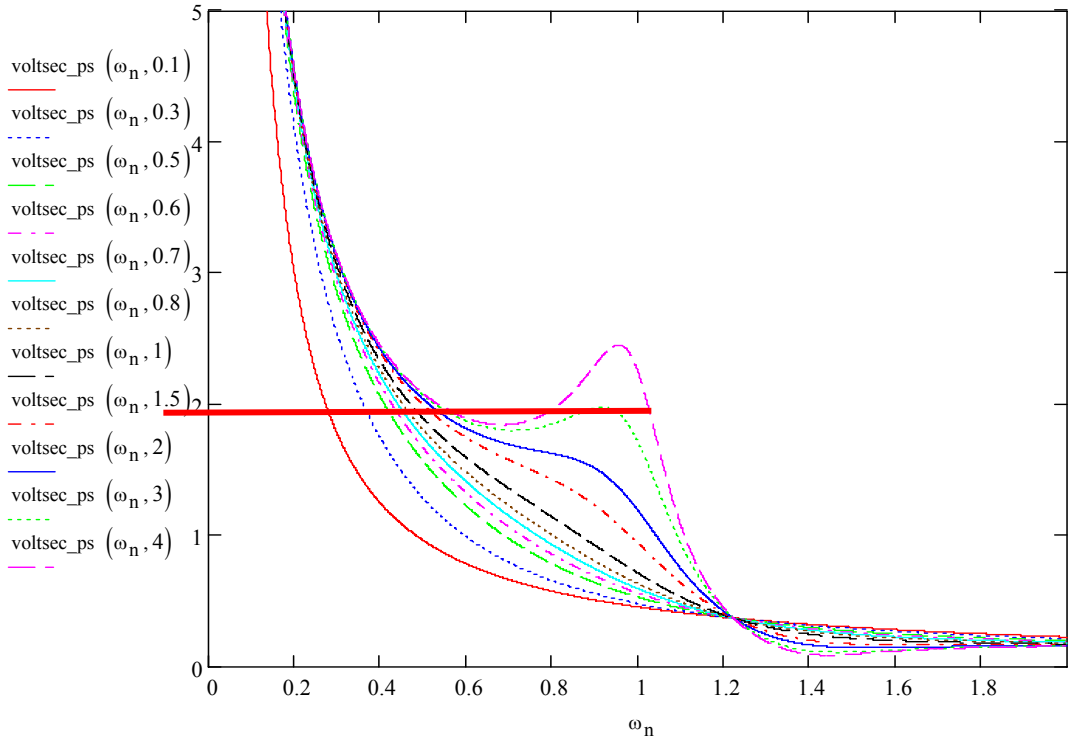


Figure 3-19. Transformer volt-second curves in practical structure varied with different quality factors and normalized switching frequency

The dotted curve in Fig. 3-17 shows the volt-second value for a transformer design using the MCPFCC method. The peak value is 1.5 mVs, which is 25% less than the peak

value of the CPFCC charging method. Correspondingly, Fig. 3-18 shows the charging trajectories.

With the aforementioned methodology, the charging profile can be illustrated by Fig. 3-19. The peak value of the transformer volt-second occurs at the final point when the output voltage gain is highest or at the initial charging period where the volt-second is very sensitive to the switching frequency. Together with the power factor curves shown in Fig. 3-14, the new charging profile can be completed.

3.4. Charging control implementation

Two methods have been used to achieve the non-linear charging profile; one is output voltage based variable frequency control (VFC), and the other is the proposed phase-locked loop (PLL) control. The pros and cons of these two methods are introduced below, as is the detailed design procedure.

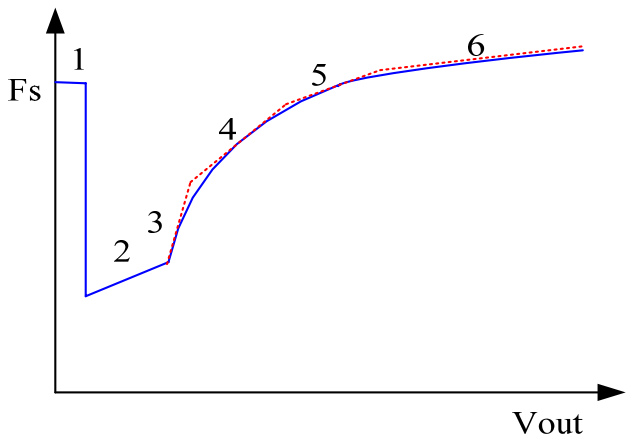


Figure 3-20. Practical system charging profile

3.4.1. Charging control implementation with piece-wise method

In practice, a high switching frequency is used for soft startup to avoid the inrush current

during the initial charging time. Consequently, the charging profile is illustrated by the solid curve in Fig. 3-20. In order to implement a nonlinear charging profile, the charging profile is divided into four segments. Therefore, the entire charging profile has six segments, which are illustrated by the dashed line in Fig. 3-20.

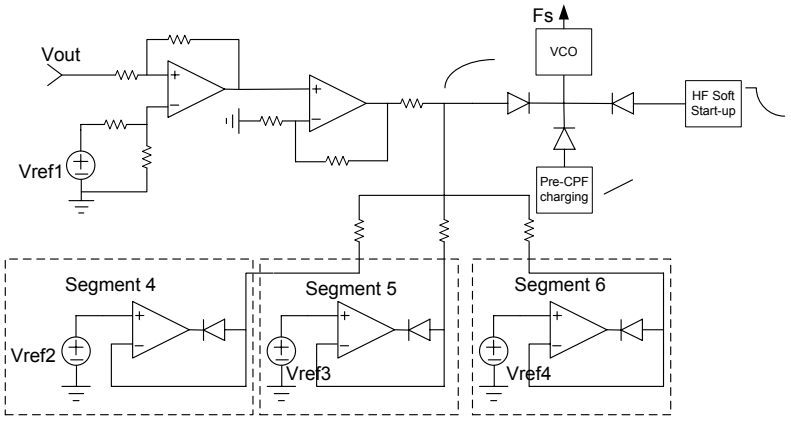


Figure 3-21. Schematic of controller implementation

The schematic of the controller for the charging profile implementation is depicted in Fig. 3-21. First, a high voltage is generated by the HF soft start-up block for high-frequency start-up, and a low voltage slew rate is generated by the pre-CPF charging block. The four piecewise linear segments are achieved by three clamping circuits. When the inverting input voltage of the operational amplifier is lower than the non-inverting input voltage, the diode is off and the clamping circuit has infinite impedance. The first segment of CPF charging is achieved. As long as the measured output voltage reaches the preset value, the diode will turn on and the inverting input voltage will be clamped by the non-inverting input voltage. The rate of frequency change will be slowed down by the clamping circuit. Then each segment will be generated consecutively as the output voltage increases. Due to the nonideality of the diode turn-on property, each section can be smoothly switched to the next one as the measured output voltage increases and

reaches each reference voltage. More clamping circuits can be added if more segments are need for piecewise distribution.

The performance of the schematic for VFC control can be verified with a signal generator. Figure 3-22 shows the experimental result. The feedback of the output voltage can be simulated by a 100Hz, 10V triangle signal provided by a signal generator. Then the varied frequency of the VFC control board can be extracted in SABER simulation software. For each cycle of the triangle waveform, the related varied frequency curve is shown in the bottom plot in Fig. 3-22.

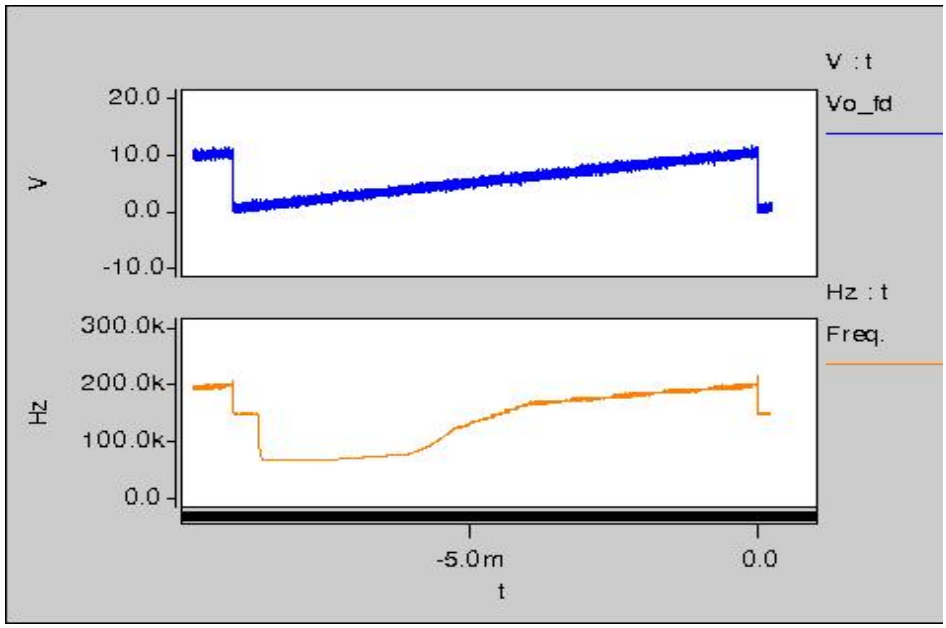


Figure 3-22. Experimental results of the schematic of VFC control

If the charging profile is determined, almost any nonlinear charging curve can be achieved by adjusting the parameters. However, it is difficult to ensure ZVS operation and maximum power transfer while charging with this method. First, the non-linear charging profile is obtained by simulation and calculation. Even if the circuit can deliver the same charging profile, the charging profile itself may not exactly express the practical resonant converter behavior. Second, the sensed output voltage is noisy. An excessive

margin, obtained by using a high switching frequency, is always needed to guarantee ZVS operation in practical implementation and to account for possible variations in resonant parameters. When the switching frequency is far beyond the resonant frequency, high circulating energy will be induced, which reduces the maximum power delivery and generates high conduction loss. The other problem of the output-voltage-based VFC comes from the varied input voltages. The controller has to sense the input voltage to adjust based on varied input voltages, which results in a complex design. Another way to deal with varied input voltages is to further increase the margin to tolerate the varied input voltages, which is detrimental to the performance of the converter, and may not work if the range of varied input voltages is too wide.

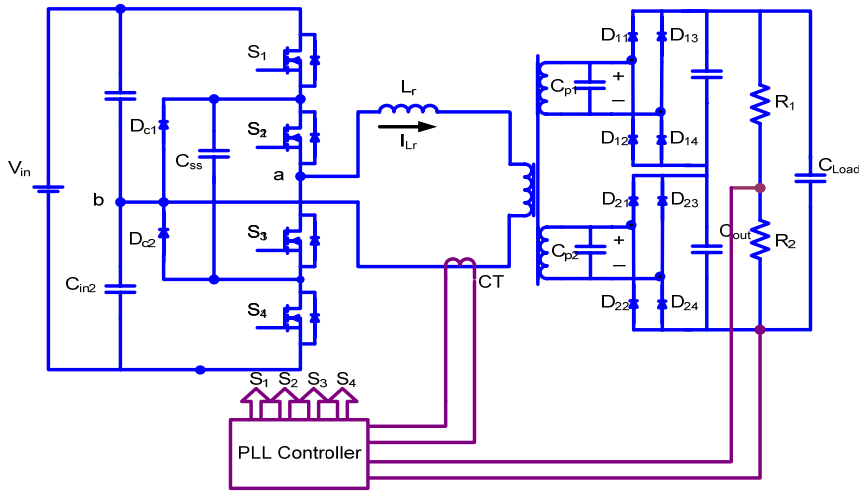


Figure 3-23. Three-level parallel resonant converter for capacitor charging with PLL control

3.4.2. The operating principle in capacitor charging with PLL

These problems, along with the output-voltage-based VFC, can be solved by frequency tracking control with a phase-locked loop (PLL), shown in Figure 3-23. PLL-based control has been used widely in induction heating and motor drives [D-3]-[D-7], but has not been introduced for capacitor charging. Furthermore, for each case that employs a

phase-locked loop for tracking the resonance frequency of the load, there are no analysis or design methods offered for the resonance frequency tracking system. Instead, only qualitative explanations and experimental results are presented.

The proposed PLL control method can ensure the maximum output power for capacitor charging and ZVS operation with variable input and parameter conditions. The switching frequency is based on the measured inductor current frequency instead of frequency estimation by output voltage. The sensed output voltage is only needed for maintaining the converter charging level. Thus the switching frequency is generated by the resonant converter itself instead of imposing an external switching signal. As long as the phase shift, which is the resonant tank input voltage angle that leads the input current angles, is between 0^o and 90^o, the converter can be self-sustaining using the sensed current frequency [D-8][D-9]. According to the analysis in [D-9], the proposed control methods can be extended to other resonant converters, including SRC and SPRC.

3.4.3. PLL design and analysis

The control diagram for a PLL system for a PRC capacitor charger is shown in Figure 3-24. These control blocks can be implemented with a commercial PLL IC and its peripheral interface circuits.

The input signal is measured by using a current transformer on the resonant inductor current. This sinusoidal waveform is processed by a zero-crossing comparator to generate a square wave signal, which serves as the reference signal for the PLL. Attention must be paid to the zero-crossing comparator design due to the possibility of noise interference. In order to generate the leading time needed to achieve ZVS and compensate the delay time due to the filter, comparator, etc., the feedback signal passes a leading phase shift

generation circuit before being compared with the current signal.

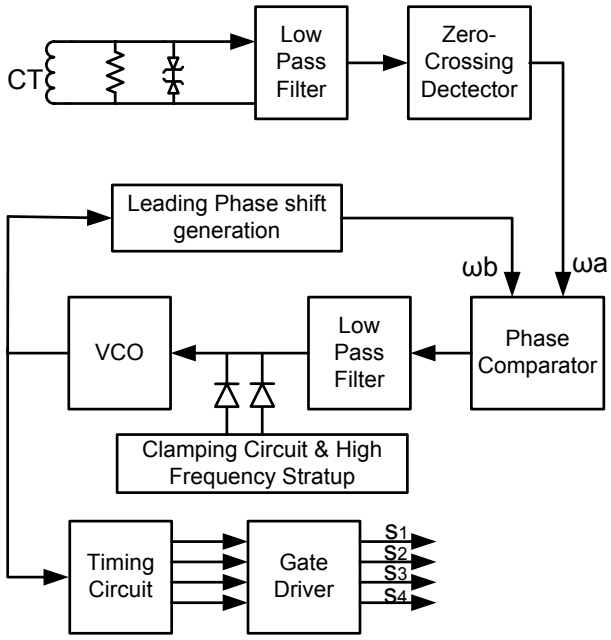


Figure 3-24. PLL control diagram for PRC capacitor charger

Before the converter starts to charge the load capacitor, the input of the voltage-controlled oscillator (VCO) is high. As soon as the startup signal is triggered, the VCO input voltage begins to gradually decrease and is finally clamped by the minimum voltage. The slow increase in voltage is necessary to excite the resonant inductor and capacitor and help the PLL lock to the reference frequency smoothly, and then the output of the PLL automatically starts to follow the resonant frequency.

The performance of the controller for the most part depends on the PLL design and its peripheral interface circuits, including the phase detector selection, the reference square waveform generation, and the low-pass filter design. There are two phase detectors in the commercial PLL IC (such as the CD4046). The second type of phase detector, the so-called PFD, is the preferred type in this application.

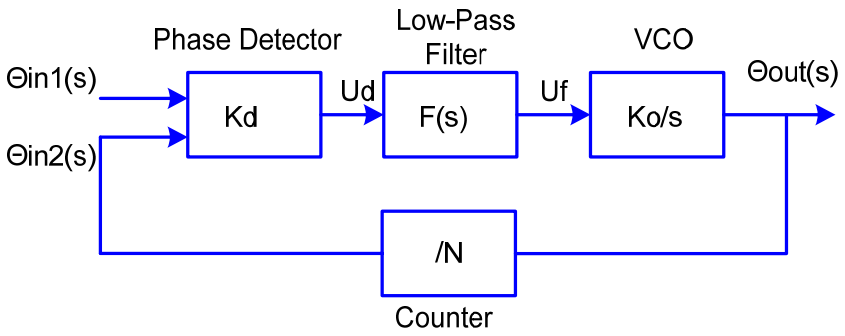


Figure 3-25. PLL transfer function block diagram

A. PLL Architecture

A phase-locked loop (PLL) [D-10]-[D-12] is a circuit that synchronizes the signal from an oscillator with a reference signal. Generally a PLL consists of three blocks: a phase detector, a low pass filter, and a VCO, shown in Fig. 3-25. The block of N counter is used to increase the output frequency to be N times the input reference signal. In this application, the output signal from the VCO is directly connected to one of the inputs of the phase detector without the N counter. The gain of the phase detector of Kd is determined by the type of phase detector. For a phase-frequency detector (PFD), Kd can be computed by

$$Kd = \frac{U_d}{4\pi} \tag{3-8}$$

where U_d is the output signal of the phase detector.

The angular frequency of the VCO can be given by

$$\omega_{out} = \omega_0 + K_0 u_f(t) \tag{3-9}$$

where ω_0 is the center (angular) frequency of the VCO, K_0 is the VOC gain, and $u_f(t)$ is the input signal of the VCO.

The frequency is equal to the phase derivative, and θ_{out} can be expressed by the

integral over the frequency variation $\Delta\omega$, which can be solved by Equation (3-10).

$$\Delta\omega(t) = K_0 \cdot u_f(t) \tag{3-10}$$

Then, θ_{out} is given by

$$\theta_{out}(t) = \int \Delta\omega(t)dt = K_0 \int u_f(t)dt \tag{3-11}$$

Applying the Laplace transform, the above equation can be written as:

$$\theta_{out}(s) = \frac{K_0}{s} u_f(s) \tag{3-12}$$

Hence, the transfer function of the VCO can be obtained:

$$\frac{\theta_{out}(s)}{u_f(s)} = \frac{K_0}{s} \tag{3-13}$$

From the above function, we see that, in essence, the VCO is an integrator for a phase signal.

If the transfer function of the low-pass filter is $f(s)$, the closed-loop transfer function of the PLL can be expressed by:

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in1}(s)} = \frac{G(s)}{1+G(s)} = \frac{K_d \cdot K_0 \cdot f(s)}{s + K_d \cdot K_0 \cdot f(s)} \tag{3-14}$$

where $G(s) = \frac{K_d \cdot K_0 \cdot f(s)}{s}$; $G(s)$ is also called the open-loop gain.

The highest power of s in the denominator is called the PLL order. If $f(s)$ has n-1 poles in the form of $\frac{1}{s^{n-1}}$, $G(s)$ will have n poles in the form of $\frac{1}{s^n}$, which means the n^{th} order PLL.

B. Low-pass filter design

In order to guarantee ZVS while keeping maximum power delivery, the phase change

tracking ability of the PLL as determined by the order of the PLL is very important. The higher the order of the PLL, the better its tracking ability will be. So the low-pass filter is the key element in the application of PLLs in capacitor charging. The order of the loop filter that needs to be implemented can be determined by examining the performance of a few different filters under input stress.

Using the final value theorem of the Laplace transform, we can write the phase error $\theta e(s)$ as

$$\lim_{t\to\infty} \theta e(t) = \lim_{s\to 0} s \cdot \theta in(s) \cdot \frac{s}{s + K_0 \cdot K_d \cdot f(s)} = \lim_{s\to 0} \theta in(s) \cdot \frac{s^2}{K_0 \cdot K_d \cdot f(s)} \tag{3-15}$$

where $\theta in(s)$ is the signal at the reference input of PLL.

As an estimate for $\theta e(s)$, we can use an input signal that includes a step position, velocity and acceleration.

If there is a phase step,

$$\theta in(s) = \frac{\Delta\theta}{s}. \tag{3-16}$$

If there is a frequency step or phase velocity,

$$\theta in(s) = \frac{\Delta\omega}{s^2}. \tag{3-17}$$

If there is a frequency ramp or phase acceleration,

$$\theta in(s) = \frac{\Delta\dot{\omega}}{s^3}. \tag{3-18}$$

Table 3-1 shows the steady state error of each loop filter in relation to the different the input signals.

Table 3-1 – PLL steady state errors for different input signals

PLL	Low pass filter	Input signals		
		Phase step	Frequency step	Frequency ramp
1st order	0 order	0	$\frac{\Delta\omega}{K_0 \cdot K_d}$	Monotonically increasing
2nd order	1st order	0	0	$\frac{\dot{\Delta\omega}}{K_0 \cdot K_d}$
3rd order	2nd order	0	0	0

From the above analysis, we can see that in order to obtain zero steady state, the first-order PLL can track a phase step, while the second-order PLL can track a frequency step and the third-order PLL can track a frequency ramp. Unlike the other applications, which typically design the PLL based on the performance when a frequency step is applied to its reference input, the PLL as used for capacitor charging with the proposed charging profile needs to deal with the response for a nonlinear varied frequency curve. Though the charging profile can be described with a curve fitting method, such as $K\sqrt{t}$, for a conservative design, the design is based on the worst case using the steepest segment with the piecewise method, such as segment 3 in Fig. 3-20. This segment can be described as a mathematic equation.

$$f_s(t) = f_o + k_c \cdot t \tag{3-19}$$

where k_c is the slope of the steepest segment.

It should be noted that in the practical design, the rate of change of the resonant frequency may not be as large as the piecewise-linear segment, due to the interaction of the switching frequency and resonant frequency.

If the nonlinear reference input signal is piecewise-linear, the PLL references a frequency ramp. Considering the fact that the phase is the integral of the frequency, in

theory the input signal is accelerated, and a third-order PLL is needed in order to have zero final phase errors. Because each pole of the transfer function causes a phase shift of nearly 90^o, the overall phase shift can approach 270^o. The loop stability thus becomes an issue.

Because the steady state phase error is both linearly dependent on the magnitude of the acceleration and natural frequency of the PLL transfer function, a second-order PLL should be able to cope with the slow frequency velocity, without overly affecting performance. The benefit in terms of performance of a third-order PLL over a second-order PLL would be fairly small. A second-order PLL seems therefore to be the best tradeoff between design complexity and performance. In this application, the passive lead-lag filter is utilized as low pass filter, as shown in Fig. 3-26.

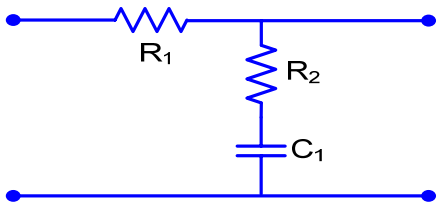


Figure 3-26. Passive lead-lag low pass filter

The transfer function the lead-lag filter is given by

$$f(s) = \frac{1 + s \cdot \tau_2}{1 + s \cdot (\tau_1 + \tau_2)} \tag{3-20}$$

where $\tau_1 = R_1 \cdot C_1$ and $\tau_2 = R_2 \cdot C_1$.

Substituting for $f(s)$ in Equation (3-12), the transfer function of the second order PLL can be obtained:

$$H(s) = \frac{K_d \cdot K_0 \cdot \frac{1 + s \cdot \tau_2}{\tau_1 + \tau_2}}{s^2 + s \cdot \frac{1 + K_d \cdot K_0 \cdot \tau_2}{\tau_1 + \tau_2} + \frac{K_d \cdot K_0}{\tau_1 + \tau_2}} \tag{3-21}$$

For a second-order transfer function, it is common practice to write the denominator of the transfer function in so-called normalized form:

$$H(s) = \frac{s \cdot \omega_n \cdot \left(2\zeta - \frac{\omega_n}{K_0 \cdot K_d}\right) + \omega_n^2}{s^2 + 2s \cdot \zeta \cdot \omega_n + \omega_n^2} \tag{3-22}$$

where natural frequency $\omega_n = \sqrt{\frac{K_0 \cdot K_d}{N(\tau_1 + \tau_2)}}$, and damping factor $\zeta = \frac{\omega_n}{2} \cdot \left(\tau_2 + \frac{1}{K_0 \cdot K_d}\right)$.

If $K_0 \cdot K_d >> \omega_n$ the PLL system is said to be a high-gain loop, which can be true in most applications. For a high-gain loop, Equation (3-22) can be changed as below:

$$H(s) \approx \frac{2s \cdot \zeta \cdot \omega_n + \omega_n^2}{s^2 + 2s \cdot \zeta \cdot \omega_n + \omega_n^2}. \tag{3-23}$$

Consequently, the error transfer function can be expressed by

$$H_e(s) \approx \frac{s^2}{s^2 + 2s \cdot \zeta \cdot \omega_n + \omega_n^2}. \tag{3-24}$$

Because the phase signal is the integral over the frequency variation, the input phase signal can be obtained based on Equation (3-25).

$$\theta_{in}(t) = \int f_s(t)dt = f_0 \cdot t + k_c \cdot \frac{t^2}{2}. \tag{3-25}$$

Therefore, the Laplace transform $\theta_{in}(s)$ becomes

$$\theta_{in}(s) = \frac{f_0}{s^2} + \frac{k_c}{s^3}. \tag{3-26}$$

So the phase error θ_e is obtained from

$$\theta_e(s) = H_e(s) \cdot \theta_{in}(s) . \tag{3-27}$$

Inserting Equations (3-24) and (3-26) into Equation (3-27) yields

$$\theta_e(s) = \left(\frac{f_0}{s^2} + \frac{k_c}{s^3} \right) \cdot \frac{s^2}{s^2 + 2s \cdot \zeta \cdot \omega_n + \omega_n^2} . \tag{3-28}$$

Applying the inverse Laplace transform to Equation (3-28), the transient response of phase-error $\theta_e(t)$ is shown in Fig. 3-26 and 3-27 in respect to different natural frequencies and damping factors in the transfer function.

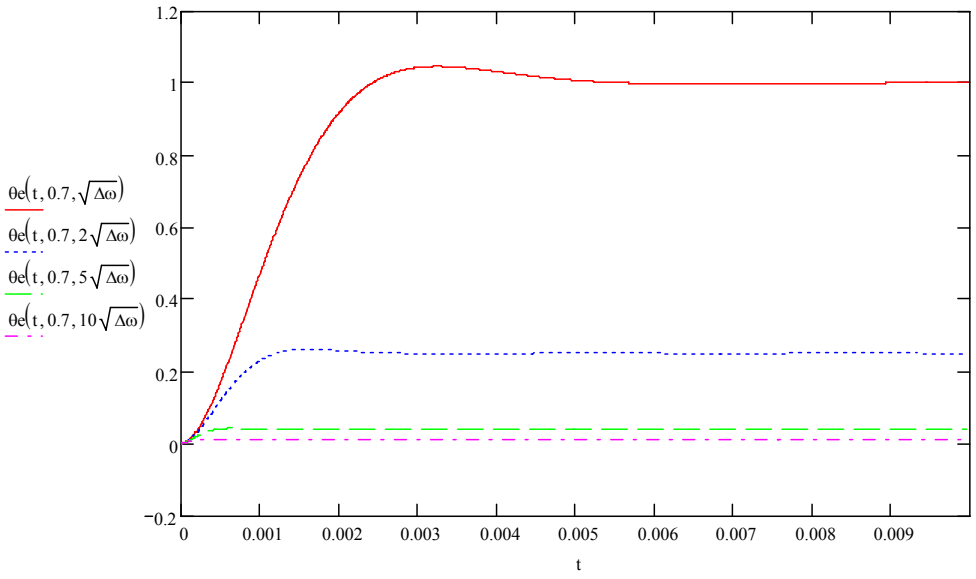


Figure 3-27. Transient response of a linear second-order PLL to a frequency ramp; Δω applied to its reference input at t=0 with varied natural frequencies of the second-order PLL

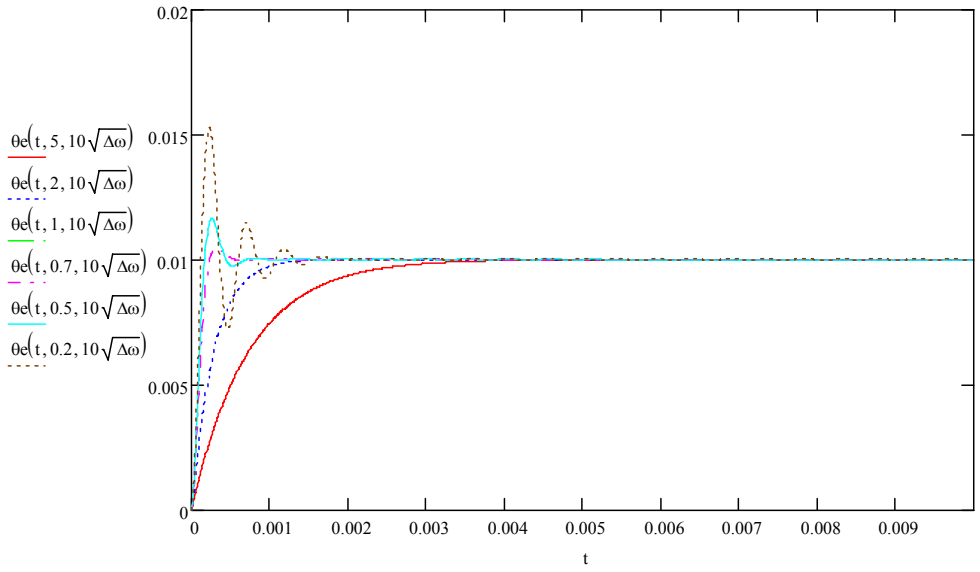


Figure 3-28. Transient response of a linear second-order PLL to a frequency ramp; $\Delta\Omega$ applied to its reference input at t=0 with varied damping factors of the second-order PLL

The final phase error $\theta_e(\infty)$ can be calculated by applying the final value theorem of the Laplace transform.

$$\theta_e(\infty) = \lim_{s\to 0} s \cdot H_e(s) \cdot \theta_{in}(s) = \frac{k_c}{\omega_n^2} \tag{3-29}$$

The expression $\omega_n = \sqrt{2 \cdot k_c}$ provides the practical design limit for $\Delta\dot{\omega}_{\max}$ to avoid lockout [D-10].However, a minimal phase error is necessary to keep the converter operating at ZVS without larger circulating energy. In this application, to restrict the maximum phase error within one tenth of the phase shift, the minimum natural frequency is considered to be:

$$\omega_n \geq 5 \cdot \sqrt{k_c} \tag{3-30}$$

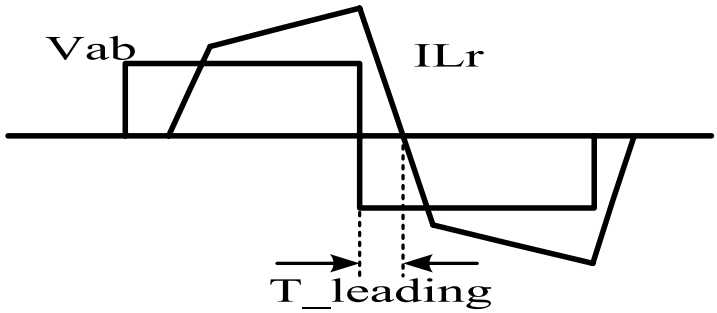
$1/\sqrt{2}$ is typically chosen for ζ in order to obtain an optimally flat transfer function. Finally, the parameters of the low-pass filter can be obtained based on the above equations.

C. Deadtime and leading time

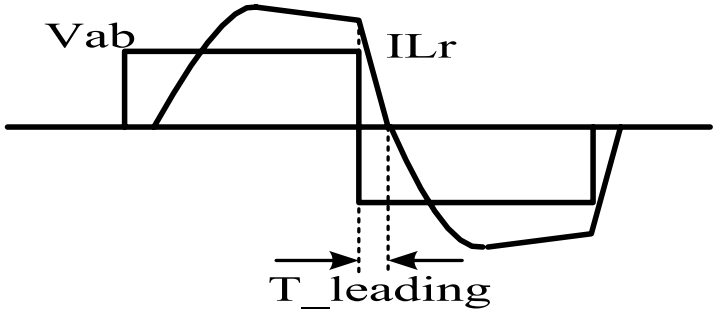
With the PLL, the frequency tracking control can be achieved by utilizing the feedback signal from the resonant inductor current to generate the switching signal instead of using the output voltage to generate the switching signal. While following the resonant frequency, a leading phase shift is needed to generate inductive current for ZVS operation.

As in the aforementioned PRC ZVS condition, in contrast with the conventional PWM converter, implementing a leading phase shift is complex because the converter continues transferring energy to load during the commutation.

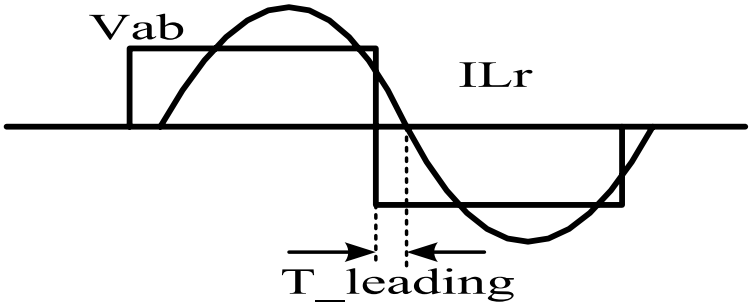
During the charging period, the output voltage and inductor current are varied; thus the ZVS condition is varied. In order to have enough energy in the inductor, the switching signals must have a leading phase shift for a certain inductive turn-off current, which determines the inductor energy and needs a certain amount of deadtime for the switch capacitor charging and discharging under the worst conditions. To simplify the implementation, a leading time is used rather than the leading phase angle, as shown in Figure 3-29. The control will be stable if the phase angle of voltage leading current the phase angle is between 0 and $\pi/2$; in other words, if the leading time is larger than zero and less than a quarter period [D-13].



(a)



(b)



(c)

Figure 3-29. The inverter output voltage and resonant inductor current. (a) M=0.5, Q=0.7 (b) M=1.5, Q=2 (b) M=3, Q=4

Therefore, in order to guarantee ZVS operation and minimize the circulating energy, the minimum leading times related to the turn-off current and deadtime need to be identified for the worst ZVS condition.

The load for the capacitor charger can be represented by an equivalent resistance during charging. The equivalent resistance, and thus load quality factor Q, increases as the load capacitor voltage goes up. Consequently, the current waveforms change during the whole charging period. Figure 3-29 shows the current waveforms at different stages. When the voltage gain is less than one, the turn-off current is always inductive and equal to the peak value of inductor current, shown in Figure 3-29(a). Therefore it is easy to achieve ZVS in this stage due to the sufficient turn-off current. When the voltage gain is larger than one, the turn-off current may not be high enough for ZVS operation, or it may

not even be inductive.

The minimum leading time and deadtime can be found with the ZVS equivalent circuit shown in Fig. 3-4; the closed-form solution can be derived by:

$$v_c(t) = (V_{co} - \frac{V_o}{n}) \cdot \cos(\frac{1}{\sqrt{L_r \cdot C_{eq}}} t) - \frac{I_{Lo}}{\sqrt{\frac{C_{eq}}{L_r}}} \cdot \sin(\frac{1}{\sqrt{L_r \cdot C_{eq}}} t) + \frac{V_o}{n} \tag{3-31}$$

where v_c is the voltage across the switch capacitor; C_{eq} is the total equivalent capacitance of two series switch capacitors the and external capacitors if any are in parallel with the switch; V_{co} is equal to the input voltage; I_{Lo} is the turn-off resonant inductor current; V_o is the output voltage; and n is the transformer turns ratio. It should be noted that the three-level structure is treated as a half-bridge in the above equation because of the non-phase-shift operation between the switches in the same leg; the sinusoidal waveform of resonant current is assumed.

For example, if the input voltage is 600V and each switch has a 15nF snubber capacitor, $V_{co} = 600V$, and $C_{eq} = 7.5nF$. The polarity of the capacitor voltage in the equivalent circuit in Fig. 3-4 will be reversed in ZVS operation. With the help of Equation (3-31), the minimum turn-off current needed for ZVS operation can be derived as:

$$I_{LO\_\min}(t) = -\sqrt{\frac{C_{eq}}{L_r}} \cdot \frac{-\cos(\frac{1}{\sqrt{L_r \cdot C_{eq}}} t) \cdot Vco + \cos(\frac{1}{\sqrt{L_r \cdot C_{eq}}} t) \cdot \frac{Vo}{n} - \frac{Vo}{n} - Vco}{\sin(\frac{1}{\sqrt{L_r \cdot C_{eq}}} t)} \tag{3-32}$$

Figure 3-30 shows the needed turn-off current for ZVS operation with varied output voltages. The x-axis shows how much time is needed for the capacitor charging and discharging time, which can indicate the needed deadtime.

The leading time, which determines the turn-off current and deadtime selection, is a tradeoff among the voltage stress on the MOSFET, duty cycle loss and a ZVS guarantee. Though Fig. 3-30 shows the minimum turn-off current for ZVS operation, ZVS cannot be achieved if the deadtime is too short or too long. The deadtime has to be between the two intersections of the turn-off current and the minimum turn-off current curve. For instance, the peak curve in Fig. 3-30 shows the minimum turn-off current needed for ZVS operation when the output voltage transformed to the primary side is 1000V. If the practical turn-off current is 100A, the deadtime has to be between point a and point b. If the deadtime is less than point a, 100ns, the switching capacitor doesn't fully discharge to zero before its gate signal becomes too high. On the other side, if the deadtime is longer than point b, 350ns, the switching capacitor voltage bounces up after it drops to zero when its gate signal becomes high. In terms of efficiency, a minimal deadtime is preferred. A long deadtime means large duty cycle loss, but a short deadtime requires high turn-off current for ZVS achievement. The converter turns off at hard-switching mode while ZVS is achieved for turn-on operation. The voltage stress associated with the voltage spike on the MOSFET limits the turn-off current. Moreover, the high turn-off current may not be attained at low Q and low output voltage.

Since the leading time is defined instead of the leading phase angle for the turn-off current, it is difficult to set the leading time because the current waveform during low *Q* is not sinusoidal, and the amplitude and frequency increases as Q increases. Compared with a high Q and a high output voltage condition, determining how to achieve ZVS at low Q and low output voltage is more critical. Though low turn-off current is needed for ZVS at low *Q* because the energy transferred to the load is low when the output voltage is

low, a long leading time is needed for ZVS operation at low Q due to low current frequency and low amplitude. Again, the same leading time causes excessive turn-off current at the final point that will impact the Vds spike because the current at high Q has high frequency and amplitude. Hence there is a trade-off between ZVS condition and Vds ringing.

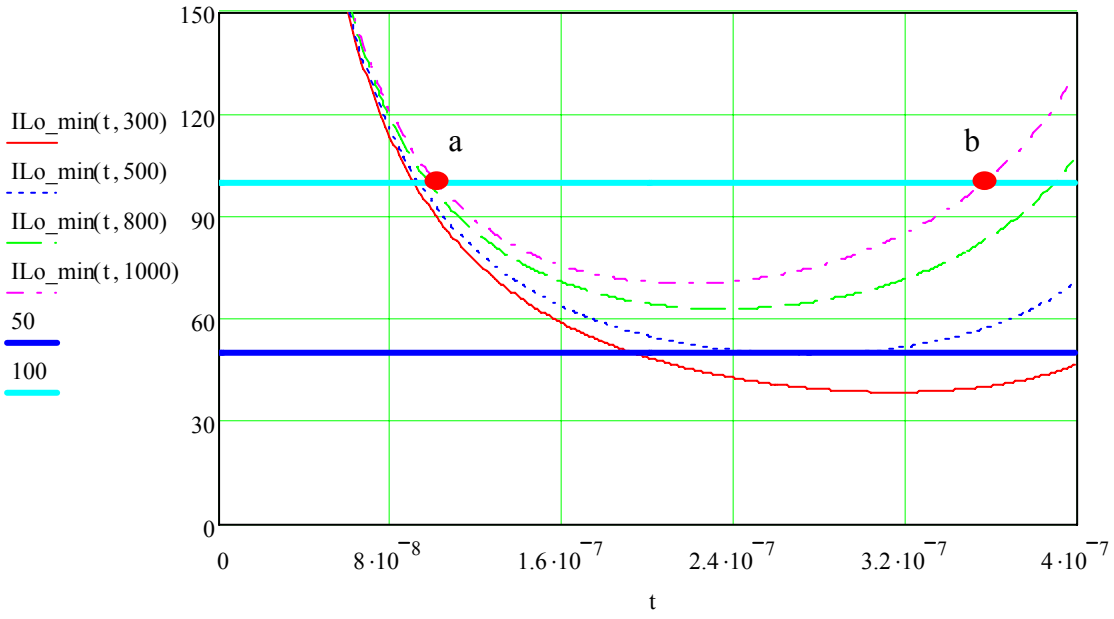


Figure 3-30. The needed deadtime vs. turn-off current and output voltage

With the help of simulation, the leading time is set 300ns in this system, which could be slightly tuned in a practical circuit. The turn-off current varies from 50A to 100A during the entire charging period. In addition, in order to compensate the delay time due to the filter, comparator, etc., the leading time needs a margin plus the necessary time designed for ZVS.

According to the determined turn-off current and Fig. 3-30, the longest deadtime needed for ZVS operation is 190ns. Therefore, the deadtime is set as 200ns based on the actual setup and the need for an overall compromise.

D. Reference frequency generation

The reference frequency generation circuit is comprised of a current transformer, zero-crossing detection and a monostable multivibrator, as illustrated in Figure 3-31.

Theoretically, the reference frequency can be sensed from the resonant inductor current or resonant capacitor voltage. In this application, the resonant inductor current is sensed. The current transformer not only transforms the resonant inductor current to the needed value by its turns-ratio, but also provides electrical isolation. The current conversion ratio, i.e. the turns-ratio of the current transformer, is set to a specific value to avoid high voltage, and to protect the CMOS in IC while it maintains the minimal voltage needed to be detectable.

The zero-crossing detector (ZCD) design is very critical due to the noisy environment. In order to obtain a clean signal, which can reflect the correct frequency of resonant inductor current, the ZCD is comprised of a comparator with hysteresis. Furthermore, the output signal of the ZCD goes through a monostable multivibrator before it is connected to one of the inputs of the PLL phase detector.

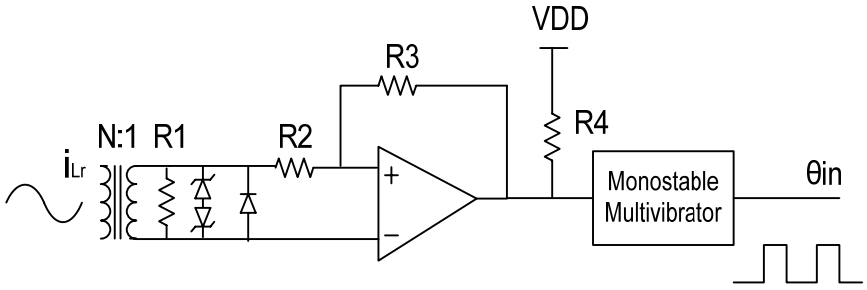


Figure 3-31. Circuit for reference signal generation

3.4.4. Simulation and experimental verification

The verification of the proposed PLL control was completed by simulation in Simplis and by experiment. The three-level parallel resonant converter was built using a scaled-

down version. The input voltage varies from 60V to 100V, and the load capacitor is charged to 1kV within half a second.

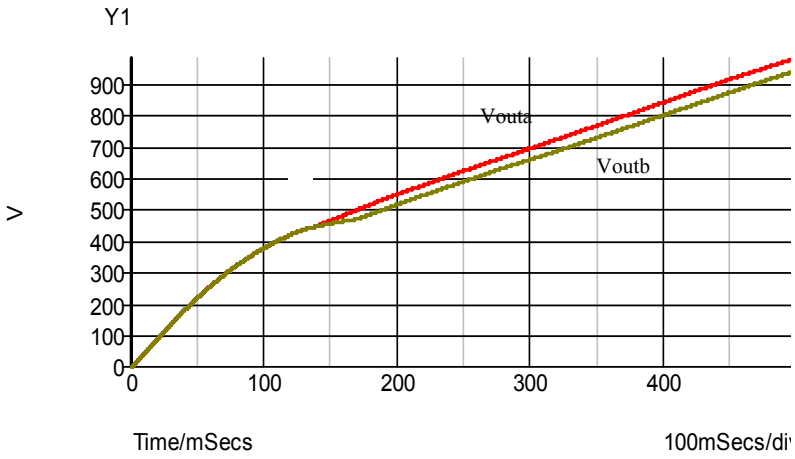


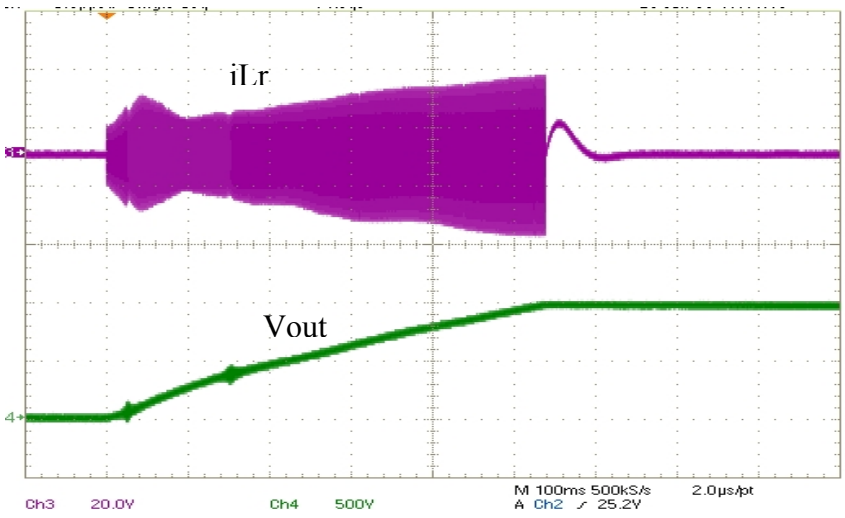
Figure 3-32. Simulated output capacitor voltage during charging: Vouta by PLL control and Voutb by output-voltage-based VFC.

Figure 3-32 shows that the load capacitor voltage with two control methods. V_{outa} in Fig. 3-32 increases smoothly with PLL control. However, V_{outb} with a sensed output voltage control has a low slope. Obviously, PLL control can deliver more power to the load while keeping ZVS operation when compared with the VFC method. In order to guarantee ZVS operation, the VFC needs a large margin for the switching frequency, which increases the varied switching frequency range and affects the efficiency. Therefore, VFC needs a longer time to charge the load at the target voltage and a wide switching frequency range.

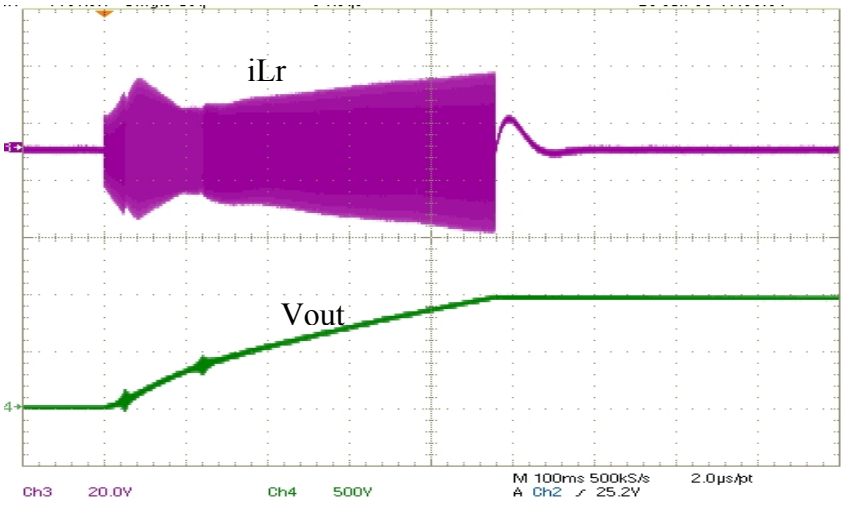
The advantage of PLL control is also verified by experimental results. Figure 3-33 shows the key waveforms of capacitor charging with these two control methods. The charging time with VCF control is 536 ms, while PLL control only needs 485 ms, which means that the PLL control can improve the converter power by around 10%.

The waveforms of ZVS operation at low Q and high Q are given in Fig. 3-34 and Fig.

3-35, respectively. During the transient charging period, the gate signals are stable at the setting phase shift, and V_{ds} is very clean because of ZVS operation achievement.



a



b

Figure 3-33. Key waveforms for capacitor charging (a) VCF method, charging time =536ms (b) PLL method, charging time=485ms.

Figure 3-36 shows the experimental waveforms of the control signals in the PLL control board. The control signal form the control board has no jitter and keep the stable leading phase shift.

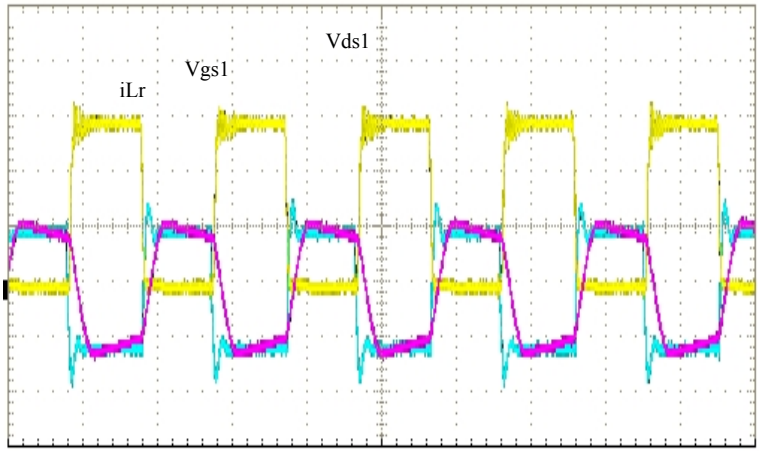


Figure 3-34. Resonant inductor current (iLr), Vds and Vgs of S1 switch at low Q. (10A/div, 10v/div, 10v/div, 5us/div)

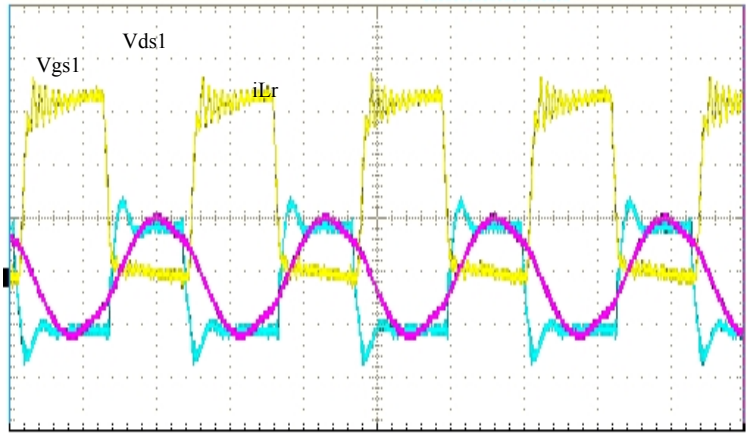


Figure 3-35. Resonant inductor current (iLr), Vds and Vgs of S1 switch at high Q. (10A/div, 10v/div, 10v/div, 2us/div)

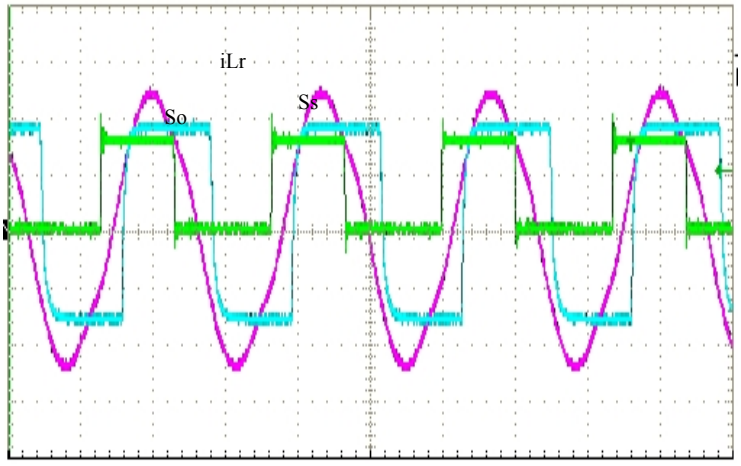


Figure 3-36. Resonant inductor current (iLr), measured current signal after zero-crossing detector (Ss), and the output signal of PLL (So) (10A/div, 5v/div, 5v/div, 2us/div)

3.5.Summary

The findings in this section can be summarized into three main conclusions:

The proposed NPS and PLL frequency-tracking control method for capacitor-charging three-level PRC can not only solve the problems inherent in the conventional control method, but can also improve the system efficiency and reduce the component stress. The theoretical analysis and experimental results demonstrate the advantages of the NPS control scheme over a conventional PS control scheme. With PLL frequency-tracking control, the capacitor charging converter can ensure ZVS operation and maximum power transfer during the transient capacitor charging period, even when the input voltage varies or resonant parameters change. The implementation of the PLL controller and the related issues have been detailed. The simulation and experimental results verify the control method and design. PLL method can improve the converter power by 10% compared with conventional VCF control method.

NPS operation mode is fully compared with PS operation mode. The analysis results can be extended to all three-level resonant converters when variable switching frequency control is used. NPS operation will improve these converters' power capability and efficiency and reduce the voltage stress on the main switches.

Capacitor charging with proposed charging profile is the perfect application for PLL. The detailed design procedure can be extended to other resonant converters for capacitor charging. The proposed control has a simple circuit configuration using low-cost components.

Chapter 4 Detection Method and Protection

Fault detection and protection is an important design aspect for any power converter, especially in high-power high-voltage applications, where cost of failure can be high. Furthermore, the margin for the system design is minimized for a high-power-density converter design. Any abnormal operation could be dangerous to the system, which urges the need of an effective fault detection and protection method. When the power density calculation is based on the whole system, any part in the system could damage the system power density if it is not optimized. Or the power density would be meaningless if the power density only calculated the main part or the converter was not unstable. Therefore, attention has been paid on the system detection and protection circuit design.

The three-level dc-dc converter and its varied derivatives are the attractive topologies in high-power high-voltage applications [B-1]-[B-12]. The main advantage of the three-level dc-dc converter is that the main switches only withstand half of the input voltage, so low–voltage-rating devices with better performance can be used.

However, everything has two sides. The three-level structure is subject to voltage unbalance [E-1], which can lead to damage to components and subsequent system failure. The reliable operation of a converter would require that the system operates stably at all times or the appropriate remedial action will be taken in time if a fault occurs. For a three-level converter, a protection is required against voltage unbalance, in addition to all the other conventional protection functions: over current protection, over/under output voltage protection and over/under input voltage lockout.

4.1.Introduction

Reference [E-1] has analyzed two possible conditions, at open voltage loop and light load, for the unbalanced voltage across the switches in the same leg, and introduced related solutions. However, Vcss could also be changed under other conditions, such as ZCS/non-ZVS operation, high voltage ripple on input capacitors, and unbalanced duty cycle. Furthermore, even in carefully designed circuits, faults can occur, resulting in system failure. One of real failures was captured in our laboratory, shown in Fig. 4-1. As the Figure 4-1 shows, the switch S1 suddenly has a short failure so that the other device S2 in the same leg with S1 has to withstand the full input voltage. Since no protection circuit can detect this fault, S2 finally failed after around 300us, as well as the other two switches in other leg.

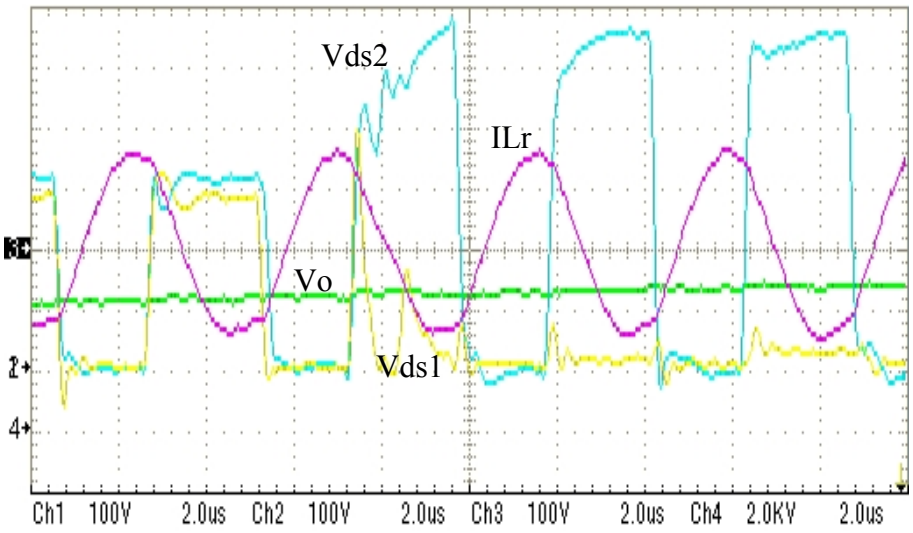


Figure 4-1. S1 fails to short without protection circuit. (Vds1 (100V/div),Vds2 (100V/div), Iin (100A/div), Vout (2kV/div), 2us/div)

[B-13] proposes a control circuit to balance the unsymmetrical duty cycle by monitoring voltage across the flying capacitor. However, this method can only keep the flying capacitor voltage equal to half of the input voltage when the duty cycles are

slightly unbalanced. This proposed control circuit which is based for DC-DC converters with non-phase leg structure, such as buck, boost, can not be used in the DC-DC converter based on phase leg structure. The implementation circuit will be very complex if the control tries to use flying capacitor voltage to adjust the unbalanced duty cycles. In addition, again, this method still can not eliminate the unbalanced voltage stresses in three-level structure, not to mention the uncontrolled faults.

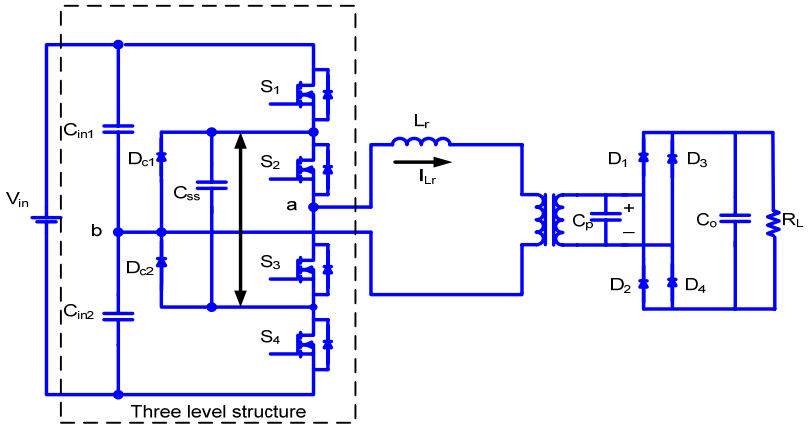


Figure 4-2. Topology of three-level parallel resonant converter.

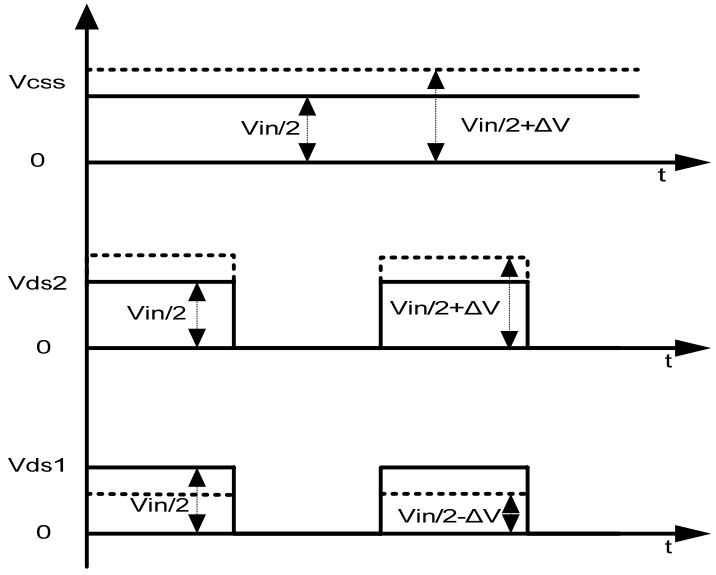


Figure 4-3. Unbalanced voltages across the switches. (S1 voltage stress (Vds1), S2 voltage stress (Vds2) and Vcss).

While there have been previous studies on the protection of three-level inverter or other types of dc-dc converters [E-2]-[E-11], these methods either are very common protection circuits for various types of converters or only partially work for certain topologies or applications; no study has been conducted specially for the protection of three-level dc-dc converters.

The concept of [E-3] for inverter protection based on neutral point voltage detection can to be applied to three-level dc-dc converter. But only limited problems can be detected by the neutral point protection. For example, the inner switch will suffer full input voltage if it turns off before outer switch in the same leg while the neutral point voltage is normal. Furthermore, the neutral point detection is less sensitive to faults due to the relatively large input capacitance compared with flying capacitance.

The proposed novel protection method is based on the detection of voltage across the flying capacitor (Vcss), shown in the Figure 4-2.

The flying capacitor is initially introduced to decouple the charging and discharging sequence of the switch paralleled capacitors for phase shift operation, which also can clamp the inner switches' voltage stress. The voltage across the flying capacitor is equal to the half of the input dc voltage in normal three-level converter operations. However, the three-level structure is subject to voltage unbalance. Figure 4-3 shows the Vcss and the imbalance of the switches' voltage stress. The solid lines indicate the voltage stresses of switch S1 and S2 when the flying capacitor has a normal voltage, which is half of the input voltage. The dotted lines indict the voltage stresses of switch S1 and S2 when the flying capacitor suffers abnormally high voltage ($V_{in}/2+\Delta V$). The voltage stress of the inner switch S2 (Vds2), which is clamped by the flying capacitor, also increases to

$V_{in}/2+\Delta V$; while the voltage stress of the outer switch S1 decreases to $V_{in}/2-\Delta V$. Due to the symmetrical structure, the other two switches, S3 and S4, should have complementary waveforms. If the unbalanced voltage stresses on the switches become worse, the switch with high voltage stress may fail due to over-voltage.

The advantages of the proposed protection scheme based on flying capacitor voltage include:

1) No additional components on the power stage are used, not even additional current sensors; therefore there is no impact on normal converter operation and performance.
2) Sensitive to unbalanced voltage stress and detectable for multiple faults.
3) Fast response time (e.g. ≈0.7 μs in the converter designed for shoot-through fault).
4) Low cost and easy to implement.
5) Able to replace under/over input voltage lockout.

4.2.Unbalance voltage stresses due to abnormal operation

Reference [E-1] has analyzed two possible conditions, at open voltage loop and light load, for the unbalanced voltage across the switches in the same leg, and has introduced related solutions. However, Vcss could also be changed under other various conditions, such as ZCS/non-ZVS operation, high voltage ripple on input capacitors, unbalanced switching timing, etc. In essence, these can be fixed when the problem is stopped by protection and located. The solutions to the issues are introduced. A thoroughly analysis on the abnormal conditions is necessary for designers to understand the converter operation and know the limits so that a protection can be designed to tolerate to normal operation without losing sensitivity. These abnormal conditions can be classified into three main categories discussed below.

4.2.1. Abnormal input capacitor voltages due to input voltage

As shown in Fig. 4-2, two input capacitors (Cin1 and Cin2) are needed to split the input voltage equivalently. Thus the neutral point, Point b in Fig. 4-2, has half of the input voltage ($V_{in}/2$). So the neutral point voltage and Vcss are fundamentally determined by the input voltage. If the input voltage varies beyond the allowed range, obviously, the over/under input voltage lockout can be triggered by monitoring the Vcss. The voltages across the two input capacitors keep same when input voltage is abnormal, too high or too low.

4.2.2. Abnormal input capacitor voltages due to unbalanced neutral point voltage

Another main abnormal performance of input capacitor voltages is unbalanced voltages. When the voltage across Cin1 is higher than $V_{in}/2$, the flying capacitor will be charged through down clamping diode Dc2, shown in Fig. 4-4. If the Cin2 voltage is higher than $V_{in}/2$, the flying capacitor will be charged through clamping diode Dc1, shown in Fig. 4-5. More explicitly, the flying capacitor will be paralleled with the input capacitor which has high voltage stress. It should be noted that this is also why the flying capacitor helps to alleviate the voltage unbalance of the input capacitors mentioned in [B-8]. No matter which input capacitor has higher voltage, or, in other words, no matter the neutral point has higher or lower voltage than $V_{in}/2$, the flying capacitor voltage will be charged to the peak voltage of the input capacitor, which has higher voltage stress. So unequal capacitances of input capacitors, unbalanced duty cycles or mismatched switching timings, etc. belong to this case, which contributes the unbalanced input capacitor voltages and then the abnormal flying capacitor voltage. When the problem is caused by these issues, it is can easily solved in circuit. Normally these tiny unbalanced

capacitances and duty cycles can be tolerated without serious consequence. In addition, the unbalanced duty cycles can be alleviated by the flying capacitor in phase shift operation. [B-13] proposes a control circuit to balance the unsymmetrical duty cycle by monitoring voltage across the flying capacitor for non phase leg structure, such as buck, boost by mentoring the Vcss, by monitoring Vcss. It also can be adjusted for the circuit with phase leg structure by when the unbalanced duty cycle is an issue.

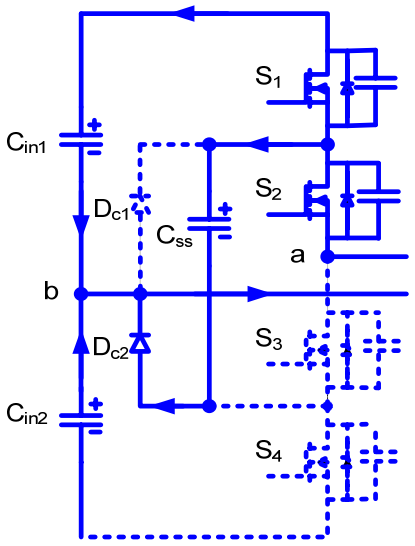


Figure 4-4. Charging loop when the voltage of Cin1 is higher than half of the input voltage.

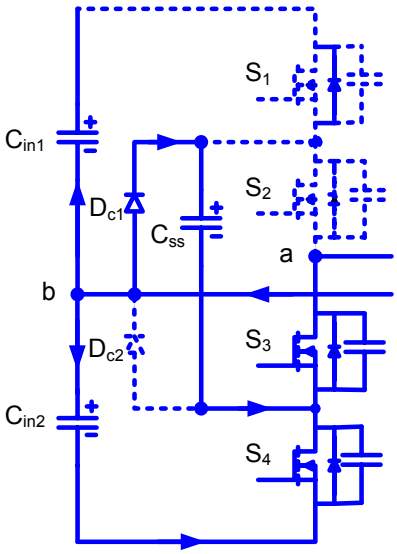


Figure 4-5. Charging loop when the voltage of Cin2 is higher than half of the input voltage.

Moreover, even if the voltages across the input capacitors are balanced, the Vcss still can be influenced by the voltage ripple on the input capacitor. According to the above analysis, the peak voltage on the input capacitor will pump energy to the flying capacitor, thus, Vcss is can be calculated with equation (4-1):

$$V_{css} = \frac{(1+k)}{2} V_{in} \tag{4-1}$$

where V_{in} is the input voltage, and k is the allowed voltage ripple percentage for input capacitors, which usually is determined by equation (4-2). This can explain why the Vcss

increases slightly even in a normal operation.

$$k = \frac{C_{in} \cdot I}{f_s \cdot V_{in}} \cdot 100\% \tag{4-2}$$

Where C_{in} is one of input capacitors, I is the average current through the input capacitor in half of the switching cycle, f_s is the switching frequency and V_{in} is the input voltage.

4.2.3. Losing discharging loop even with normal input capacitor voltages

Even if the neutral point voltage is normal, the unbalanced voltage stresses still can happen in some conditions. The flying capacitor can be charged through upper claming diode (Dc1) or S1. Due to the symmetrical structure, it can be charged through bottom claming diode (Dc2) and S4. The only discharging loop is S2 or S3.

With the conventional phase shift control (S1 is turned off before S2, and S4 is turned off before S3), the commutation of the phase shift provides a discharge loop for flying capacitor when ZVS operation is desired. However, when the converter loses ZVS, such as at light load; or the switching timing is wrong, such as when S2 is switched off before S1 or S3 is switched before S4; the flying capacitor voltage will be charged to instead of discharging. The Vcss could increase to approximate the input voltage due to losing discharging loop. Fig. 4-6 shows an abnormal case of accidental ZCS operation mode. The current in the inductor has changed its direction when S1 is turned off. The upper side of the flying capacitor is connected with the input voltage through the body diode of S1. And the bottom side of the flying capacitor is connected with the ground when S4 is turned on after S1 is off. In this case, the flying capacitor will be charged to full input voltage instead of discharging. Due to the symmetrical structure, this case can happen when S4 is turned off. At light load, if the converter loses the ZVS operation for lagging switch, or even worse, loses ZVS for both leading switch and lagging switch, the

mechanism is the same as ZCS condition. In order to solve this issue, ZVS has to be guaranteed in three-level converter design for all of its operation conditions, from heavy load to light load.

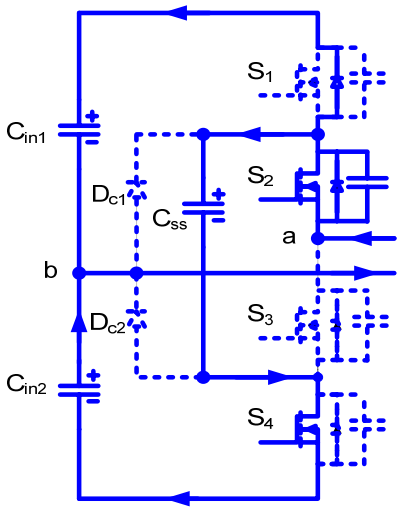


Figure 4-6. Charging loop for wrong operation mode of ZCS.

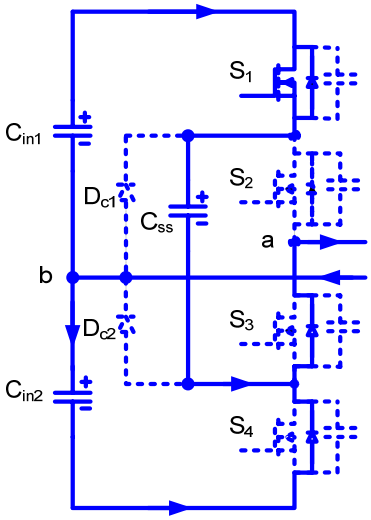


Figure 4-7. Charging loop for reverse switching timing.

Figure 4-7 shows another case of reverse switching timing. When S2 is turned off before S1, the upper side of the flying capacitor is connected to the input voltage through S1 and the lower side of the flying capacitor is connected to the ground through the body diode of S4. Thus the flying capacitor suffers the full input voltage. One simple solution is enlarging the phase shift between the switches in same leg. [E-1] proposes another effective way to this problem by paralleling external capacitors in the inner switches so that the inner switch will turn off later due to its increased switching time.

To some extent, the fault condition is the worst case of these abnormal conditions. For example, when S2 fails to open, it is like avoiding the rule that S2 should be turn off no earlier than S1.

4.3.Multiple detectable faults by V_{css}

System failures caused by active device failure are most common, such as when the components undergo thermal runaway, there is noise interference on the controller, the components are defective, etc. The unpredicted noise interference which becomes worse in high-power operation can be a converter killer. The noise could even completely interrupt the controller performance, and then generate the wrong switching signals. Because of the features of three-level structure, the failure of one of the switches usually initiates the failure of all the rest of the switches. In addition, System failures also could happen in some circumstances, such as component voltage broken down, magnetics saturation, shirt/open load etc.

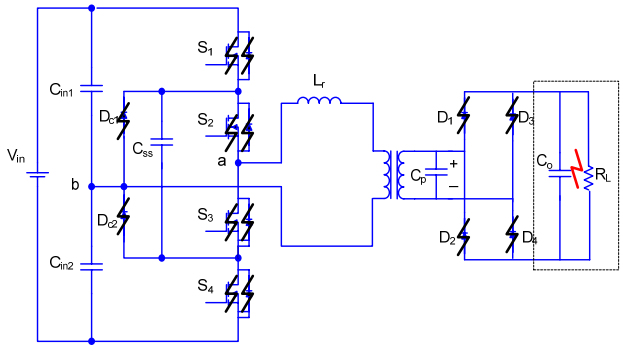


Figure 4-8. Possible faults on the three-level parallel resonant converter

Figure 4-8 shows the most common faults associated with active device failure and open/short load cases. Each device can fail to open circuit or short circuit. This study covers the open/short failure of the two switches in the same leg, S1 and S2, one clamping diode (Dc1), and one rectifier diode (Dr1), as well as short/open load (SL/OL). Since the results of the short circuit case of body diodes should be the same as the short circuit case of their main switches, only the open cases of the body diodes (D1 and D2) of switch S1 and S2 are included. Due to the symmetrical structure, the results will be the

same as the counterpart failures occur. To some extent, the fault condition is the worst case of these abnormal conditions. For example, when S2 fails to open, it is like avoiding the rule that S2 should be turn off no earlier than S1.

A. Outer Switch Open

If outer switch (e.g. S1) has an open circuit, the loop is still complete for inductive load current so that the energy in the bottom input capacitor, Cin2, is continuously transferred to load when S3 and S4 are on. However, when S3 and S4 are off and S2 turns on, the upper input capacitor (Cin1) will be isolated because the upper claming diode (Dc1) will provide the short circuit loop for the inductor current, shown in Fig. 4-9. But the energy in the bottom input capacitor, Cin2, will gradually discharge to zero, as does Vcss. The transformer will be saturated soon due to negative biased DC voltage stress.

B. Outer Switch Short

If S1 has a short circuit, the flying capacitor will be directly connected with input power source when S3 and S4 are on. Vcss is equal to full input voltage, as does S2. But the neutral point voltage won't be influenced by this fault.

C. Inner Switch Open

If S2 has an open circuit, Vcss also increases to full input voltage soon. This reason is not as obvious as last case, S1 short circuit case. But the mechanism is the same, i.e. both violate the rule that S1 has to turn off before S2 turns off. When S2 fails to open, it means that S2 always turns off before S2 turns off. The Vcss increases to full input voltage by the through the S1 and the body diodes of S3 and S4, shown in Fig. 4-10. But the neutral voltage, Vb, almost keeps normal value. The converter will stop delivering power to the load with this fault.

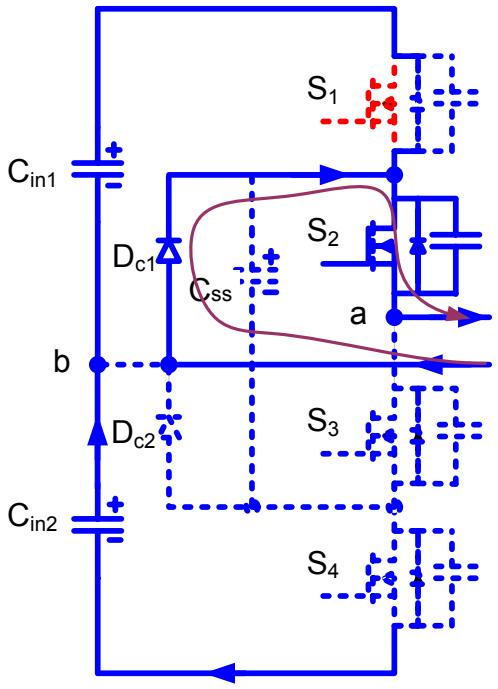


Figure 4-9. S1 has an open circuit when S3 and S4 are off.

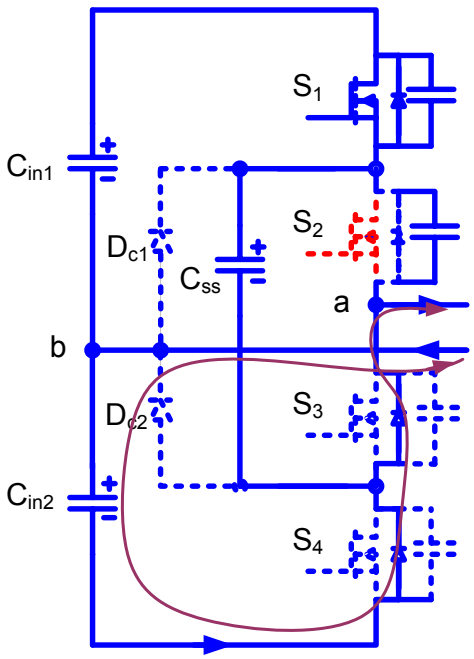


Figure 4-10. S2 has an open circuit when S1 is on.

D. Inner Switch Short

If S2 has a short circuit, when S3 and S4 turn on, the flying capacitor will be shorted through S2, and S3 and the bottom input capacitor Cin2 will be shorted through upper claming diode, S2, S3 and S4, shown in Fig.4-11. Meanwhile, S1 has to withstand full input voltage. When S3 and S4 turn off, the fault doesn't effect converter operation as usual and the flying capacitor and Cin2 will be charged back to half of the input voltage. Hence, the Vcss and neutral point voltage are pulses from zero to half of the input voltage with the same frequency as switching frequency. The transformer will be saturated soon due to the positive biased voltage stress.

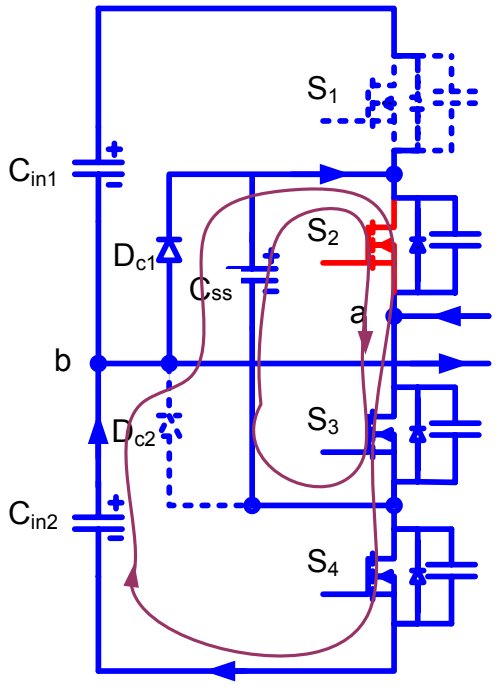


Figure 4-11. S2 has a short circuit when S2 and S4 are on.

E. Outer Switch Body Diode Open

If the switch S1's body diode D1 fails to open, this fault doesn't have any effect on the converter operation. As the Fig. 4-12 shows, when S4 turns off and S3 is still on, the inductor current will go through the bottom claming diode back to the resonant tank instead of D1 after the S4's switch capacitor is charged to half of the input voltage and S1's switching is discharged to zero. Even if it is good, the D1 will never be conducted or involved in any commutation. The system is never affected by this fault. Certainly, this fault is undetectable by Vcss.

F. Inner Switch Body Diode Open

If the switch S2's body diode D2 fails to open, the converter can work when the S1 and S2 are on. When the S3 turns off after S4 turns off, the inductor current start the charge the S3' switch capacitor and discharge the S2's switch capacitor. But the inductor current

has no way to go after the S3's switch capacitor are charged to half of the input voltage and S2's switch capacitor are discharged to zero due to the open circuit of D2, shown in Fig. 4-13. Therefore S3 will suffer high voltage spike in this fault case. But the Vcss keeps normal value. The protection can not detect this fault unless the noise caused by high voltage spike triggers the protection. It is possible in practical high power converter due to the high abnormal noise when ZVS is lost.

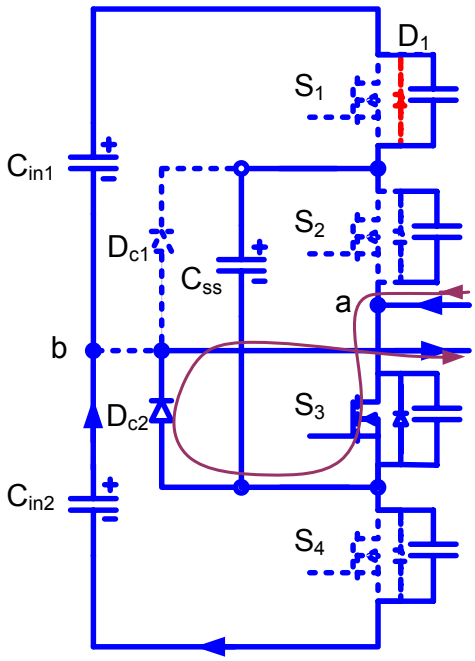


Figure 4-12. D1 has an open circuit when S4 starts to turn off while S3 is still on.

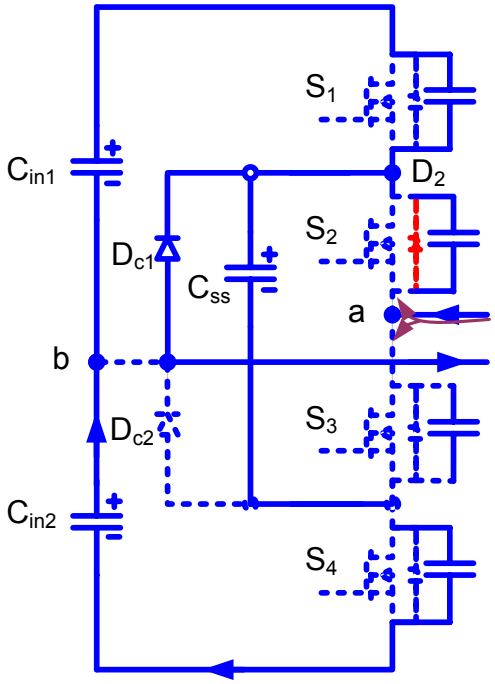


Figure 4-13. D2 has an open circuit when S3 and S4 turn off.

G. Clamping Diode Open

If the claming diode Dc1 fails to open, the converter ideally works as normal. But the converter will practically lose the advantages of the three-level structure without claming diode. As long as the switch's voltage stresses are not balanced, this fault can be detected by Vcss.

H. Clamping Diode Short

If the clamping diode Dc1 fails to short, the neutral point voltage will be connected with the positive polarity of the input voltage and charged to full input voltage when S1 is on, so does flying capacitor. Meanwhile, the transformer suffers negative DC bias voltage.

I. Rectifier Diode Open

If the rectifier diode Dr1 fails to open, no more energy will be transferred to load when the resonant capacitor voltage is positive. But the converter keeps transferring the energy to the load when the resonant capacitor is negative. This imbalance energy transfer will result in positive DC biased voltage stress to the transformer. The neutral point voltage will decrease to zero while the Vcss increase to the full input voltage. It should be noted that the neutral point voltage will gradually increase if the rectifier diode in opposite bridge is open while the Vcss still increases.

J. Rectifier Diode Short

If the rectifier diode Dr1 fails to short, the resonant capacitor will be shorted when the polarity of the resonant capacitor voltage is negative. So more energy can be transferred to the transformer secondary side when S3 and S4 are on than when S1 andS2 are on. It follows that the neutral point voltage gradually decreases and flying capacitor voltage increases. Same as Dr1 open fault case, the neutral point voltage will gradually increase if the rectifier diode in opposite bridge is short while the Vcss still increases.

K. Open Load

If open load happens, the output voltage will increase significantly due to the PRC inherent boost property. But the converter will operate normally except for high current when the switching frequency is higher than resonant frequency. Otherwise, the converter

will lose ZVS operation and the fault will be found with the increased Vcss.

L. Short Load

If short load happens, the converter still keeps ZVS mode due to PRC property. Theoretically it can not be detected by Vcss. But the turn-off current which depends on the switching frequency will increase due to the triangle current waveform. High voltage spike due to the high turn-off current still may practically trigger the protection with Vcss detection. It should be noted that the response of Vcss to open load and short load in this paper may vary in other three-level topologies because the inherent properties of PRC is dominated in these faults.

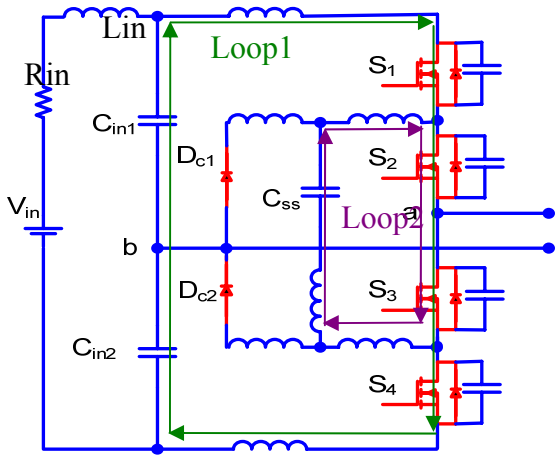


Figure 4-14. Current loops as shoot-through occurs.

Of all the possible contingencies, the protection against shoot-through is the trickiest one, and is much depended on the parasitic inductance. Obviously, the voltages of input capacitors and flying capacitors are equal to the half of the input voltage without any parasitic inductance, even during a shoot-through fault. However, the three-level structure is specially designed for high-power high-voltage applications. The parasitic inductance is not negligible, but relatively large. Figure 4-14 shows two current loops during the

initial time of shoot-through. In order to simplify the analysis, the following assumptions are made:

- ✓ The output inductance (L_{in}) of the power supply is larger or at least comparable to the parasitic inductance in Loop 1 shown in Fig. 4-14.
- ✓ The capacitance of the input capacitors is much larger than the flying capacitor.
- ✓ The inductance in Loop 1 is much larger than the inductance in Loop 2 due to the definitely large loop area.

For high-power high-voltage applications, the above three assumptions are reasonable in most cases. Based on the above assumptions, Figures 4-15 and 4-16 show the equivalent circuits of each current loop, where each kind of component is lumped into one component. The wire resistance can be integrated into the device on-resistance, and the current from the power supply is neglected during the initial occurrence of shoot-through.

$$R_1 = 4 \cdot R_{dson} \tag{4-3}$$

$$R_2 = 2 \cdot R_{dson} \tag{4-4}$$

$$V_1 = I_1 \cdot (2 \cdot R_{dson}) \tag{4-5}$$

where R_{dson} is on-resistance of each one device, and I_1 can be solved through the LCR circuit in Figure 4-15. Therefore, the Vcss drop rate of can be estimated by solving the equivalent circuit shown in Fig. 4-16. For the prototype in this dissertation, the Loop1 inductance is around 200 nH and the Loop2 inductance is around 40 nH. For the purpose of shoot-through detection, the smaller flying capacitance means shorter detection time; however, this also means more sensitivity to noise. So the trade-off between the noise immunity and fast detection time is needed. Considering the 10 μs short circuit

endurance time for IGBTs and the better short circuit endurance of MOSFETs [E-12], the detection time is not an issue based on the test, which is short enough to allow the controller to take related protection actions.

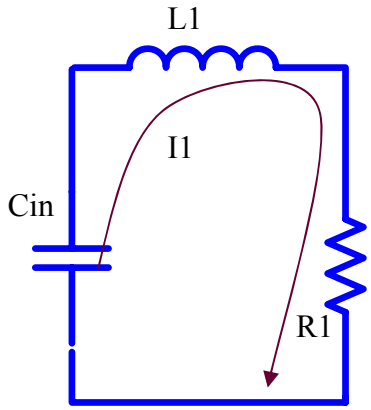


Figure 4-15. Equivalent circuit for current Loop 1.

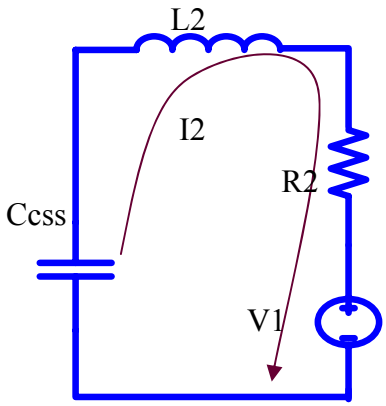


Figure 4-16. Equivalent circuit for current Loop 2.

The analysis is verified with simulation in Saber. A three-level parallel resonant converter shown in Fig. 1 runs with phase shift mode at 200 kHz. Each switch operates at nearly 50% duty cycle. The 600 input voltage is increased to 10kV load voltage with turns-ratio of 11 and boost property of PRC. The simulation results are summarized in Table I where the abbreviations ov and oc are used to indicate the over-voltage and over-current. The phenomenon of Vcss may vary slightly with different three-level topologies and operation schemes due to the PRC characteristics. It should be noted that the undetectable cases mean the voltage stresses are balance based on the simulation with symmetrical parameters. Except the fault case of D1 open, all of the other detectable cases will finally cause unbalanced voltage stresses, and then detected by Vcss.

TABLE 4-I. FAULT CASE STUDY WITH PHASE-SHIFT THREE-LEVEL PARALLEL RESONANT CONVERTER

Device / Fault Case	S1	S2	S3	S4	Dc 1	Dc 2	Results
S1 Open	ov				oc		*Vcss=0 gradually
S1 Short		ov	ov				*Vcss=Vin

Device / Fault Case	S1	S2	S3	S4	Dc 1	Dc 2	Results
S2 Open		ov	ov				*Vcss=Vin
S2 Short	ov		ov		oc	oc	*Vcss=0,Vin pulse
D1 Open							***No serious consequence
D2 Open		ov	ov				***S2 lose ZVS, S3 suffers huge voltage spike, Vcss=1/2Vin
Dc1 Open							***Have potential serious consequence*
Dc1 Short		ov	ov				*Vcss=Vin
Dr1 Open		ov	ov				*Vcss=Vin
Dr1 Short		ov	ov				*Vcss=Vin, OC for the other three rectifier diodes
OL	oc	ov oc	ov oc	oc			**Vcss=Vin if switching frequency is higher than resonant frequency, but Transformer secondary side components suffer high voltage.
SL							***Have potential serious consequence
* Detectable case		**Possible detectable case					***Undetectable case

Figures 4-17 and 4-18 show the simulation results with varied inductances of input parasitic inductor (Lin) and varied capacitances of flying capacitor (Css). The input current has two peaks when shoot-through happens. The first peak is determined by the loop 1 resonance and the second peak is determined by the resonance of Lin and Loop1. Vcss drops to zero in 0.5 μs in Figure 4-17. Even with 100 nH Lin, the second peak comes after around 4 μs which is long enough for Vcss detection. The Vcss detection time is influenced by the Css shown in Figure 4-18. However, it is still fast enough to detect the fault within 10 μs. Though [E-12] mentions the MOSFET short-circuit capability, further study on the MOSFET short-circuit behavior and capability is needed.

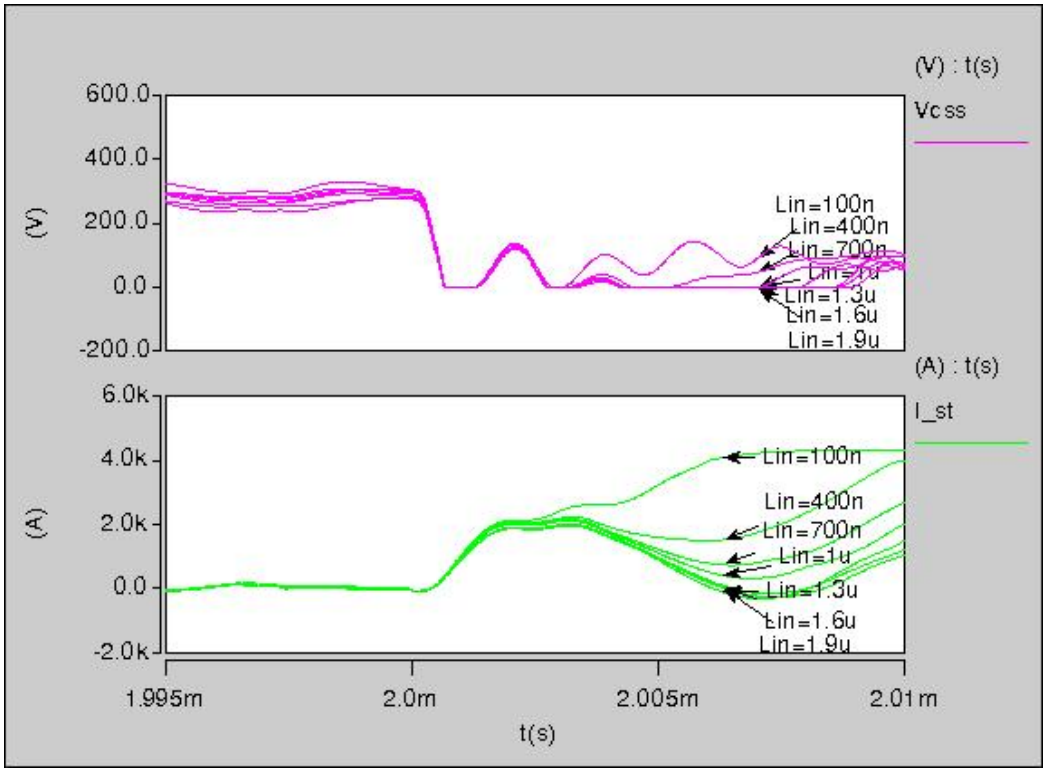


Figure 4-17. The Vcss and input current when shoot-through happens with varied inductance of input inductor (Lin.)

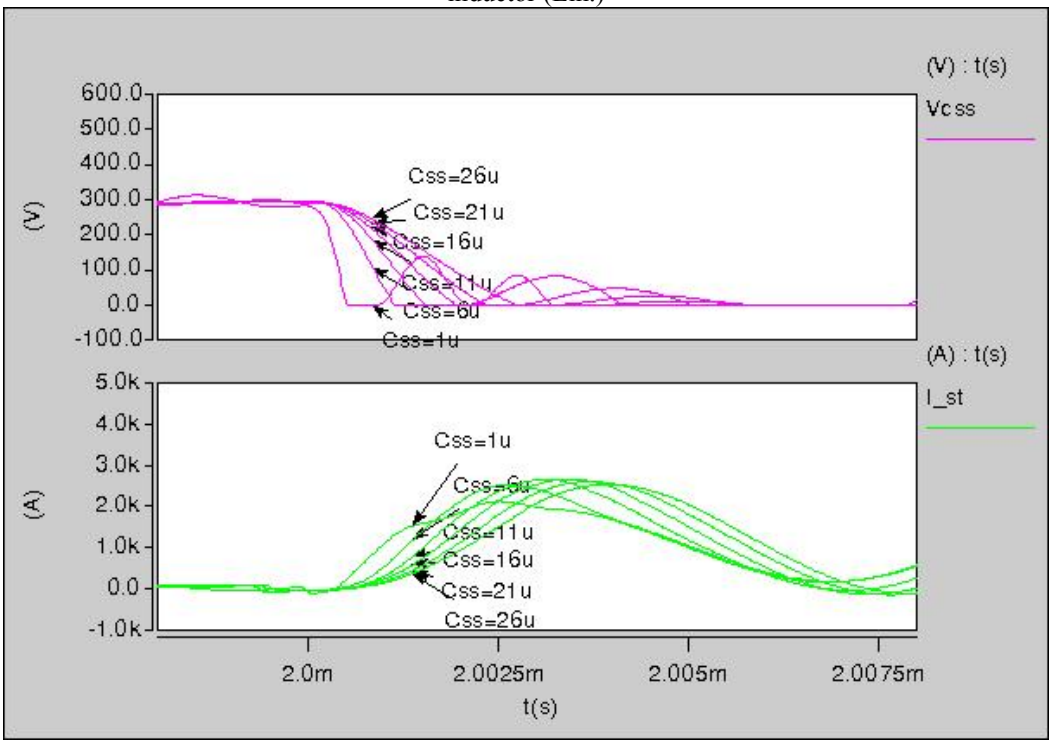


Figure 4-18. The Vcss and input current when shoot-through happens with varied capacitance of flying capacitor (Css).

4.4.Design and characteristics of proposed protection circuit

For three-level structures, balance resistors are needed for the capacitors' voltage balance before the converter starts to operate. Figure 4-19 shows the connection of balance resistors. R_1 and R_2, R_3 and R_6 are equal respectively. In order to have half the input voltage, the sum of R_4 and R_5 is equal to the sum of R_3 and R_6. For a protection circuit, R_4 and R_5, with appropriate resistance, can be used as a voltage divider for the sensor of Vcss. The schematic of the proposed protection circuit is shown in Figure 4-20. The sensed voltage is processed by a window detector with an isolated auxiliary power supply. Thus only a digital signal is transferred to the system controller through a high-speed optocoupler.

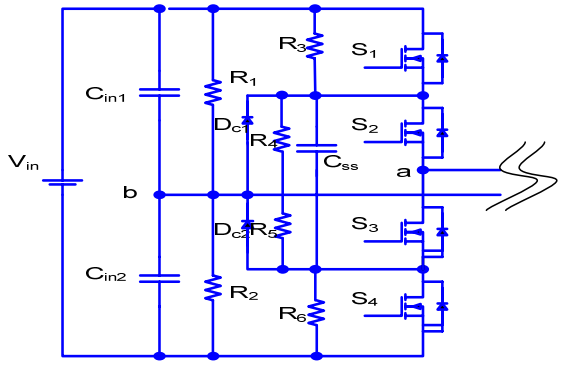


Figure 4-19. Three-level structure with balance resistors.

A. Flying capacitor design

Though flying capacitor design is not directly related with the protection circuit design, the proposed protection method has to be based on flying capacitor. In the conventional three-level converter with phase-shift control, the functions of the flying capacitor can be defined as follows:

1. decoupling the switching transitions of S1 and S4,S2 and S3;

2. balancing the unbalanced voltages between the two input capacitors
3. acting as a snubber capacitor for inner switches,S2 and S3.

The decoupling effect is depended on the ratio of capacitance, shown in equation (4-6)

$$\frac{V_{css}}{V_{sw}} = \frac{C_{ss}}{C_{sw}} \tag{4-6}$$

where V_{sw} is the minimum left voltage of any one of switches when its gate signal is becoming high during switching transition. ZVS is achieved when V_{sw} is near zero. C_{ss} is the capacitance of flying capacitor. C_{sw} is the sum of the capacitance of switch capacitor and any external paralleled capacitor. For better decoupling and voltage clamping effect, the capacitance of the flying capacitor should be no less than the calculated number with equation (4-6).

According to the above analysis, the problems cannot be solved by simply removing the flying capacitor. However, these problems can be detected by the flying capacitor. Even if a phase shift control scheme is not employed and the flying capacitor is not necessary, the flying capacitor can still be added as a snubber capacitor and work for the proposed protection circuit.

B. Design criteria

The Vcss is determined by the input voltage in steady-state operation. As the converter is running, the Vcss is mainly influenced by the voltage ripple of the input capacitors. Due to the clamping diode, the flying capacitor can be charged to the maximum voltage of the input capacitors, while the normal minimum Vcss is equal to the half of the low-line input voltage. So the high and low reference voltages have different considerations, and are expressed by (4-7) and (4-8).

$$V_{ref\_H} = \frac{(1+k\%)}{2 \cdot n} V_{in\_high} \tag{4-7}$$

$$V_{ref\_L} = \frac{V_{in\_low}}{2 \cdot n} \tag{4-8}$$

where V_{in_high} and V_{in_low} are the high input voltage and low input voltage, respectively; k is the percentage of the voltage ripple of the input capacitor; and n is the ratio of the R_4/R_5 voltage divider. Due to the high response time requirement and the large resistance of voltage divider, it is recommended not to put a capacitor on the input of the comparator. To avoid a false trigger, the filter capacitor can be connected on the output of optocoupler.

Limited by the three-level structure, when a fault occurs in one device, generally the remaining devices will be subject to the full input voltage. Leaving the device with a 100% margin of voltage rating is preferred for reliability and the feasibility of protection against faults. As manufacturers are continuously improving on the devices' ruggedness, it is reasonable to suppose that the devices have a chance to survive some of faults if the protection circuit can response fast enough, even with less voltage margin.

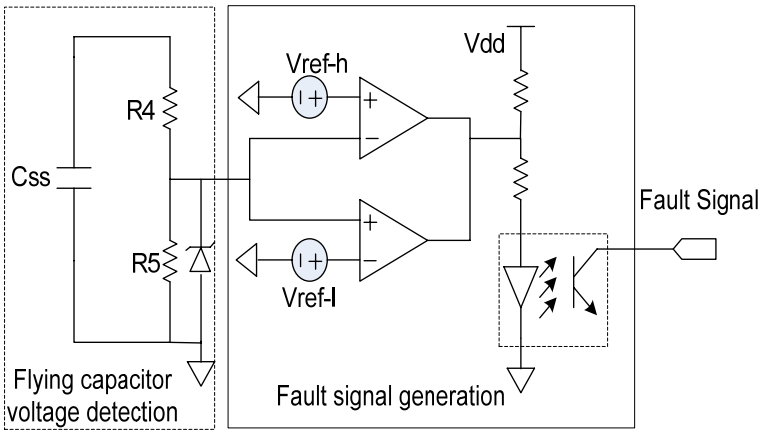


Figure 4-20. Detection circuit through monitoring Vcss.

4.5.Features of the proposed detection method and its extension

4.5.1. Features of proposed detection method

The proposed protection circuit does not need any additional components on the power stage circuit. The detection circuit is very simple and fast. The only delay time is caused primarily by the comparator and optocoupler, and this delay can be greatly reduced when high-speed components are used. The main purpose of the protection circuit is to prevent the serious results that can occur when unbalanced voltage stress on the switches is detected in a three-level structure due to charge accumulation on the flying capacitor. Besides this function, the input under/over voltage lockout can be replaced by the Vcss diction circuit.

Based on the analysis by simulation, the varied active devices' failures may be detected by the proposed detection circuit in time. The fast response time makes it possible for possible remedial actions against faults, though the effective remedial actions in various fault cases needs further study. For example, a soft shut-down is needed to avoid voltage overshoot in a shoot-through fault.

According to the above analysis, the new detection method obviously shows advantages, including stability against noise, fast response time, high efficiency, ease of implementation, and low cost. Due to the serious results of shoot-through, several different current detection methods are developed for shoot-through, e.g. use of a fuse, shunt resistor, current transformer, Vce detection, etc. Vce detection is used for IGBT protection, also called "desaturation detection". For MOSFETs, the comparable method is "Vdson detection". In the following analysis, Vce detection is indicated for both IGBTs and MOSFETs. The first three sensing methods induce an external component into the

power stage. The advantages and disadvantages of each method are well detailed in [E-13]. Hence, only the comparison between Vce detection and Vcss detection is summarized in Table II. Excluded from this table are the common properties of these two methods, such as fast response time, no lossy components needed, non-isolated with power stage, etc. Both perform well when the detection time is fast enough to allow enough time for protective action. Undoubtedly, Vcss detection has a lower cost without a complex circuit.

It should be noted that the conventional driver IC has built-in short circuit protection, which can directly shut down the device with the least delay time. Nevertheless, the first off switch will withstand the full input voltage, which has the potential to damage the device due to the high voltage. A system turn-off signal is necessary to synchronously turn off all of the switches as faults occur.

Table 4-II. PROPERTIES OF VCSS DETECTION COMPARED WITH VCE DETECTION

	Advantages	Disadvantages
Vcss Detection	✓ Less noise interference due to the DC signal ✓ No extra delay and logic signal process to extract the device on-state ✓ Simple circuit on detection	✓ Only for shoot-through protection. No accurate current value measured. ✓ Depends on practical parasitic inductance.

4.5.2. Application extension of proposed detection method

The conventional three-level structures combined with PWM converters or resonant converters are introduced for different applications. And varied derivatives of the three-level structure are developed to overcome the limitations of conventional structure, such as enlarging the ZVS achievement range, achieving the soft-switching in secondary rectifier bridge, etc., [E2]-[E12]. But all of the topologies keep the original advantage of a

thee-level structure, having the main switches withstood half of the input voltage stress. The flying capacitor voltage keeps half of the input voltage if it is added. So the proposed protection method can be extended to other three-level dc-dc converters.

4.6. Experimental verification

One of the real failures was protected by the proposed protection and captured in our laboratory, and is shown in Fig. 4-21. The three-level parallel resonant converter was designed to supply 30kW with 600V dc input voltage and 200 kHz switching frequency. 600V voltage rating MOSFET modules are used as main switches. As Fig. 4-21 shows, due to the transformer high voltage broken down, the converter can not achieve ZVS suddenly. The voltage stress of the inner switch, S3, immediately increases and is higher than the voltage stress of the outer switching, S4, which can be clearly observed in Fig. 4-21. Based on previous analysis, the flying capacitor voltage is also abnormally increased. Therefore, the proposed protection is triggered and protects the converter against system failure. Note that as the transformer is broken down, the resonant capacitor voltage is discharged to zero. Therefore, the current waveform becomes triangle waveform after one cycle. In order to verify the analysis and the feasibility of the proposed circuit, the scaled-down experiment operates with $1/10^{th}$ the input voltage and same prototype.

Figures 4-22 to 4-26 show the five selected faults respectively: S1 short, S1 open, S2 short, S2 open and shoot-through. The experimental results are consistent with the simulation analysis. As S1 fails to open, as shown in Fig. 4-22, the freewheeling current of resonant current flows through the clamping diode Dc1 and discharges the flying capacitor; thus Vcss gradually decreases. Finally the Vcss reaches the predetermined low voltage limit and triggers the protection circuit. However, the clamping diode Dc1 has to

withstand high conduction current as the fault of an open S1 occurs. Other than the open S1 case, the Vcss varies sharply and the converter is shut down promptly as the fault occurs. The fastest response time is around 700 ns in this repeatable experiment for shoot-through fault.

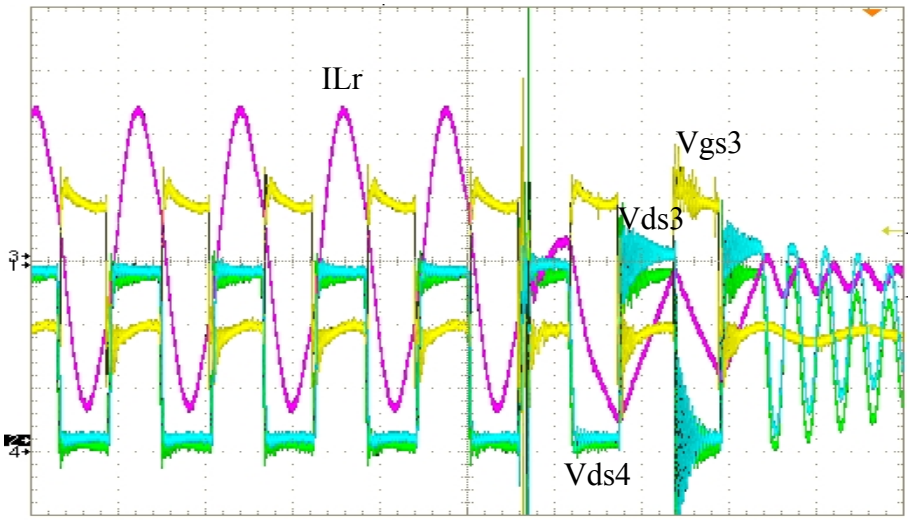


Figure 4-21. Abnormal waveforms when transform primary winding and secondary winding are voltage broken down.(Vgs3 (10 V/div),Vds3 (100 V/div), ILr (100 A/div), Vds4 (100 V/div), 2 us/div)

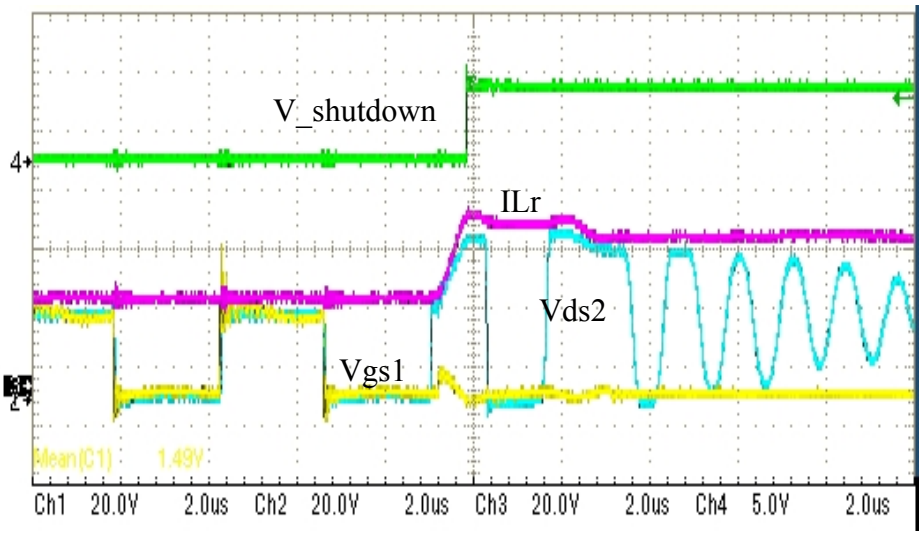


Figure 4-22. Protection circuit against S1 short case (Vds1 (20 V/div), Vds2 (20 V/div), Vcss (20 V/div), Vshutdown (5 V/div), 2 us/div)

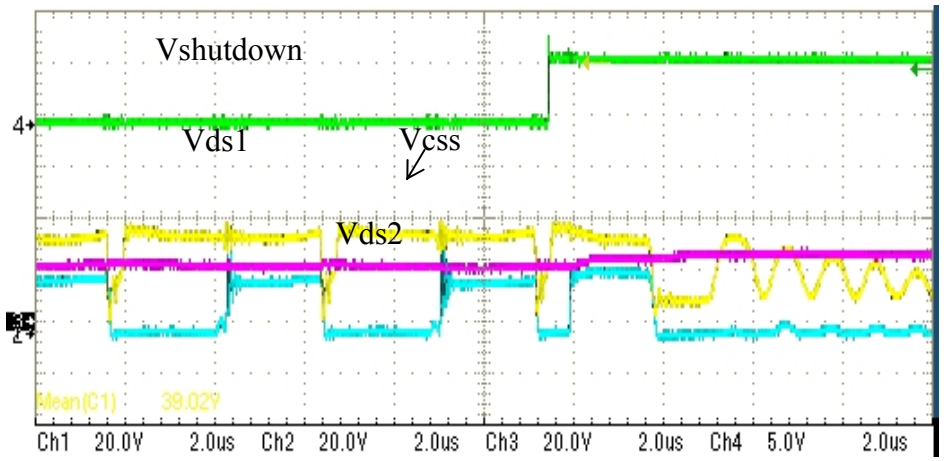


Figure 4-23. Protection circuit against S1 open case (Vds1 (20 V/div), Vds2(20 V/div), Vcss (20 V/div), Vshutdown (5V/div), 2 us/div)

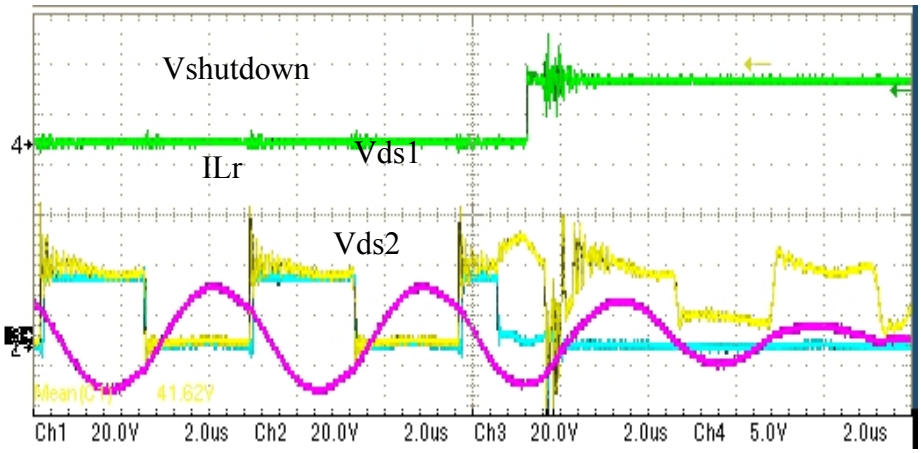


Figure 4-24. Protection circuit against S2 short case (Vds1 (20 V/div), Vds2 (20 V/div), ILr (20 A/div), Vshutdown (5 V/div), 2 us/div)

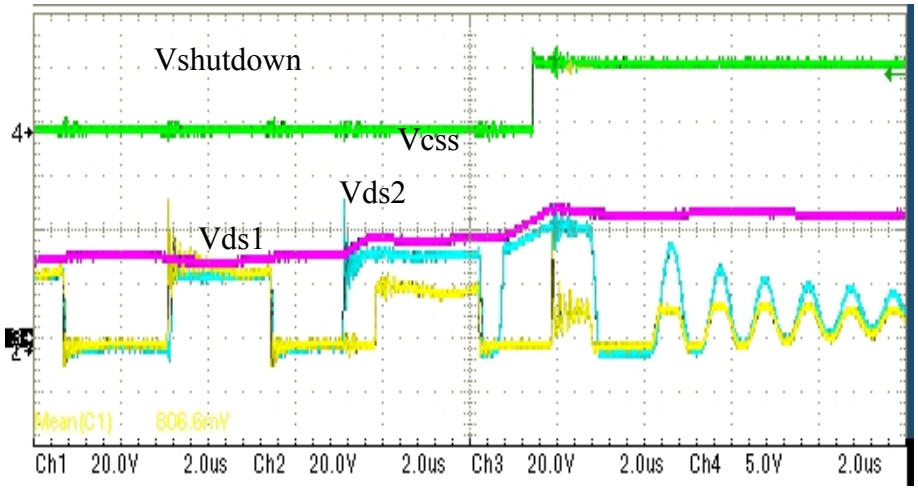


Figure 4-25. Protection circuit against S2 open case(Vds1(20 V/div), Vds2 (20 V/div), Vcss (20 V/div), Vshutdown (5 V/div), 2 us/div)

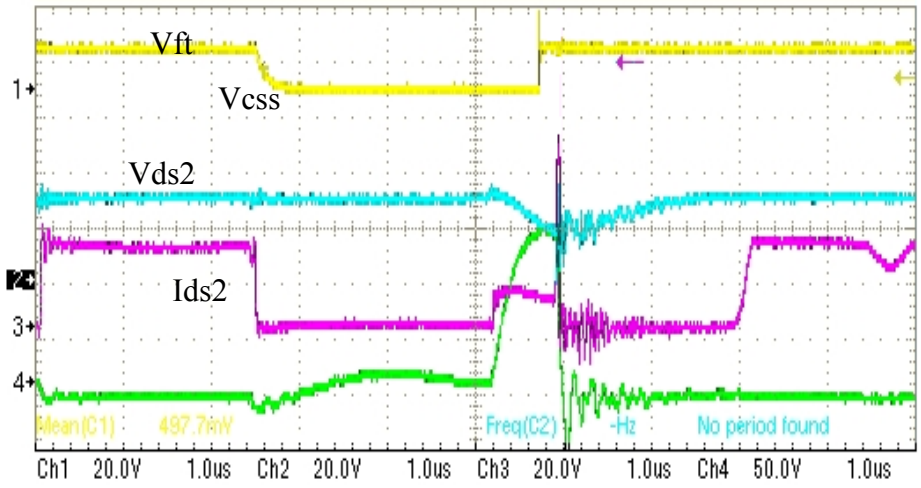


Figure 4-26. Protection circuit against shoot through (Fault trigger signal Vft(20 V/div), Vcss (20 V/div), Vds2 (20 V/div), Ids2 (50 A/div), 1 us/div)

4.7. Summary

A novel protection scheme based on flying capacitor voltage detection is presented in this part. The reasons for the unbalanced voltage stress are fully categorized and illustrated in detail, as well as the possible faults. The proposed protection method can effectively avoid device failure caused by unbalanced voltage stress on switches in a three-level structure, and will protect the system even if a device failure or a shoot-through fault occurs. The solutions to abnormal unbalanced voltage problems are provided. Remedies can be taken to prevent the consequent damages of the faults when the new protection method is employed. A detection circuit is proposed, and its design is thoroughly addressed. The application of the protection scheme can be extended to other three-level dc-dc converters, and the theoretical analysis and simulation results are verified by experimental results.

Chapter 5 System Design and Hardware Implementation

This chapter discusses building the prototype and experiments carried out using the prototype. The high power density converter is not only the target of the design, but also verifies all of the previous contributions. The final hardware implementation includes system design, selection of the main components and design, and experimental results.

5.1.System conceptual design

A proper design for system integration is essential in achieving high power density for power converters. Integration of converter components must be considered from the initial stages of design. Factors such as mechanical connection, electrical connection, the form factor of the components, insulation, grounding and cooling are all important to consider. A conceptual system design was created before the hardware implementation.

5.1.1. Benchmark design

A conceptual design was created in order to find the possible problems with integration and to estimate the power density of the baseline resonant converter for this pulse application. Commercial components were chosen during topology design, and these were roughly drawn according to datasheets. Mechanical support and electrical connections were not drawn in this conceptual design, but were considered in the layout of components. Electrical isolation and natural cooling were also accounted for by leaving reasonable space between components. Sensors and control are not included in

these drawings since they are typically small. Figure 5-1 shows a conceptual drawing of the primary-side MOSFET system. Figure 5-2 shows a similar conceptual drawing of the secondary-side silicon diode system with liquid cooling. Figure 5-3 shows conceptual drawings of the transformer and resonant inductor for the baseline design. These components are considered the focal points of the design. Commercial capacitors are represented by rectangular solids based on dimensions from the datasheets and are incorporated around the components mentioned above. Figure 5-4 shows the complete conceptual drawing of the converter with a cut-away box. The volume distribution of the converter is shown in Fig. 5-5. Table 5-I shows solid and packaged volume estimations along with power density calculations.

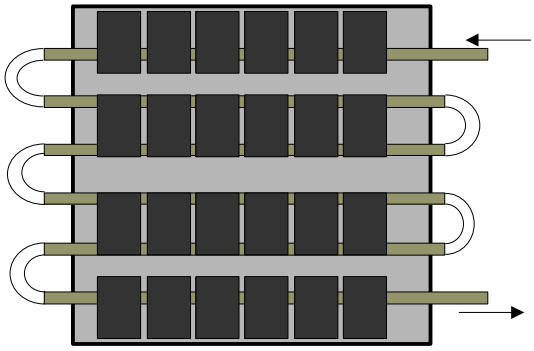


Figure 5-1. Primary-side MOSFET system

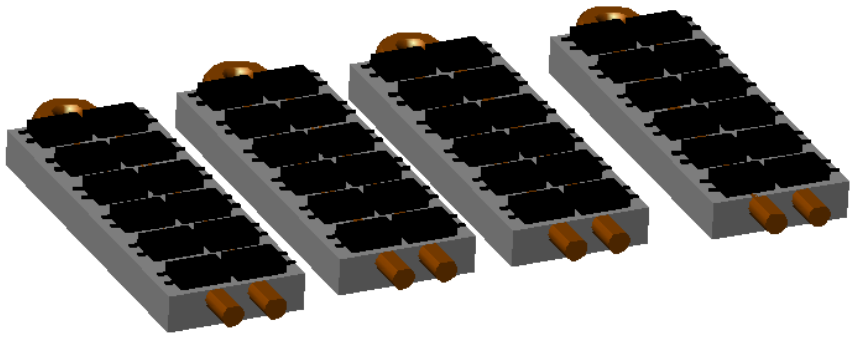


Figure 5-2. Si diode rectifier bridge

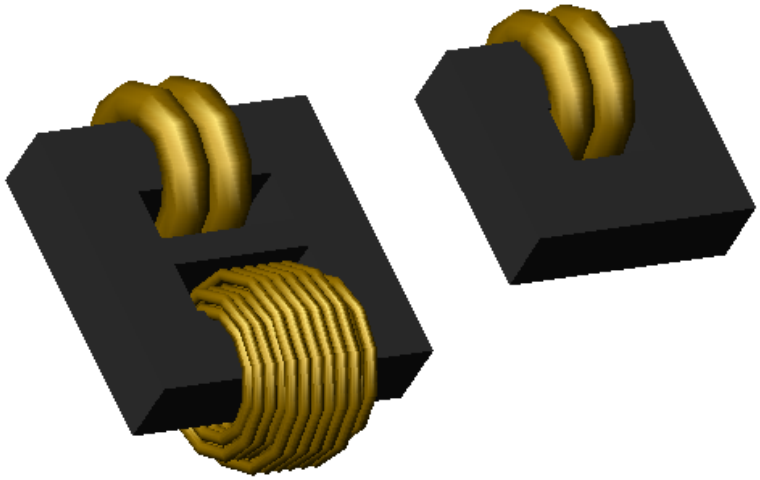


Figure 5-3. Transformer and inductor drawings

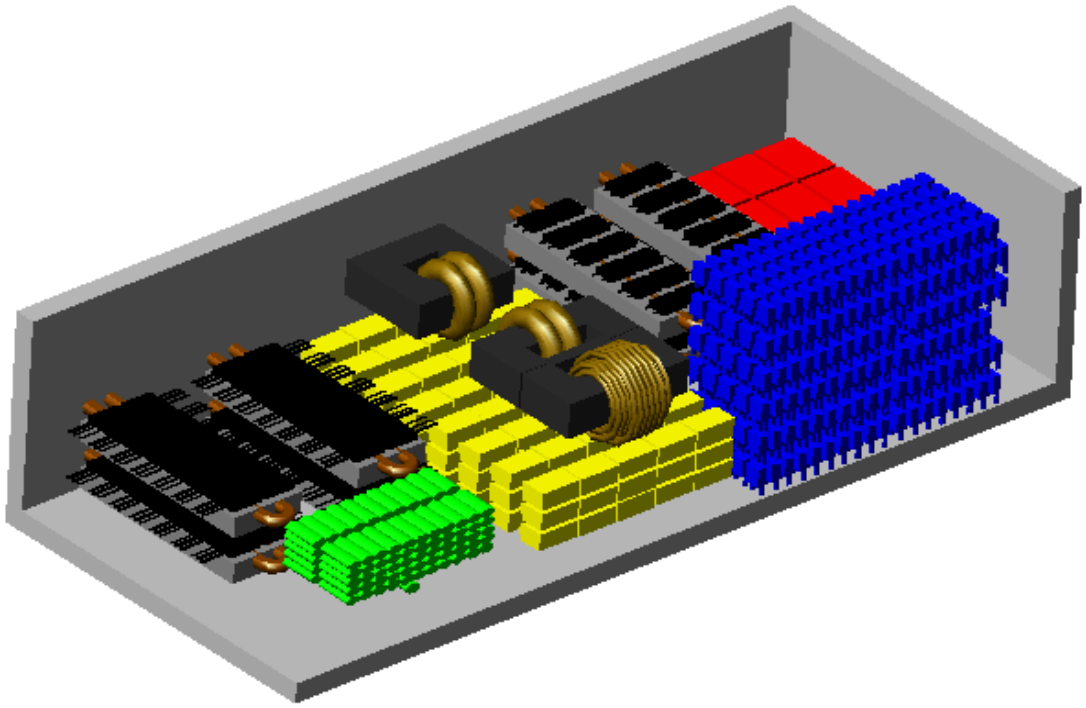


Figure 5-4. Conceptual System layout of baseline system design in cut away box representing the case for the system

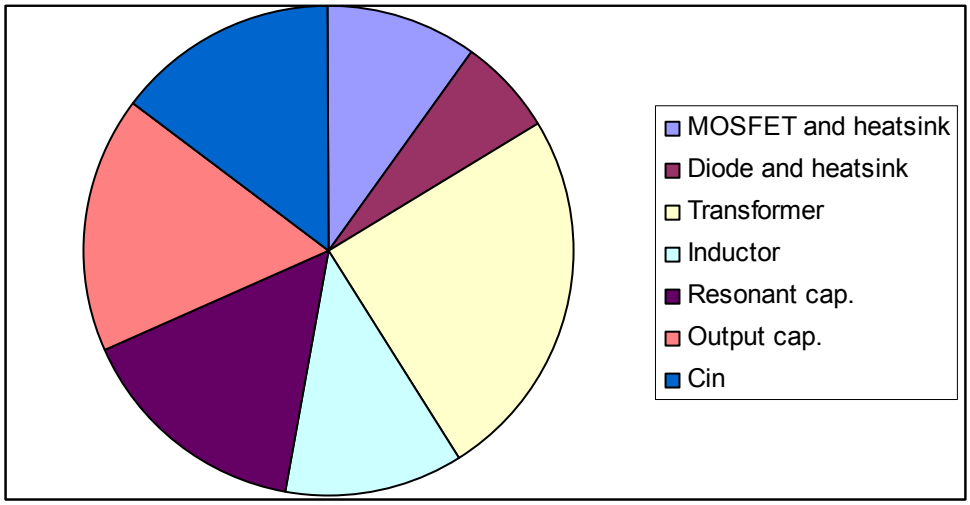


Figure 5-5. Volume distribution of baseline design.

TABLE 5-I. VOLUME AND POWER DENSITY RESULTS OF A 30KW PULSED POWER SUPPLY

	Volume	Power	Power Density
Solid	206 in3	30 kW	146 W/in^3
Packaged	510 in3	30 kW	59 W/in^3

5.1.2. Issues found with concept design

A conceptual system design was created for the baseline resonant converter. The design can be used to investigate how to improve component design and choice as well as system-level packaging in order to improve power density. Solid power density seems very high for the converter components, but this could be improved further by using custom components and optimizing the design. For instance, the resonant capacitor needs accurate capacitance and meets the required voltage and current rating so that a great number of commercial discrete capacitors are needed in parallel and in series.

The packaged power density is considerably lower than the solid power density. This

can be seen in the number of capacitors, MOSFETS, and Si diodes used in the design. Custom components, which have higher ratings, could help improve the packaged volume and therefore increase the power density. In addition, the transformer is the bulkiest component in the whole system, which also could make the whole package loose. Electrical and mechanical connection could help increase power density with the use of high-current printed circuit boards (PCBs).

A compact system design with a higher power density is achieved in the hardware with a custom design and new technology according to the issues found in the conceptual design.

5.2.Hardware implementation and design consideration

5.2.1. Hardware implementation

A. Semiconductor Devices

From the device point of view, better-performing devices mean devices with low power loss and high thermal conductance, leading to a small heatsink. In order to evaluate a power device for high power density applications, the high power density figure of merit (HPDFOM) is developed based on the figure of merit in [F-12]-[F-14], considering the switching time, power loss, thermal handling capabilities, and package size. The formula of the HPDFOM is shown in equation (5-1).

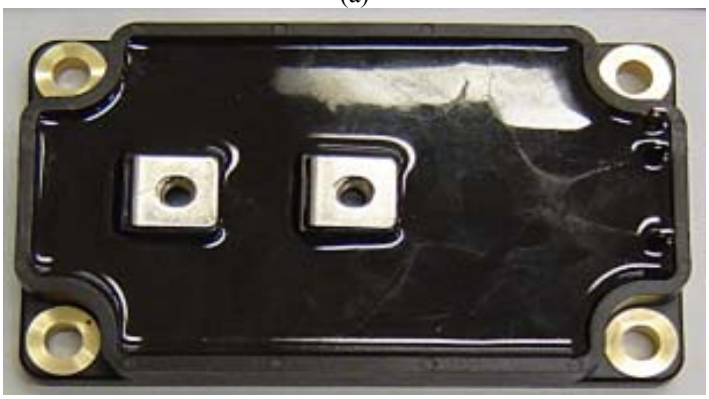
$$HPDFOM = \frac{1}{R_{on} Q_{gd} A_{pack} R_{th}} \tag{5-1}$$

where R_{on} is the device on-state resistance, Q_{gd} is the gate charge, A_{pack} is the device package area, and R_{th} is thermal resistance. According to equation (5-1), for a high-power-density device, devices with a small package area, low thermal resistance, and low

power loss are desirable. Thus the high-frequency operation, small cooling system and high-power operation can be achieved within a given junction temperature rise.

After a comparison of devices from various manufacturers, the power MOSFET APT60M75L2FLL with a fast reverse-recovery body diode is chosen. Considering the system specifications, six APT60M75L2FLL MOSFET dies are connected in parallel to realize each switch. The power MOSFET module used for the converter is shown in Figure 5-6, as well as its counterpart of six silicon discrete MOSFETs.

(a)



(b)

Figure 5-6. (a) Discrete MOSFETs (b) MOSFET module with 6 dies inside

For the secondary rectifier power diode, the basic requirements are low reverse-recovery charge for low switching loss and low forward voltage drop for low conduction loss. The series-connected diodes are used to achieve high output voltage. Low reverse recovery loss, good thermal performance and high operational temperature make SiC

Schottky diodes ideal for the rectifier bridge. In fact, the claimed zero reverse recovery loss is the most attractive characteristic of the SiC Schottky diode used in this application. The performance of the SiC Schottky diode is experimentally evaluated and compared with an ultra-fast Si diode. A negligible recovery current is observed for the SiC Schottky diode, so no snubber circuit is needed. Twelve CSD20120 SiC Schottky diodes are placed in series to realize each rectifier leg to meet the system requirements. Each diode has a $1\,M\Omega$ high voltage resistor in parallel for static voltage sharing and a $0.47\,nF$ ceramic high-voltage capacitor for dynamic voltage sharing. The rectifier structure is shown in Fig. 5-7.

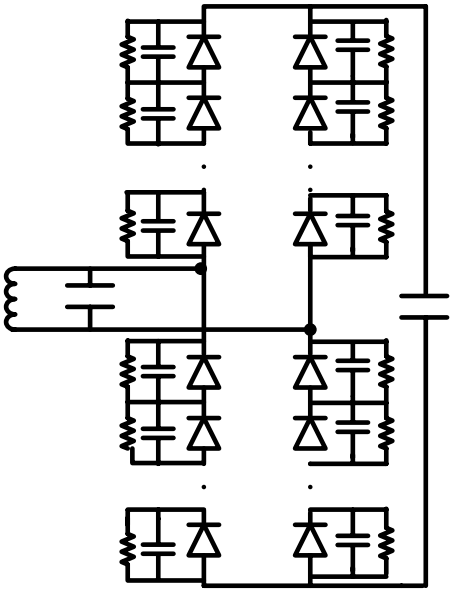


Figure 5-7. High-voltage rectifier bridge comprised of SiC diode and balance resistor and capacitor.

B. Magnetics

As one of the most important components of the converter, the transformer will significantly influence the overall size. To develop a high power density transformer, a nanocrystalline core material is used as the isolation transformer core because of its high

saturation flux density (more than 1 Tesla), superior low loss density, and high operating temperature characteristics. The details of the design approach for minimizing the transformer size are given in [F-15][F-16]. The primary winding and two secondary windings are symmetrically divided and put on the two legs of the U core. With proper design, the leakage inductance is utilized as a resonant inductor to further reduce the system volume. The volume of the nanocrystalline core transformer is 3.5 times smaller than a transformer using a Ferrite core.

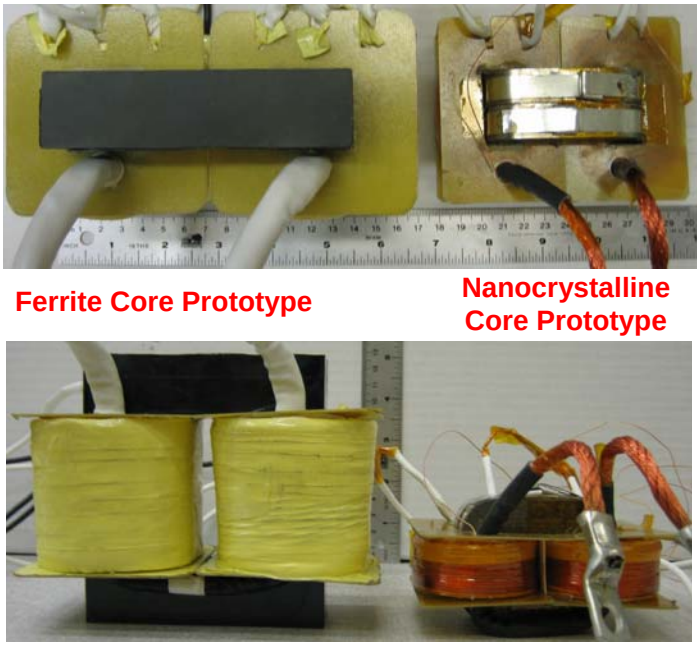


Figure 5-8.Nanocrystalline core transformer with integrated resonant indcutor

Figure 5-8 shows the comparison between the built nanocrystalline core transformer and Ferrite core transformer. It should be noted that the height of the transformer determines the height of system due to the bulky physical size of the transformer compared with other components. Thus the dimensions of transformer should be considered before the system is assembled.

C. Input capacitor

In a three-level topology, two identical input capacitors in series are needed to equally

split the input voltage into a three-level voltage. A high ripple on the input capacitor will result in unbalanced voltage on the switches and cause abnormal converter operation. A capacitor with larger capacitance works more like a voltage source. Usually equation (5-2) is used to calculate the needed input capacitance.

$$C_1 = C_2 \geq \frac{I_{avg}}{\Delta V / \Delta t} \tag{5-2}$$

where C_1 and C_2 are input capacitances, I_{avg} is the average current during half of the switching cycle, ΔV is the allowed voltage ripple on the input capacitor, and Δt is half of the switching period or each switch's conduction time if there is deadtime. Based on this equation, $24\,\mu F$ is needed for the input capacitor if a 5% input voltage ripple is allowed.

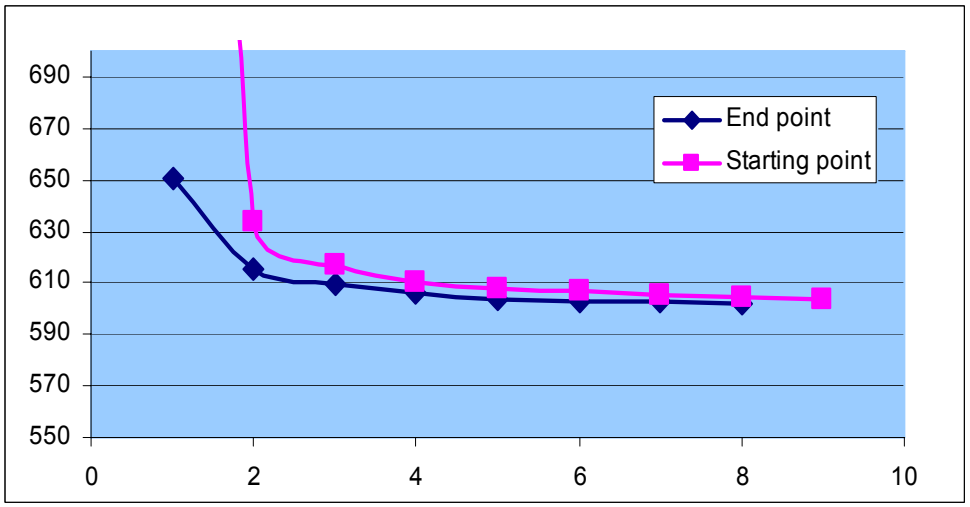


Figure 5-9. Voltage ripple vs. input capacitance when input inductance is 4uH.

However, the above equation is based on an assumption that all of the current is provided by the input capacitor, or that there is a large input inductance before the input capacitor. Therefore, the calculated value is estimated for the worst case. Hence, with a

larger input capacitance and low voltage ripple, power density is compromised for more input capacitors.

In this application, the maximum possible input inductance is 3 μH . Thus part of the current is shared by the input power supply. Considering the variable frequency control, Fig. 5-9 shows the voltage ripple vs. the capacitance of the input capacitor at two conditions; the starting point or minimum switching frequency, and the end point or maximum switching frequency. Four μF input capacitors can meet the design requirement.

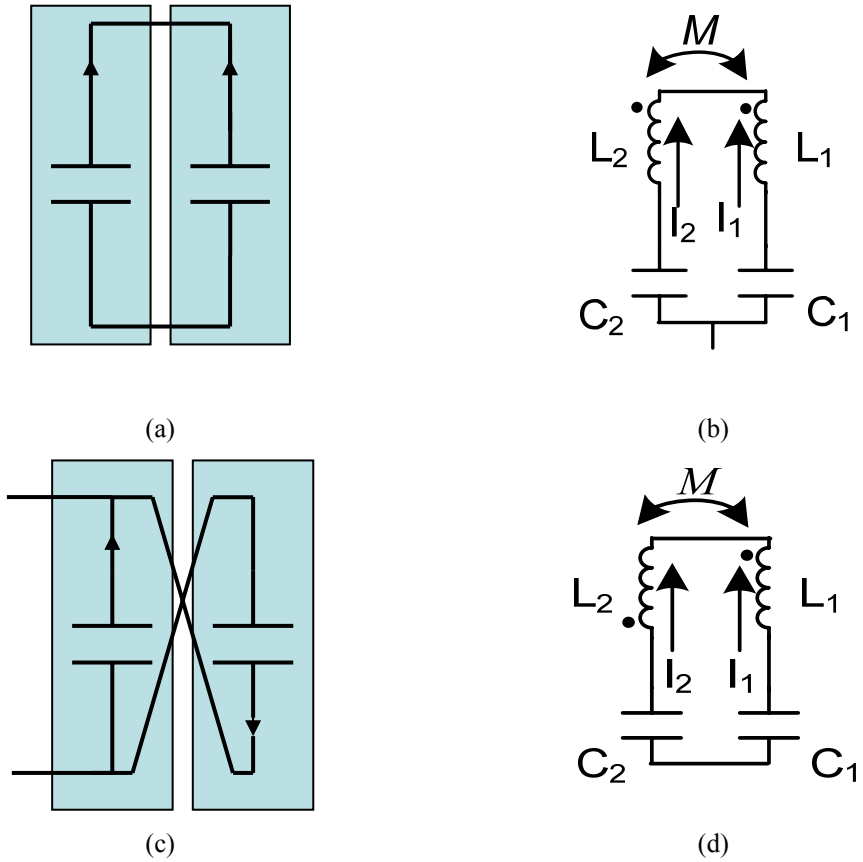


Figure 5-10. Input capacitor connection methods. (a) Coupled connection. (b) Equivalent circuit of coupled connection. (c) Decoupled connection. (d) Equivalent circuit of decoupled connection.

Due to the high capacitance and current requirement, a polypropylene film capacitor is

found to be suitable because of its low loss, choice of a wide range of available capacitance, and good mechanical characteristics.

While the input capacitance limits its voltage ripple, the parasitic inductance of the input capacitor is the main contributor to the voltage spike on the main switches. Figure 5-10 shows two possible connections for the input capacitors. With the decoupled connection method, the parasitic inductance causing the switching voltage spike is only from the wiring inductance in the busbar PCB. Without slowing down the switching speed, the voltage spike can be reduced by 50% when the input capacitors ares connected in a decoupled way.

D. Resonant Capacitor

The resonant capacitor choice is critical to not only the converter operation performance, but also to the system power density. First of all, the criteria for the resonant capacitor selection include the stability of the capacitance with a wide thermal range and switching frequency, as well as the ability to withstand high output voltage. Two capacitors are required to circulate about 25KVA at 5kVAC and 200 kHz. To meet these requirements and reduce size, two mica capacitors are selected for their small temperature coefficient, excellent frequency characteristic, and good insulation. An oil-cooled customized mica capacitor is used in the converter, as shown in Figure 511. The capacitor consists of several stacked pieces. The gap between the pieces improves their thermal performance.

Figure 5-11. Oil-cooled Mica resonant capacitors.

E. Flying Capacitor

For better decoupling and voltage clamping effect, a larger capacitance is desired, which also can provide stable detection signal. Though non-phase shift operation is employed, the flying capacitor is still required to clamp the inner switches' voltage stress. The larger capacitance of the flying capacitor is always desired for its better clamping effect and stable voltage.

The equation for flying capacitance calculation is given in Equation 4-3. Considering the 10nF C_{sw}, a 2 μF 500V ceramic capacitor is selected.

F. Thermal Management

Pulsed-power characteristics allow the thermal design to utilize the system rest time and the thermal capacitance of the components [F-16]. The average temperature rise depends on the total thermal resistance of the system, and the peak junction temperature rise is determined by the thermal time constant of the components and the system operation duty cycle. The system thermal model is built with a 1-D equivalent circuit in SABER, shown in Fig. 5-12. The thermal model is corrected by thermal measurement. To effectively cool the system and reduce the size, 90^{o}C oil-based liquid cooling is used. A customized heatsink is designed to fit the four MOSFET modules' footprint. The heatsink

with its internal structure is shown in Fig. 5-13.

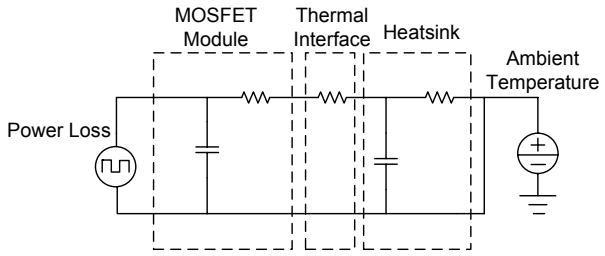


Figure 5-12. 1-D MOSFET modules thermal model

Figure 5-13. Custom design heatsink

5.2.2. Design considerations

It is exceptionally challenging to operate a 30kW module at 200kHz, especially with a minimized margin for a high power density design. Each failure is dreadful and frustrating. Based on experimental experience, the design considerations are summarized as follows:

A. Soft startup/shutdown(high frequency and unsymmetrical duty cycle)

Fast switching speed is desired to reduce the switching loss at high–power, high switching frequency operation. Due to the relatively large parasitic inductance, the over-transient voltage stress on the main switch is the one of the serious problems in converter operation. High turn-off current has to be avoided, though ZVS is guaranteed for turn-on during the period of charging. Due to the resonant converter, the converter could suffer high transient voltage stress during startup and shutdown. Unsymmetrical duty cycle startup and synchronized shutdown are designed for soft startup and shutdown. Additionally, unsymmetrical duty cycle startup is also necessary to avoid transformer saturation. Figure 5-14 illustrates the issues with startup high-voltage stress, and unsymmetrical duty cycle startup. The dotted lines show the startup without an unsymmetrical duty cycle. Even though the turn-off current during startup is reduced

when high-frequency is employed to eliminate the inrush current, the startup turn-off current still results in serious voltage spikes. The solid lines in Figure 5-14 show that the turn-off current can be significantly reduced with the unsymmetrical duty cycle soft-startup method.

Since the inductor current becomes sinusoidal at the end of charging, the uncontrolled shutdown signal may occur at the wave crest of the inductor current. The high turn-off current induces a dangerous voltage spike and causes serious consequences. In order to shut down the converter around the wave trough of the inductor current, a soft shutdown signal is adjusted through synchronization with the gate signal.

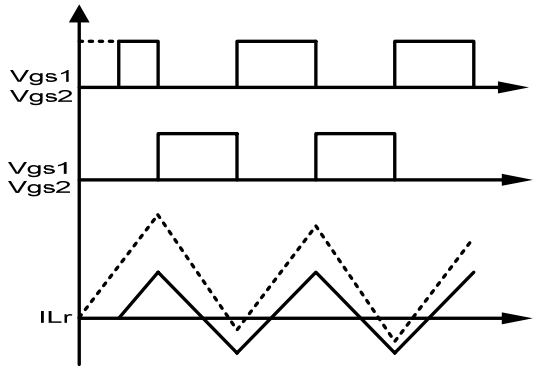


Figure 5-14. Asymmetrical duty cycle startup.

B. Noise interference

The converter still suffers high noise interference due to a hard turn-off, whereas soft-switching ZVS is achieved in the PRC for turn-on. The high dv/dt and di/dt generate high-frequency conducted and radiated EMI noise.

Based on the experiment, the common mode (CM) is conduction noise through the gate driver where the isolation component, optocoupler or transformer, is critical to attenuation the differential mode (DM) noise. The DM noise is the radiation noise that is the dominant noise for the controller. The solutions to each type of noise are summarized

below.

Solutions to DM noise:

- Use CMOS IC to increase its noise immunity.
- Shorten the traces' loop to reduce the parasitic inductance.
- Add decoupling capacitors as close to the component as possible.
- Use ground plane instead of a trace.
- Shielding (implemented only if necessary).

Solutions to CM noise:

- Choose optocoupler with minimum parasitic capacitance.
- Minimize the inter-winding capacitor if a transformer is used, by methods such as enlarging the distance between the primary winding and the secondary winding.
- Add a CM choke.

C. PCB layout

The controller PCB layout mainly focuses on increasing the noise immunity. For a high-current PCB design, the inherent constraint is the temperature rise. Equation (5-3) can estimate the allowable current with a given temperature rise, trace width and thickness. This formula is for outer layers, and needs to be de-rated to 50% for inner layers.

$$I = 0.025 \cdot \Delta T^{0.45} \cdot W^{0.79} \cdot Th^{0.53} \tag{5-3}$$

where I is current in Amps, ΔT is temperature rise in ^{o}C, W is the trace width in mil, and Th is the trace thickness in mil.

Usually the copper thickness of the PCB is given in oz per square foot. A thickness of 1

oz/sq foot = a minimum of 1.2mil to 1.4mil thickness depending on the manufacturer; typically 1.36mil/35mm is used.

Table 5-II lists the needed clearance vs. the breakdown voltage at different PCB conditions. Since the high-voltage rectifier bridge will be filled with insulating oil, 100mil for 5000V is applied in a high-voltage PCB layout.

TABLE 5-II. PCB CLEARANCE VS. BREAKDOWN VOLTAGE

Spacing (mil)	With Solder Mask (V)	With No Solder Clean (V)	With No Solder Hygro Dust (V)	With No Solder Flux (V)	Internal Layer (V)
7	3100	1320	620	250	>5000*
10	3500	1480	900	300	>5000*
20	3900	1620	1400	750	>5000*
40	4700	2300	2050	1300	>5000*
60	5000	3360	2820	2050	>5000*
80	>5000*	4160	3700	3000	>5000*
100	>5000*	4720	3850	3650	>5000*
*Note: Dielectric tester maximum voltage = 5000 V dc.					

5.3.Converter Assembly and Experimental Verification

5.3.1. Converter assembly

Because of the high voltage level on the transformer's secondary side, transformer oil is required as the specification for voltage insulation. Therefore the whole enclosure box is divided into two boxes; one includes the circuit on the transformer's primary side, and the other is a sealed box which contains the rest of the components and the insulating oil. Figure 5-15 shows the prototype. The primary-side box is composed of four layers stacked tightly, shown in Figure 5-16. The heatsink is the bottom layer, which has close contact with the bottom side of the primary box. In other words, the primary-side box works as part of the heatsink. MOSFET modules are the second layer on top of the heatsink. The third layer is the busbar PCB with covered input capacitors. The top layer is comprised of the system controller and gate driver. All of the components in the sealed

box are on the same level. Solid high-voltage insulation materials are added to keep distance between each component. The dimensions of the whole box are 5.2"x 15.3" x 2.7". Thus the achieved average power density is 140w/in^3.

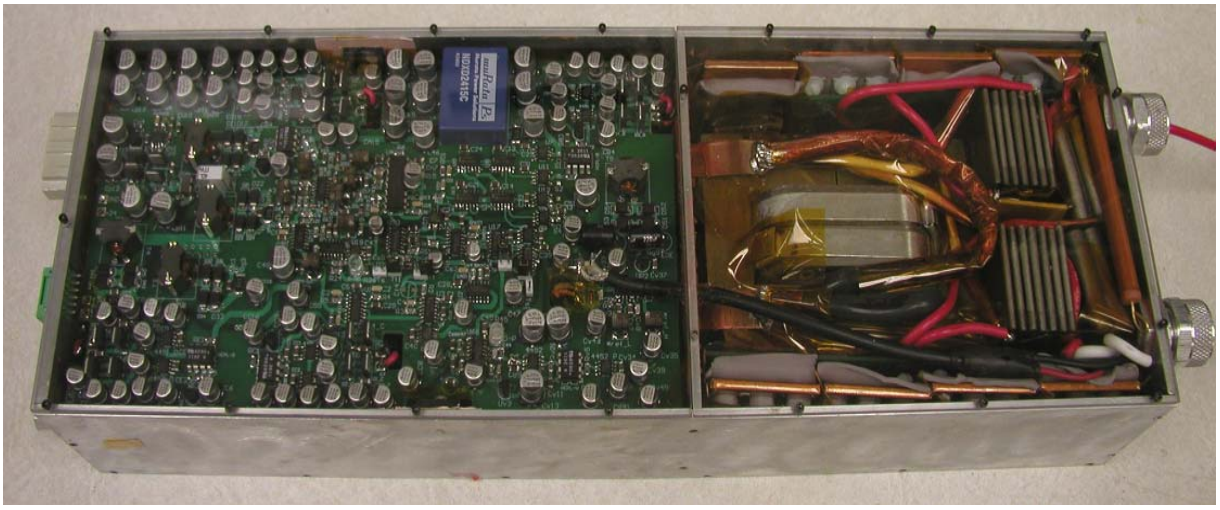


Figure 5-15. Prototype with achieved power density of140W/in^3

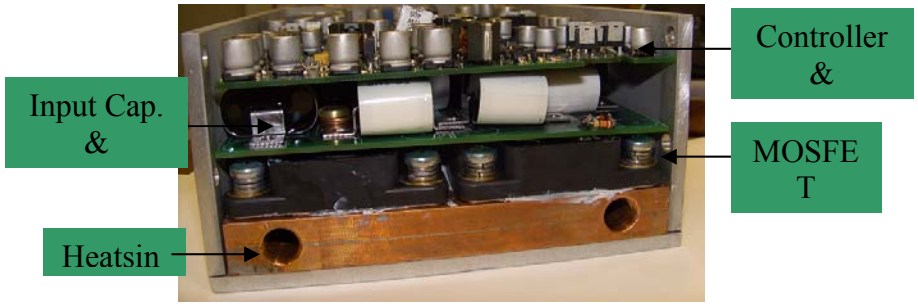


Figure 5-16. Front view of the primary-side box

Fig. 5-17 shows a comparison between the final prototype and the initial baseline design. The volume of the MOSFET and heatsink is larger than the discrete components because the drain of the discrete MOSFET is not insulated, whereas the MOSFET module is an insulated package. Though the MOSFET module volume is larger than six discrete MOSFET devices, it is easy to assembly and helps to achieve a compact design.

The detailed solid volume distribution is shown in Figure 5-18. Here package factor is defined to indicate the compactness of the assembly, which is equal to the solid volume

of components except the metal enclosure divided by the box volume. The primary side box has 78% package factor and the secondary side box has 64% package factor Compared with the primary side box. The low package factor of sealed unit is mainly due to the high voltage insulation requirement. From the package factor value, a higher power density can be expected by a more compact design when the dimensions of the bulky components, such as transformer and resonant capacitors, are well organized.

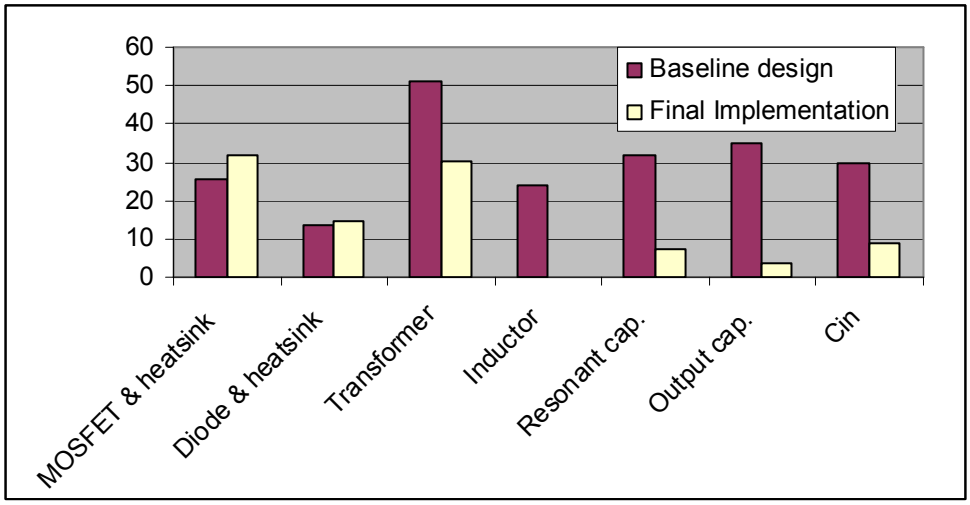
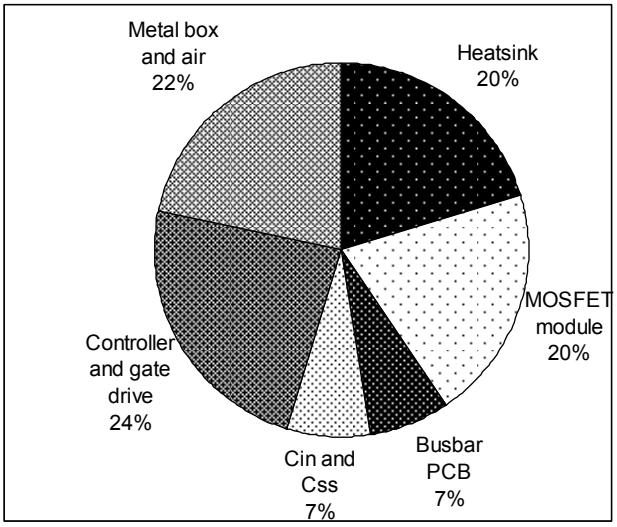
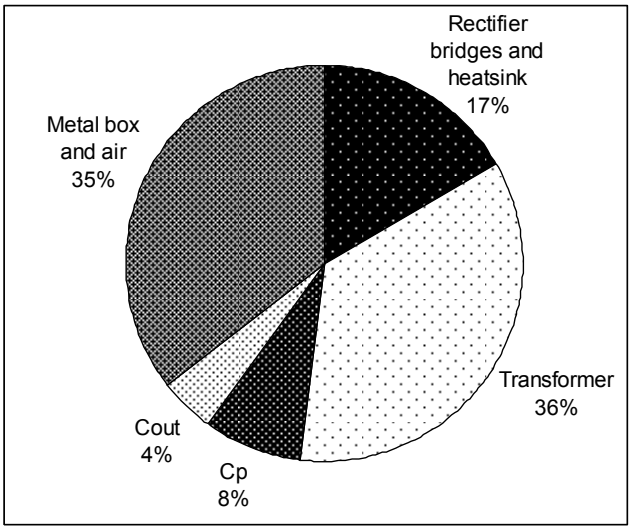


Figure 5-17. Component volume compared between conceptual design and final implementation.



(a)



(b)

Figure 5-18. Prototype component volume distribution. (a) Primary side box (total volume 122 inch^3) (b) Secondary side box (total volume 87 inch^3)

5.3.2. Experimental verification

The prototype is tested in the laboratory to verify the design. Figures 5-19 and 5-20 verify the asymmetrical startup and synchronizing shutdown. After the soft startup and shutdown are employed, the voltage spike is significantly reduced during the converter startup and shutdown. The worst case of voltage spike happens at end of the constant frequency operation, in segment 2. Figure 5-21 shows the Vgs and Vds waveforms per cycle for one of the inner switches, (S2). It is clear that ZVS turn-on is achieved. The entire single charging period is shown in Fig. 5-22. The envelope of Vds2 is caused by the varied input voltage. The maximum voltage spike of Vds2 is no more than 400 V. The clean waveform of Vds2 during entire charging period means the ZVS achievement. Fig.5-23 provides the waveforms during trickle charging.

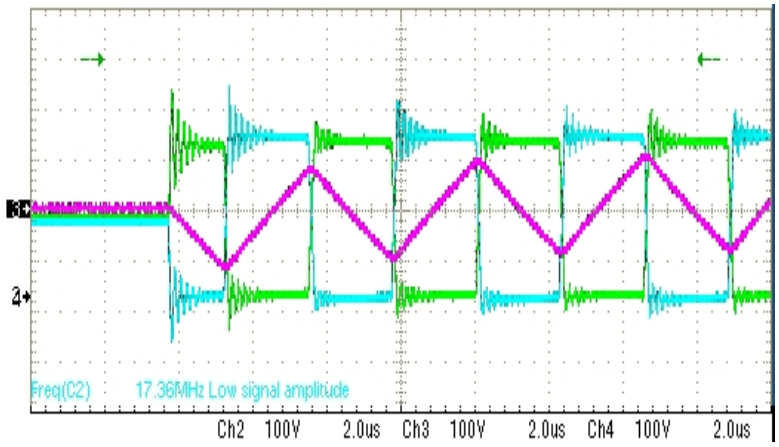


Figure 5-19. Asymmetrical duty cycle startup (Vds2, 100V/div, Vds3, 100V/div, ILr, 100A/div, 2us/div)

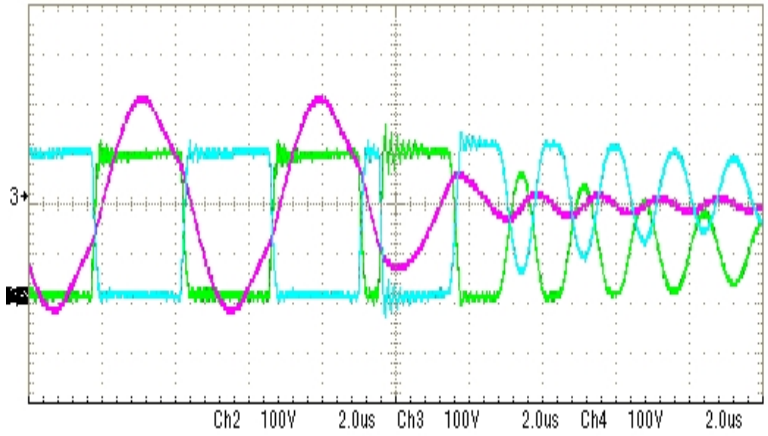


Figure 5-20. Soft shutdown (Vds2, 100V/div, Vds3, 100V/div, ILr, 100A/div, 2us/div)

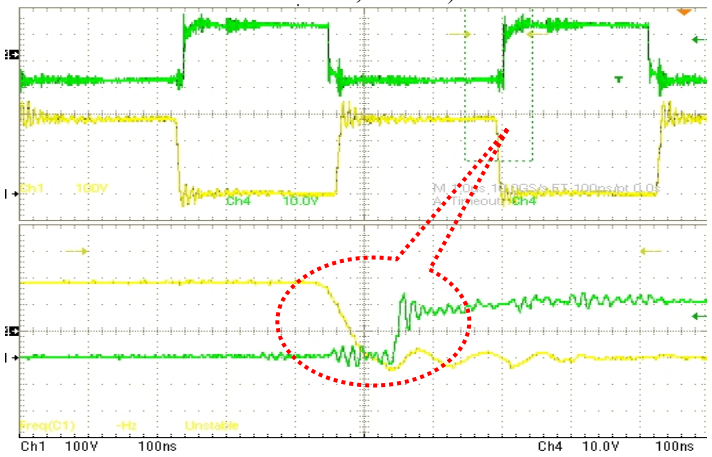


Figure 5-21. ZVS operation (Vds2,200V/div,Vgs2,10V/div)

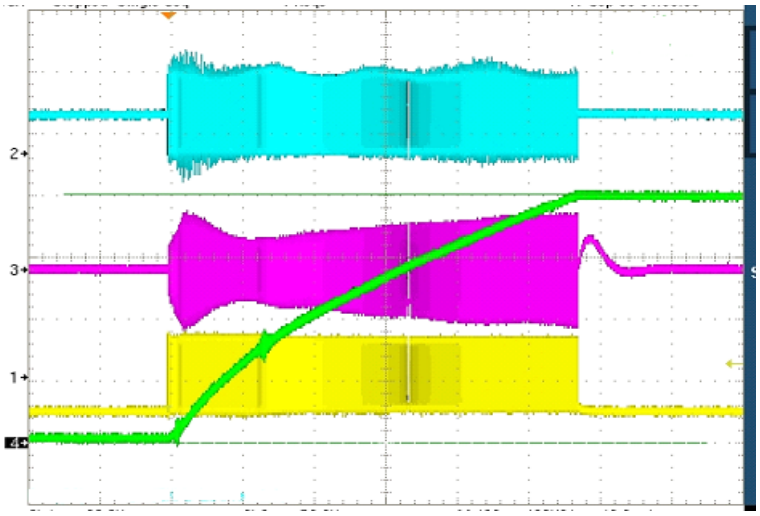


Figure 5-22. Principal waveforms during charging (Vgs2 20V/div, Vds2 200V/div, ILr 250A/div, Vo 2.5kV/div)

Figure 5-23. Trick charging after Vo=10kV (Vds2, 200V/div, iLr, 200A/div, Vo=25kV/div, 1s/div)

One way to understand the possibility of high power density improvement is to know the system's power delivery capability. Based on the passive components' thermal measurements, shown in Figure 5-24, the maximum temperature is around 56 ^{o}C. Considering the 90 ^{o}C cooling oil, the MOSFET modules' junction temperature should be the bottleneck for higher power delivery. The MOSFET module's on-resistance is measured in the circuit to estimate the junction temperature inside. Based on this method,

Figure 5-25 shows the experimental waveforms for the MOSFET modules' forward voltage drop measurement. Figure 5-26 shows each on-resistance and estimated junction temperature when the case temperature is gradually increased. A 130 ^{o}C junction temperature is estimated by the measured on-resistance when the case temperature increases to 90 ^{o}C. Considering the 150 ^{o}C maximum operational junction temperature of the chosen Si device, it is possible to push the converter to a higher power for higher power density. It has to be noted that ±20% measurement error has to be considered when unavoidable noise is induced on the in-circuit forward voltage drop measurement.

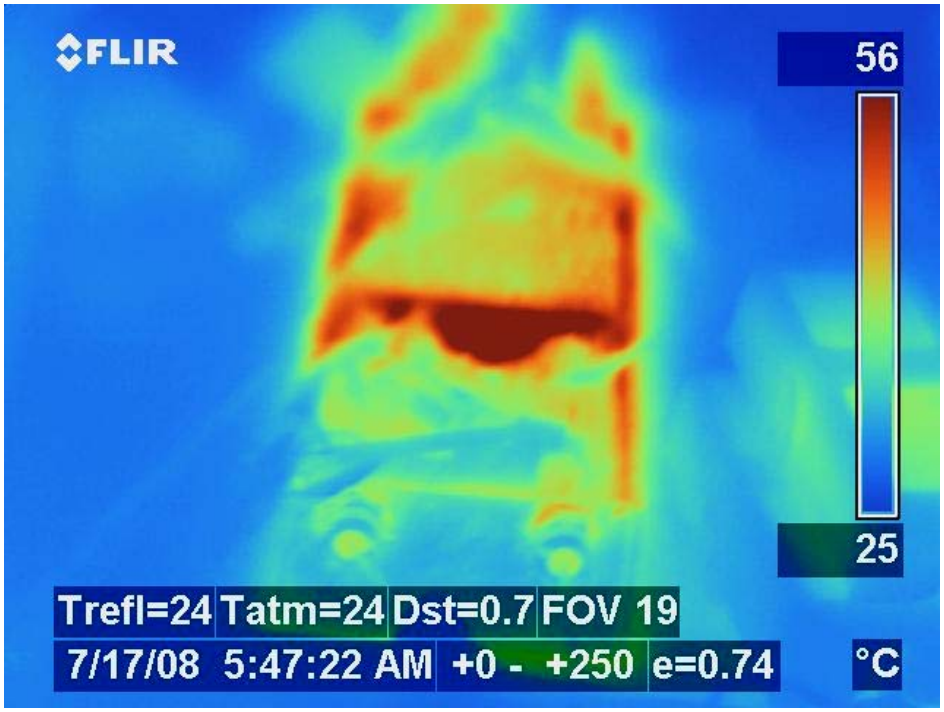


Figure 5-24. System thermal measurement

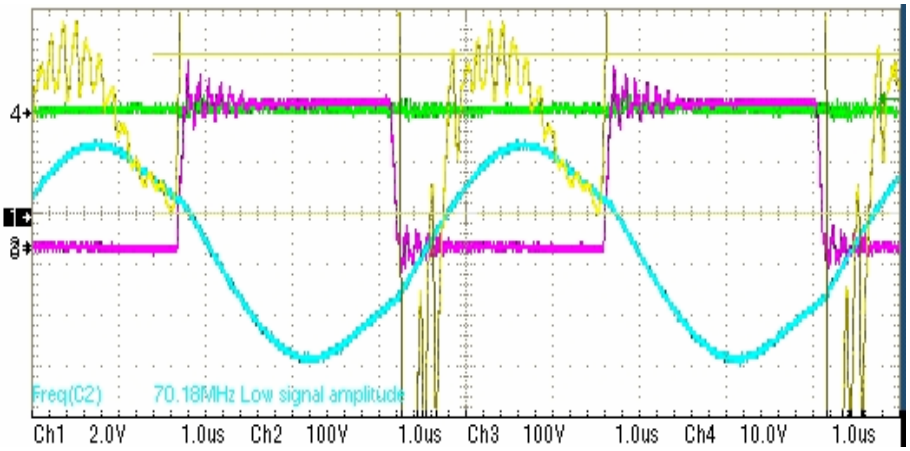


Figure 5-25. Rdson measurement waveforms (Vdson4, 2V/div, Vds4, 100V/div, ILr, 100A/div, 1us/div)

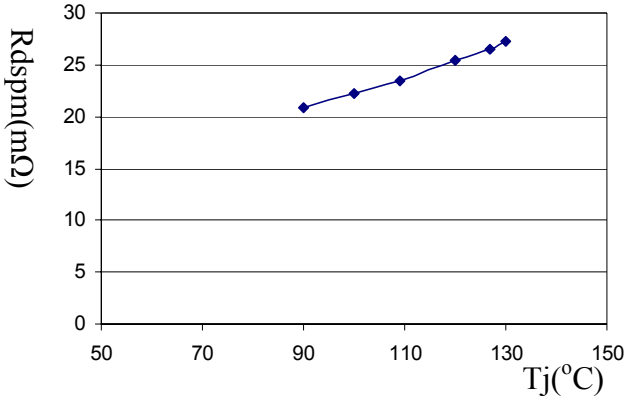


Figure 5-26. Calculated Rds_on based on in circuit measured Vds_on vs. junction temperature Tj as case temperature gradually increases

5.4. Impacts on power density

5.4.1. The impact on power density with proposed resonant tank design and control scheme

As Figure 3-17 shows, the volt-sec of transformer design can be reduced by 25% if the charging profile can be changed according to the practical structural variation I. Table 5-III lists the main parameters of the transformers with different structural variations. The transformer can be reduced by 20% with structure I. It should be noted that the core size of U60/27/12 is not commercially available. Because the near core size to the U67/27/14 is

U33/22/9 which is far lower than U67/27/14. U60/27/12 has the same dimensions as the U67/27/14 except for the reduced core thickness and window width.

TABLE 5-III. SUMMARY OF TRANSFORMER DESIGNS WITH DIFFERENT STRUCTURAL VARIATIONS

	Structure II	Structure I
wire (P)	1254*AWG38	1254*AWG38
Number of turns(P)	10	9
wire (S)	184*AWG40	184*AWG40
Number of turns(S)	110	99
Core	2*U67/27/14	2*U60/27/12
Volume	319 (cm^3)	256 (cm^3)
Pcu	190 (W)	171 (W)
Pcore	136 (W)	114 (W)
Tr	44 °C	44 °C

When the charging profile is implemented by PLL, the converter can deliver higher power with narrow switching frequency range. Since these two control methods achieve the same voltage at the charging terminal, ie. 10 kV. So the quality factor has to be changed also with different switching frequencies.

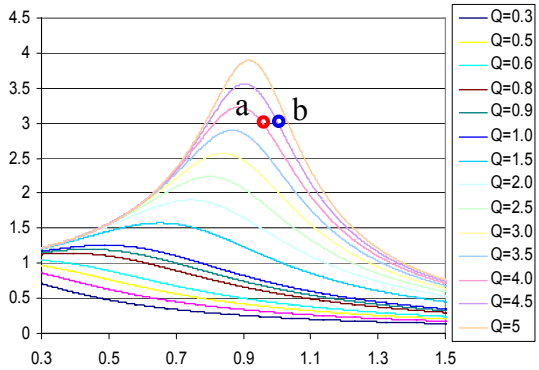


Figure 5-27. Final operating points in PRC voltage gain curves with two charging control methods.

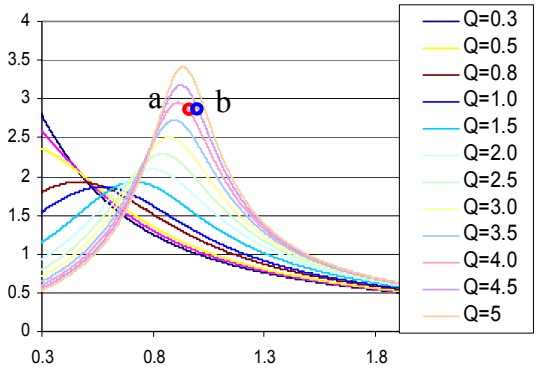


Figure 5-28. Final operating points in PRC input current curves with two charging control methods.

Point a shown in Figure 5-27 is the final operating point for PLL control, which achieves voltage gain of 3 at quality factor (Q) of 4 and switching frequency of 205 kHz. Since

VFC has to leave enough margin to guarantee ZVS operation to tolerate the error of resonant frequency estimation by output voltage. The final point of VFC is shown as Point b in Figure 5-27 with low power factor, which achieves voltage gain of 3 at quality factor (Q) of 4.5 and switching frequency of 215 kHz. The output power is reduced with VFC control, which is proved by the experimental results shown in Figure 3-33. The corresponding operating points on input current curves are shown in Figure 5-28. The input currents are almost identical for two control methods. According to the charging profile, the input currents and power losses during entire charging period are shown in Figure 5-29 and Figure 5-30 respectively.

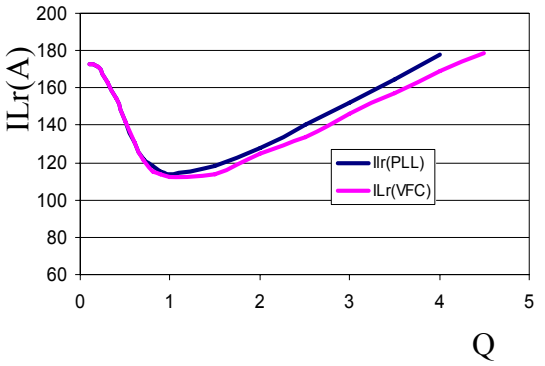


Figure 5-29. Input currents vs. quality factor (Q) with two different control methods

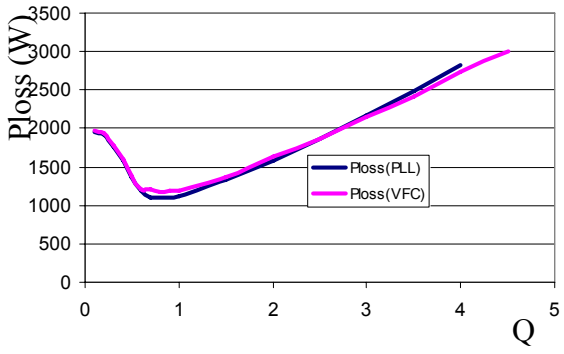


Figure 5-30. Power loss vs. quality factor (Q) with two different control methods.

The input current of VFC control is slightly shifted to right. But the a little bit low conduction loss is offset by switching loss increase due to higher turn-off current. Therefore, these two control methods generate similar power loss, but PLL control method can deliver higher output power. VFC suffers the same power loss but delivers less power to the load due to larger circulating energy. The output currents of these two control methods are shown in Figure 5-31. The average output current of VFC is around 10% lower than that of PLL control, which is verified by experimental results in Figure 3-33.

Thus, with the same converter, PLL control can improve the system power density by 10%.

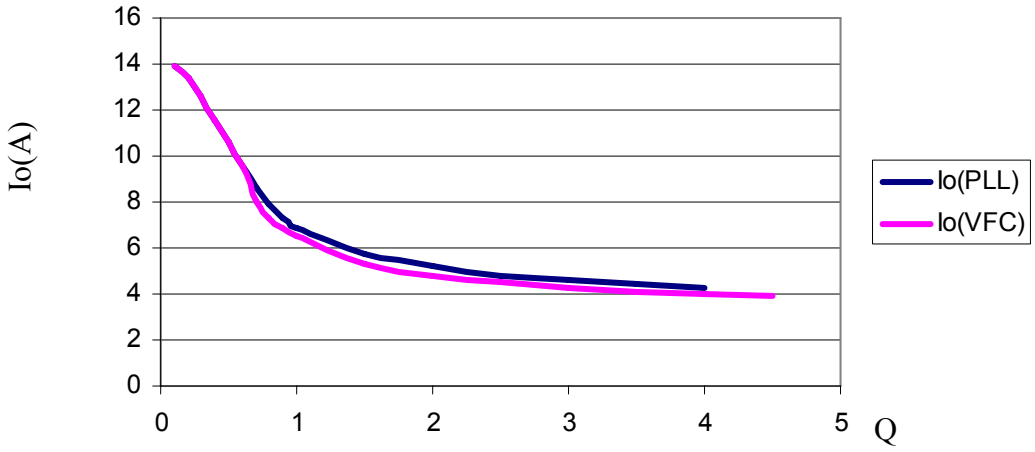


Figure 5-31. Output current vs. quality factor (Q) with two different control methods.

5.4.2. The impact of proposed detection method on power density

Table 4-III lists the faults which can be detected by Vcss. Without the proposed detection method, these faults need multiple conventional detection methods to cover these faults. Though the neutral point detection is less sensitive to the fault compared to Vcss detection, it is still a powerful method for multiple faults and doesn't need any loss components inserted into power stage. The proposed circuit for Vcss detection shown in Figure 4-17 can work for neutral point detection too. The hardware is shown in Figure 5-32.

TABLE 5-IV. PROPERTIES OF VCSS DETECTION COMPARED WITH VCE DETECTION

Device / **Fault Case**	**Results**	**Sensor except Vcss detection**
S1 Open	Vcss=0, Vnp=0	Neutral point detection
S1 Short	Vcss=Vin, Vnp=Vin/2	Voltage detection of Vds1
S2 Open	Vcss=Vin, Vnp=Vin/2	Voltage detection of Vds2

Device / Fault Case	Results	Sensor except Vcss detection
S2 Short	Vcss=0,Vin/2 pulse Vnp=0,Vin/2 pulse	Neutral point detection
Dc1 Short	Vcss=Vin Vnp=Vin	Neutral point detection
Dr1 Open	Vcss=Vin Vnp=Vin	Neutral point detection
Dr1 Short	Vcss=Vin Vnp=Vin	Neutral point detection
OL	Vcss=Vin Vnp=Vin/2	Need open load detection
Transformer winding broken down	Vcss>Vin/2 Vnp=Vin/2	Need voltage sensor
Shoot-through	Vcss<Vin/2 Vnp=Vin/2	Need shunt etc.

Since the neutral point detection cannot detect the entire unbalanced fault cases, each switch's voltage has to be measured. The pre-charge resistor still can work for voltage divider for voltage sensor. Four duplicate protection circuits with isolated auxiliary power supplies are needed. The fault of transformer winding broken down is very tricky because the voltage varies from zero to 10 kV. Like the Vcss detection, this fault will cause the unbalanced voltage stresses across the main switches so that it can be detected by unbalanced voltage stresses detection. Shoot-through is the most dangerous fault for converter. Inserting a high current rating IGBT into the bus bar has been introduced in [E-13] as an effective way with low volume. Accordingly, a heatsink with the area same as the IGBT footprint is needed. But it should be noted that it is not necessary to have other detection circuits to cover the faults detected by Vcss.

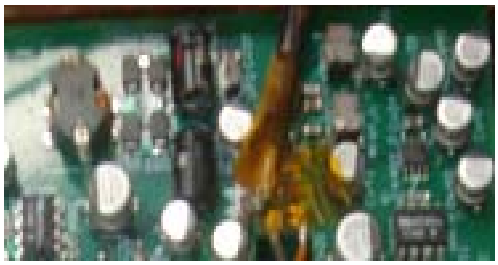


Figure 5-32. Protection circuit board with dimensions of 3.17" x 1.25" x 0.28".

5.5.Summary

A prototype 30 kW, 200 kHz high-power-density three-level parallel resonant converter has been implemented and demonstrated.

First, a conceptual design is provided to help find the issues with the system package and estimate the power density in advance. Then the detailed hardware implementation is introduced. A custom package Si MOSFET module with six dies in parallel is used as the main switch based on a figure of merit for high power density application. For a high-voltage rectifier, each bridge consists of 12 SiC Schottky diodes in series. A nanocrytalline magnetic core transformer with fully integrated resonant inductance and custom oil-cooled mica resonant capacitors all help to significantly reduce the size.

The design is fully verified by the experimental results, and possibilities for further improvements on power density are also investigated.

Chapter 6 Conclusions and Future Work

A pulsed power supply for capacitor charging features high power, high voltage, and the ability to work at a transient state. The main challenges for a high power density power supply are dealing with the components' stress reduction to minimize component stress and maximizing the power delivery to increase the power level. The conclusions obtained from this dissertation and ideas for future work are discussed in this chapter.

6.1.Summary

In this dissertation, the influence of resonant structural variation on resonant tank design is investigated. Without any impact on the converter performance, the different structures associated with the transformer's position in the resonant tank significantly affect the resonant components' stress and transformer size. However, the resonant components' volume can be treated as the same because the energy through the resonant inductor and resonant capacitor stays the same no matter which side of the transformer they are located on. However, the structural variation has a significant impact on the transformer size.

The VA product, which determines the transformer volume, changes in different structural variations due to the changed power factor. The influence on the resonant tank volume is illustrated by an example design and verified by experiment. Based on the study of the resonant tank structural variations, a methodology is provided for high power density design, as well as the design considerations when the resonant tank structure changes. When the resonant inductor is integrated into the transformer, the resonant tank

structure can be changed as easily as discrete components can be changed. The leakage distribution control method is presented. With the controlled leakage inductor, an optimum charging profile for high power density is proposed to shrink the transformer size.

Secondly, in order to achieve a non-linear charging profile, PLL is first introduced to overcome the traditional output-voltage-based varied frequency control (VFC) method. The PLL control can work under varied input voltages and guarantee ZVS operation while it is delivering maximum power to the load, which cannot be achieved by VFC.

There is a thorough analysis of the design procedure and the calculation of the parameters. The boundary of the PLL application in capacitor charging is also explored. A schematic for the PLL implementation is proposed and tested with a prototype in the lab. With PLL control, the power can be increased by around 10%, or there can be a 10% shorter charging time for the same load. In addition, for a three-level structure, phase-shift and non-phase-shift control schemes are compared. With variable switching frequency and fixed duty cycle control, non-phase-shift control has the benefits of less power loss and component stress; e.g. the voltage and current stress on the clamping diode and flying capacitor are reduced, and the effect of the parasitic inductance on the switches' voltage spike is eliminated.

Thirdly, as the three-level structure brings the benefits of the application of a low-voltage-rating MOSFET, the unbalanced voltage stress of the MOSFETs is also introduced. Furthermore, faults cannot be avoided in system operation; especially when a minimum margin is left for high power density. System failure will result in severe consequences and high costs, especially in high-power applications. A novel protection

scheme based on monitoring the flying capacitor voltage is proposed, which can not only prevent the system from unbalanced voltage stresses, but also can protect the system against multiple failures and then save the rest of the components and take corrective action. Moreover, protection can help the designer to locate the origin of the issues as the converter is promptly stopped by protection. Chapter IV categorizes and illustrates the phenomena of the abnormal conditions or faults. The analysis also explains why the flying capacitor voltage is usually slightly higher than half of the input voltage even in normal operation. Solutions to the abnormal conditions are provided. A protection circuit is proposed to implement the protection scheme, along with a detailed design procedure. The proposed protection has been verified in experiment by a real fault and simulated faults.

Finally, all of the proposed concepts and proposed methods have to contribute to a successful high power density converter. In order to achieve compact design and find the potential issues beforehand, a baseline design of hardware implementation is presented. Commercial capacitors are replaced by custom capacitors for the input capacitor, resonant capacitor and output capacitor. A MOSFET module is used instead of discrete MOSFETs for easy connection and elimination of paralleling issues. A nanocrystalline core transformer with an integrated resonant inductor also makes a significant contribution to the volume reduction when compared with a ferrite core and a discrete resonant inductor. The prototype finally achieves 140W/in^3 and is successfully demonstrated by experimental results. Further power density improvement is also evaluated and discussed.

In conclusion, the main contributions of this study include:

1. Achieving a high–power, high–voltage, high-frequency capacitor charging power supply with a breakthrough power density of 140W/in^3.
2. A thorough analysis of the influence of resonant tank structural variations on power density. The methodology based on the structural variations for DC-DC converter design is provided.
3. The advantages of using non-phase shift control instead of phase-shift control in a three-level structure are illustrated in terms of power loss, stress on components and parasitic influence.
4. PLL is introduced for capacitor charging for the first time. Its feasibility is theoretically and experimentally verified. With PLL charging control, the converter can charge the capacitor with a wide range of input voltages while guaranteeing ZVS operation and maximizing power delivery.
5. A novel protection scheme for the three-level structure is proposed to protect against reliability issues and to account for the fact that the charging behavior is always in a transient state.. This protection scheme can not only protect the converter when faults are detected, but also prevent system failure when unbalanced voltage stresses occur. Solutions to the unbalanced voltage stresses are provided as well.

Throughout the entire dissertation, these concepts are interconnected to deliver the highest power density for a high-power capacitor-charging power supply.

6.2.Future work

First, the proposed high-power-density resonant tank design and PLL should be

implemented to achieve a higher-power-density converter design. Due to the unavailable custom design nanocrystalline cores, the proposed MCPFCC leaves a large margin for the transformer with previous design. Therefore the transformer can be optimized for a lower volume with a smaller core size. In addition, PLL control method has been verified with a scale down power level because of a concern of noise interference. A higher power density can be expected by the implementation of new transformer design and PLL charging control.

Secondly the main reason for using a three-level structure is the unavailable high-voltage-rating Si MOSFET with desired loss performance. As the emerging semiconductor power devices such as the SiC JFET and SiC MOSFET mature, their influence on high power density is worth further study and comparison with the current state-of-the-art Si MOSFET. The zero reverse-recovery loss of the SiC Schottky diode also partly proves the superior performance of SiC power devices.

Thirdly, multiple units in parallel are always the preferred option for higher charging capability. Though the PRC has the feature of a current source, which is desired for paralleling without current-sharing, the paralleling characteristics of the three-level parallel resonant converter still need to be investigated when the resonant inductor is integrated into the transformer. A three-phase PRC could be a better choice for increasing power capability. The three-phase PRC can not only keep the benefits of paralleled converters, such as interleaving operation for ripple reduction, but can also reduce the transformer's volume by removing the neutral leg. Further study is needed for the system design and control.

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