An Investigation of Sensitization Conditions and Test Effectiveness for CMOS Faults

by

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(ABSTRACT)

Testing of digital circuits ensures functionality and reliability of the circuits. Previous research has addressed the inadequacies of conventional test methods based on line stuck-at faults in testing CMOS circuits and has proposed new test methods. In this research, the effectiveness of propagation delay testing for open and short faults and supply current monitoring for short faults is investigated. Representative circuits are modeled and simulated over a wide range of fault severities. Factors, such as circuit and fault features, that affect test effectiveness are evaluated and analyzed. From the results, general conclusions are drawn and future research is proposed.

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Table of Contents

Chapter 1. Introduction 1

Chapter 2. CMOS Faults and Test Methods 4

2.1 Fault Models 5

2.1.1 Defects 5

2.1.2 Open Fault 6

2.1.3 Short Fault 6

2.1.4 Difference From Stuck-at Fault 6

2.2 Testing CMOS Faults 7

2.2.1 Testing Open Faults 7

2.2.2 Testing Short Faults 8

2.3 Circuit Models 9

2.3.1 Gate-Level Models 10

2.3.2 Switch-Level Models 10

2.3.3 Transistor-Level Models 10

2.4 Objectives of This Research 11

Chapter 3. Simulation and Measurement Methodology **12**

3.1 Transistor-Level Fault Modelling 13

3.2 Test Stimuli 14

3.3 Simulation 14

3.3.1 Process Parameters 15

3.4 Simulator 15

3.5 Measurements 17

3.5.1 Transition Delay Measurement 17

3.5.2 Supply Current Measurement 19

3.6 Test Effectiveness 21

3.6.1 Fault Severity 21

3.6.2 Differentiation 22

3.6.3 Effectiveness 23

Chapter 4. Results For Combinational Logic Circuits **26**

4.1 Inverter Chain 27

4.1.1 Circuit Characteristics 27

4.1.2 Fault Locations 27

4.1.3 Test Stimuli and Fault Sensitization 28

4.1.3.1 Open Fault 28

4.1.3.2 Short Fault 28

4.1.4 Results 29

4.1.4.1 Open Fault 29

4.1.4.2 Short Fault 29

4.1.5 Observations 30

4.1.5.1 Open Fault 31

4.1.5.2 Short Fault 31

4.1.6 General Conclusions 32

4.2 Four-bit Ripple Carry Adder 32
4.2.1 Circuit Characteristics 32
4.2.2 Fault Locations 33
4.2.3 Test Stimuli and Fault Sensitization 33
4.2.3.1 Open Fault 34
4.2.3.2 Short Fault 34
4.2.4 Results 34
4.2.4.1 Open Fault 35
4.2.4.2 Short Fault 35
4.2.5 Observations 36
4.2.5.1 Open Fault 36
4.2.5.2 Short Fault 36
4.2.6 General Conclusions 37
4.3 8-to-3 Priority Encoder 37
4.3.1 Circuit Characteristics 37
4.3.2 Fault Locations 39
4.3.3 Test Stimuli and Fault Sensitization 39
4.3.3.1 Open Fault 40
4.3.3.2 Short Fault 40
4.3.4 Results 40
4.3.4.1 Open Fault 40
4.3.4.2 Short Fault 41
4.3.5 Observations 41
4.3.5.1 Open Fault 41
4.3.5.2 Short Fault 42
4.3.6 General Conclusions 43

Chapter 5. Results For Sequential Circuits 44

5.1 Parallel In Serial Out Register 45
5.1.1 Circuit Characteristics 45
5.1.2 Fault Locations 46
5.1.3 Test Stimuli and Fault Sensitization 46
5.1.3.1 Open Fault 47
5.1.3.2 Short Fault 47
5.1.4 Results 47
5.1.4.1 Open Fault 48
5.1.4.2 Short Fault 48
5.1.5 Observations 49
5.1.5.1 Open Fault 49
5.1.5.2 Short Fault 50
5.1.6 General Conclusions 51
5.2 Eight-bit Up/Down Counter 52
5.2.1 Circuit Characteristics 52
5.2.2 Fault Locations 54
5.2.3 Test Stimuli and Fault Sensitization 54
5.2.3.1 Open Fault 56
5.2.3.2 Short Fault 56
5.2.4 Results 57
5.2.4.1 Open Fault 57
5.2.4.2 Short Fault 58
5.2.5 Observations 59
5.2.5.1 Open Fault 59
5.2.5.2 Short Fault 60
5.2.6 General Conclusions 61
5.3 Bit-Serial Adder (FCMOS Logic) 63
5.3.1 Circuit Characteristics 63

5.3.2 Fault Locations 64
5.3.3 Test Stimuli and Fault Sensitization 64
5.3.3.1 Open Fault 65
5.3.3.2 Short Fault 65
5.3.4 Results 65
5.3.4.1 Open Fault 66
5.3.4.2 Short Fault 66
5.3.5 Observations 67
5.3.5.1 Open Fault 67
5.3.5.2 Short Fault 68
5.3.6 General Conclusions 69
5.4 Bit-Serial Adder (Domino Logic) 70
5.4.1 Circuit Characteristics 70
5.4.2 Fault Locations 71
5.4.3 Test Stimuli and Fault Sensitization 72
5.4.3.1 Open Fault 72
5.4.3.2 Short Fault 73
5.4.4 Results 73
5.4.4.1 Open Fault 74
5.4.4.2 Short Fault 74
5.4.5 Observations 75
5.4.5.1 Open Fault 75
5.4.5.2 Short Fault 76
5.4.6 General Conclusions 77

Chapter 6. Analysis of Results and Implications for Test 78
6.1 Strengths and Limitations for Test Methods 78
6.1.1 Propagation Delay Test 79

6.1.2 Supply Current Test 80
6.2 Circuit Features Affecting Test 81
6.2.1 Combinational Circuits 81
6.2.2 Sequential Circuits 82
6.3 Fault Features Affecting Test 83

Chapter 7. Summary 84

Bibliography 86

Appendix A. Circuit Diagrams 90

Appendix B. Test Effectiveness Results 101

Vita 123

List of Illustrations

Figure 1. Process parameters for two-micron CMOS technology from MOSIS. 16

Figure 2. Deviation of transition delay for RELAX versus SPICE. 18

Figure 3. Definitions of propagation delay measurement. 20

Figure 4. Graphical depiction of effectiveness metrics. 25

Figure 5. The UP(t) waveform with respect to the ϕ_1(t) waveform. 55

Figure 6. Inverter chain 91

Figure 7. Four-bit ripple carry adder 92

Figure 8. 8-to-3 priority encoder. 93

Figure 9. (a) One bit of priority assignment element, and (b) encoding element. 94

Figure 10. Four-bit parallel in serial out register 95

Figure 11. Fault modelling at 96

Figure 12. Schematic of bit-cell i in the 8-bit up/down counter 97

Figure 13. Open and short faults in 98

Figure 14. Bit-serial adder. 99

Figure 15. Domino logic full adder 100

Figure 16. Delay differentiation for open fault in inverter chain. 102

Figure 17. Delay differentiation for short fault in inverter chain. 103

Figure 18. Current differentiation for short fault in inverter chain 104

Figure 19. Delay differentiation for open fault in four-bit RCA. 105

Figure 20. Delay differentiation for short fault in four-bit RCA. 106

Figure 21. Current differentiation for short fault in four-bit RCA. 107

Figure 22. Delay differentiation at node $A_0(t)$ for open fault in priority encoder. 108
Figure 23. Delay differentiation at node $A_0(t)$ for short fault in priority encoder. 109
Figure 24. Current differentiation for short fault in priority encoder. 110
Figure 25. Delay differentiation for open fault in parallel in serial out register 111
Figure 26. Delay differentiation for short fault at A_1 at clock speed of 112
Figure 27. Delay differentiation for short fault at A_2 at clock speed of 113
Figure 28. Current differentiation for short fault at clock speed of 114
Figure 29. Delay differentiation for open fault in up/down counter 115
Figure 30. Current differentiation for short fault in up/down counter. 116
Figure 31. Delay differentiation for open fault: 117
Figure 32. Delay differentiation for open fault: 118
Figure 33. Current differentiation for short fault in bit-serial adder (FCMOS logic). 119
Figure 34. Delay differentiation for open fault: 120
Figure 35. Delay differentiation for open fault: 121
Figure 36. Current Differentiation for short fault in bit-serial adder (domino logic). 122

List of Tables

Table 1. Clock frequency for different cases 49

Table 2. Resistor range for different Δ values 58

Table 3. Slack for different cases 67

Table 4. Resistor range for different Δ values 75

Chapter 1. Introduction

An accurate evaluation of tests is essential to ensure test efficiency and the quality of digital integrated circuits (ICs). Conventional methods to determine if a fault is tested, although often computationally complex, are relatively straight forward when a standard line stuck-at model is assumed. Recent research has focused on the inadequacies of stuck-at test sets when applied to complementary metal-oxide semiconductor (CMOS) ICs [1].

Different manufacturing technologies introduce different physical defects that need different fault models and test methods. In CMOS technology, physical defects can be modeled as open and short faults. Open faults model broken or low conduction between circuit nodes. Their severity is high when the conduction is low. Short faults model the existence of an unwanted current path created between two nodes. Severity increases with the increase of conductivity in short faults. Open and short faults may or may not affect the circuit performance depending on several factors, such as severity, fault propagation length, circuit depth, combinational versus sequential nature of the circuit, clock speed, and slack.

Together with the introduction of new fault models, new test procedures have also been developed in this thesis. Propagation delay testing [2] and supply current monitoring [3] are two test approaches for detecting CMOS faults. In propagation delay testing, the transition delay

at an observable output of the circuit under test (CUT) is compared with the transition delay of a fault-free circuit. An increase in transition delay indicates a fault. In supply current monitoring, the steady state supply current of the CUT is compared with the current of a fault-free circuit. An increase in current indicates a fault.

The introduction of propagation delay test and supply current monitoring complicates the analysis of test effectiveness. This research examines the effectiveness of propagation delay test and supply current monitoring over a wide range of fault severities. Several circuit features and factors affecting the effectiveness of these tests are analyzed and evaluated from the results. Finally, general conclusions are drawn from the analysis.

To study the effectiveness of both propagation delay test and supply current test, representative circuits with different circuit features are considered. For each circuit investigated, open and short faults are considered and the circuits are simulated over a wide range of fault severities. Open faults are modeled with an open resistor in a conducting path of the circuit, and short faults are modeled with a short resistor connecting two nodes in the circuit. Appropriate test vectors are selected to test the fault.

Propagation delay testing is considered for both open and short faults. In propagation delay test, the transition delay is propagated to the observable outputs and measured there. Supply current monitoring is used only with the short faults. In supply current test, steady state supply current is measured when the test vector is applied. The measurements are made for fault severities ranging from the fault-free condition to the most severe fault condition not resulting in stuck-at behavior.

From the measurement of delay and current due to faults of different severities, differentiation of transition delay and supply current measurements can be plotted versus fault severity for each circuit. Differentiation is denoted as the difference between the faulty measurement and the fault-free measurement divided by the fault-free measurement. The effectiveness of

propagation delay test and supply current test is evaluated and analyzed based on the circuit features. Test effectiveness denotes how well a test detects faults. Conclusions are drawn from the analysis based on the simulation results. The conclusions indicate relationships between test effectiveness and circuit features and between test effectiveness and fault features.

Propagation delay increases with an increase in fault severity. The increase is significant in circuits with a short propagation path from the fault to an observable output. The increase becomes insignificant when the propagation path is long. In addition to length of propagation path, circuit depth also affect test effectiveness. Deep circuits have many transistors in series from V_{DD} to output node or from output node to V_{SS} and shallow circuits have small number of transistors in series. In general, faults in shallow circuits are harder to detect than faults in deep circuits due to the strong pull-up or pull-down ability of the shallow circuit. In combinational circuits, stuck-at behavior occurs when the gate output does not change value. In sequential circuits, stuck-at behavior can also be detected when the transition delay is larger that the designated pulse width of the clock. Therefore, faults are easier to detect using propagation delay test when the clock speed is faster.

In general, short faults raise the steady-state supply current of the circuit. The current is larger for a more severe fault. Supply current test is also more effective in testing short faults than propagation delay test. The measurement of supply current, however, has to be performed using slow clock speed to allow the current to settle to a steady state.

Chapter 2 provides details of CMOS faults and test methods. Chapter 3 describes the simulation and measurement methodology used in this research. Circuit descriptions, results and observations are given for three combinational circuits in Chapter 4 and for four sequential circuits in Chapter 5. Chapter 6 discusses general observations about test effectiveness based on the results. Chapter 7 summarizes the thesis. Circuit diagrams are provided in Appendix A. Appendix B containing detailed results.

Chapter 2. CMOS Faults and Test Methods

As technology progresses, the minimum transistor size has been reduced. As transistors in integrated circuits become smaller, more transistors can be integrated into a single die. As a result, today's integrated circuit can perform more functions than earlier integrated circuits.

As the complexity of an integrated circuit increases, the circuit is more susceptible to failure due to faults. At the same time, high reliability is required for integrated circuits fabricated today. Testing and design for testability therefore become necessities in the production of integrated circuits.

Since the introduction of integrated circuits, there has been much research and investigation of fault detection for integrated circuits. Traditionally, stuck-at faults were assumed in testing digital circuits. Today, the stuck-at fault model is still widely used in fault detection and test generation at the behavioral and gate levels [4,5,6]. With the introduction of CMOS circuits, however, the stuck-at fault was found to be inadequate in modelling faults in CMOS circuits [7,8,9,10,11]. As a result, R. L. Wadsack introduced the stuck-open fault model in 1978 for testing CMOS circuits [1]. The bridging fault model was introduced by other researchers and can be traced back to A. D. Friedman [12].

This research investigates a general case of stuck-open faults and bridging faults. For simplicity, the faults are called open faults and short faults.

With the introduction of open and short faults, new test procedures have been developed. Propagation delay testing and supply current monitoring are two proposed approaches. In propagation delay testing, transition delay of faulty gate is propagated to the observable output. The measured propagation delay is compared to a known fault-free value. In supply current monitoring, steady state supply current is measured and compared to a known fault-free current value.

2.1 Fault Models

This section introduces fault models based on physical defects in integrated circuits.

2.1.1 Defects

Defects depend on the manufacturing technology. Defects in today's CMOS technology can be divided into two categories: global defects and localized defects [13]. Different factors result in different types of defects. For example, cracks on the wafer introduce global defects. Global defects can usually be detected during processing or by inspection. Localized defects, caused by factors such as impurities on a wafer or improper deposition of materials, can only be detected during testing.

2.1.2 Open Fault

Open faults can be caused by an insufficient deposition of conducting materials or the existence of non-conducting impurities [14,15]. A severe open fault completely breaks a necessary conduction path in the circuit. For a less severe fault condition, an open fault only reduces the conductivity of the path.

An open fault is modelled with a resistor, R_o, connecting two nodes along the same path. The severity of the open fault is increased by raising the open resistor value.

2.1.3 Short Fault

Short faults can be caused by an unwanted deposition of conducting materials or existence of conducting impurities [16]. A short in the circuit creates a conducting bridge between two nodes. For a less severe fault condition, a short fault creates a low conduction bridge between two nodes. For a more severe fault condition, the conduction increases. For the most severe fault condition, the bridge is perfectly conducting.

A short fault is modelled with a resistor, R_s, connecting two different nodes. The severity of the short fault is increased by reducing the short resistor value.

2.1.4 Difference From Stuck-at Fault

In general, open and short faults are different from line stuck-at faults. In the line stuck-at fault model, the affected node produces a constant logic 0 or a logic 1. The severity of a stuck-at fault is either 0 or 1. In CMOS faults, the faulty gate may cause a certain magnitude of in-

crease in propagation delay and/or supply current. The severity of open and short faults range continuously from 0 to 1.

A complete open at a gate output line or a complete short between two gate outputs produces a stuck-at fault. For the most severe open or short faults considered in this research, stuck-at behavior also occur. However, open or short faults can occur at any transistor and shorts can happen between any two or more internal nodes in a gate.

2.2 Testing CMOS Faults

Not only CMOS faults are different from stuck-at faults; stuck-at tests are inadequate for testing CMOS faults. In testing a stuck-at fault, the line is driven to the opposite logic value. In the presence of CMOS faults, the gate behaves as a memory element and the output may or may not be driven to the desired value, depending on the previous value at the gate output.

Two primary test methods have been developed to detect open and short faults in CMOS circuits. The use of these two methods, propagation delay testing and supply current monitoring, to detect open and short faults is discussed below.

2.2.1 Testing Open Faults

R. L. Wadsack introduced the stuck-open fault in 1978 [1]. He and other researchers observed that a stuck-open fault in a combinational CMOS circuit converts the circuit into a sequential circuit [17,18]. A two pattern test, $<T_1, T_2>$, was proposed to test stuck-open faults [19,20].

The initialization vector, T_1, presets the output of gate under test to a known logic value. The test vector, T_2, drives the gate output to the opposite logic value.

In testing open faults in the n-network, the initialization vector is selected to turn off the n-network and the test vector is applied to create a conduction path in the n-network. Similarly, in testing open faults in the p-network, the initialization vector turns off the p-network and the test vector turns on a path in the p-network. A transition occurs almost immediately at the gate output of a fault-free circuit. In the presence of an open fault, the conduction of the path is reduced and thus the transition is slow, if it occurs at all, and a large delay occurs. The increase in transition delay or stuck-at behavior is propagated to an observable output. Propagation delay test, therefore, can be used to test stuck-open faults. Propagation delay test is also referred as AC parametric test [18].

Stuck-open faults in complex gates have been found to be hard to detect due to charge sharing and input timing delay [21,22]. As a result, Reddy, Reddy and Kuhl [21] proposed a circuit modification with two additional transistors and a three pattern test for stuck-open faults. Another modification with four transistors and a two pattern test is also proposed in the same paper. Rajsuman, Jayasumana and Malaiya [23] further improved the modification with two transistors so that only a single input pattern is needed in testing open faults. Since one pattern is applied, the effect of input time delay is eliminated. This method also reduces the test application time by 50 percent.

2.2.2 Testing Short Faults

The short fault model can be traced back to 1974 when A. D. Friedman discussed shorts in combinational circuits [12]. Today, in CMOS technology, shorts can happen between any two or more internal nodes. In a fault-free CMOS circuit, when the p-network (n-network) is on,

the n-network (p-network) is off. There is no current path between V_{DD} and V_{SS}. As a result, a fault-free circuit draws almost no current during steady state.

In the presence of a short fault at the p-network (n-network), the short creates a current path from the gate output to V_{DD} (V_{SS}). If the n-network (p-network) is on at the same time due to the input vector, current flows from V_{DD} to the gate output and from the gate output to V_{SS}. A current path is thus established and a large current is drawn during steady state. As a result, a short fault is detected by observing a large supply current during steady state [3,24].

Although the probability of a fault being a short has been estimated to be about 30 percent [13], short faults did not draw much attention among the test community because test patterns for testing open faults in the p-network of an FCMOS implementation are the same as test patterns for testing short faults in the n-network and vice versa [14].

Therefore, propagation delay test can also be used in testing short faults. To detect short faults in the n-network (p-network), the initialization vector turns on a path in the n-network (p-network) and the test vector turns off the n-network (p-network). The output of the fault-free circuit rises (falls) immediately. In the presence of short faults, the output of the faulty circuit rises (falls) more slowly.

2.3 Circuit Models

Test generation for open and short faults in CMOS circuits can be performed using several levels of circuit models. This section discusses gate-level, switch-level, and transistor-level models.

2.3.1 Gate-Level Models

Gate-level modelling was first introduced by El-Ziq and other investigators [25]. Tests for open faults at the gate level are modified from tests for stuck-at faults [26,27,28,29]. However, gate-level models do not provide information about timing and output logic strength. The internal view of gates are also unknown, which reduces test accuracy.

2.3.2 Switch-Level Models

For a more realistic test, switch-level models were proposed [2,30,31,32,33,34,35]. An ideal MOS transistor behaves like a switch, either conducting (ON) or not conducting (OFF). An open fault is modelled as a permanent OFF at the switch [36] or a break in a connection, while a short fault is modelled as a permanent ON switch or an extra connection in the circuit.

Switch-level fault simulation may use multiple values to represent output behavior [37,38,39]. However, timing information is unavailable. Hayes modified the switch-level representation of a transistor with a resistor in series and a capacitor in parallel with the switch [40]. In this way, the RC network provides a more realistic model for timing simulation. New algorithms have been developed for switch-level simulation and test generation [41,42].

2.3.3 Transistor-Level Models

Switch-level behavior is far from the actual behavior of physical circuits. The fabrication parameters are not considered in switch-level models. A closer look at circuit behavior requires use of a transistor-level model [43,44,45]. In simulation at the transistor-level, accurate volt-

age and current values are calculated with model equations taking into account geometrical and processing parameters. Transient conditions are also calculated. Because of the extensive calculations, simulation at the transistor-level takes a long time [46].

2.4 Objectives of This Research

In previous work, the effectiveness of test methods has been measured using fault coverage. Fault analysis [13,47] and statistical approaches [48,49,50,51] for timing delay analysis have also been used. Supply current measurement has been performed in detecting defects in fabricated integrated circuits [52,53]. However, there is no research on how effective a test is in measuring propagation delay and steady state supply current of circuits with different characteristics. Different circuits with different characteristics may produce different behavior in the presence of faults. Different behavior results in different test effectiveness. This research investigates the behavior of different circuits for a wide range of fault severities for a set of representative circuits having different characteristics. From the behavior of the circuit due to the presence of faults, insight into test effectiveness can be gathered. General conclusions can thus be made about test effectiveness for circuits having different characteristics.

Chapter 3. Simulation and Measurement Methodology

The behavior of a circuit in the presence of fault of different severity is found from simulation. In this research, simulation is performed at the transistor level to observe the transition delay at observable outputs and the steady-state supply current of the circuit.

Circuits are designed and transformed into appropriate circuit description files, such as SPICE circuit description files. Open and short faults are introduced in selected locations in each circuit. Fault severities are changed by varying the resistor value.

In propagation delay test, specific input vectors are needed to propagate the transition delay from the faulty gate to the observable output. In current monitoring, an input vector is applied to turn off the sensitized path and to create two different voltages at the shorted nodes so that current flows along the shorted path.

For every circuit, simulations are performed using appropriate input vectors, from fault-free condition to the most severe fault condition. The behavior of faulty circuits are compared with

the behavior of the fault-free circuit. The difference in behavior between faulty circuits and the fault-free circuit are used for test effectiveness evaluation.

The remainder of this chapter provides a detailed description of the methodology and test effectiveness definition used in this research.

3.1 Transistor-Level Fault Modelling

In transistor-level fault modelling, an open fault is modelled with an open resistor, R_o, connecting two nodes. In that way, the conduction along the sensitized path is reduced. A low resistor value for R_o represents low fault severities. The severity of an open fault is raised by increasing the resistor value. When the resistor value is high, the sensitized path is totally cut off [54].

A short fault is modelled with a short resistor, R_s, connecting two nodes in the circuit. A short creates a current path between the shorted nodes. A high resistor value for R_s represents low fault severities. The severity is increased by lowering the resistor value. When the resistor value is low, the shorted path conducts perfectly.

In a fully-complementary implementation, an open fault model in the p-network has a corresponding short fault model in the n-network which produces the same behavior, and vice versa. Similarly, a test for any open fault in the p-network can also test the corresponding short fault in the n-network, and vice versa. As a result, an open fault and a short fault in this research are introduced only in the n-network of all circuits considered. A detailed description of the fault location in each circuit is given in the next two chapters.

3.2 Test Stimuli

To test an open fault in the n-network, the first, or initialization vector, turns off the n-network to produce a 1 at the gate output. The second, or test vector, turns on the sensitized path in the n-network to produce a fall at the gate output. All other paths in the n-network are kept off throughout the test.

To test a short fault in the n-network, the initialization vector is applied to turn on the sensitized path in the n-network. The test vector turns off the sensitized path to produce a rise at the gate output. The test vector also creates a potential difference between the shorted nodes. All other paths in the n-network are also kept off throughout the test.

The transition delay at the faulty gate output is propagated to the observable output nodes with an appropriate input vector. Several test invalidation factors such as input time skew and charge sharing [19] are taken into consideration when selecting input vectors.

3.3 Simulation

A circuit description file is written with appropriate descriptions of input waveforms and process parameters in the format recognized by the circuit simulator.

For each circuit, the fault-free circuit is simulated first. In subsequent simulations, the severity of the fault is increased until stuck-at behavior occurs.

3.3.1 Process Parameters

Process parameters used in the simulation are based on the two-micron scalable CMOS technology provided by the University of Southern California Information Sciences Institute [55]. The parameters used for all simulations are given in Figure 1.

3.4 Simulator

In this research, two circuit simulators were used. In the early stage of the research when the circuit size was small, SPICE3b1 [56] was used on VAXstation running ULTRIX to perform the simulation. When the circuits become larger and more complex, SPICE exhibited well-known convergence problems. The simulation time of SPICE also increases exponentially as the number of transistor increases. The convergence problems can be partially solved by raising error tolerance, but the simulation time is not reduced.

Another circuit simulator, RELAX [57] was thus used. RELAX 2.3 is about five times faster than SPICE3b1. The advantages and disadvantages of RELAX compared to SPICE are described below.

RELAX has several disadvantages for transistor-level simulation.

1. There are not many component descriptions available in RELAX compared to SPICE. For example, a bipolar junction transistor description is not available.
2. The model definition in RELAX uses fewer processing and material parameters than the model definition in SPICE, which results in less accurate simulations.
3. No information about supply current is provided by RELAX.

```
*TECHNOLOGY: SCP                          FEATURE SIZE: 2.0um
*M88K  SPICE PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 LD=0.351807U TOX=409.000000E-10
+ NSUB=2.262929E+16 VTO=1.044 KP=5.178000E-05
+ GAMMA=1.03029 PHI=0.6 UO=613.34 UEXP=0.145054
+ UCRIT=65543.9 DELTA=1.000000E-06 VMAX=71075.1
+ XJ=0.250000U LAMBDA=2.413533E-02 NFS=1.225648E+12
+ NEFF=1 NSS=1.000000E+12 TPG=1.000000 RSH=21.530001
+ CGDO=2.970146E-10 CGSO=2.970146E-10 CGBO=5.318802E-11
+ CJ=4.116000E-04 MJ=0.438200 CJSW=5.949000E-10
+ MJSW=0.371300 PB=0.840000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.06 um

.MODEL CMOSP PMOS LEVEL=2 LD=0.419496U TOX=409.000026E-10
+ NSUB=1.173988E+16 VTO=-0.853937 KP=2.361000E-05
+ GAMMA=0.74208 PHI=0.6 UO=279.682 UEXP=0.361736
+ UCRIT=37757.5 DELTA=1.000000E-06 VMAX=33016.8
+ XJ=0.250000U LAMBDA=7.536808E-02 NFS=8.719274E+11
+ NEFF=1.001 NSS=1.000000E+12 TPG=-1.000000 RSH=75.830005
+ CGDO=3.541613E-10 CGSO=3.541613E-10 CGBO=1.764491E-10
+ CJ=2.397000E-04 MJ=0.389300 CJSW=2.970000E-10
+ MJSW=0.155400 PB=0.570000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.21 um
```

Figure 1. Process parameters for two-micron CMOS technology from MOSIS.

RELAX can be used for this research since it provides component descriptions needed for modelling CMOS circuits and the information about supply current can be obtained by circuit modification. To determine supply current, a 1 Ω resistor is inserted between the power supply and the V_{DD} node of the circuit. The voltage across the resistor is the supply current. Since the ON resistance of a p-channel or n-channel transistor is on the order of hundreds of Ωs, a 1 Ω resistor has little influence on the total circuit performance. As mentioned above, convergence problem in SPICE can be solved partially by setting a larger error tolerance. This, however, reduces the accuracy of simulation and thus reduces the advantages of using SPICE over RELAX. Even with a large error tolerance, SPICE takes a longer for a simulation than Relax. To compare results, an inverter chain was constructed and simulated over a wide range of fault severities. The deviation is calculated as the difference between SPICE results and RELAX results devided by SPICE results. The difference and deviation of RELAX output from SPICE output is given in Figure 2. Note that the deviation is quite small.

3.5 Measurements

From the simulation results, two types of measurement are determined. In propagation delay test for both open and short faults, the transition delay at the observable output nodes are recorded. Steady state supply current is also monitored in supply current test for short faults.

3.5.1 Transition Delay Measurement

From the output waveform, the transition time is recorded. The transition time of a signal is defined as the time at which the signal reaches 0.9 of its total voltage swing. For example, a rise time is the time at which the signal rises to 0.9 of its total voltage rise. Similarly, a fall

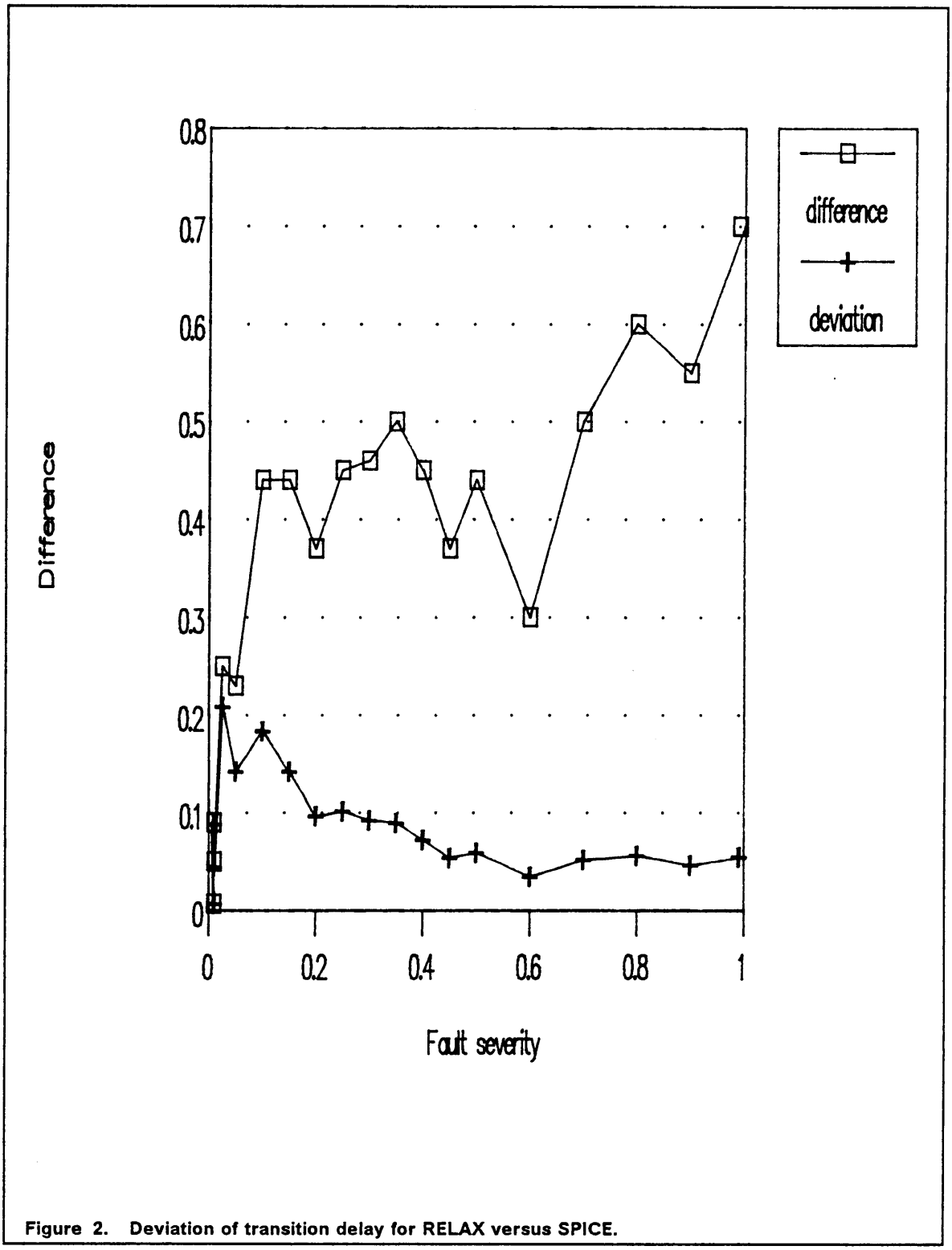

Figure 2. Deviation of transition delay for RELAX versus SPICE.

time is the time at which the signal falls 0.9 of its total voltage drop. For the output of a fault-free circuit with a voltage of 5 volts and a minimum voltage of 0 volt, the rise time is the time at which the signal rises to 4.5 volts and the fall time is the time at which the signal falls to 0.5 volts. The definitions are provided in Figure 3.

Transition delay, τ_d, is defined as the interval between the input transition time and the output transition time of a combinational circuit. For sequential circuits, τ_d is defined as interval between the rise time of the activating clock pulse and the transition time of the output. The increase in time delay, δ_τ, is measured as the increase in transition delay at output nodes of faulty circuits when compared to the transition delay of a fault-free circuit.

3.5.2 Supply Current Measurement

For the supply current test, supply current, I_{DD}, is measured during steady state when the current path is conducting. In simulations using SPICE, the measurement is obtained as the current across a dummy voltage source of 0 volt which connects the 5 volt voltage source and the V_{DD} node of a circuit. In simulations using RELAX, the dummy voltage source is replaced with a 1 Ω resistor. Supply current is determined based on the voltage drop across the resistor.

The increase in steady state supply current, δ_I, is measured as the increase in supply current of faulty circuits above the supply current of a fault-free circuit.

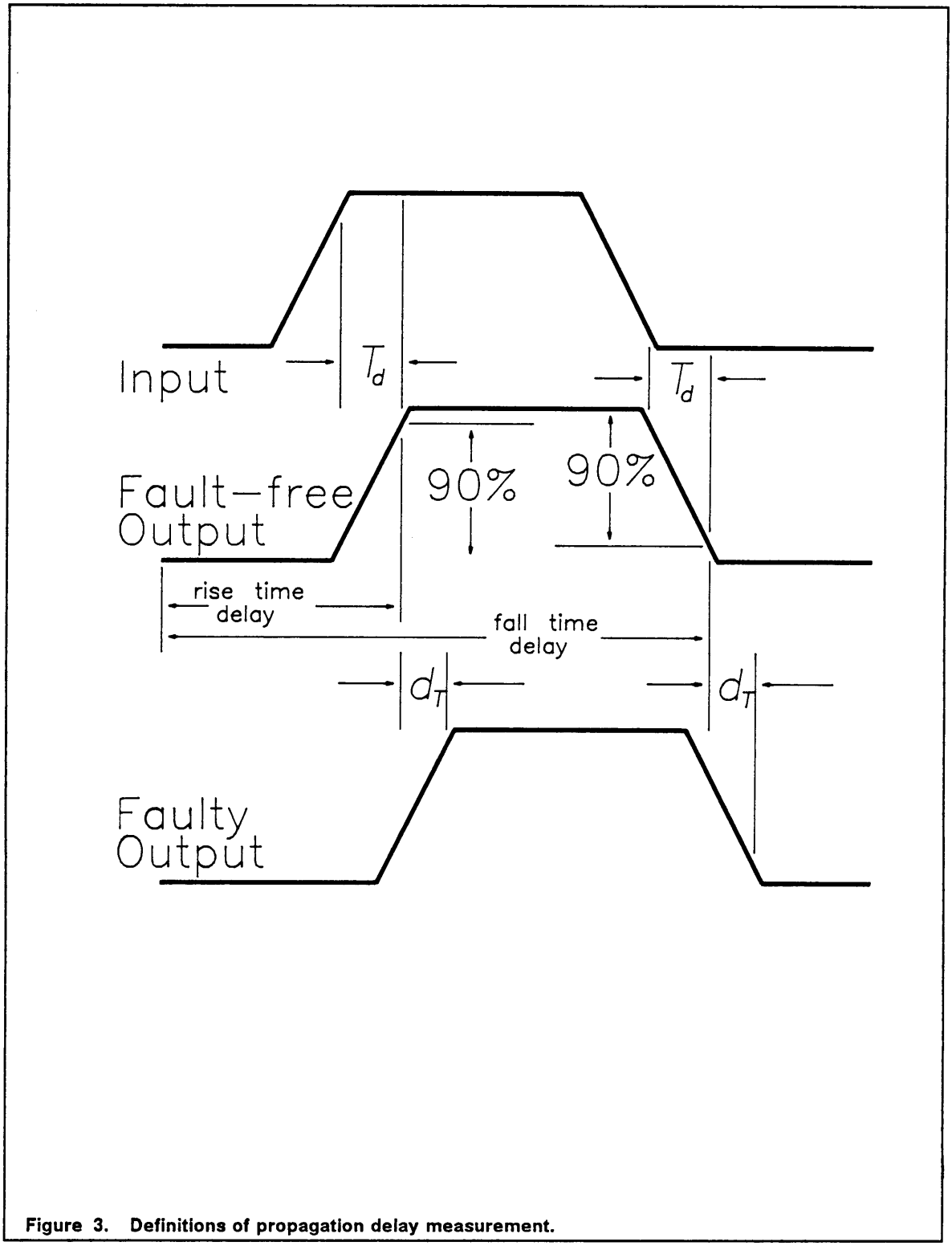

Figure 3. Definitions of propagation delay measurement.

3.6 Test Effectiveness

This research investigated open and short faults over a wide range of fault severities. The measurements for a faulty circuit are compared to the measurements for the fault-free circuit. The difference at each fault severity is calculated and plotted. Two effectiveness metrics are defined to evaluate the effectiveness of a test. A more detailed definition is given in [58].

3.6.1 Fault Severity

Fault severity, S, indicates the relative severity of a fault when compared to the most severe CMOS fault beyond which stuck-at behavior occurs. The range of S is between 0 and 1, with 0 being the fault-free condition and 1 indicating the most severe fault condition, beyond which stuck-at behavior occurs. For example, an open fault with S = 1 corresponds to the highest open resistance value, beyond which stuck-at behavior occurs. For a short fault, S = 1 indicates the lowest short resistance value below which stuck-at behavior occurs. For an open fault, fault severity is thus defined as

$$S = \frac{R_o}{R_{o(h)}} \qquad [3.1]$$

where $R_{o(h)}$ is the highest open resistor value beyond which stuck-at behavior occurs.

For a short fault, fault severity is defined as

$$S = \frac{R_{s(l)}}{R_s} \qquad [3.2]$$

where $R_{s(l)}$ is the lowest short resistor value beyond which stuck-at behavior occurs.

Let S_A be the maximum acceptable severity of a fault and S_T be the minimum severity of a fault that can be detected by a test T. The range of test T, R indicates the ability of the test to detect the presence of an unacceptably severe fault. The range of test T is given by

$$R = \frac{1 - S_T}{1 - S_A} \qquad [3.3]$$

If the test can detect any fault of severity greater than S_A, then $R = 1$ or the test is 100 percent efficient. If S_T is less than S_A, the test is too sensitive and may reject a circuit that has acceptable defects. If S_T is greater than S_A, the range of test T is less than 1 and the test may fail to detect some unacceptable defects.

3.6.2 Differentiation

The differentiation is the fraction of increase in the measure for the faulty circuit above the expected value of the measurement in a fault-free circuit.

Suppose that a test T requires measurement M to be made. M might be a measure of transition delay τ_d in delay testing or steady-state supply current I_{DD} in current testing. For both, the measurement increases monotonically with the fault severity. Let M_G be the maximum value of the measurement expected for a fault-free circuit and M_F denote the minimum value of the measurement expected for a faulty circuit. Since the value of measurement depends on fault severity, the differentiation also depends on fault severity and is given by

$$D(S) = \frac{M_F(S) - M_G}{M_G} \qquad [3.4]$$

For propagation delay test, delay differentiation is used and defined as the ratio of increase in delay due to a fault and the transition delay of a fault-free circuit. Delay differentiation is thus denoted as

$$DD(S) = \frac{\delta_\tau(S)}{\tau_d} \qquad [3.5]$$

For supply current test, current differentiation is used and defined as the ratio of increase in supply current due to a fault and the steady-state supply current of a fault-free circuit. Current differentiation is therefore given as

$$CD(S) = \frac{\delta_{I_{DD}}(S)}{I_{DD}} \qquad [3.6]$$

3.6.3 Effectiveness

Test effectiveness evaluates how good or bad a test performs using delay differentiation or current differentiation. Two effectiveness metrics, range effectiveness and differentiation effectiveness, are defined to evaluate and compare tests considering two possible criteria.

The range effectiveness of a test assumes a fixed minimum acceptable difference, D_A, between the fault-free circuit and the observed measurement on which to base the failure of the circuit under test. D_A is set based on performance criteria such as propagation delay and supply current. The range effectiveness of the test is simply the range of fault severities that can be detected given D_A. For a given test T, define S_T to be minimum severity such that $D(S_T) = D_A$. Differentiation below D_A is considered acceptable and differentiation above D_A is unacceptable. The range effectiveness is then denoted as

$$E_R = 1 - S_T \qquad [3.7]$$

Figure 4 shows values for D_A and corresponding S_T. The range effectiveness, E_R, is also shown in Figure 4.

The differentiation effectiveness of a test assumes that there is a maximum acceptable fault severity, S_A. S_A may be set based on process parameters and circuit or device simulation results. Defects with severity larger than S_A are unacceptable and defects with severity lower than S_A are accepted. The differentiation effectiveness measures the minimum difference between the measurement for a fault-free circuit and the circuit with a fault of severity greater than or equal to S_A. For a given test T, define differentiation D_T such that $D_T = D(S_A)$. The differentiation effectiveness is then defined as

$$E_D = D_T = \frac{M_F(S_A) - M_G}{M_G} \qquad [3.8]$$

Figure 4 also shows values for D_T and S_A, and differentiation effectiveness, E_D.

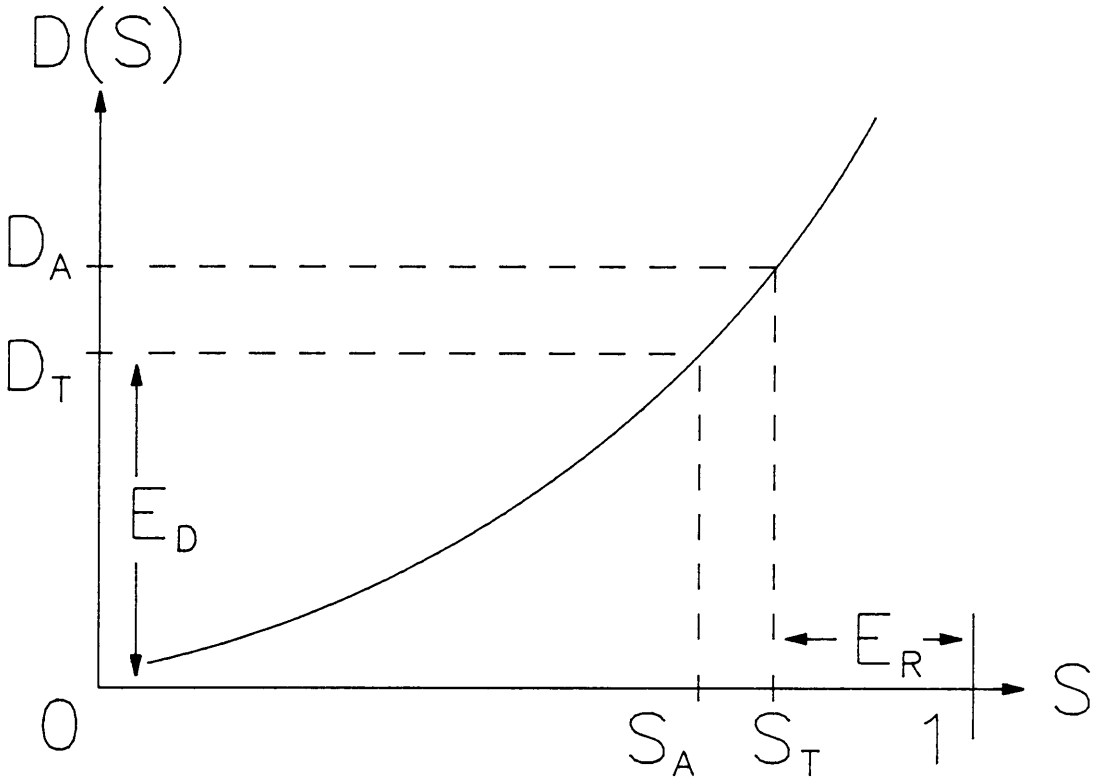

Figure 4. Graphical depiction of effectiveness metrics.

Chapter 4. Results For Combinational Logic Circuits

In integrated circuits, combinational circuits plays an important role in function implementation. Strictly speaking, almost all integrated circuits are composed of combinational circuits since sequential circuits can be viewed as combinational circuits with clock pulses being input signals.

It is known that in the presence of open or short faults, a combinational circuit can turn into a sequential circuit by retaining the previous output logic as current output logic and thus causes a large transition delay. The increase in transition delay may be masked out or reduced after the signal is propagated through several stages of gate.

Short fault increases the steady state supply current. The magnitude of increase may be affected by the fault severity and the size of combinational circuit.

Three representative circuits of different characteristics are chosen. All three circuits allow the propagation of signal from faulty gate to observable output nodes. The circuits are

1. inverter chain
2. four-bit ripple carry adder

3. eight-to-three priority encoder

Circuit diagrams are in Appendix A and test effectiveness results appear in Appendix B. The circuits and results are discussed below.

4.1 Inverter Chain

4.1.1 Circuit Characteristics

The inverter chain is composed of a chain of seven inverters as shown in Figure 6. The seventh inverter provides output load at the output node of the sixth inverter. There is one primary input node and one primary output node. When a transition occurs at the primary input, the transition signal is inverted when propagated through each inverter.

4.1.2 Fault Locations

An open fault and a short fault are introduced at the first inverter of the chain. Open resistor, R_o, connects the source of the n-channel transistor and V_{SS} as shown in Figure 6(a). This reduces the conductivity of the n-network during pull-down. The first type of short fault is modelled as shown in Figure 6(a), and the second type of short fault is modelled as shown in Figure 6(b). The type 1 short fault is modelled with a short resistor, R_s, connecting node X and V_{SS}. In the type 2 short fault, R_s connects node X and node Y in different inverter chain.

4.1.3 Test Stimuli and Fault Sensitization

The input $A = <1,0,1>$ is applied to test the open fault and type 1 short fault. To test the type 2 short fault, an input $E = 1$ is added to drive node Y to logic 0.

In a faulty circuit, the transition delay increases. The increase in delay is propagated through the inverter chain and eventually is observed at the primary output node.

4.1.3.1 Open Fault

An open fault in the n-network slows the fall of the first inverter output. The slow fall causes the rise time delay of the second inverter to increase. The increase in transition is propagated to the observable output node. For a more severe open fault, the transition delay at the observable output nodes increases more. When the fault becomes most severe, the output signal at node X does not change; stuck-at behavior occurs at the first inverter and is propagated to the observable output node.

4.1.3.2 Short Fault

A short fault in the n-network creates a current path that pulls against the rise of the inverter output at X. The slow transition is propagated to the observable output node. The current path also carries a large amount of current and thus raises the steady state supply current of the circuit. When the short fault becomes more severe, the current path is more conductive. The output at X rises more slowly and the large transition delay is propagated to the observable output node. At the most severe short fault, the current path is perfectly conducting and the output at X does not rise. Stuck-at behavior is then propagated to the observable output nodes.

4.1.4 Results

Signals at node *B* and node *D* are discussed. Note that node *D* is the observable output.

4.1.4.1 Open Fault

An open resistor, R_o, in this circuit is changed from a low severity value of 1 kΩ to a high severity value of 180 kΩ. An open resistor below 1 kΩ produces insignificant fault severity, while an open resistor above 180 kΩ produces stuck-at behavior.

The delay differentiation for node *B* and node *D* is plotted in Figure 16. For both, delay differentiation increases linearly as the fault severity increases. The delay differentiation at node *B* increases more quickly than the delay differentiation at node *D*. For example, at fault severity 0.2, the delay differentiation is 2.3 at node *B* and is 0.8 at node *D*. When fault severity is 0.6, the delay differentiation at node *B* increases to 6, while the delay differentiation at node *D* increases to only 2. At a fault severity of 1, the delay differentiation at *B* reaches 10 and the delay differentiation at *D* reaches 3.2.

4.1.4.2 Short Fault

A short resistor, R_s, in this circuit is changed from a low value of 5 kΩ to a high value of 100 kΩ. A short resistor below 5 kΩ produces stuck-at behavior and a short resistor above 100 kΩ produces an insignificant increase in delay when compared to the transition delay in a fault-free inverter chain.

Delay differentiation at the two nodes for the type 1 short fault and the type 2 short fault is plotted in Figure 17.

In the type 1 short fault, the delay differentiation at nodes *B* and *D* increases exponentially as the fault severity increases. The delay differentiation at node *B* increases more quickly. At a fault severity of 0.2, the delay differentiation is 0.4 at node *B* and 0.2 at node *D*. At a fault severity of 0.5, the delay differentiation is 2 at node *B* and 0.6 at node *D*. At a fault severity of 0.63, the delay differentiation at node *B* reaches 8.2, while the delay differentiation at node *D* reaches 1.6. Beyond a fault severity of 0.63, stuck-at behavior occurs.

In the type 2 short fault model, the delay differentiation also increases exponentially with fault severity. Again, the delay differentiation at node *B* increases more quickly. At a fault severity of 0.5, the delay differentiation is 1 at node *B* and is 0.4 at node *D*. At fault severity 1, the delay differentiation is 8.4 at node *B* and is 1.8 at node *D*.

The current differentiation for both types of short fault is plotted in Figure 18. The current differentiation for both types increases as the fault severity increases. At a fault severity of 0.3, the current differentiation of the faulty circuit with the type 1 short fault is 12, and the current differentiation of the circuit with the type 2 short fault is 11. At a fault severity of 0.63, the current differentiation for the type 1 short fault increases to 22, and the current differentiation for the type 2 short fault increases to 18. Beyond a fault severity of 0.63, circuit with the type 1 short fault exhibits stuck-at behavior, whereas the circuit with a type 2 short fault has a current differentiation greater than 18, and exhibits stuck-at behavior beyond a fault severity of 1.

4.1.5 Observations

In a fault-free circuit, the transition delay at node *B* is smaller than the transition delay at node *D*. In the event of open or short faults, transition delay of the circuit increases. A small increase in transition delay at node *B* is large when compared to the small transition delay at

node *B* of a fault-free circuit. The same increase in transition delay, however, produces an insignificant increase at node *D* when compared to the large transition delay at node *D* of a fault-free circuit.

4.1.5.1 Open Fault

During pull-down, the n-channel transistor conducts to create a current path between node *X* and V_{SS}. An open fault connecting the source of an n-channel transistor and V_{SS} raises the resistance of the n-network. The conductivity of the n-network is reduced. Node *X* of a faulty circuit takes longer to discharge than node *X* of a fault-free circuit. The fall time delay increases. The slower fall causes the second inverter output node to rise more slowly and the increase in transition delay is eventually propagated to the observable output nodes.

4.1.5.2 Short Fault

A short fault connecting node *X* and V_{SS} creates a current path. When the p-network conducts and the n-network cuts off, node *X* is changed to logic 1 in a fault-free circuit. In a faulty circuit, a short fault pulls against the rise at node *X*. As a result, the rise time delay at node *X* increases. At the same time, the conducting p-network and the short resistor create a current path between V_{DD} and V_{SS}. The steady state supply current increases.

When a short resistor connects between an output node and V_{SS}, the resistor creates a current path from the output node to V_{SS}. When a short resistor connects an output node of a gate with an output node of a second gate which is at logic 0, the short resistor and the ON resistor of the n-channel transistor at the second gate create a conducting path. The total resistor value of the type 2 short fault is larger and, therefore, the strength pulling against the rise is less than the strength of the type 1 short fault. The second type of short fault also draws a smaller

amount of current than the first type of short fault due to a higher total resistor value. As a result, at the same fault severity, the type 1 short fault produces a larger transition delay and draws a larger supply current than the type 2 short fault.

4.1.6 General Conclusions

When there is a short propagation path between the faulty gate and the observable output node, a slight increase in transition delay due to a fault is significant. When the propagation path between the faulty gate and the observable output node is long, the increase in delay due to a fault becomes insignificant when compared to a large delay at a fault-free output.

Also, it is harder to detect a short fault between two output nodes than a short fault between an output node and V_{ss}.

The steady state supply current increases as the short fault becomes more severe.

4.2 Four-bit Ripple Carry Adder

4.2.1 Circuit Characteristics

A four-bit ripple carry adder is composed of a chain of four full adders as shown in Figure 7(a). The carry-out signal of stage 1 is the carry-in signal of stage 2, and so on. Figure 7(b) shows a CARRY gate and Figure 7(c) shows a SUM gate. The complex gates implement the following equations.

$$C_{OUT}(t) = A_{IN}(t) \times B_{IN}(t) + A_{IN}(t) \times C_{IN}(t) + B_{IN}(t) \times C_{IN}(t) \quad [4.1]$$

$$S(t) = A_{IN}(t) \oplus B_{IN}(t) \oplus C_{IN}(t) \quad [4.2]$$

There are nine primary input nodes: A_0 to A_3, B_0 to B_3, and C_0. There are five observable output nodes: S_0 to S_3, and C_4.

4.2.2 Fault Locations

An open fault and a short fault are introduced at the CARRY gate of the first full adder, as shown in Figure 7(b). An open fault is modelled with R_o connecting node X and V_{SS} along path 1. This reduces the conductivity of the n-network along path 1. A short fault is modelled with a resistor connecting X and Y, creating a current path when n_A is off.

4.2.3 Test Stimuli and Fault Sensitization

When an open or short faults occur at the faulty gate, the transition delay at gate output increases. In this circuit, the transition delay at node C_1 increases.

Only two primary inputs, A_0 and B_0, control the conduction of path 1 of the faulty gate. In testing an open fault, path 1 has to be off in the initialization phase and on during the test phase. In testing a short fault, path 1 has to be on during the initialization phase and off during the test phase. Transistor n_B is turned on by setting $B_0 = 1$ throughout the process. Transistor n_A is turned on and off by toggling the signal at node A_0 such that $A_0(t) = <1,0,1>$. The signal at node C_0 is 0 to turn off path 2. To propagate the transition to all subsequent observable outputs, $A_1A_2A_3 = 111$ and $B_1B_2B_3 = 000$.

4.2.3.1 Open Fault

An open fault in path 1 slows the fall of the signal at node $\overline{C}_1$ and thus the signal at node C_1 rises more slowly. When a fault is less severe, a small increase in delay is observed at node C_1. The increase in rise time delay is propagated to all subsequent observable output nodes. When an open fault becomes very severe, the signal at node $\overline{C}_1$ does not fall and thus the signal at node C_1 does not rise. Stuck-at behavior is propagated to other observable output nodes.

4.2.3.2 Short Fault

A short fault in path 1 creates a current path which reduces the pull-up strength of the gate. The signal at node $\overline{C}_1$ rises more slowly, and thus the signal at node C_1 falls more slowly. The increase in fall time delay is propagated to other observable output nodes. When a short fault becomes very severe, the signal at node C_1 does not fall and stuck-at behavior results.

4.2.4 Results

Only four observable output nodes are affected by the increase in delay due to either open or short faults.

4.2.4.1 Open Fault

An open resistor, R_o, in this circuit is changed from a low value of 1 kΩ to a most severe value of 32 kΩ. An open resistor below 1 kΩ produces an insignificant fault severity and an open resistor above 32 kΩ produces stuck-at behavior.

The delay differentiation of the affected output increases linearly as the fault severity increases. The plots are shown in Figure 19. The delay differentiation at node S_1 increases most quickly, followed by the delay differentiation at node S_2, node S_3, and node C_4.

4.2.4.2 Short Fault

A short resistor, R_s, in this circuit is changed from a high value of 40 kΩ to a low value of 1.2 kΩ. A short resistor above 40 kΩ produces an insignificant fault severity. A short resistor below 1.2 kΩ produces stuck-at behavior.

All four plots in Figure 20 show an exponential increase in delay differentiation as the fault severity increases. The delay differentiation at node S_1 increases most quickly, followed by the delay differentiation at S_2, at S_3, and at C_4.

The steady state supply current of a faulty circuit also increases as the fault severity increases. The current differentiation is shown in Figure 21.

4.2.5 Observations

As expected, the fault-free transition delay at node S_1 is the smallest among all affected observable output the signals. A slight increase in transition delay becomes significant. The

fault-free transition delay at node S_2 is larger than the fault-free transition delay at node S_1, and thus the increase of transition delay at S_2 is less significant than the same magnitude of increase at S_1. The fault-free transition delays at node S_3 and C_4 are even larger, and thus the same magnitude of increase in transition delay at both nodes becomes even less significant.

4.2.5.1 Open Fault

When an open fault occurs, the increase in delay at node C_1 is propagated to nodes S_1 and C_2. The increase in delay at node C_2 is then propagated to node S_2 and C_3. The increase in transition delay is finally propagated to nodes S_3 and C_4. Since node S_0 is not affected by the fault, the transition delay of the signal at node S_0 does not increase.

4.2.5.2 Short Fault

Similar to the case of open fault, the increase in delay at C_1 due to short fault is propagated to all observable nodes, except S_0.

The short resistor also creates a current path that draws a large supply current when the p-network is on and the n-network is off. As the short fault becomes more severe, more supply current is drawn through the short resistor. As a result, the supply current increases with the fault severity.

4.2.6 General Conclusions

When the transition delay of a fault-free circuit is small, the increase in transition delay due to a fault is more noticeable. When a fault-free circuit has a long propagation path, the tran-

sition delay becomes large and the increase in transition delay becomes less significant. While delay differentiation test becomes inefficient in testing a circuit containing a lengthy propagation path between the faulty gate and the observable output nodes, the supply current test is just as effective for testing a short fault.

4.3 8-to-3 Priority Encoder

4.3.1 Circuit Characteristics

An 8-to-3 priority encoder is composed of a set of eight priority assignment elements (*PE*'s) and one encoding element as shown in Figure 8. Figure 9(a) shows a priority assignment element and Figure 9(b) shows an encoding element. The priority encoder has eight primary inputs, denoted as I_0 to I_7 . The circuit has four observable outputs, denoted A_0 to A_2 and g_0.

Figure 9(a) shows that a priority assignment element i (PE_i) is composed of one NAND gate, one NOR gate, and one inverter. The NAND gate has I_i and g_{i+1} as inputs and $\overline{E}_i$ as an output. The inverter produces E_i. The NOR gate has I_i and $\overline{g}_{i+1}$ as inputs and g_i as an output. The gates implement the following functions.

$$E_i(t) = g_{i+1}(t) \times I_i(t) \qquad [4.3]$$

$$g_i(t) = \overline{\overline{g_{i+1}(t)} + I_i(t)} = g_{i+1}(t) \times \overline{I_i(t)} \qquad [4.4]$$

From the equation, $g_{i+1}(t)=0$ produces $E_i(t)=0$ and $g_i(t)=0$. Otherwise, $E_i(t)=I_i(t)$ and $g_i(t)=\overline{I_i(t)}$.

The priority elements assign a higher priority to a higher bit of I. I_7 therefore has a higher priority than I_6 which has a higher priority than I_5, and so on. $g_i(t)$ is a priority flag for PE_i. If $g_{i+1}(t)=0$, a priority has been set for an input of priority i+1 or higher. A logic 1 at a higher priority bit of input is transmitted. Any logic 1 at a lower priority bit is ignored. If $g_{i+1}(t)=1$, no priority is set for higher bits. If $I_i(t)=1$, the priority is set for bit i by producing $g_i(t)=0$. Any logic 1 at a lower priority bit cannot be transmitted. Otherwise, $g_i(t)=1$ allows the transmission of a logic 1 at an input with a lower priority.

When all primary inputs are 0, all A's are 0 and $g_0=1$, which indicates no active inputs. When one of the primary inputs is 1, the logic 1 is transmitted and encoded. An input vector of a single logic 1 also produces $g_0=0$. When more than one of the primary inputs are 1, logic 1 of a higher priority input is transmitted to the encoding element, and logic 1 of a lower priority input is ignored. For example, if I_6 and I_2 are 1, I_6 is transmitted as E_6 and I_2 is ignored, so $E_2=0$.

Figure 9(b) shows that the encoding element is composed of three four-input OR gates encoding the E's as follows.

$$A_2(t) = E_4(t) + E_5(t) + E_6(t) + E_7(t) \qquad [4.5]$$

$$A_1(t) = E_2(t) + E_3(t) + E_6(t) + E_7(t) \qquad [4.6]$$

$$A_0(t) = E_1(t) + E_3(t) + E_5(t) + E_7(t) \qquad [4.7]$$

Since only one of the E's equals 1 at any time, there is no input contention at the encoding element. A correct output vector is produced.

4.3.2 Fault Locations

An open fault and a short fault are introduced at the NOR gate of PE_6, as shown in Figure 9(a). The open fault is modelled with a resistor connecting node X and V_{SS}. A short fault is modelled with a resistor connecting g_6 and X, creating a current path even when n_g and n_i turn off.

4.3.3 Test Stimuli and Fault Sensitization

When $g_6(t)=1$, no priority is set for either $I_7(t)$ or $I_6(t)$. A logic 1 is propagated through the priority assignment elements until an input of logic 1 is detected at one of the priority assignment elements, which produces a logic 0 at the corresponding node g. When $g_6(t)$ is at logic 0, either $I_7(t)$ or $I_6(t)$ is encoded. The logic 0 at g_6 is eventually propagated to node g_0. Since both logic 0 and logic 1 can be propagated along the priority assignment elements, a transition in signal $g_6(t)$ should be propagated also.

An input of $I_1(t)I_6(t)=<10,11>$ is applied to test the open fault. An input of $I_1(t)I_6(t)=<11,10>$ is applied to test the short fault. Other inputs remain 0 throughout both tests.

4.3.3.1 Open Fault

When $I_6(t)$ rises, an open fault in the NOR gate of PE_6 slows the fall at node g_6. The slower fall at g_6 blocks the transmission of any lower priority bit more slowly. An increase in delay may occur at the encoded signal. In the event of a more severe fault, an incorrect output may occur.

4.3.3.2 Short Fault

When $I_6(t)$ falls, a short fault in the NOR gate of PE_6 slows the rise at node g_6. The slow rise at g_6 causes a lower priority input to be encoded more slowly. An increase in delay may occur at the encoded signal. When a short fault becomes more severe, an incorrect signal may occur.

4.3.4 Results

Only the transition delay at A_0 is discussed.

4.3.4.1 Open Fault

An open resistor value lower than 5 kΩ produces an insignificant increase in delay, when compared to the transition delay of a fault-free circuit. An open resistor larger than 100 kΩ produces stuck-at behavior. The delay differentiation at node A_0 is plotted in Figure 22. The delay differentiation increases quickly with the fault severity.

4.3.4.2 Short Fault

A short resistor value lower than 8 kΩ produces stuck-at behavior, and a short resistor larger than 200 kΩ produces an insignificant fault severity.

In the event of a short fault, the signal at node A_0 rises more slowly than in the fault-free circuit. When the fault becomes more severe, the rise time delay increases. The delay differ-

entiation is plotted in Figure 23. The delay differentiation increases exponentially with the fault severity.

While the delay differentiation increases to less than 1 for a fault severity of 1, current differentiation increases linearly and quickly with the increase of fault severity. The current differentiation is plotted in Figure 24.

4.3.5 Observations

4.3.5.1 Open Fault

In a fault-free circuit, a rise at node I_6 pulls the signal at node g_6 down almost immediately. In a faulty circuit, an open resistor in the n-network reduces the conduction and the signal at node g_6 falls more slowly. The increased delay is propagated down the chain of primary assignment elements. As a consequence, the signal at node g_2 falls more slowly and a logic 1 at PE_1 is blocked more slowly.

Before the fall at node g_2, a logic 1 at node I_1 is transmitted to the encoding element. At the same time, a logic 1 at node I_6 is also transmitted. Input contention occurs at the encoding element as two logic 1's are encoded simultaneously. The output signal at node A_0 is supposed to fall when the signal at node I_6 rises. However, since the signal at node I_1 is also 1 and is transmitted due to the slower fall of $g_2(t)$, the output signal at node A_0 remains at logic 1 before node I_1 is blocked. When the logic 1 at node I_1 is blocked, the output signal at node A_0 falls to logic 0. A correctly encoded signal is then produced.

When the open fault becomes more severe, the signal at node g_6 falls more slowly, and thus the incorrect output signal is sustained longer. For the most severe fault, $g_6(t)$ does not fall and stuck-at behavior occurs.

4.3.5.2 Short Fault

In a fault-free circuit, the fall at node I_6 causes $g_6(t)$ to rise immediately. In a faulty circuit, a short resistor in the n-network creates a current path between nodes g_6 and V_{SS} that pulls down the signal at node g_6. The current path results in high supply current consumption and a slow rise at node g_6. When $g_6(t)$ rises more slowly, $g_5(t)$ also rises more slowly, as does $g_2(t)$.

Before the signal at node g_2 rises, a logic 1 at input node I_1 is not transmitted. In the meantime, node E_6 produces a logic 0 due to a logic 0 at input node I_6. The output signals at node A_2 and node A_1 are affected by the input signal at node I_6 and thus fall immediately. The signal at node A_0 is affected by the input signal at node I_1. Due to a slower rise at node g_2, a logic 1 at input node I_1 is transmitted more slowly. As a consequence, the output at node A_0 rises more slowly.

When the short fault becomes more severe, the signal at node g_6 rises more slowly, and thus the incorrect output signal is sustained longer. At the most severe short fault, the signal at node g_6 does not rise and stuck-at behavior occurs.

4.3.6 General Conclusions

When a propagation delay is relatively small compared to a fault-free gate delay, a slight increase of the gate delay results in a significant increase in the transition delay of the observ-

able output. When the propagation delay is relatively large compared to a fault-free gate delay, a slight increase in gate delay due to a fault causes an insignificant increase in the observable output delay.

In a faulty circuit, if the previous output value of the affected node is 1 and the current output value is 1, there may be a transient logic 0 if momentarily no logic 1 is encoded.

When only one of the observable output nodes is affected by the fault and its previous output is different from the current output, the node produces a larger transition delay when compared to the other two output nodes. A momentarily false output is produced.

Even when the propagation delay test is not effective due to the stated factors, the supply current test is still effective for testing short faults.

Chapter 5. Results For Sequential Circuits

Sequential circuits by nature operate using a fixed clock period. The times at which inputs and outputs are valid are critical for sequential circuits. In sequential circuits, inputs to the latches are transmitted whenever the clock is active, or valid. Sequential circuits are, therefore, designed so that inputs are always valid when the clock is valid.

In a fault-free sequential circuit, any valid transition of gate outputs occur before the clock is valid. In the presence of open or short faults, the transition of gate outputs may occur more slowly. A transition may or may not be transmitted depending on the magnitude of increase in transition delay at a gate output, which depends on the severity of the fault.

Four sequential circuits considered in this research. All circuits use a level-sensitive, two-phase non-overlapping clock. Two timing parameters are varied to investigate test effectiveness of propagation delay test and supply current test. The first parameter, clock speed, is varied from slow to fast. The second parameter, slack, is also varied over a wide range of values. Slack is the interval between the time at which the input to the latches is valid and the time at which the clock of the latches rises.

Detailed descriptions of circuit characteristics and faults, results and observations are given in the rest of this chapter for the four circuits:

1. four-bit parallel in serial out register
2. eight-bit up/down counter
3. bit-serial adder (FCMOS logic), and
4. bit-serial adder (domino logic).

Circuit diagrams are in Appendix A and test effectiveness results appear in Appendix B. The circuit and results are discussed below.

5.1 Parallel In Serial Out Register

5.1.1 Circuit Characteristics

A four-bit parallel in serial out register is composed of four bit-cells, as shown in Figure 10. The bit-cell is a modified static D flip-flop. The register has seven primary inputs: four parallel inputs, I_1, I_2, I_3, and I_4, one serial input, A_0, and two control signals, *Sh* and *Wr*. For every bit-cell, there are two non-overlapping clock signals, ϕ_1 and ϕ_2. The observable outputs are A_1, A_2, A_3, and A_4.

A qualified clock, $Wr \cdot \phi_1$, loads the parallel inputs into the register. Another qualified clock, $Sh \cdot \phi_1$, shifts the signal from the previous stage into the register. A third qualified clock, $\overline{Wr} \cdot \overline{Sh} \cdot \phi_1$, refreshes the signal by transmitting the output of individual bit-cell back into the bit-cell. Only one of the transmission gates is turned on at any time.

When $Wr \cdot \phi_1(t) = 1$, transmission gate 1 of bit-cell i transmits the parallel input, $I_i(t)$, to node B_i. When $Sh \cdot \phi_1(t) = 1$, transmission gate 2 of bit-cell i transmits the serial input, $A_{i-1}(t)$, to node B_i. When $\overline{Wr} \cdot \overline{Sh} \cdot \phi_1(t) = 1$, a hold operation is performed by turning transmission gate 3 on. Inverter INV_1 of bit-cell i inverts the signal at node B_i to produce a signal at node C_i. When $\phi_2(t) = 1$, the signal at node C_i is transmitted to node D_i. Inverter INV_2 inverts the signal at node D_i to produce a signal at node A_i as $A_i(t+1) = \overline{D_i(t)}$.

5.1.2 Fault Locations

An open fault and a short fault are introduced at inverter INV_2 of bit-cell 1 as shown in Figure 11. An open fault is modelled with a resistor R_o connecting node X and V_{SS} of inverter INV_2, reducing the conductivity of the n-network. A short fault is modelled with a resistor R_s connecting A_1 and V_{SS}. This creates a current path even when the n-channel transistor is off.

5.1.3 Test Stimuli and Fault Sensitization

Parallel inputs are initially loaded by setting $Wr \cdot \phi_1 = 1$ in the first cycle. The parallel input vector is $I_1 I_2 I_3 I_4 = 0101$. In every subsequent cycle, the register shifts in the serial inputs. The data in each bit-cell is transferred to a subsequent bit-cell. The serial input signal used is $A_0 = <1,0,1,0>$. In this way, the four observable outputs $A_1 A_2 A_3 A_4$ toggle at each clock cycle. In a fault-free circuit, the transition delay of observable outputs is small.

5.1.3.1 Open Fault

An open fault in INV_2 of bit-cell 1 slows the fall of the signal at node A_1. The increase in fall time delay is propagated to the next bit-cell of the register during a shift operation. In the event of a more severe open fault, the signal at node A_1 does not fall and stuck-at behavior is produced. Stuck-at behavior is also propagated to the subsequent bit-cells.

5.1.3.2 Short Fault

A short fault in INV_2 of bit-cell 1 slows the rise of the signal at node A_1. The slow rise causes a large rise time delay in the subsequent bit-cell during a shift operation. When a more severe short fault occurs, the signal at node A_1 does not rise, and the effect is propagated to subsequent bit-cells as stuck-at behavior.

5.1.4 Results

There are four observable output nodes: A_0 to A_3. Only two observable output nodes, A_1 and A_2, show an increase in transition delay with the increase of fault severity. The transition delay of an output is measured as the interval between the rise of $\phi_2(t)$ and the transition of the signal.

5.1.4.1 Open Fault

In this circuit, the open resistor, R_o, is changed from a least severe value of 1 kΩ to a most severe value of 36 kΩ. An open resistor below 1 kΩ produces a fault of insignificant severity, while an open resistor above 36 kΩ produces stuck-at behavior.

Figure 25 shows the delay differentiation at node A_1 and node A_2. Curve $A(1)$ shows the delay differentiation at node A_1, and curve $A(2)$ shows the delay differentiation at node A_2. The delay differentiation at node A_1 increases with the fault severity. The increase in delay at node A_1 affects the delay at node A_2.

5.1.4.2 Short Fault

Short faults are examined for seven values of clock frequency, to investigate the effect of clock speed or slack on test effectiveness. Since the faults are introduced at inverter INV_2 of bit-cell 1, the variations in effectiveness of tests for short faults at different clock frequencies can be used to expect the variations in effectiveness of tests for open faults at different clock frequencies.

For any given case, a short resistor below 1 kΩ produces stuck-at behavior, while a short resistor higher than 20 kΩ produces an insignificant increase in delay when compared to the fault-free delay. The clock frequency for all seven cases are shown in Table 1.

The transition delay at nodes A_1 and A_2 for a fault-free circuit is first examined. The fault-free transition delay of all cases deviates by no more than ten percent. From seven cases, three cases are selected. The delay differentiation at A_1 is plotted in Figure 26. The delay differentiation at A_2 is plotted in Figure 27. The current differentiation is plotted in Figure 28.

Table 1. Clock frequency for different cases: $R_{s(l)} = 1$ kΩ and $R_{s(h)} = 20$ kΩ

Case	Clock Speed (ns.)
1	20
2	25
3	30
4	35
5	40
6	45
7	50

5.1.5 Observations

5.1.5.1 Open Fault

An open fault in INV_2 of bit-cell 1 reduces the conductivity during pull-down. The fall time delay thus increases. As the open fault severity increases, the fall time delay at node A_1 increases more.

In the event of a slightly severe open fault, the fall time delay is blocked by transmission gate 2 of bit-cell 2. The small increase in delay is not propagated to bit-cell 2, and thus no increase in delay is produced at node A_2. When the open fault becomes more severe, bit-cell 1 produces a weak logic 0 at node A_1, in addition to the large transition delay. The increase in delay is reduced by the transmission gate 2 of bit-cell 2, but the weak logic 0 is transmitted to B_2 when transmission gate 2 is turned on. A weak logic 0 causes INV_1 of bit-cell 2 to switch more slowly in addition to the increase in transition delay at node B_2, and thus produces a large increase in transition delay at node C_2. The increase in delay is propagated to node A_2.

Although bit-cell 2 produces a large fall time delay, it produces a strong logic 0. The increase in delay is blocked by the transmission gate and a strong logic 0 causes a fast switch at INV_1

of bit-cell 3. Therefore, the transition delay of the signal at node A_3 is not affected by the fault severity.

For the most severe open fault considered, the open fault cuts off the conduction path to produce stuck-at behavior at node A_1. Stuck-at behavior is propagated to the higher-order bit-cells.

5.1.5.2 Short Fault

A short fault in INV_2 of bit-cell 1 creates a current path between node A_1 and V_{SS}. The conduction path reduces the pull-up strength of the faulty inverter, and thus the rise time delay at node A_1 increases. As the short fault severity increases, the rise time delay at node A_1 increases.

Similar to the open fault, the short fault produces a weak logic 1 in addition to a large rise time delay. The increase in rise time delay is reduced by transmission gate 2 of bit-cell 2, but the weak logic 1 is transmitted to node B_2. The weak logic 1 causes INV_1 of bit-cell 2 to switch more slowly. Adding to the increase in transition delay at node B_2, it results in a large rise time delay at node A_2. A strong logic 1 at node A_2 causes no increase in rise time delay at node A_3.

When the qualified clock rises, the logic value at node A_1 is transmitted to node B_2. In the event of a small increase in delay, the signal at node A_1 rises before the qualified clock rises, and thus the increase in delay is not transmitted. In the event of a more severe fault, the signal at node A_1 rises more slowly. If the clock speed is slow, the rise takes place before the rise of the qualified clock. A small increase in delay is created at node A_2 due to the effect of a weak logic 1. If the clock speed is fast, the rise of the qualified clock takes place before the rise of the signal at node A_1. The increase in delay is transmitted in addition to the weak logic

1. The consequence is a large increase in delay at node A_2. As the fault severity becomes more severe, the signal at node A_1 rises more slowly. A circuit with a low clock frequency has sufficient time to transmit the logic value at node A_1 to node B_2, and produce an increase in transition delay. A fast clock speed cuts off the transmission gate 2 of bit-cell 2 before the rise of signal node A_1, which results in the incorrect transmission of the logic value. As a result, the same fault severity that produces a large transition delay in a circuit with a slow clock speed may produce stuck-at behavior in a circuit with a fast clock speed.

With a slow clock speed, the supply current has sufficient time to decay to a steady state before another gate turns on to produce a current spike. The steady state supply current is on the order of a few micro amperes. When a faulty circuit draws a large supply current, the increase in current is significant. With a fast clock speed, the transitions are constantly producing current spikes. The supply current has no time to settle at a steady state. As a result, a large current is produced even in a fault-free circuit. When a large current is produced due to the short fault, the increase becomes insignificant when compared to the large supply current of the fault-free circuit. Supply current test is therefore less effective in a circuit with a high clock frequency.

5.1.6 General Conclusions

An open fault or a short fault not only produces an increase in transition delay, but also produces a weak logic 0 or a weak logic 1. A transmission gate blocks the transmission of a small increase in delay, but the weak logic value causes a slow transition delay in the next stage of gate. When the increase in transition delay is large, the transmission gate reduces the amount of increase when transmitting the signal. However, the weak logic value produced by the faulty gate is transmitted and switches the next stage more slowly. The combination

of the increase in transition delay and a weak logic value contributes to a large increase in transition delay at the next stage of the faulty circuit.

There are two ways of producing stuck-at behavior. In the first, the transition at the faulty gate output occurs more slowly than the fall of qualified clock. The transition is not propagated and stuck-at behavior occurs. In the second, the faulty gate produces permanent, or stuck-at output logic value.

The delay test is more efficient in testing a circuit with a fast clock than with slow clock. The current test, however, has to be performed under a slow clock speed.

5.2 Eight-bit Up/Down Counter

5.2.1 Circuit Characteristics

The eight-bit up/down counter is composed of eight cells. As shown in Figure 12, each individual cell combines static combinational logic gates with a static flip-flop, to produce one bit of the counter output $A_0(t)$, $A_1(t)$, ... ,$A_7(t)$. There are five control signals, load ($LD(t)$), up ($UP(t)$), down ($DN(t)$), preset ($PST(t)$), and clear ($CLR(t)$). Only one control signal is enabled at any time. The static combinational logic gates are two levels of NAND gates producing the output signal $T_i(t)$ at node T_i as follows.

$$T_0(t) = UP + DN$$

$$T_i(t) = UP(t) \times \sum_{j=0}^{i-1} A_j(t) + DN(t) \times \sum_{j=0}^{i-1} \overline{A_j(t)} \quad , \text{ for i } = 1,2, \ldots ,7 \qquad [5.1]$$

Two of the five control signals are the inputs to the NAND gates as shown in Figure 12(a). The other three control signals drive transmission gates in the register as shown in Figure 12(b).

As the number of primary inputs to the first level NAND gates, G_{i1} and G_{i2}, increases, the size of the gates also increase. The driving capability of the gates is reduced by having many n-channel transistors in series between node X_i and V_{SS} or between node Y_i and V_{SS}. The rising and falling of gate outputs are, therefore, slow. To increase the driving capability and cause faster rising and falling at each gate output, the larger NAND gates are decomposed into combination of smaller gates. The smaller gates have medium depth with a maximum of four transistors between the output node and V_{SS}. Due to the decomposition, the signal from the primary inputs to node T_i has a propagation path of either two or three gates.

Based on Equation 5.1 and Figure 12(a), for all but cell 0, $T_i(t)=1$ if $X_i(t)$ or $Y_i(t)=0$. $T_0(t)=1$ if either $UP(t)$ or $DN(t)$ is 1. $T_i(t)$ drives the flip-flop of cell i. Figure 12(b) shows that for each cell i, there are two feedback paths driven by $T_i(t)$ and $\overline{T_i(t)}$. The paths are wire-ORed at node B_i. For $T_i(t)=0$, node $B_i(t)$ receives the uncomplemented signal $A_i(t)$. For $T_i(t)=1$, $B_i(t)=\overline{A_i(t)}$. In short, $B_i(t) = T_i(t) \oplus A_i(t)$. To implement the load function, the third control signal, LD, is added to drive the input signal $I_i(t)$ to node B_i. The signal at node B_i is propagated to node A_i through two transmission gates and two inverters. The two transmission gates are driven by two non-overlapping clock signals, $\phi_1(t)$ and $\phi_2(t)$. The two inverters act as buffers for driving the output signal.

Signal $B_i(t)$ is propagated to node C_i when $\phi_1(t)=1$. With the inverter, $D_i(t)=\overline{C_i(t)}$. When $\phi_2(t)=1$, $D_i(t)$ is propagated to node E_i and output to node A_i as $\overline{E_i(t)}$. Since the transmission gate is passing the signal, the correct signal (logic value) has to stabilize at B_i before or during the rise of ϕ_1 and at D_i before or during the rise of $\phi_2(t)$.

5.2.2 Fault Locations

An open fault and a short fault are introduced at gate G_{11}. The faulted gate is shown in Figure 13. The open fault is modelled as a resistor R_o connecting the bottom n-channel transistor to V_{SS}. This reduces the conductivity through the n-network during pull-down. The short fault is modelled as a resistor R_s connecting X_1 and V_{SS}, creating a current path between V_{DD} and V_{SS} when the n-network is off and the p-network is on.

5.2.3 Test Stimuli and Fault Sensitization

Gate G_{11} has two inputs, $A_0(t)$ and $UP(t)$. To control the response of gate G_{11}, we apply the input signal $UP(t)$ such that $UP(t)$ toggles with $\phi_1(t)$. The $UP(t)$ signal leads $\phi_1(t)$ by a slack of Δ and falls simultaneously with $\phi_1(t)$, as shown in Figure 5. When $UP(t)=0$, $X_1(t)=1$, regardless of $A_0(t)$. At the same time, $DN(t)$ is kept constant at 0, which makes $Y_1(t)=1$, and $T_1(t)=\overline{X_1(t)}$.

For small slack Δ, $UP(t)$ rises more slowly than $A_0(t)$ switches. In that case, even when $A_0(t)$ rises, $X_1(t)$ can fall only after $UP(t)$ rises. The signal is then propagated to node T_1 which drives node B_1 to the correct logic value. In a fault-free circuit, $UP(t)=1$ propagates $A_0(t)$ to node T_1. For example, assume $A_0(t)=1$. Then $T_1(t)=1$ when $UP(t)=1$ and $B_1(t)=\overline{A_1(t)}$ which will later produce an output of $A_1(t+1)=\overline{A_1(t)}$. For a large slack Δ above some threshold value, $UP(t)$ rises before $A_0(t)$ changes. $T_1(t)$ then becomes dependent on changes in $A_0(t)$.

5.2.3.1 Open Fault

An open fault in gate G_{11} slows the fall of signal $X_1(t)$, and hence $T_1(t)$ rises more slowly. If the rise time delay of $T_1(t)$ is large, B_1 may not stabilize at $\overline{A_1(t)}$ when $\phi_1(t)$ is high. When an un-

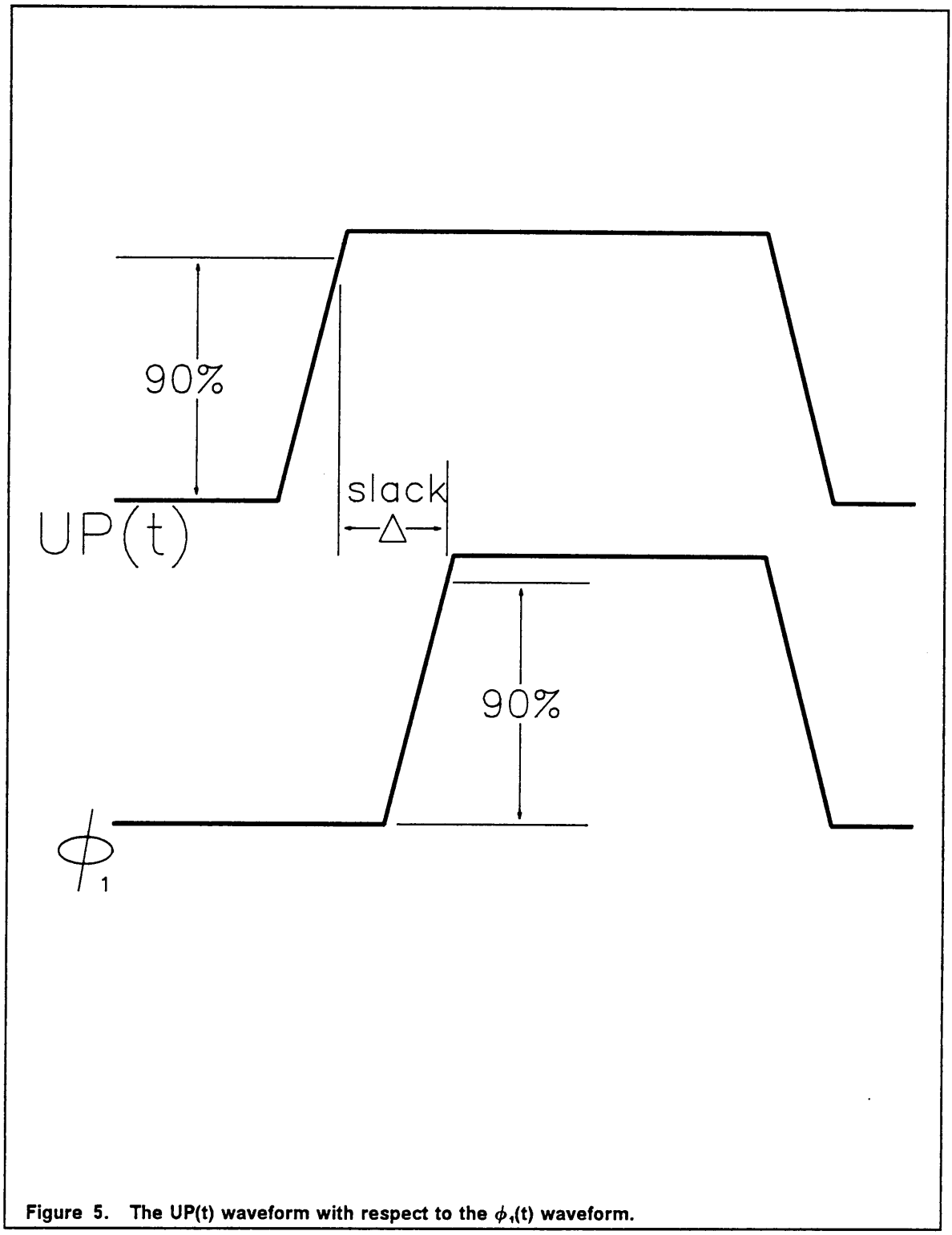

Figure 5. The UP(t) waveform with respect to the ϕ_1(t) waveform.

stabilized $B_1(t)$ is propagated through the transmission gates and the inverters, a less severe fault results in an increase in the transition delay and a more severe fault results in an incorrect logic value at the output node A_1. Since $A_0(t)$ is leading $\phi_1(t)$ by a constant time interval and the transition at T_1 depends on the transition at A_0 for a circuit with large slack Δ, $T_1(t)$ is also leading $\phi_1(t)$ by a constant time interval. As a consequence, as Δ is larger than a certain value, any open resistor value results in the same large increase in delay at T_1 regardless of Δ value. Stuck-at behavior also occurs for one resistor value for all circuits with Δ larger than the threshold value.

5.2.3.2 Short Fault

A short fault in gate G_{11} may slow the rise of $X_1(t)$, and $T_1(t)$ will then fall more slowly. Since $T_1(t)$ falls more slowly and rises more quickly, node B_1 receives the complemented signal $\overline{A_1(t)}$ more quickly than it receives $A_1(t)$. Although node B_1 receives $\overline{A_1(t)}$ more quickly in the faulty case than in the fault-free case, the signal is not transmitted to node C_1 until the rise of $\phi_1(t)$. $\phi_1(t)$ prevents the early transmission of the signal and hence the signal $A_1(t+1)$ changes without any increase in delay. Also, since $T_1(t)$ falls more slowly, signal $A_1(t)$ is transmitted to node B_1 more slowly. The further transmission of the signal to node A_1 in the next clock cycle is also delayed. But since $A_1(t+1) = A_1(t)$, the delay is not detected. However, as the rise of $X_1(t)$ becomes very slow, or even stuck at logic 0, the complemented signal $\overline{A_1(t)}$ is constantly transmitted even when $A_1(t)$ is supposed to be transmitted. An incorrect logic value is produced, resulting in stuck-at behavior at $A_1(t)$.

5.2.4 Results

Although all observable outputs are affected during a severe fault condition that results in stuck-at behavior, it is found that only signal $A_1(t)$ is delayed by the open and short faults in gate G_{11}. Other output delays remain constant throughout the range of open and short fault severities for all cases. As a result, the delay differentiation is discussed only for signal $A_1(t)$. Current differentiation is discussed for the short fault.

5.2.4.1 Open Fault

Open faults are examined for ten different values of slack Δ. For any given value of Δ, an open resistor value lower than $R_{o(l)}$ produces an insignificant increase in delay, while an open resistor larger than $R_{o(h)}$ produces stuck-at behavior at node A_1. The ranges of the resistor values for all ten cases are shown in Table 2.

The transition delay of the fault-free circuit is examined first. The transition delay decreases as the slack increases. When the slack is 1 nanosecond, the delay is at a high value of 7.5 nanoseconds. When the slack increases to 9 nanoseconds, the delay is reduced to 5.9 nanoseconds. When the slack is 19 nanoseconds, the delay is only 5.3 nanoseconds.

The delay differentiation values for all ten cases were recorded. The curves are categorized into three groups based on the results and are shown in Figure 29. The first three cases, where the slack is less than or equal to 5 nanoseconds, make up the first group. The majority of the simulated cases fall into the second group, where the slack is between 7 nanoseconds and 17 nanoseconds. The third group is the case where $\Delta = 19$ nanoseconds.

Table 2. Resistor range for different Δ values: $R_{o(l)}$ = low resistor value, $R_{o(h)}$ = high resistor value.

Case	Δ (ns.)	$R_{o(l)}$ (kΩ)	$R_{o(h)}$ (kΩ)
1	1	1	6
2	3	1	12
3	5	1	18
4	7	1	24
5	9	1	28
6	11	1	32
7	13	1	34
8	15	1	34
9	17	1	36
10	19	1	36

5.2.4.2 Short Fault

In this circuit, the short resistor, R_s, is changed from a least severe value of 50 kΩ to a most severe value of 4.5 kΩ. Any resistor value below 4.5 kΩ produces stuck-at behavior.

The transition delay at A_1 is not influenced by the severity of the short fault. As discussed above, the short fault in gate G_{11} affects only the hold operation of the circuit. However, in a hold operation, the slow propagation of the same logic value of $A_1(t)$ cannot be detected by the propagation delay test. The current test, however, can detect this type of short fault. The steady state current increases as the fault severity increases as shown in Figure 30.

5.2.5 Observations

5.2.5.1 Open Fault

During the counting up operation, the flip-flop for cell 1 requires $T_1(t)$ to be high before or when $\phi_1(t)$ is high to toggle the logic value. Since the open fault occurs at gate G_{11}, and $Y_1(t)$ remains

1 at all times, the open fault increases the fall time delay of $X_1(t)$ and hence the rise time delay of $T_1(t)$.

Assume $A_0(t)=1$ and Δ is small. When $T_1(t)$ is 0, the uncomplemented logic value, $A_1(t)$, is initially transmitted to node B_1. As $T_1(t)$ rises, $\overline{A_1(t)}$, is transmitted to change the logic value at B_1. In the fault-free case, $B_1(t)$ changes to a correct logic value before the rise of $\phi_1(t)$. For a low fault severity condition, $B_1(t)$ is changed during the rise of $\phi_1(t)$. The signal at B_1 is almost stable at the correct logic value when $\phi_1(t)$ rises. When $\phi_1(t)$ falls, C_1 stabilizes at the correct logic value. The output voltage level and the delay are only slightly affected. After the second transmission gate and the second inverter, the increase in switching delay is further reduced and the voltage level is stabilized. The resulting effect is insignificant delay differentiation with no voltage distortion.

If the fault severity is large, signal $B_1(t)$ changes while $\phi_1(t)$ is high. $B_1(t)$ may not have sufficient time to stabilize when $\phi_1(t)$ cuts off the transmission gate. As a result, $C_1(t)$ may settle somewhere between 0 and 5 volts. The voltage level depends on when $B_1(t)$ changes before the transmission gate turns off. If $B_1(t)$ has a longer time to change before $\phi_1(t)$ falls, the unknown voltage level is closer to the correct logic value. But, if $B_1(t)$ is given a short time to change before $\phi_1(t)$ falls, the unknown voltage level is closer to the incorrect logic value. The weak correct (incorrect) logic value is then propagated through the inverter. Since the signal is weak, the output of the inverter switches slowly and additional delay occurs. The increase in delay is propagated through the transmission gate controlled by ϕ_2 and is observed at A_1. However, since the incorrect logic value of $A_1(t+1)= A_1(t)$, no increase in transition delay is detected. Nevertheless, the incorrect output is detected.

If the slack is large, a small increase in delay at $T_1(t)$ has no effect on the transmission of the complemented signal $\overline{A_1(t)}$ to node B_1. Since $T_1(t)$ rises long before the rise of $\phi_1(t)$, node B_1 still has sufficient time to charge or discharge to the correct logic value. There is essentially no increase in the delay at the output response of $A_1(t)$.

As the open resistor value increases, the delay in $T_1(t)$ increases. The signal at B_1 begins to change more slowly and an undetermined logic value may appear at node C_1. The same fault effect occurs. As a result, the effect of an open fault is reduced by an increase in the slack.

5.2.5.2 Short Fault

The short fault in gate G_{11} increases the rise time delay of $X_1(t)$ and, therefore, the fall time delay of $T_1(t)$. The short fault also reduces the fall time delay of $X_1(t)$ and the rise time delay of $T_1(t)$.

When $A_0(t)=1$, the fall of signal $UP(t)$ results in the fall of $T_1(t)$ after approximately two gate delays. The uncomplemented signal is transmitted to B_1 when $T_1(t)$ is low. However, $\phi_1(t)$ is low at the same time, which blocks the further transmission of the uncomplemented signal to the output.

When $UP(t)$ rises, the fault-free cell performs the counting up operation as usual. In the event of the short fault, $T_1(t)$ turns on the transmission gate earlier to transmit the complemented signal to B_1. However, the earlier transmission of the complemented signal is blocked by the clock $\phi_1(t)$. When $\phi_1(t)=1$, $B_1(t)$ is always stable at $\overline{A_1(t)}$ and no extra delay is produced at A_1.

When $A_0(t)=0$, $A_1(t+1)$ remains unchanged from $A_1(t)$ in the fault-free circuit. In the presence of a short fault, $T_1(t)$ falls more slowly and rises earlier. $A_1(t)$ is transmitted to node B_1 only when $T_1(t)=0$, and $\overline{A_1(t)}$ is transmitted during $T_1(t)=1$. Since $T_1(t)$ falls more slowly, $\overline{A_1(t)}$ is initially transmitted and then, when $T_1(t)$ falls, $A_1(t)$ is transmitted before the rise of $\phi_1(t)$. The pull to both logic 1 and logic 0 at node B_1 is similar to the situation occurring due to the open fault in the counting operation. However, for a less severe fault condition, $A_1(t+1)=A_1(t)$, and thus no transition delay can be detected. For a very severe fault condition, an incorrect logic

value is produced. Hence, the propagation delay test cannot be used to detect this kind of short fault.

Nevertheless, the short fault in G_{11} creates a conduction path between V_{DD} and V_{SS} when the n-network is supposed to be off. A higher fault severity creates a path with higher conductance. In addition, a severe fault severity creates an intermediate voltage level at C_1 that turns on both the p-network and the n-network of the inverter partially, thus creating another path between V_{DD} and V_{SS}. The conduction paths contribute to a large steady state supply current.

5.2.6 General Conclusions

In this circuit, open and short faults affect the transition time of the control signal to the register. The increase in the transition time of the affected gate may or may not affect the observable output of the register.

When the slack is small, a slight increase in the rise time delay of the driving signal affects the transition delay of an internal node, such as B_1, in the register. When the added delay at the internal node is small, the effect of the delay is filtered out by the two transmission gates driven by non-overlapping clock signals. When the transition delay is large, however, the transmission gates do not filter out the effect of the delay and an increase in delay is observed at the register output.

When the slack is large, a less severe fault slows the rise at the output of the faulty gate. If the increase in the delay is smaller than the slack, the correct feedback occurs before the rise of $\phi_1(t)$. No increase in delay is detected at the register output. If the increase in the delay is larger than the slack, the delay is detected at the output as in the case of small slack.

In this circuit, signal $T_1(t)$ and its complement signal, $\overline{T_1(t)}$, are driving two feedback paths. One path, the complementing path, produces $A_1(t+1)=\overline{A_1(t)}$ and the other path, the non-complementing path, produces $A_1(t+1)=A_1(t)$. In the event of an open fault, the transition delay is observed at the output since the output signal of the faulty gate is driving the complementing path. In the event of a short fault, no transition can be observed since the output signal of the faulty gate is driving the non-complementing path. As a result, no transition delay can be detected for the short fault considered in this circuit.

There are two ways a fault can produce stuck-at behavior at the register output. In the first case, the faulty signal is not stuck at a logic value, but changes more slowly than the rise of $\phi_1(t)$. Node B_1 is charged or discharged to the correct logic value more slowly than $\phi_1(t)$ turns on. B_1 receives the correct logic value, but too late to be transmitted through ϕ_1. The incorrect logic value is then transmitted and stuck-at behavior occurs. In the second case, the faulty driving signal is actually stuck at 0 or 1. The incorrect signal is transmitted to node $B_1(t)$ through the feedback path to produce stuck-at behavior at the register output.

5.3 Bit-Serial Adder (FCMOS Logic)

5.3.1 Circuit Characteristics

The bit-serial adder is composed of a full adder and a feedback path as shown in Figure 14. The full adder consists of a CARRY gate and a SUM gate, as shown in Figure 19. Both gates are implemented in a fully complementary design equivalent to the equations implemented in ripple carry adder of the previous chapter.

The feedback path consists of two transmission gates and two inverters. The first transmission gate is driven by the qualified clock of $\overline{LD(t)} \cdot \phi_1(t)$ to transmit $C_{OUT}(t)$ to node D. The first inverter then complements the signal to produce $E(t) = \overline{D(t)}$. The second transmission gate is driven by $\phi_2(t)$ to transmit the signal to node F. The second inverter then inverts $F(t)$ to produce $C_{IN}(t+1)$ for the next clock cycle, so $C_{IN}(t+1) = C_{OUT}(t)$. To clear the carry bit, a transmission gate is connected from V_{SS} to node D and is driven by the qualified clock $LD(t) \cdot \phi_1(t)$.

The input signals to the bit-serial adder are two data inputs, $A_{IN}(t)$ and $B_{IN}(t)$, and a control signal $LD(t)$. There are two non-overlapping clock signals, $\phi_1(t)$ and $\phi_2(t)$. The observable output signals are $C_{IN}(t)$, $C_{OUT}(t)$, and $S(t)$.

Outputs $C_{OUT}(t)$ and $S(t)$ depend on $A_{IN}(t)$, $B_{IN}(t)$, and the previous output $C_{OUT}(t-1)$. The circuit performs the add operation in a bit-serial manner with the least significant bits added first.

5.3.2 Fault Locations

An open fault and a short fault are introduced at path 1 of the CARRY gate, as shown in Figure 19(a). The open fault is modelled with a resistor R_o connecting node X and V_{SS} along path 1. This reduces the conductivity of the n-network along faulty path 1. A short fault is modelled with a resistor R_s connecting X and Y, creating a current path even when n_A is off.

5.3.3 Test Stimuli and Fault Sensitization

Although the carry gate has three inputs, only $A_{IN}(t)$ and $B_{IN}(t)$ affect the conductivity of the faulty path. Since an open fault prevents conduction along the faulty path and a short fault

creates a current path across the transistor n_A, one set of vectors is needed to test the open fault and another set is needed to test the short fault. At the same time, path 2 must be disabled to prevent any switching that may invalidate the output response.

When $C_{IN}(t)=1$, any transition of $A_{IN}(t)$ or $B_{IN}(t)$ activates path 2, which invalidates the initialization or the test. To prevent this invalidation, $C_{IN}(t)$ is preset to 0. $A(t)B(t) = <00,11>$ is applied to test an open fault, and $A(t)B(t) = <00,01>$ is used to test a short fault. Each input is applied before the rise of $\phi_1(t)$ by slack Δ.

For small slack, there is a small interval between the transition of $C_{OUT}(t+1)$ and the fall of $\phi_1(t)$. A low severity fault is sufficient to increase the transition delay of $C_{OUT}(t+1)$ such that the transition takes place after the fall of $\phi_1(t)$. $C_{OUT}(t)$ is transmitted instead of $C_{OUT}(t+1)$ and stuck-at behavior occurs. When the slack becomes large, the interval between the transition of $C_{OUT}(t+1)$ and the fall of $\phi_1(t)$ also increases. In that situation, $C_{OUT}(t+1)$ has sufficient time to be transmitted. It takes a more severe fault to produce a larger transition delay at C_{OUT} so that $\phi_1(t)$ falls before the transition takes place.

5.3.3.1 Open Fault

An open fault in path 1 slows the fall of $\overline{C_{OUT}(t)}$ and hence $C_{OUT}(t)$ rises more slowly. When the fault is less severe, a small delay is observed at node C_{OUT}, yet $C_{OUT}(t)$ stabilizes at 1 when $\phi_1(t)=1$. The effect is not reflected in $C_{IN}(t+1)$ of the next cycle. When the increase in delay is large, the transition delay at node C_{IN} is affected. The transition delay at node C_{IN} also increases, but the value is smaller than the increase in delay at node C_{OUT}. As the fault condition becomes severe, $C_{OUT}(t)$ may rise more slowly than $\phi_1(t)$ falls and an incorrect logic value will be produced at node C_{IN}.

5.3.3.2 Short Fault

In testing the short fault at this location of this circuit, no input vector is found that simultaneously cuts off path 2 and activates path 1. With the applied input vector of AB = <00,01>, $\overline{C_{OUT}(t)}$ = <1,1> and $C_{OUT}(t)$ = <0,0>. Since the logic value at node C_{OUT} does not change, no transition delay is produced. As the fault severity increases, the current path becomes more conductive and thus the voltage level of $\overline{C_{OUT}(t)}$ may drop to a level that is too low to be detected as a logic 1. An incorrect logic value is produced at node C_{OUT}.

5.3.4 Results

There are three observable output nodes: C_{OUT}, S, and C_{IN}. Since the SUM gate is fault-free, only the delay at nodes C_{OUT} and C_{IN} is discussed. The delay at C_{OUT} is measured as the interval between the transition at node A_{IN} or B_{IN} and the transition at C_{OUT}. The delay at node C_{IN} is measured as the interval between the rise of $\phi_2(t)$ and the transition at node C_{IN}. Current differentiation is discussed for the short fault.

5.3.4.1 Open Fault

The open fault is examined for five different slack values. For any given case, an open resistor value lower than 1 kΩ produces an insignificant increase in delay, while an open resistor larger than 250 kΩ results in stuck-at behavior at node C_{OUT}.

The transition delay of the fault-free circuit is first examined. The transition delay of the fault-free circuit is the same for all values of Δ.

Table 3. Slack for different cases: $R_{o(l)} = 1\ k\Omega$, $R_{o(h)} = 250\ k\Omega$, $R_{s(l)} = 1\ k\Omega$, $R_{s(h)} = 100\ k\Omega$.

Case	Δ (nsec)
1	0
2	4
3	8
4	12
5	16

The delay differentiation for the five cases is recorded and plotted. For three of the cases, the delay differentiation at node C_{OUT} for the three cases is plotted in Figure 31, and the delay differentiation at node C_{IN} is plotted in Figure 32.

5.3.4.2 Short Fault

Short faults are also examined for five different values of slack Δ. For any given case, a short resistor value lower than 1 kΩ produces stuck-at behavior, and a value above 100 kΩ produces an insignificant increase in delay.

Since the input vectors do not change the output $C_{OUT}(t)$, the delay test cannot detect this type of short fault.

Supply current test can be used. The steady state current for the five cases is examined. The currents of all cases are found to be within a range of plus or minus 2 microamperes for every value of fault severity, with the lowest value being 8 microamperes. The current differentiation for the circuit with $\Delta = 8$ nanoseconds is given in Figure 33. The steady state current increases as the fault severity increases.

5.3.5 Observations

5.3.5.1 Open Fault

Signal $\overline{C_{OUT}(t)}$ is initialized to logic 1 by the input vector of $A_{IN}(t)B_{IN}(t)=00$. $C_{OUT}(t)$ is initialized to logic 0. When $A_{IN}(t+1)B_{IN}(t+1)=11$, path 1 is conducting to produce $\overline{C_{OUT}(t+1)}=0$ and $C_{OUT}(t+1)=1$ in a fault-free circuit.

An open fault reduces the conductivity of path 1, increasing the fall time delay of $\overline{C_{OUT}(t+1)}$ and thus increasing the rise time delay of $C_{OUT}(t+1)$. When the fault is less severe, the conductivity is less affected and thus the increase in delay is small. When the fault is more severe, the conductivity is reduced and causes a large increase in delay. For the most severe fault condition, the conduction path is basically turned off and stuck-at behavior occurs.

When the slack is 0, there is a small time interval between the transition at C_{OUT} and the fall of the qualified clock. In a fault-free circuit, the signal at node C_{OUT} switches while the qualified clock is high. A slightly severe fault increases the transition delay at node C_{OUT}. The increase in transition delay is transmitted through the feedback path to be reflected in the transition delay at node C_{IN}. As the fault severity increases, the transition delay at node C_{OUT} increases. For a more severe fault, the delay becomes so large that the signal at node C_{OUT} rises more slowly than the qualified clock falls. The previous value at node C_{OUT} is transmitted instead of the current value, so stuck-at behavior results.

When the slack is larger than 0, the signal at node C_{OUT} in a fault-free circuit rises and stabilizes before the qualified clock rises. In the event of a slightly severe fault, the signal at node C_{OUT} still rises before the qualified clock rises. The transition delay is observed at node C_{OUT}, but the increase in delay is not transmitted through the transmission gate. When the fault becomes more severe, the transition delay at node C_{OUT} is so large that the signal at node

C_{OUT} rises when the qualified clock turns on the transmission gate. The inverter INV_C has to charge two parasitic capacitors when its output rises, one at each side of the transmission gate. The result is an even slower rise of the signal at node C_{OUT}. As the transition delay becomes larger, the large increase in transition delay is propagated to node C_{IN}, as in case 1.

5.3.5.2 Short Fault

In testing the short fault, $C_{OUT}(t)$ is also initialized to logic 0. When $A_{IN}(t+1)B_{IN}(t+1)=01$, n_A turns off path 1 and n_C turns off path 2. $\overline{C_{OUT}(t+1)}$ remains at logic 1 and $C_{OUT}(t+1)$ remains at logic 0 in a fault-free circuit. A short fault across n_A creates a current path between C_{OUT} and V_{SS} when $B_{IN}(t+1)=1$, regardless of the logic value of $A_{IN}(t)$. If $A_{IN}(t+1)=0$, the p-network is turned on and the n-network is cut off in a fault-free circuit. With the short fault, the p-network and the short resistor are pulling against each other.

When the short fault is less severe, the current path is less conductive. Signal $\overline{C_{OUT}(t)}$ is driven closer to logic 1 by V_{DD} through the p-network. $C_{OUT}(t)$ remains at logic 0 without any transition, so no delay can be detected. There is, however, a current path that increases the supply current.

When the short fault becomes more severe, the conductivity of path 1 increases, and the steady state supply current increases. Signal $\overline{C_{OUT}(t+1)}$ is also driven closer to logic 0. For the most severe fault considered, signal $\overline{C_{OUT}(t+1)}$ is driven to a voltage level which is considered logic 0. $C_{OUT}(t+1)=1$ and stuck-at behavior occurs.

5.3.6 General Conclusions

In this circuit, the open fault affects the transition time of the observable output signal. The transmission gates block a slight increase in delay at node C_{OUT}, or reduce the value if the delay is transmitted. The short fault does not affect the transition time of the observable output signal, but does affect the steady state supply current of the circuit.

It is the transition time at node C_{OUT} that causes the increase in delay at node C_{IN}. When the transition time at node C_{OUT} is closer to the rise time of $\phi_1(t)$, less increase in delay is transmitted to node D. When the transition time at node C_{OUT} is closer to the fall time of $\phi_1(t)$, a large delay is transmitted to node D and eventually to C_{IN}.

For a short fault at this location, no input set is available to create a transition at the output signal of $C_{OUT}(t)$, so the delay test cannot be used. The current test, however, can still detect the existence of the current path.

There are two ways stuck-at behavior can occurs in this circuit. In the first case, the signal at node C_{OUT} switches more slowly than the qualified clock falls. The previous logic value at node C_{OUT} is transmitted to produce an incorrect value at node C_{IN}. In the second case, stuck-at behavior actually occurs at the faulty gate, which produces a permanent logic 0 or logic 1.

When a fault is less severe, the small increase in the transition delay at node C_{OUT} does not increase the transition delay at node C_{IN}. As the delay at node C_{OUT} becomes large, the transition delay at node C_{IN} increases. If the signal at node C_{IN} is driving the faulty path, the increase in the input transition delay produces a larger increase in the output delay at node C_{OUT}. The increase of delay at node C_{OUT} produces a larger increase in delay at node C_{OUT} and so on. The cumulative effect results in a larger and larger increase in the output delay, and produces an incorrect logic value after a few clock cycles. In this simulation, this kind of

stuck-at behavior does not occur because of two reasons. First, the feedback input is not on the faulty path. Second, the outputs are observed for only two clock cycles.

5.4 Bit-Serial Adder (Domino Logic)

5.4.1 Circuit Characteristics

The bit-serial adder is composed of a full adder and a feedback path as shown in Figure 14. The full adder consists of a CARRY gate and a SUM gate, as shown in Figure 15. The gates implement the same equations as the FCMOS logic of Section 5.3, but use domino logic.

The p-network consists of a large p-channel transistor, denoted p_{ϕ_1}, driven by clock signal $\phi_1(t)$. A large n-channel transistor, denoted n_{ϕ_1}, is also driven by $\phi_1(t)$. n_{ϕ_1} connects the bottom of the n-network to V_{SS}.

The feedback path consists of two transmission gates and two inverters. The first transmission gate is driven by the qualified clock $\overline{LD(t)} \bullet \phi_1(t)$ to transmit $C_{OUT}(t)$ to node D. The first inverter then complements the signal to produce $E(t) = \overline{D(t)}$. The second transmission gate is driven by $\phi_2(t)$ to transmit the signal to node F. The second inverter then inverts $F(t)$ to produce signal $C_{IN}(t+1)$ for the next clock cycle, so $C_{IN}(t+1) = C_{OUT}(t)$. To clear the circuit, a transmission gate is connected from V_{SS} to node D and is driven by the qualified clock $LD(t) \bullet \phi_1(t)$.

The input signals to the bit-serial adder are two data inputs, denoted $A_{IN}(t)$ and $B_{IN}(t)$, a control signal $LD(t)$, and two non-overlapping clock signals, $\phi_1(t)$ and $\phi_2(t)$. The observable output signals are $C_{IN}(t)$, $C_{OUT}(t)$, and $S(t)$.

At time t, the current outputs of $C_{OUT}(t)$ and $S(t)$ depend not only on $A_{IN}(t)$ and $B_{IN}(t)$, but also on the previous carry output $C_{OUT}(t-1)$. The circuit performs the addition operation bit serially, processing the least significant bit first.

5.4.2 Fault Locations

For the experiments, an open fault and a short fault are introduced in path 1 of the CARRY gate, as shown in Figure 15(a). The open fault is modelled with a resistor R_o connecting nodes X and W. This reduces the conductivity of the n-network along faulty path 1. A short fault is modelled with a resistor R_s connecting nodes X and Y, creating a current path even when n_A is off.

5.4.3 Test Stimuli and Fault Sensitization

The same input vectors, $A(t)B(t) = <00,11>$ and $A(t)B(t) = <00,01>$, as used for the FCMOS implementation of the bit-serial adder are applied to test the open fault and short fault, respectively. Each input is applied Δ seconds before the rise of $\phi_1(t)$.

During the pre-charge phase, $\phi_1 = 0$. Transistor p_{ϕ_1} conducts and pre-charges node $\overline{C}_{OUT}$ to logic 1 and thus discharges node C_{OUT} to logic 0. In addition, if there is any conducting path between node $\overline{C}_{OUT}$ and node W, the internal nodes of the path are also charged to logic 1. During the evaluate phase, $\phi_1(t) = 1$. Transistor p_{ϕ_1} turns off and n_{ϕ_1} conducts. Node $\overline{C}_{OUT}$ is conditionally discharged during evaluation.

The input vector is not allowed to change during evaluation. Therefore, the smallest allowable slack is $\Delta = 0$. Since the signal at node C_{OUT} remains at logic 0 during the pre-charge phase,

the slack does not affect the transition delay of the signal. However, when the previous output at $\overline{C}_{OUT}$ was 1 and the expected output at $\overline{C}_{OUT}$ is 0, the input vector turns on the transistors to create a current path between the output node and node *W*. When the slack is small, the circuit has less time to charge the internal nodes to logic 1. The internal nodes in the circuit accumulate less charge and thus are discharged more easily during the evaluate phase. The signal at node C_{OUT} can then rise faster. When the slack is large, there is a long period of time for the internal nodes to be charged to logic 1. During evaluation, a longer time is needed to discharge node $\overline{C}_{OUT}$ and the signal at node C_{OUT} then rises more slowly.

5.4.3.1 Open Fault

An open fault in path 1 slows the fall of $\overline{C_{OUT}(t)}$ and $C_{OUT}(t)$ rises slowly. If a fault has low severity, a small delay is observed at node C_{OUT}, but, there is sufficient time to transmit a logic 1 to node *D* before $\phi_1(t)$ falls. The effect is not reflected in $C_{IN}(t+1)$ of the next cycle. If the transition delay at node C_{OUT} is large, the large delay is expected to affect the transition delay at node C_{IN}. The transition delay at node C_{IN} also increases, but the increase is smaller than the increase at node C_{OUT}. As the fault condition becomes more severe, $C_{OUT}(t)$ may rise more slowly than $\phi_1(t)$ falls, and an incorrect logic value will be transmitted.

5.4.3.2 Short Fault

During the precharge phase, the output signal at $\overline{C}_{OUT}$ is 1 and will remain at 1 if the short is sensitized during the evaluate phase of the test vector, i.e. no valid test vector causes a transition at $\overline{C}_{OUT}$. So, the propagation delay test cannot be used to test the short fault. However, as the fault severity increases, the current path becomes more conductive and thus the voltage level at node $\overline{C}_{OUT}$ may drop to a level which is too low to be detected as a logic 1.

An incorrect logic value will be produced at node C_{OUT}. The steady state supply current should also be larger in the faulty case than the fault-free case.

5.4.4 Results

Since the SUM circuit is fault-free, only the delay of signals at nodes C_{OUT} and C_{IN} are discussed. The delay of the signal at node C_{OUT} is measured as the interval between the rise of clock $\phi_1(t)$ and the transition at node C_{OUT}. The delay of the signal at node C_{IN} is measured as the interval between the rise of $\phi_2(t)$ and the transition at node C_{IN}. Delay differentiation is discussed for the open fault and current differentiation is discussed for the short fault.

5.4.4.1 Open Fault

The open fault is examined for five different values of slack Δ. For each case, an open resistor value lower than $R_{o(l)}$ produces an insignificant increase in delay, while an open resistor larger than $R_{o(h)}$ results in stuck-at behavior at node C_{IN}. These values for all five cases are shown in Table 4.

The transition delay for the fault-free circuit is found to be same for all five cases. The delay differentiation at node C_{OUT}, and node C_{IN} are shown for three cases. The delay differentiation at node C_{OUT} is plotted in Figure 34 and the delay differentiation at node C_{IN} is plotted in Figure 35.

Table 4. Resistor range for different Δ values: $R_{o(l)}$ = open low resistor value, $R_{o(h)}$ = open high resistor value, $R_{s(l)}$ = short low resistor value, $R_{s(h)}$ = short high resistor value.

Case	Δ (nsec)	$R_{o(l)}$ (kΩ)	$R_{o(h)}$ (kΩ)	$R_{s(l)}$ (kΩ)	$R_{s(h)}$ (kΩ)
1	0	1	70	800	2000
2	4	1	22	25	100
3	8	1	22	25	100
4	12	1	22	25	100
5	16	1	20	25	100

5.4.4.2 Short Fault

The short fault is also examined for five different values of slack Δ. For any of the five cases, a short resistor value lower than $R_{s(l)}$ produces stuck-at behavior. $R_{s(h)}$ is selected such that current differentiation becomes insignificant compared to the differentiation at $R_{s(l)}$. The ranges of short resistor values for all five cases are shown in Table 4.

Except for case 1, all slack values produce no transition in the output signal at node C_{OUT} for fault severity less than 1, which corresponds to $R_s = 25$ kΩ. For a short resistor value below 25 kΩ, C_{OUT} produces an incorrect logic value.

For case 1 where $\Delta = 0$, the signal at node C_{OUT} rises even with $R_s = 700$ kΩ which corresponds to a fault severity of 0.035. The signal at node C_{IN}, however, is not affected until R_s drops below 55 kΩ at which point an incorrect logic value is produced.

For all cases where the slack is greater than or equal to 4 nanoseconds, the current differentiation increases almost linearly with fault severity. The delay differentiation value at any fault severity for all slack values is within a range of 0.2. A representative plot of current differentiation, with $\Delta = 8$ nanoseconds, is shown in Figure 36.

5.4.5 Observations

5.4.5.1 Open Fault

The slack has an indirect effect on the output response of the faulty circuit. When the slack is large, the input vector is applied earlier to turn path 1 on earlier. Although the open resistor reduces the conduction of path 1, internal nodes $\overline{C}_{OUT}$, W, X, and Y are pre-charged to a strong logic 1 due to the long charging period before the evaluate phase. When $\phi_1(t) = 1$, all internal node capacitors have to be discharged. Since the circuit takes a long time to discharge all the nodes, the rise of $C_{OUT}(t+1)$ is slow.

When the slack is small, the input vector is applied only slightly before the evaluate phase. The internal nodes are charged to less than 5 volts. This voltage value is reduced during the evaluate phase and, since the voltage level is closer to 0 volts, the discharge process takes less time. Therefore, $C_{OUT}(t+1)$ rises faster in a circuit with small slack than in a circuit with large slack.

Even in the presence of a severe fault, the output signal rises faster in a circuit with small slack than in a circuit with large slack. As a consequence, a faulty circuit with a larger slack produces a larger rise time delay for the same open resistor value. For the same fault severity, a faulty circuit with a large slack can produce stuck-at behavior, while with a small slack, it produces only a large delay. In the circuit with $\Delta = 16$ nanoseconds, stuck-at behavior occurs if $R_o > 20$ kΩ. A circuit with $\Delta = 12$ nanoseconds or less produces only an increase in delay. The increase in delay is reduced when the slack is reduced.

A large slack not only results in a slow rise time, but also a weak logic 1 value at node C_{OUT}. The weak logic value is propagated to node D and results in a transition delay at node E that is larger than the delay at node C_{OUT}. The effect of the fault thus increases and is observed as

a severe delay at node C_{IN}. As a result, with the same open resistor value, the delay differentiation of the signal at node C_{IN} in case 2 is the smallest, followed by case 3 and case 4. For case 5, the delay differentiation of the signal at node C_{IN} increases and produces stuck-at behavior at a lower open resistor value.

5.4.5.2 Short Fault

While charge in the internal nodes reduces the switching speed of a circuit implemented using domino logic in the presence of an open fault, the charge reduces the effect of a short fault in the circuit.

When the slack is large, node $\overline{C}_{OUT}$ and internal node X in a fault-free circuit are charged to logic 1 and held at logic 1 during the evaluation phase. In the event of a short fault, a current path exists. Nodes $\overline{C}_{OUT}$, W, X, and Y are charged to logic 1 through the current path during the precharge stage. During the evaluation phase, although the current path is conducting through the short resistor, all internal nodes have to be discharged before the signal at node $\overline{C}_{OUT}$ falls to an incorrect logic value. The discharge process takes a long time as the total capacitance of the n-network is large. When the short fault is more severe, the internal node capacitance is charged more. The discharge process takes an even longer time, and the faulty circuit behaves more like a fault-free circuit.

When the slack is 0, there is no time to charge the internal nodes during the pre-charge phase. During the evaluation phase, a current path conducts to pull down the voltage at node $\overline{C}_{OUT}$. When the short fault is more severe, the signal at node $\overline{C}_{OUT}$ is pulled down more easily and an incorrect logic value is produced at node C_{OUT}.

5.4.6 General Conclusions

In this circuit, the open fault affects the transition time of the observable output signal. Depending on the fault severity, the increase in the transition delay at the output may or may not increase the transition delay at the input through the feedback path in the next cycle. The short fault does not affect the transition time of the observable output signal, but does affect the steady state supply current of the circuit.

A cumulative effect due to the feedback of the delayed input signal driving the faulty gate is expected for certain input vectors. There are also two ways that stuck-at behavior may occur in this circuit. One cause is that the signal at node C_{OUT} does not rise as expected and the other cause is that the signal at node C_{OUT} changes more slowly than clock ϕ_1 drops.

In addition to similarities in behavior with the FCMOS implementation, the domino implementation of the bit-serial adder is also affected by charge at internal nodes.

Chapter 6. Analysis of Results and Implications for Test

From the results in Chapter 4 and Chapter 5, the effectiveness of the tests can be generalized for various circuit features and faults. Both propagation delay test and supply current test show different effectiveness for testing different circuits. The results also show the limitations of these test methods for testing different circuits.

6.1 Strengths and Limitations for Test Methods

From the simulation experiments reported above, both test methods are effective for testing almost all circuits investigated. However, there are limitations for both test methods.

6.1.1 Propagation Delay Test

Propagation delay test is capable of detecting faults in combinational circuits where inputs are short pulses or in sequential circuits with a fast clock. The clock speed does not affect the propagation delay of fault-free circuits as the transition delay of fault-free circuits is small. At a slow clock speed, the faulty gate output, although having a large transition delay, has sufficient time to settle to a correct logic value. Therefore, the correct output is propagated, perhaps with a small increase in transition delay. When the input vectors are applied at a high speed, the increase in transition delay at the faulty gate output may not be propagated and stuck-at behavior can be detected. Propagation delay test is thus more effective when performed at high clock speeds.

Propagation delay test considers the time required for an output transition from logic 0 to logic 1 or from 1 to 0. In this research, 2.5 volts is assumed to distinguish logic 0 from logic 1. In actual circuits, the switching voltage is somewhat fuzzy due to variations in processing parameters. Different dies on the same wafer or even different gates in the same circuit may have different switching voltages. The transition delay at the same observable output of different circuits varies with the change of switching voltage. The effectiveness of propagation delay test can, therefore, also vary.

Propagation delay test also cannot detect general short faults in circuits implemented with domino logic, except for the most severe short faults that produce stuck-at behavior. In the testing phase, the fault-free gate output is expected to produce a strong logic 1 and the faulty gate output is expected to produce a weak logic 1 or logic 0. However, the gate output of domino logic is pre-charge to strong logic 1. The transition from logic 0 to logic 1 occurs during the precharge phase and not during evaluate phase when the output is measured. Therefore, the propagation delay test can only detect stuck-at behavior produced by the most

severe short faults in domino logic when the current path pulls the gate output completely to ground during evaluate phase.

6.1.2 Supply Current Test

Supply current test measures the steady state supply current of the circuit. The test is more effective than propagation delay test in detecting short faults in almost all circuits investigated.

However, in sequential circuits, the effectiveness of supply current test is reduced by an increase in clock speed. The supply current needs a long settling time between two transitions. In the sequential circuits investigated, a transition occurs at the rise of clock. For a circuit with a fast clock, one transition time is close to another. The settling time is reduced and the supply current of the fault-free circuit has less time to reach the steady state, and hence current measurements are large. In the presence of a short fault, the increase in supply current is insignificant and the effectiveness of supply current test is reduced.

The effectiveness of supply current test is also reduced by an increase in circuit size. The steady state supply current of fault-free CMOS circuits is the total leakage current through all OFF transistors. In a small circuit, the steady state supply current is small, and the large current drawn due to a short fault is significant. When the size of a circuit is large, the steady state supply current of the fault-free circuit is also large and the increase in current due to a short fault becomes insignificant. For example, when the circuit size increases by a factor of ten, the effectiveness reduces by a factor of ten due to a ten-fold increase in fault-free supply current. When the circuit size increases by a factor of one hundred, the effectiveness of current test reduces by a factor of one hundred.

6.2 Circuit Features Affecting Test

Besides the limitations of both test methods, circuit features also affect the effectiveness of tests. In general, CMOS faults are easier to detect in combinational circuits than in sequential circuits. In sequential circuits, however, it is easier to detect the most severe faults that produce stuck-at behavior.

Circuit features that affect test effectiveness in combinational circuits are mainly the length of the fault propagation path, the depth of the gate and the size of the circuit. In sequential circuits, test effectiveness is also affected by slack and clock speed.

In a combinational circuit, stuck-at behavior is only detected when an observable output is stuck at one value. In a sequential circuit, stuck-at behavior is also detected if the transition of the output signal occurs more slowly than the fall of the clock pulse.

6.2.1 Combinational Circuits

A circuit with a long propagation path between a faulty gate and an observable output produces an insignificant increase in transition delay. When the transition delay increases in the presence of faults, the increase is not significant when compared to a large propagation delay in the fault-free circuit. On the other hand, a circuit with a short propagation path produces a significant increase in delay in the presence of faults, due to a small propagation delay in the fault-free circuit.

The pull-down strength of a deep circuit is weaker than the pull-down strength of a shallow circuit because of a long current path between the output node and V_{SS}. An open fault in the

n-network or a short fault that connects the output node and V_{SS} are therefore easier to detect in a deep circuit. A short fault across an n-channel transistor of a deep circuit, however, is harder to detect as the ON resistance of one or more n-channel transistors in series with the short resistor increase the total resistance value. Similarly, the pull-up strength of a deep circuit is weaker than the pull-up strength of a shallow circuit due to a long current path between the output node and V_{DD}. An open fault in the p-network or a short fault that connects the output node and V_{DD} are therefore easier to detect in a deep circuit. A short fault across a p-channel transistor of a deep circuit is harder to detect.

6.2.2 Sequential Circuits

When the slack is large, the circuit tolerates a large increase in transition delay, due to a more severe fault, before stuck-at behavior is detected. In a circuit with a fast clock or small slack, when the transition delay is large, the transition may occur later than the fall of the clock and stuck-at behavior occurs. Stuck-at behavior may occur in a sequential circuit with small slack, while it does not occur with large slack, even though the fault severity is the same.

If an output signal drives the gate through a feedback path, an increase in transition delay at the output due to a fault is propagated by the feedback path back to the input of the faulty gate. The slower transition of the input at the faulty gate produces an even larger increase in transition delay at the output. The delay thus increases at each clock cycle until stuck-at behavior occurs.

In a fully complementary implementation of a sequential circuit, when the input to the gate is leading the clock pulse by a large value, i.e. the slack is large, the fault is harder to detect since the output signal has a long time to settle to the correct value before the clock falls. For a domino implementation of a sequential circuit, large slack may allow an open fault to be

detected more easily. When the slack is large, internal nodes have a long time to charge during the precharge phase. Thus, during the evaluate phase, the internal nodes take a long time to discharge and a small increase in delay can cause the previous value to be transmitted through the transmission gate.

6.3 Fault Features Affecting Test

Faults investigated in this research are open and short faults. For a slightly severe open fault, the transition delay increases slightly. Similarly, a slightly severe short fault produces a small increase in transition delay and steady state supply current. The differentiation of propagation delay or supply current is small. It is hard to use either one of the tests to detect slightly severe faults. The transition delay or supply current increases tremendously for a very severe fault. It is easy to detect a severe fault. When the fault is most severe, stuck-at behavior is easily detected.

The same open or short resistor value produces different fault severities and differentiations in different representative circuits simulated. From the variation in fault severities and differentiation, it can be concluded that faults in some locations are easier to test than those in other locations.

Chapter 7. Summary

This research investigated sensitization conditions and test effectiveness for open and short faults in CMOS circuits. In testing open faults, propagation delay test was used. Propagation delay test and supply current test are also used in testing short faults. Two metrics, differentiation effectiveness and range effectiveness were considered.

Representative combinational circuits were modeled and simulated from a fault-free condition to the most severe fault condition for open and short faults in the n-network, beyond which stuck-at behavior occurs. Several sequential circuits were also modeled and simulated over the same range of fault severities. From the observations, the effectiveness and limitations of propagation delay test and supply current test were determined. A general analysis was also made of factors affecting both propagation delay test and supply current test.

Circuit simulation at the transistor level provides accurate information about circuit behavior in a continuous domain, at the price of long simulation times. Faults have to be simulated from a fault-free condition to the most severe condition. About twenty simulations are needed to provide a close approximation of the differentiation plot. The total simulation time could take days or even weeks for a large circuit. Although there are some fast circuit simulators,

most of those produce less accurate results and some may even produce only approximate results.

To reduce the simulation time, a faster computer is needed. Speed-up in simulation can also be achieved by using an accelerator or multiprocessor computer.

In addition to the slow simulation time, SPICE and RELAX do not consider the temperature effects on circuit behavior. Electron and hole mobility vary with a change of temperature, and conductivity, switching voltage, and transition time of a gate output may vary with the change of temperature. The effectiveness of propagation delay test and supply current monitoring may vary. In SPICE and RELAX, mobilities are treated as constant values, and therefore test effectiveness does not change over the temperature. Future research could take temperature effects into account, as the same fault severity in the same circuit may produce different behavior under different temperatures conditions.

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Appendix A. Circuit Diagrams

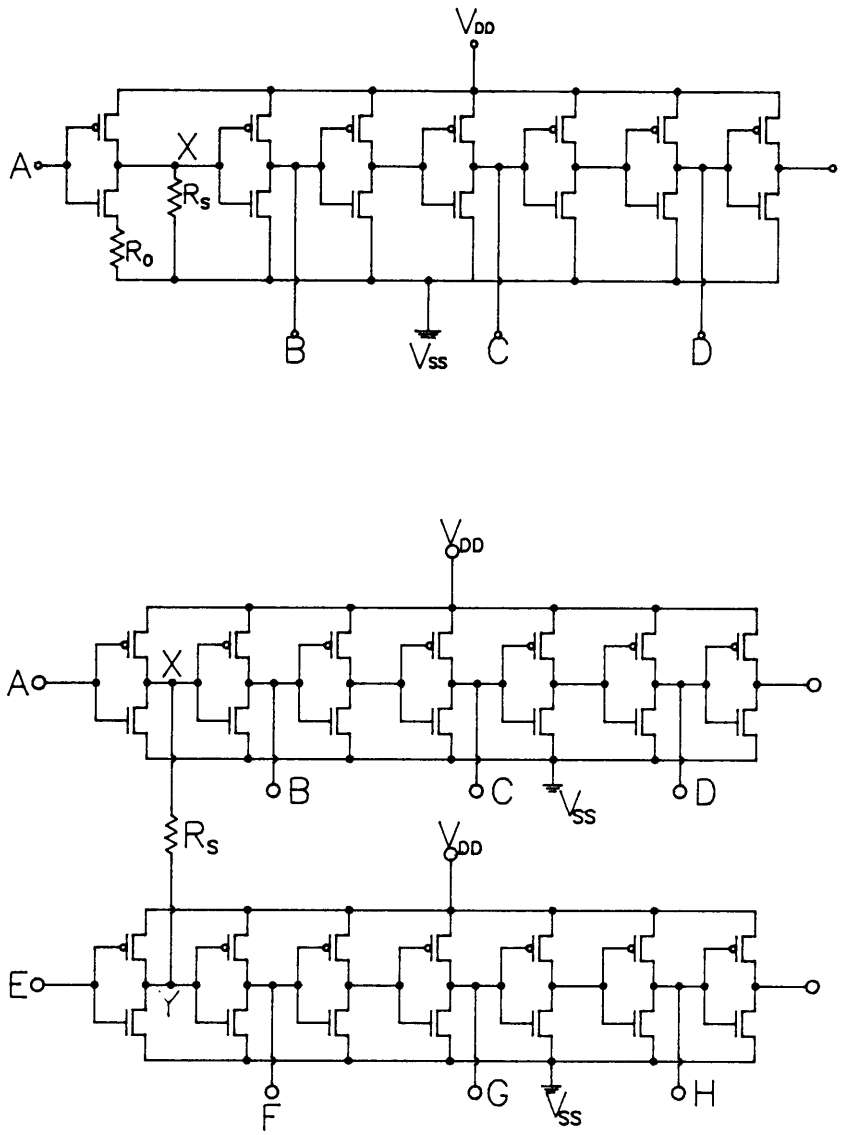

Figure 6. Inverter chain: (a) open fault and type 1 short fault, (b) type 2 short fault.

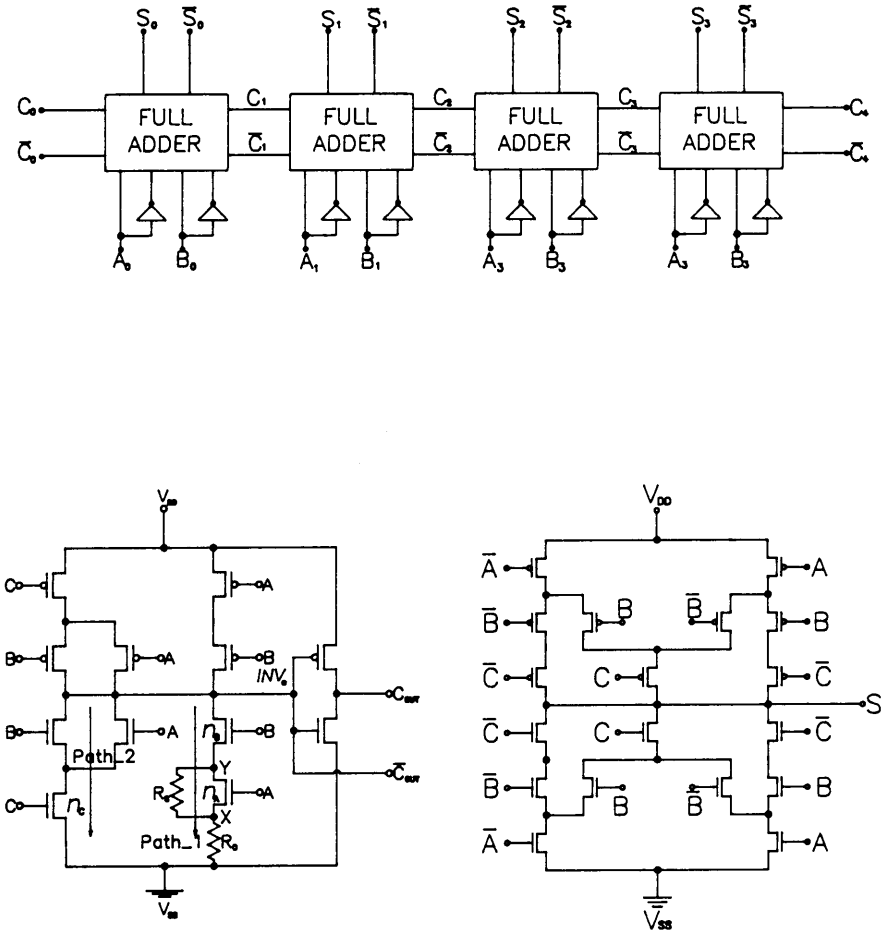

Figure 7. Four-bit ripple carry adder: (a) schematic capture, (b) complex-gate CARRY, and (c) complex-gate SUM.

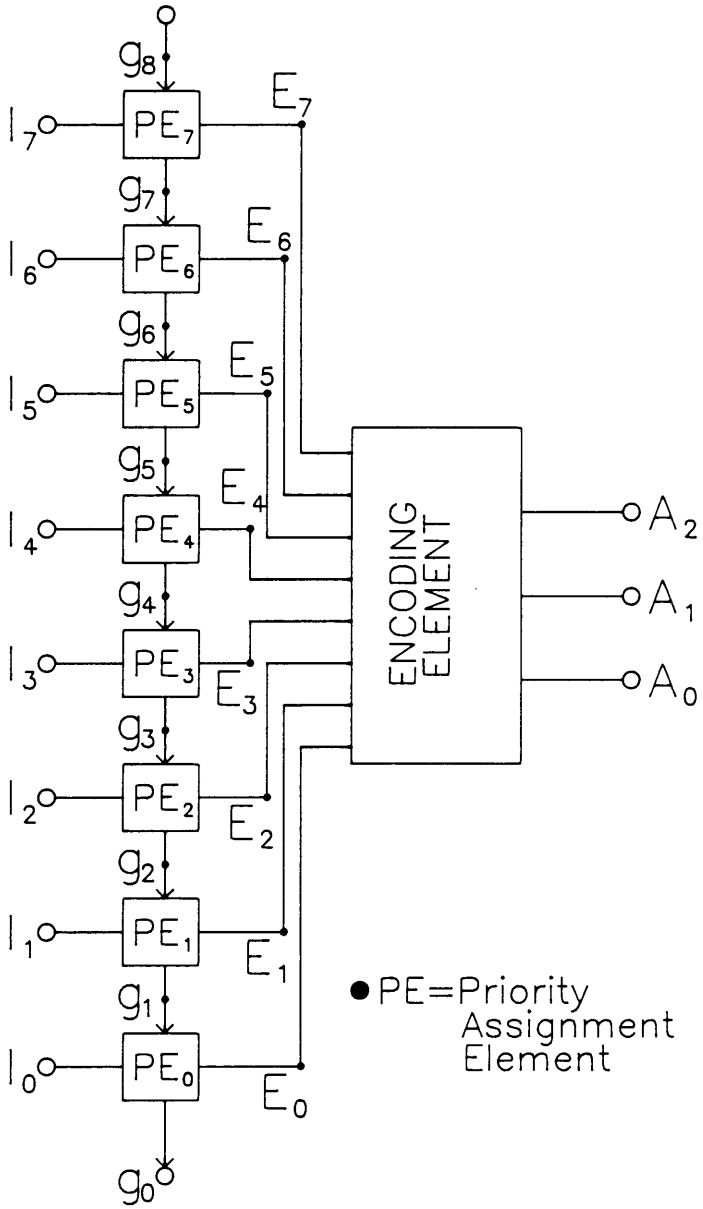

Figure 8. 8-to-3 priority encoder.

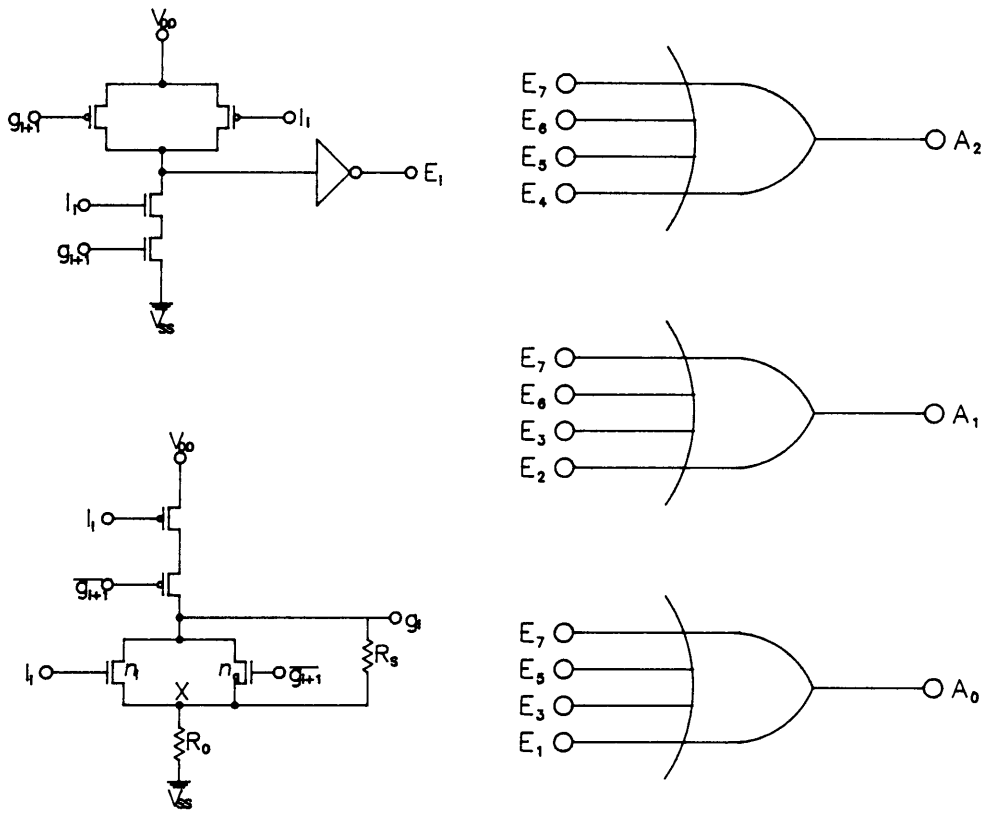

Figure 9. (a) One bit of priority assignment element, and (b) encoding element.

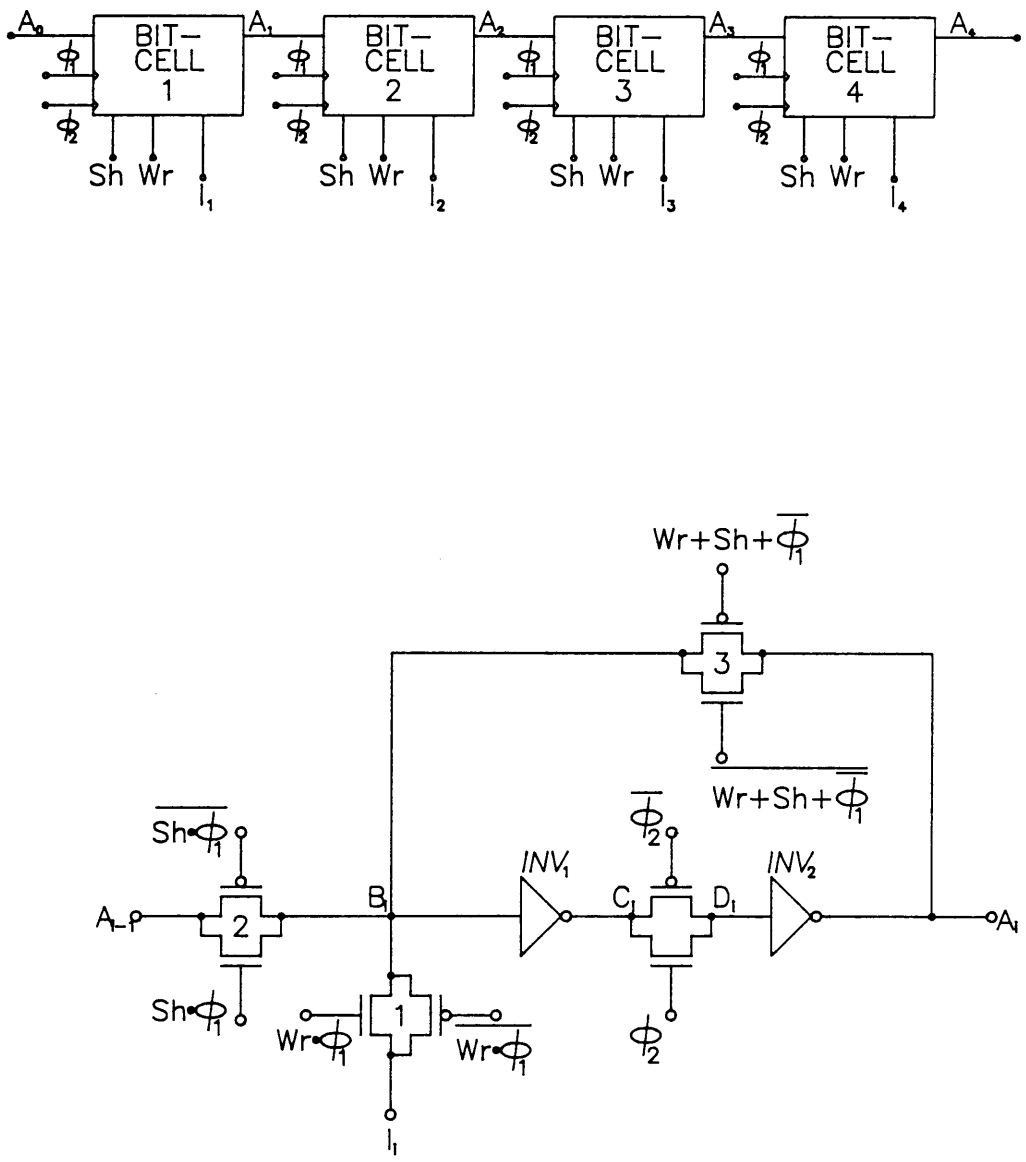

Figure 10. Four-bit parallel in serial out register: (a) block diagram, and (b) one bit-cell of the register.

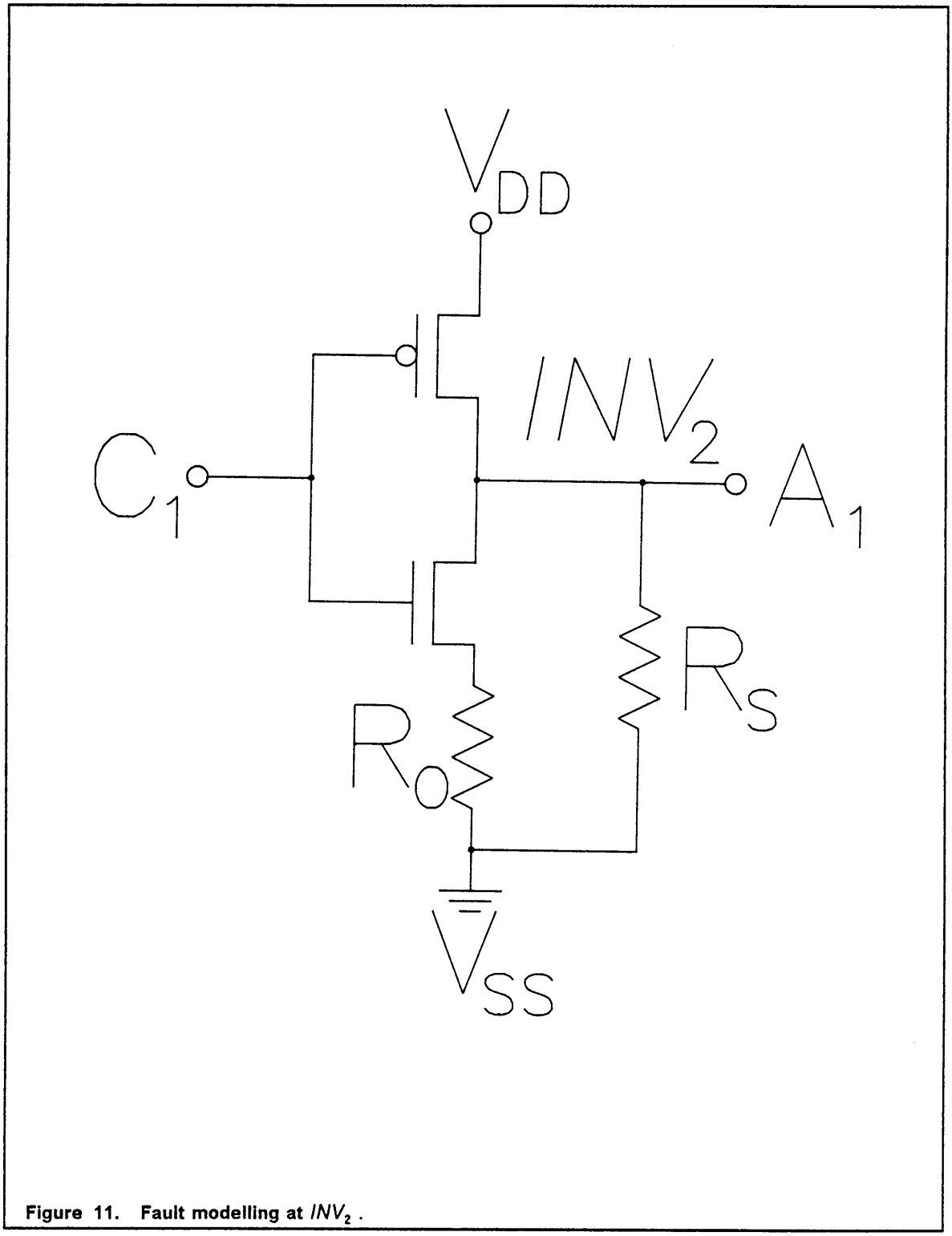

Figure 11. Fault modelling at INV_2 .

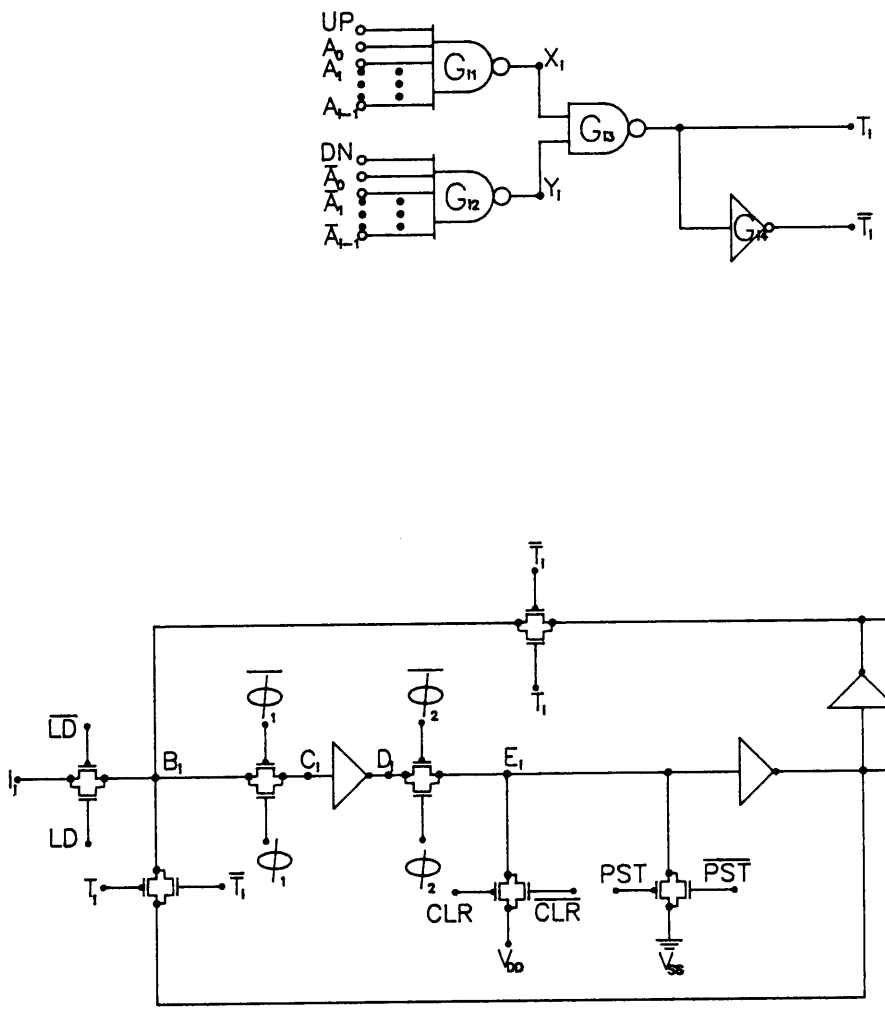

Figure 12. Schematic of bit-cell i in the 8-bit up/down counter: (a) two levels of NAND gates, (b) one-bit register.

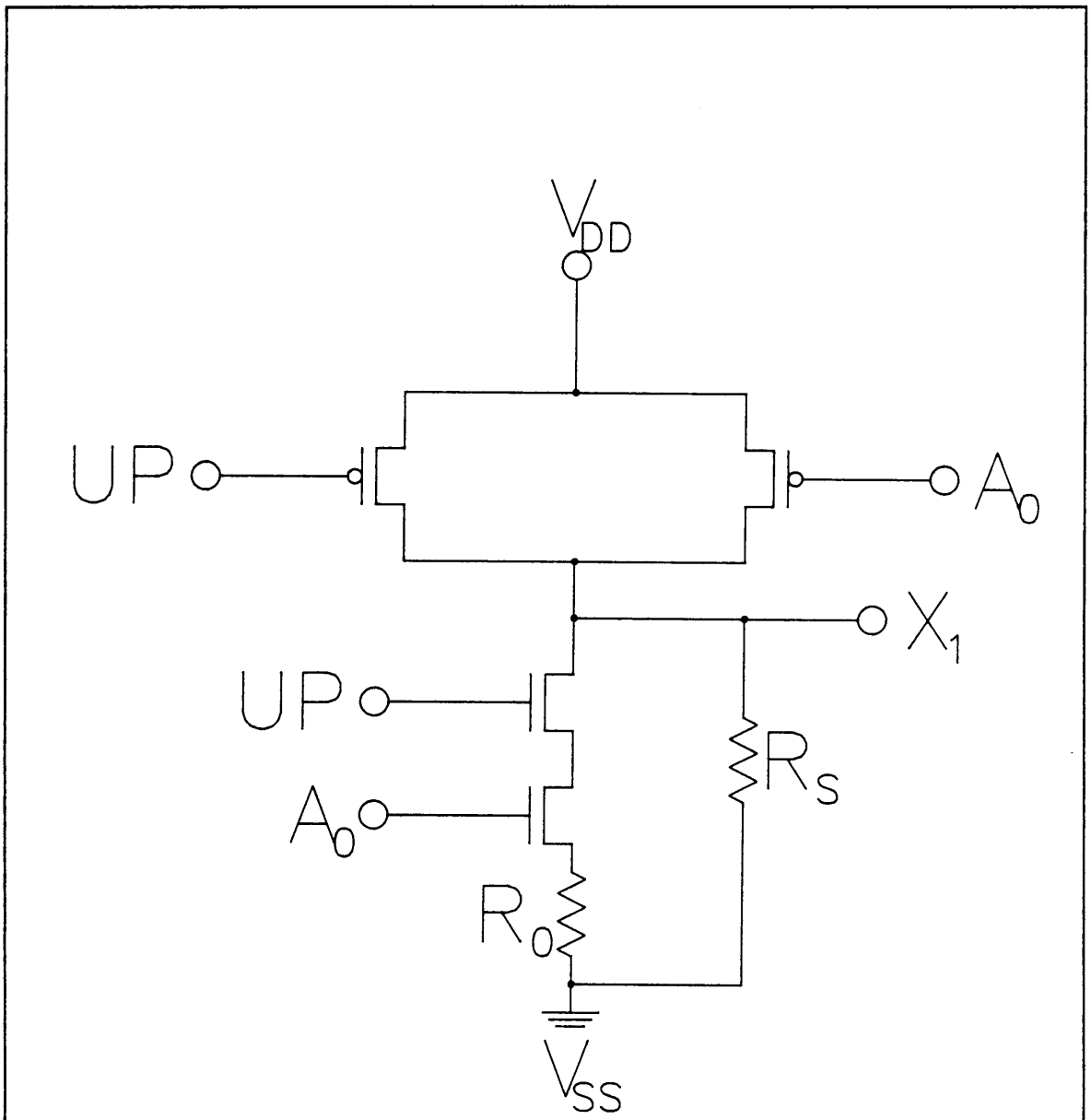

Figure 13. Open and short faults in G_{11} .

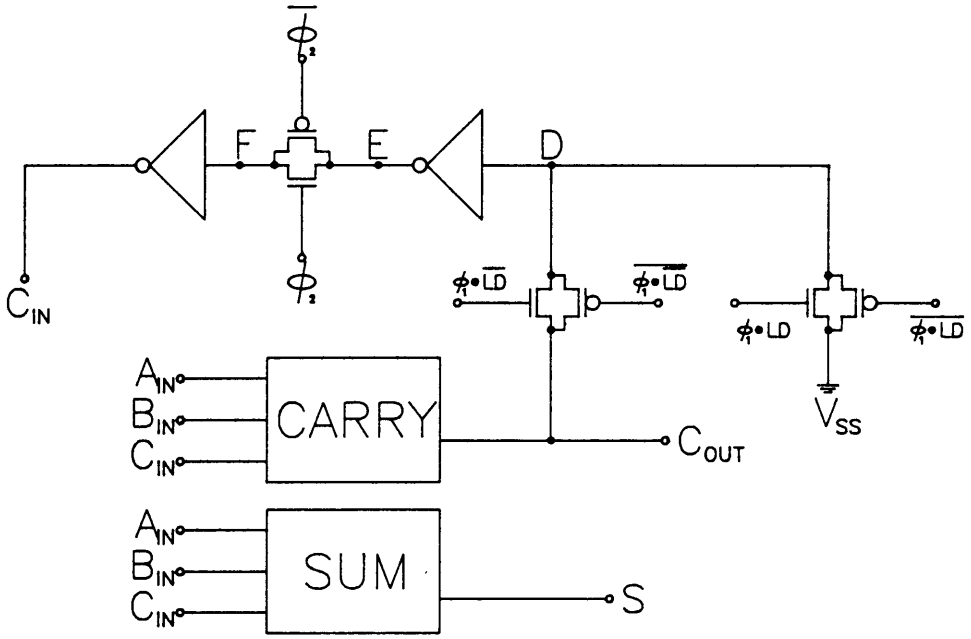

Figure 14. Bit-serial adder.

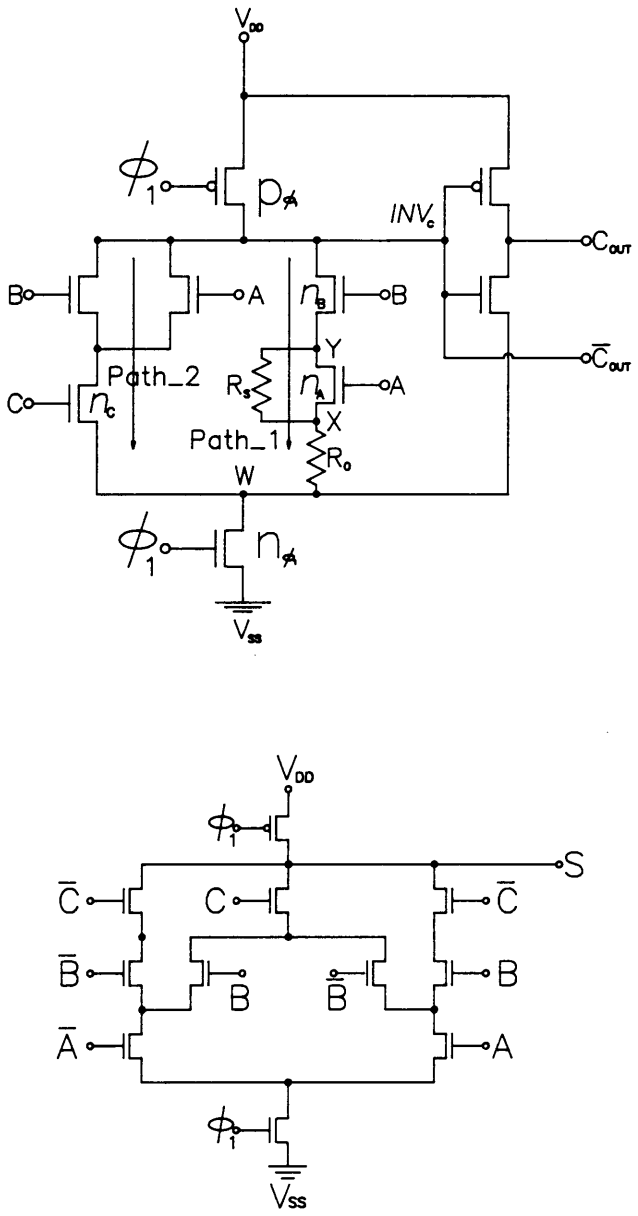

Figure 15. Domino logic full adder: (a) CARRY gate, and (b) SUM gate.

Appendix B. Test Effectiveness Results

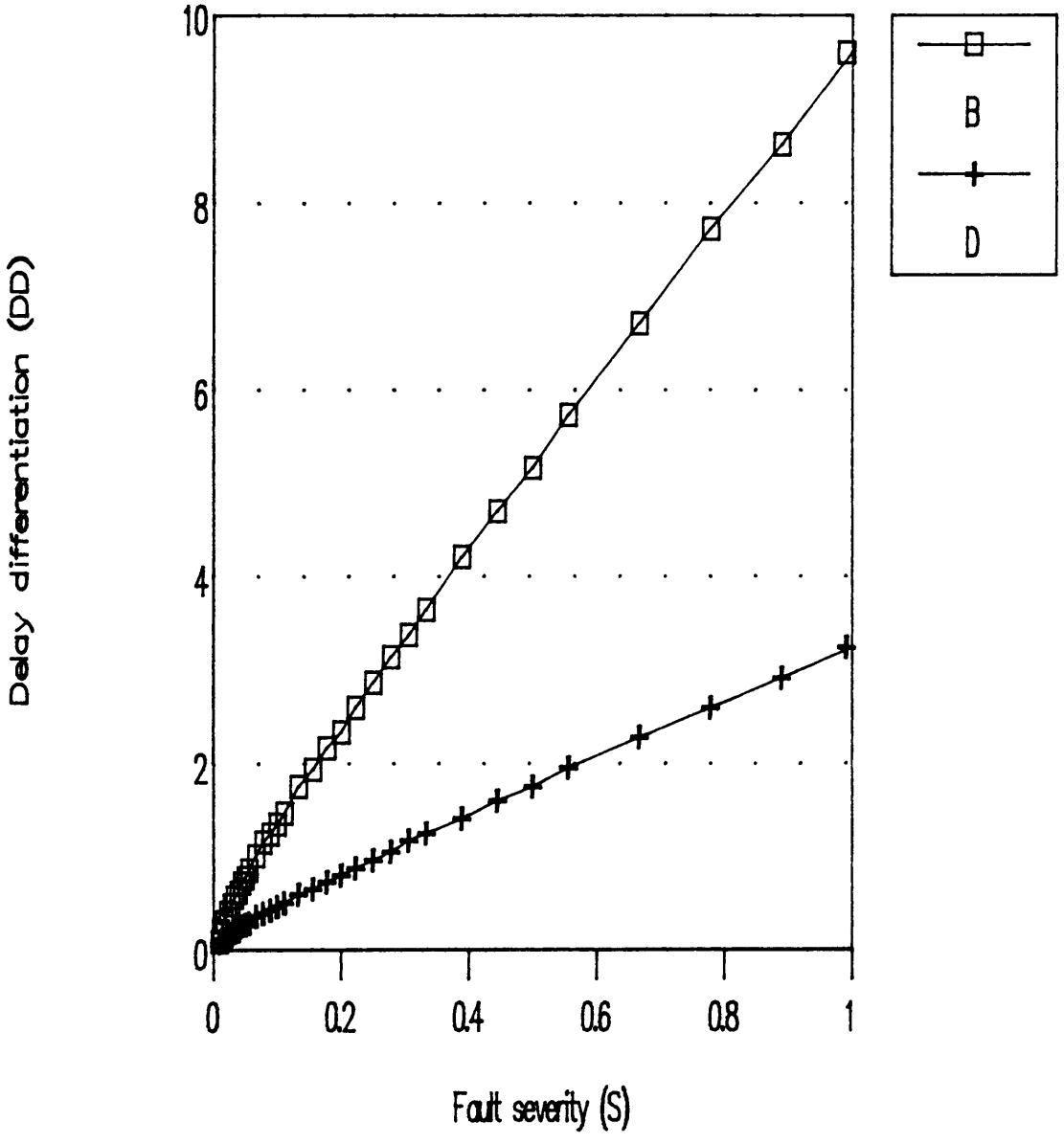

Figure 16. Delay differentiation for open fault in inverter chain.

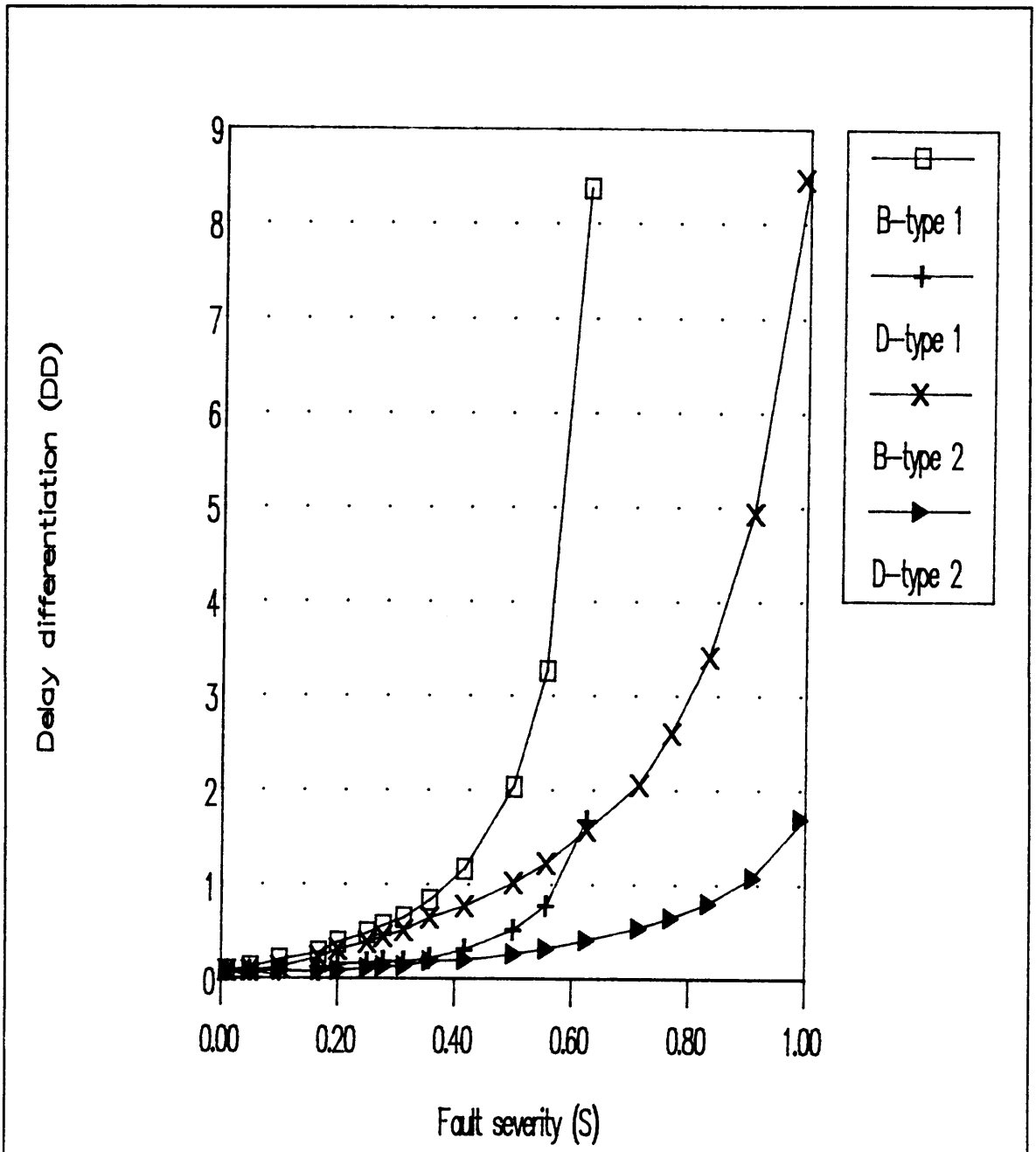

Figure 17. Delay differentiation for short fault in inverter chain.

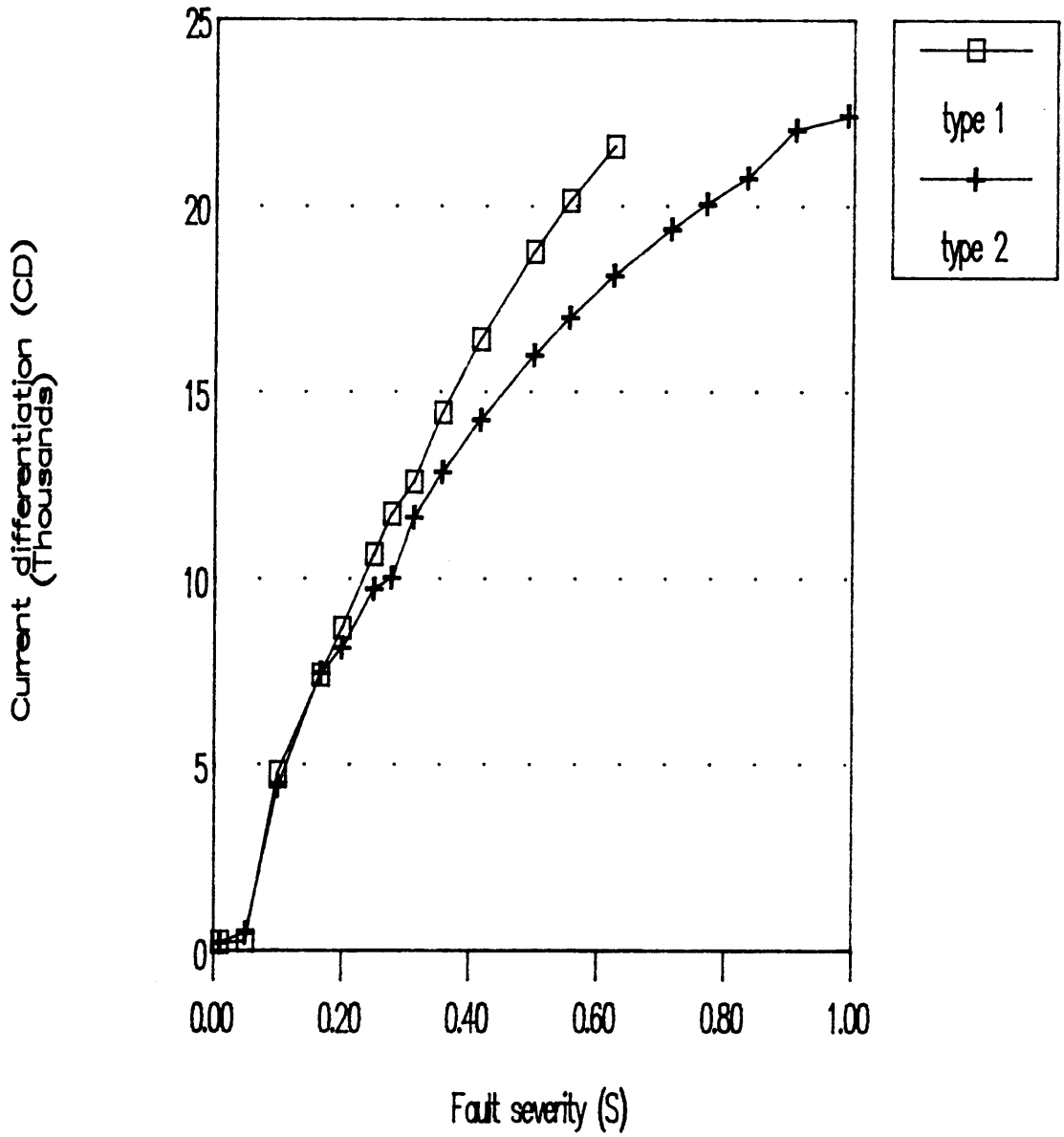

Figure 18. Current differentiation for short fault in inverter chain: (a) type 1, and (b) type 2.

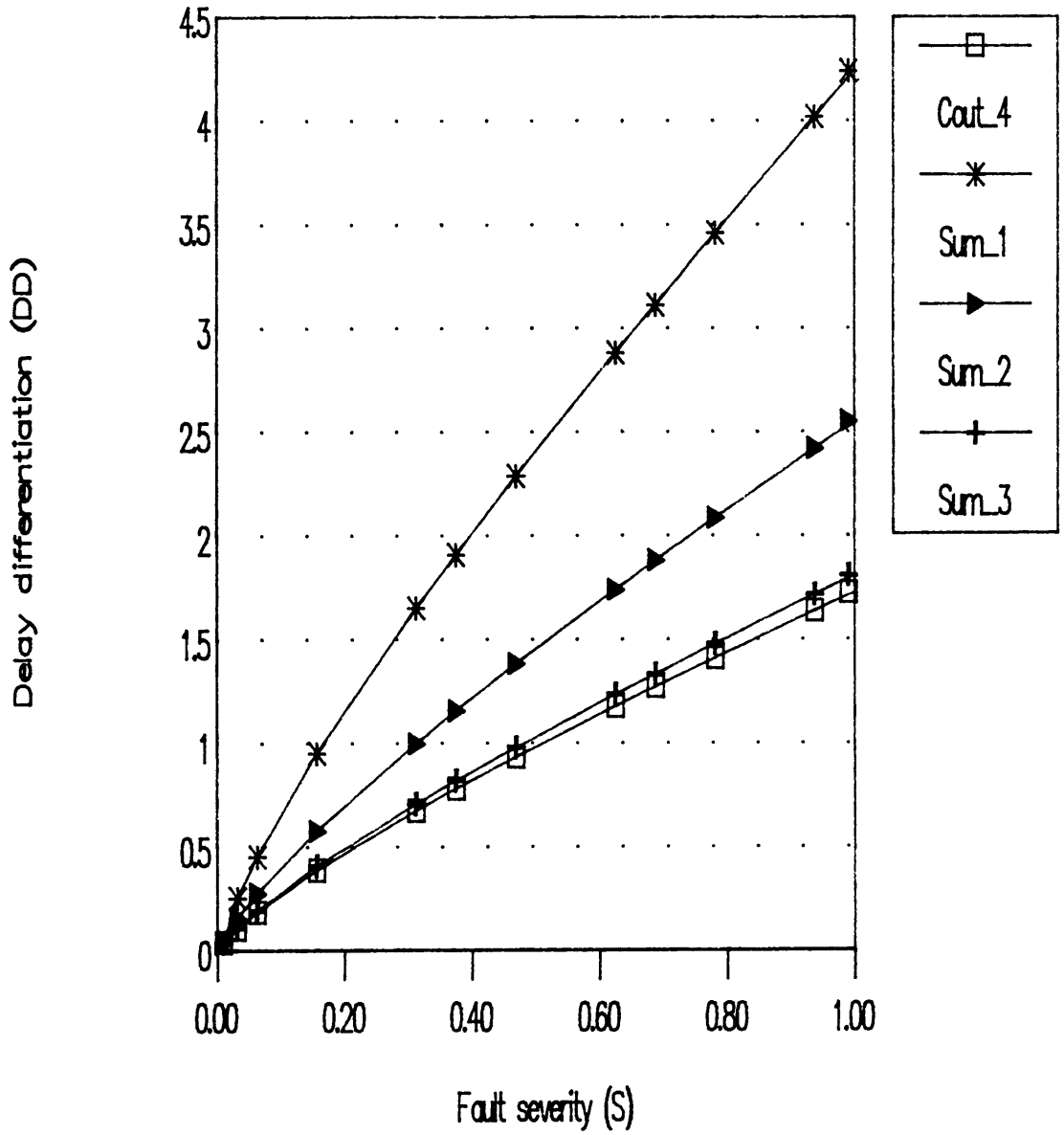

Figure 19. Delay differentiation for open fault in four-bit RCA.

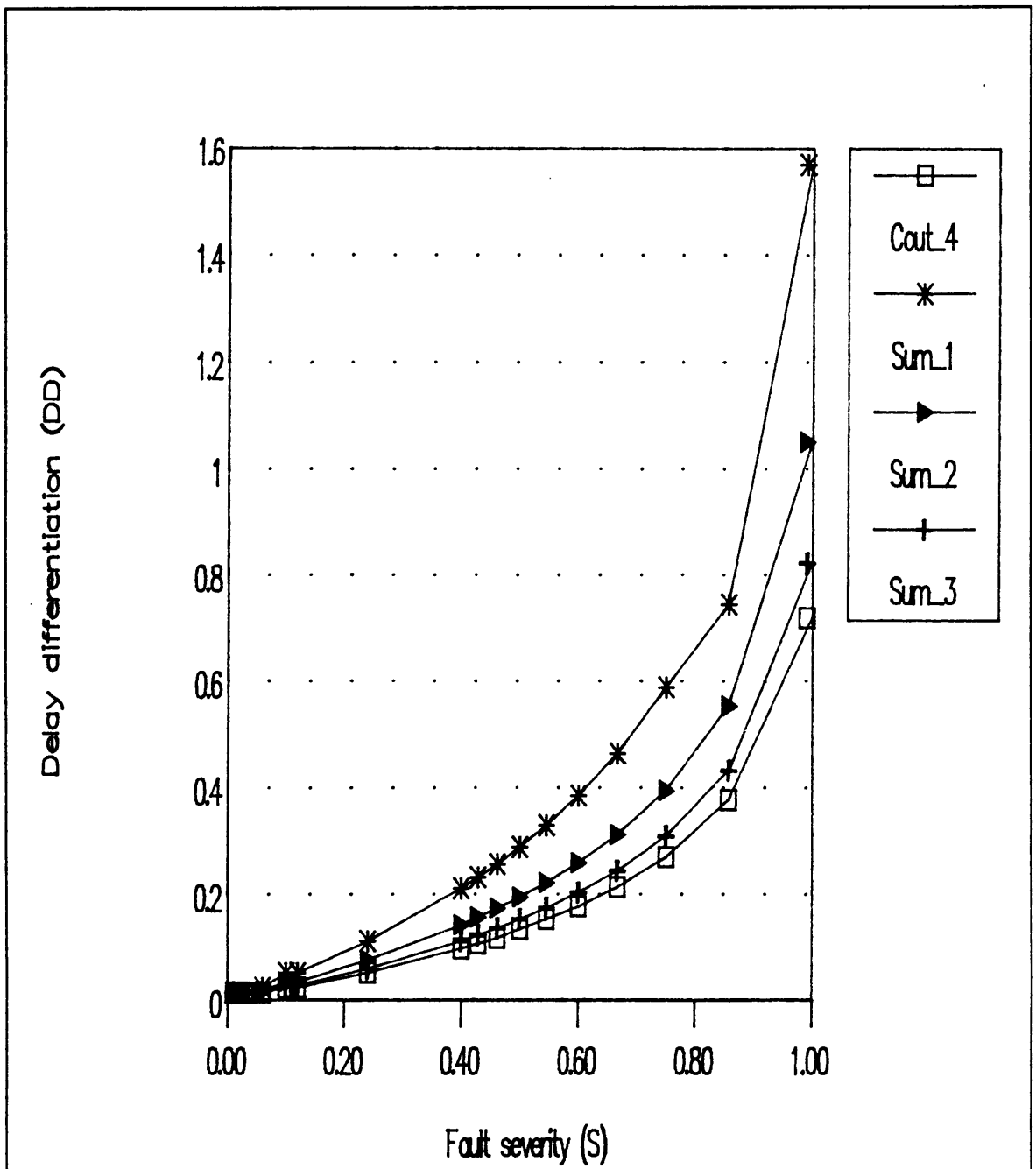

Figure 20. Delay differentiation for short fault in four-bit RCA.

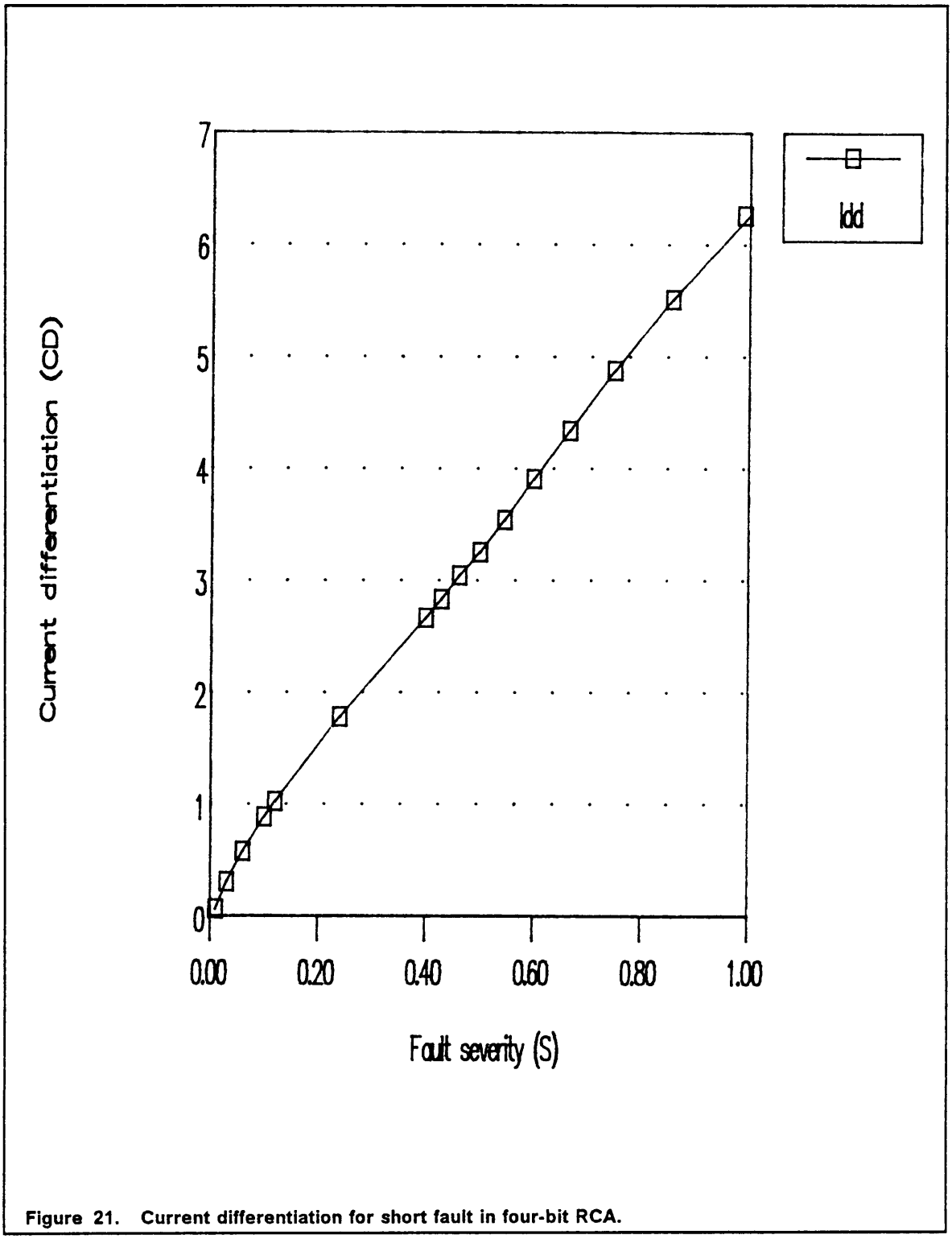

Figure 21. Current differentiation for short fault in four-bit RCA.

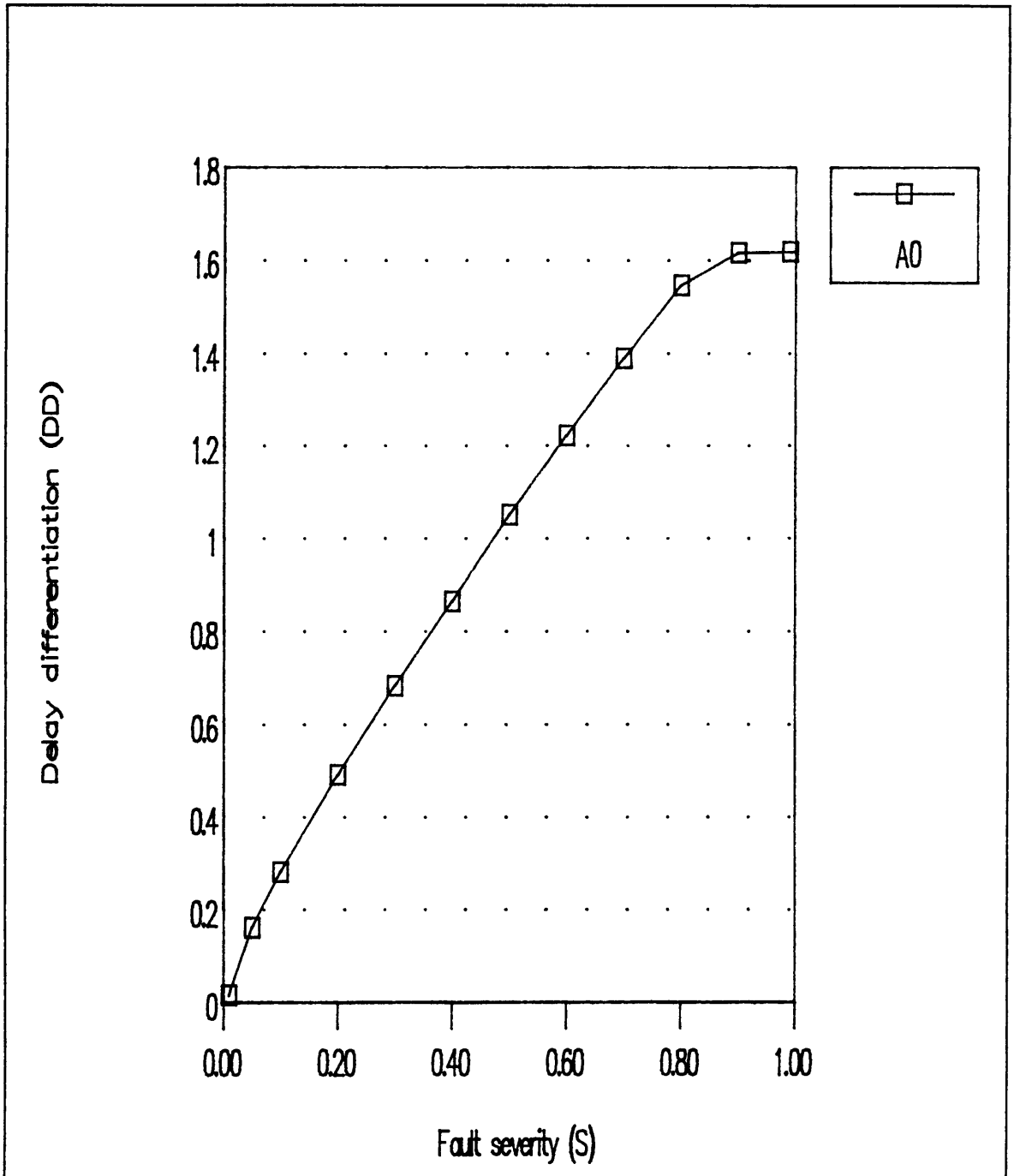

Figure 22. Delay differentiation at node $A_o(t)$ for open fault in priority encoder.

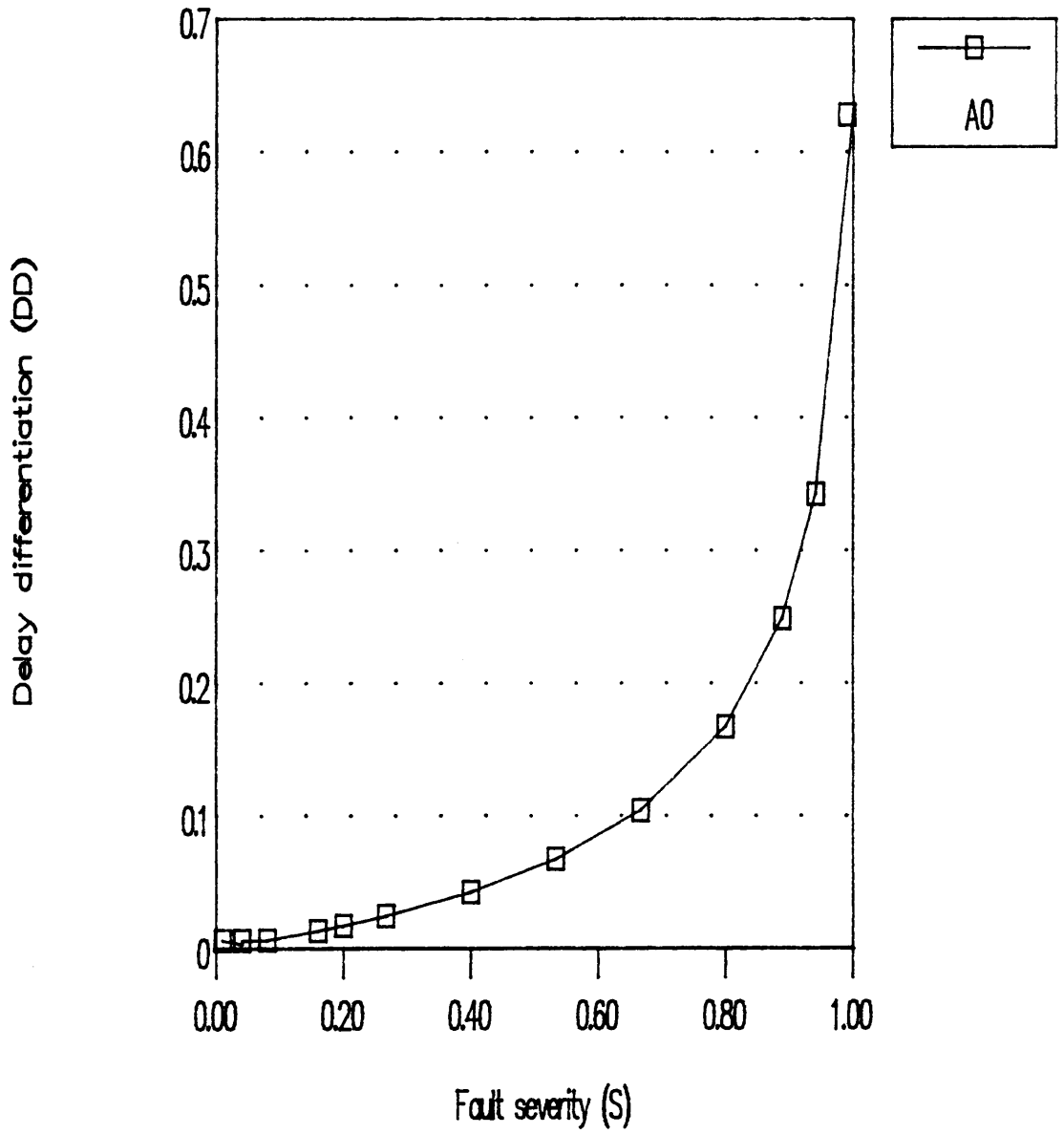

Figure 23. Delay differentiation at node $A_o(t)$ for short fault in priority encoder.

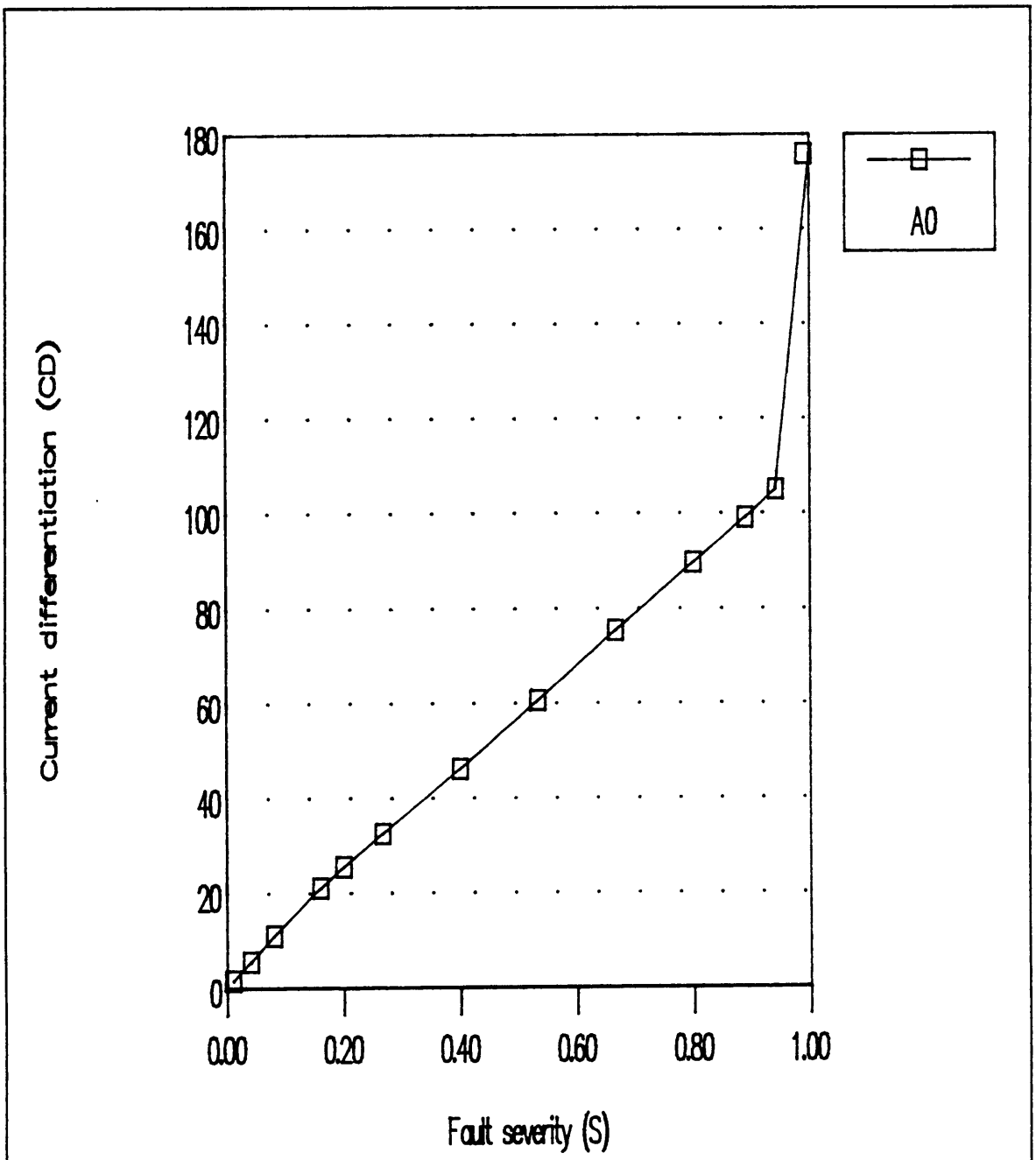

Figure 24. Current differentiation for short fault in priority encoder.

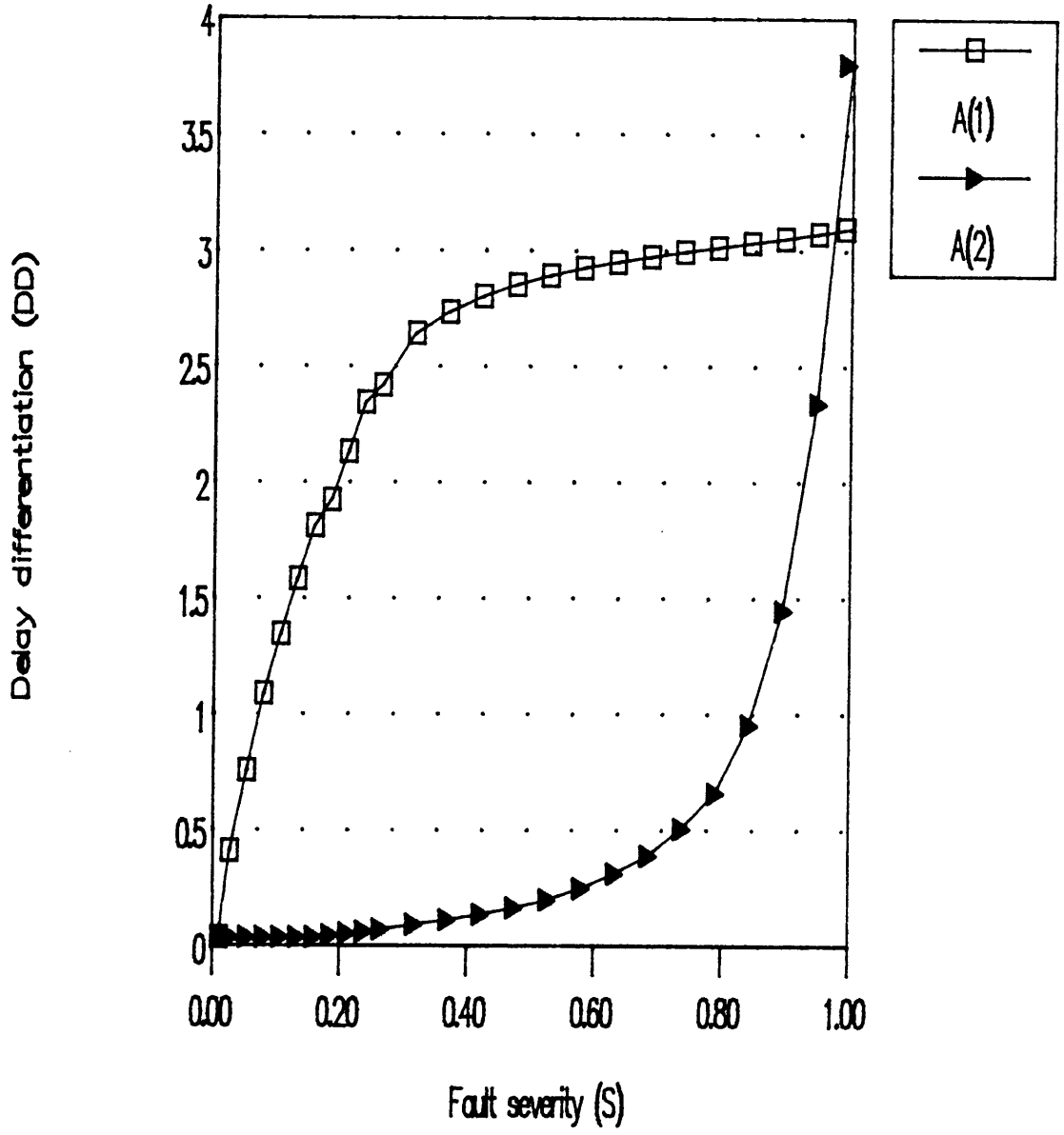

Figure 25. Delay differentiation for open fault in parallel in serial out register: node A_1 and node A_2.

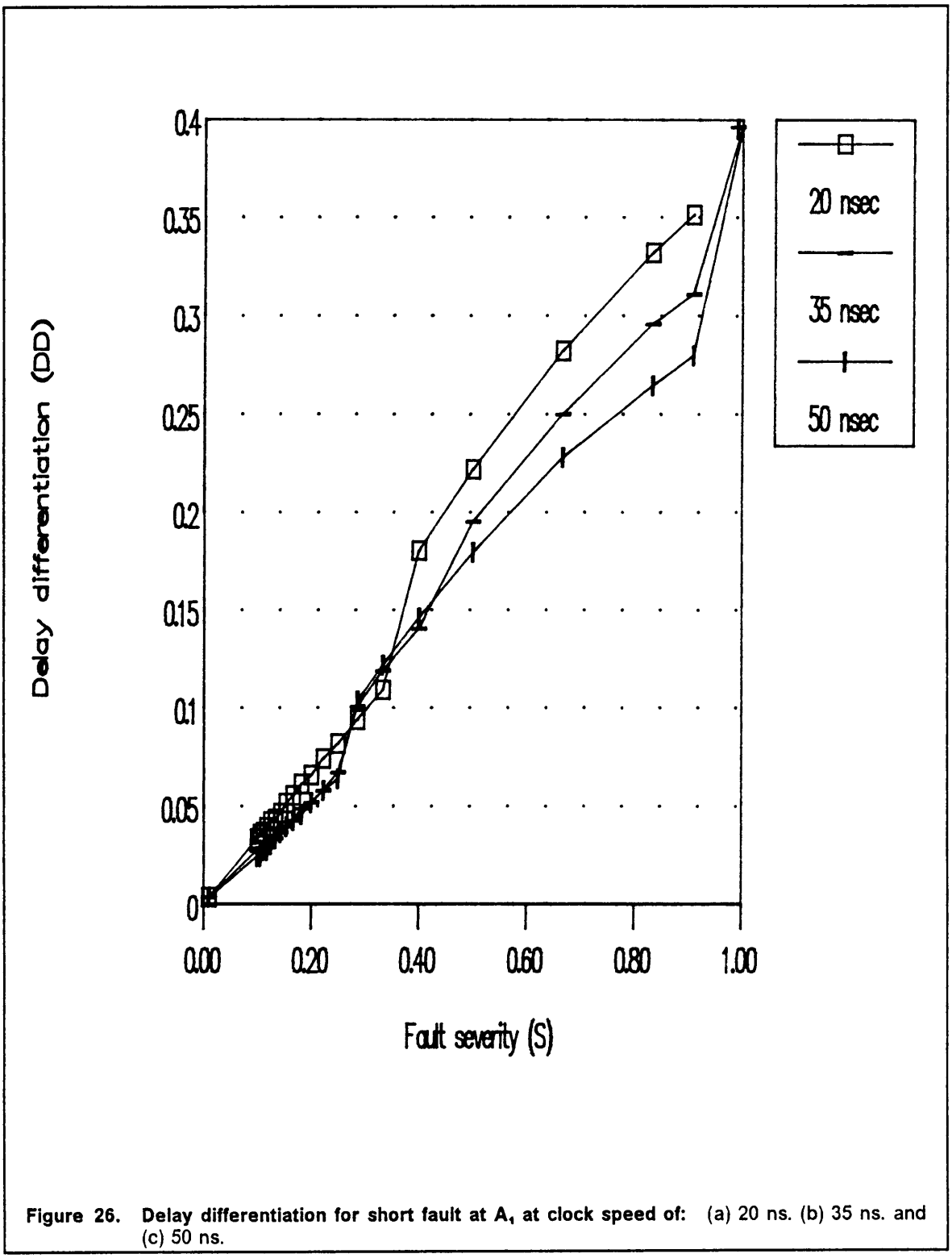

Figure 26. Delay differentiation for short fault at A_1 at clock speed of: (a) 20 ns. (b) 35 ns. and (c) 50 ns.

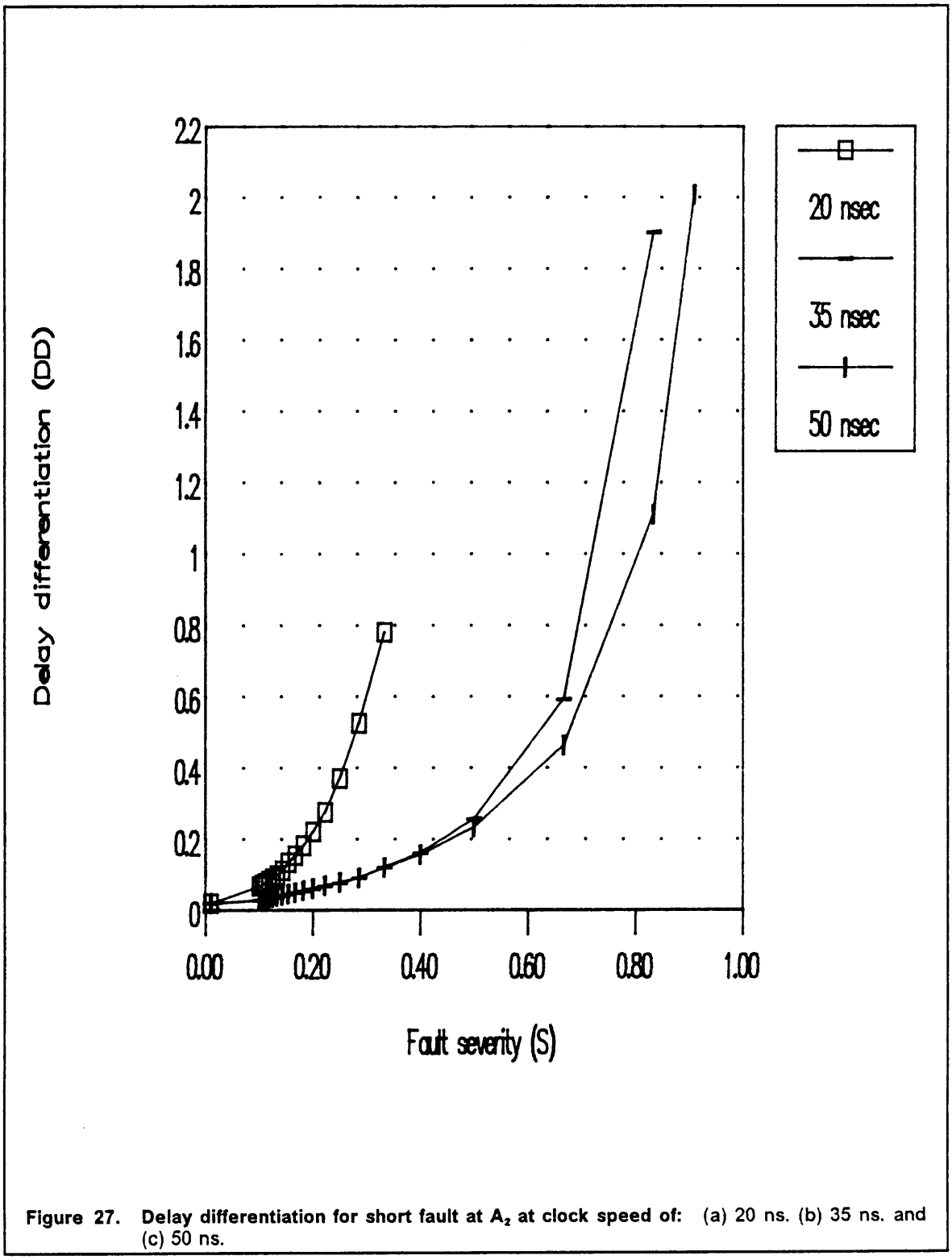

Figure 27. **Delay differentiation for short fault at A_2 at clock speed of:** (a) 20 ns. (b) 35 ns. and (c) 50 ns.

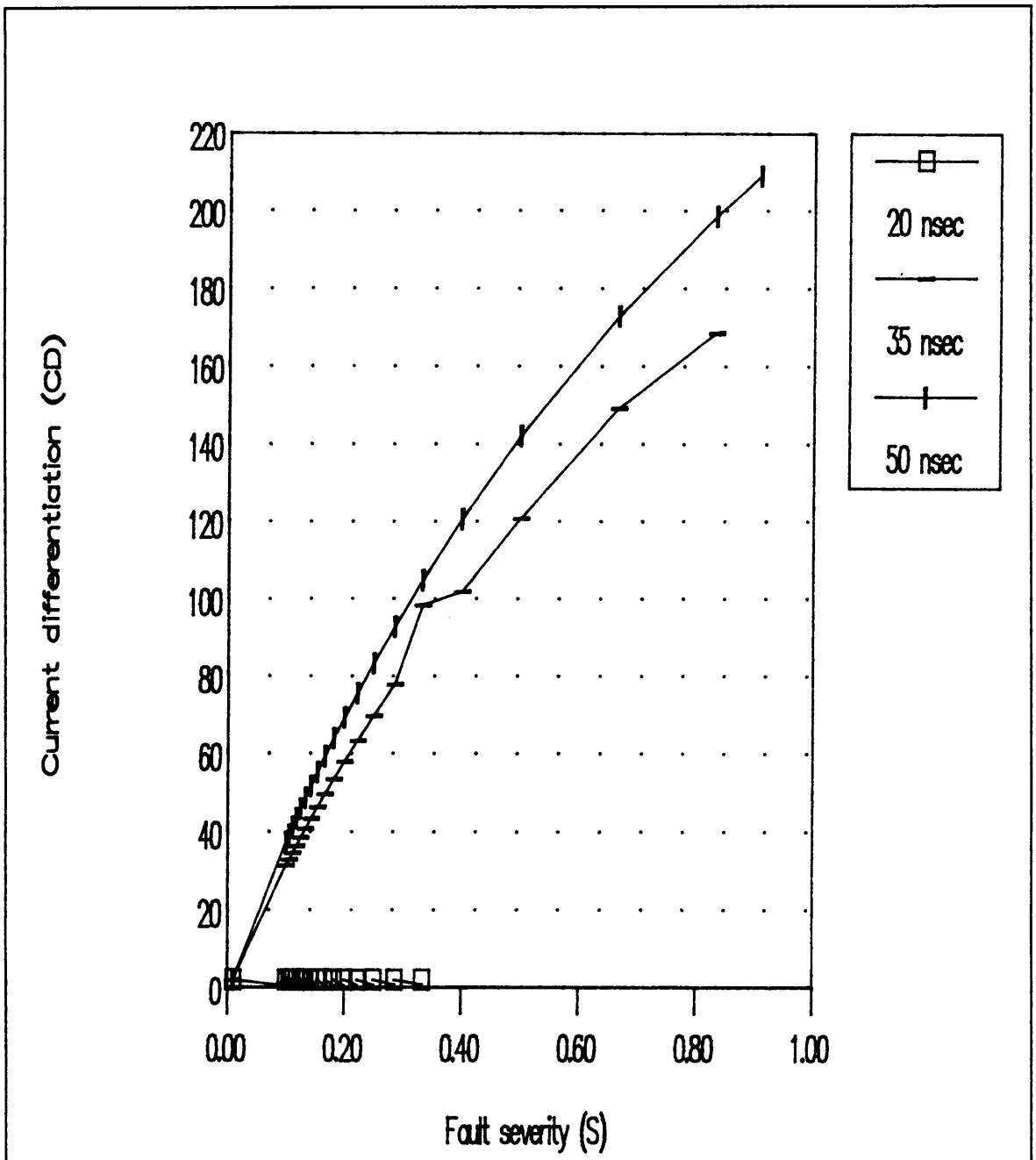

Figure 28. Current differentiation for short fault at clock speed of: (a) 20 ns. (b) 35 ns. and (c) 50 ns.

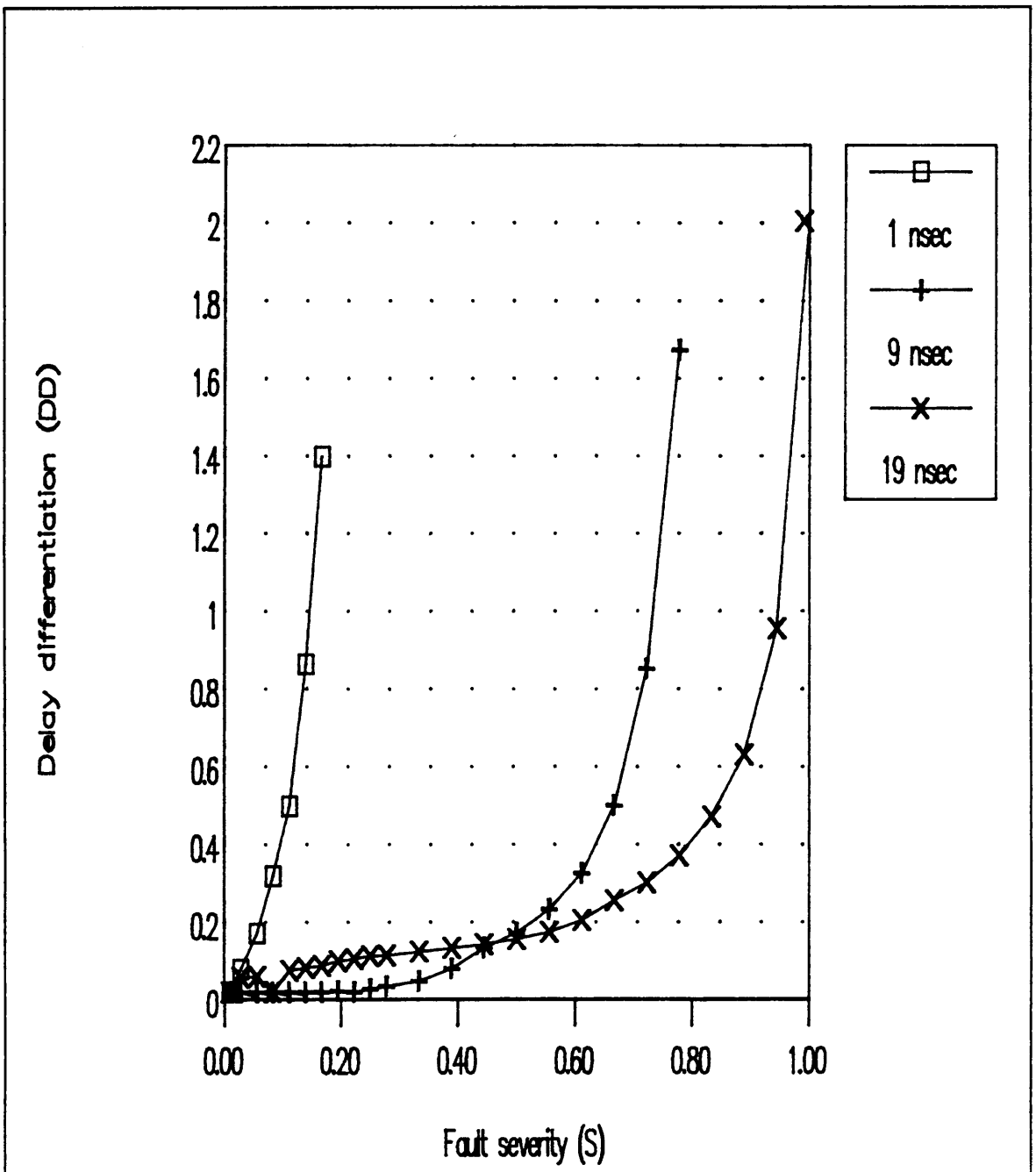

Figure 29. Delay differentiation for open fault in up/down counter: Group 1 with $\Delta = 1$ ns., Group 2 with $\Delta = 9$ ns., and Group 3 with $\Delta = 19$ ns.

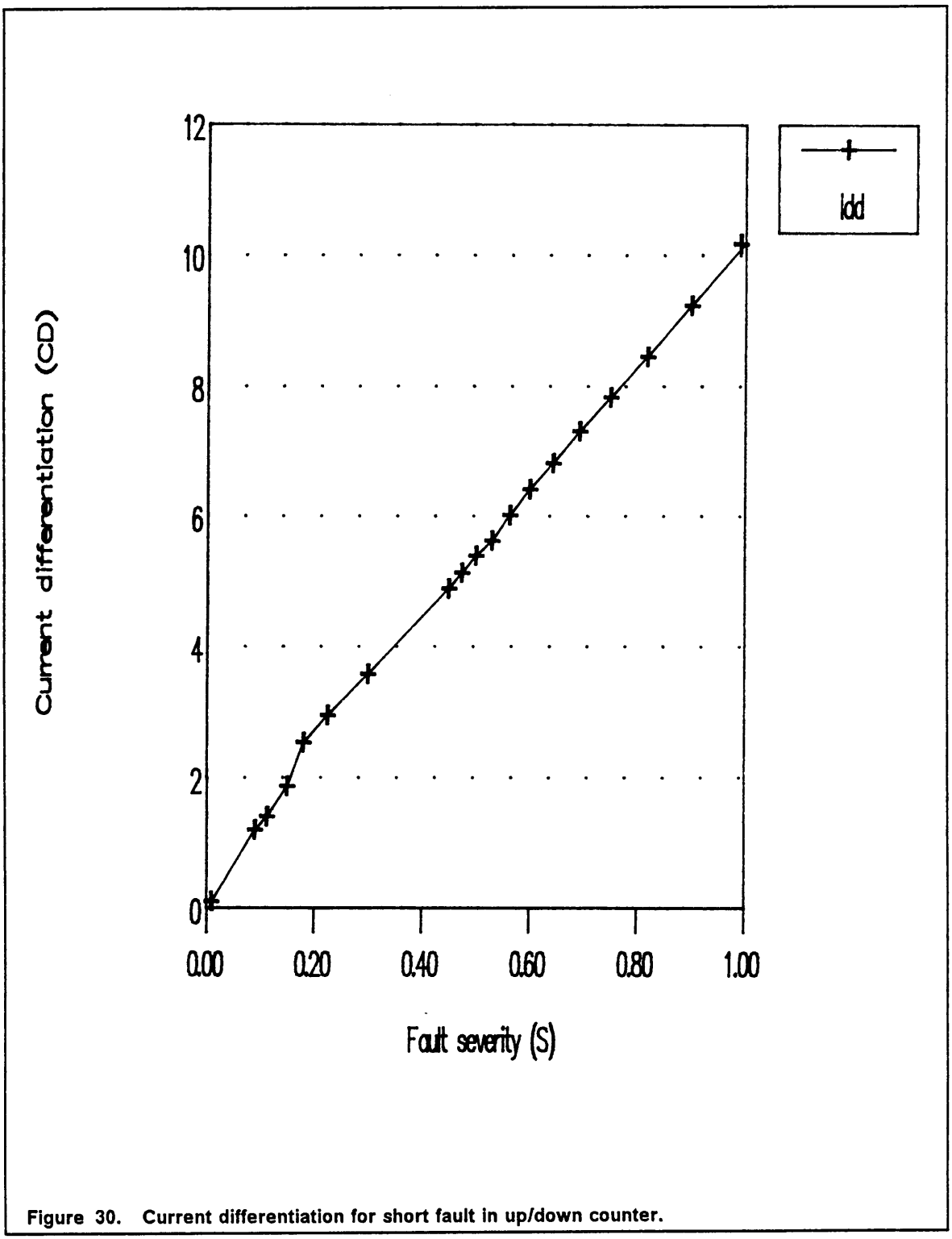

Figure 30. Current differentiation for short fault in up/down counter.

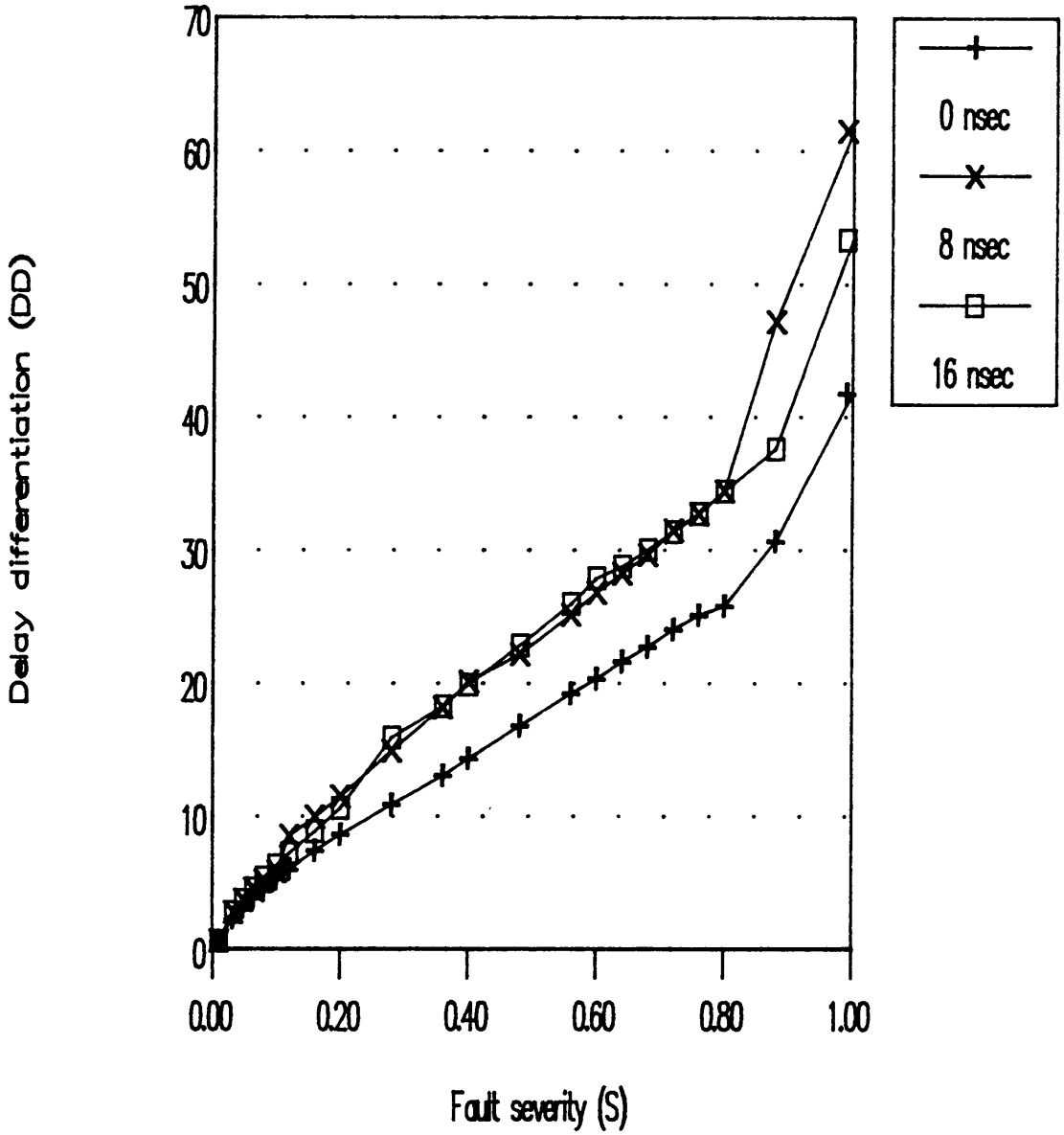

Figure 31. Delay differentiation for open fault: C_{OUT}.

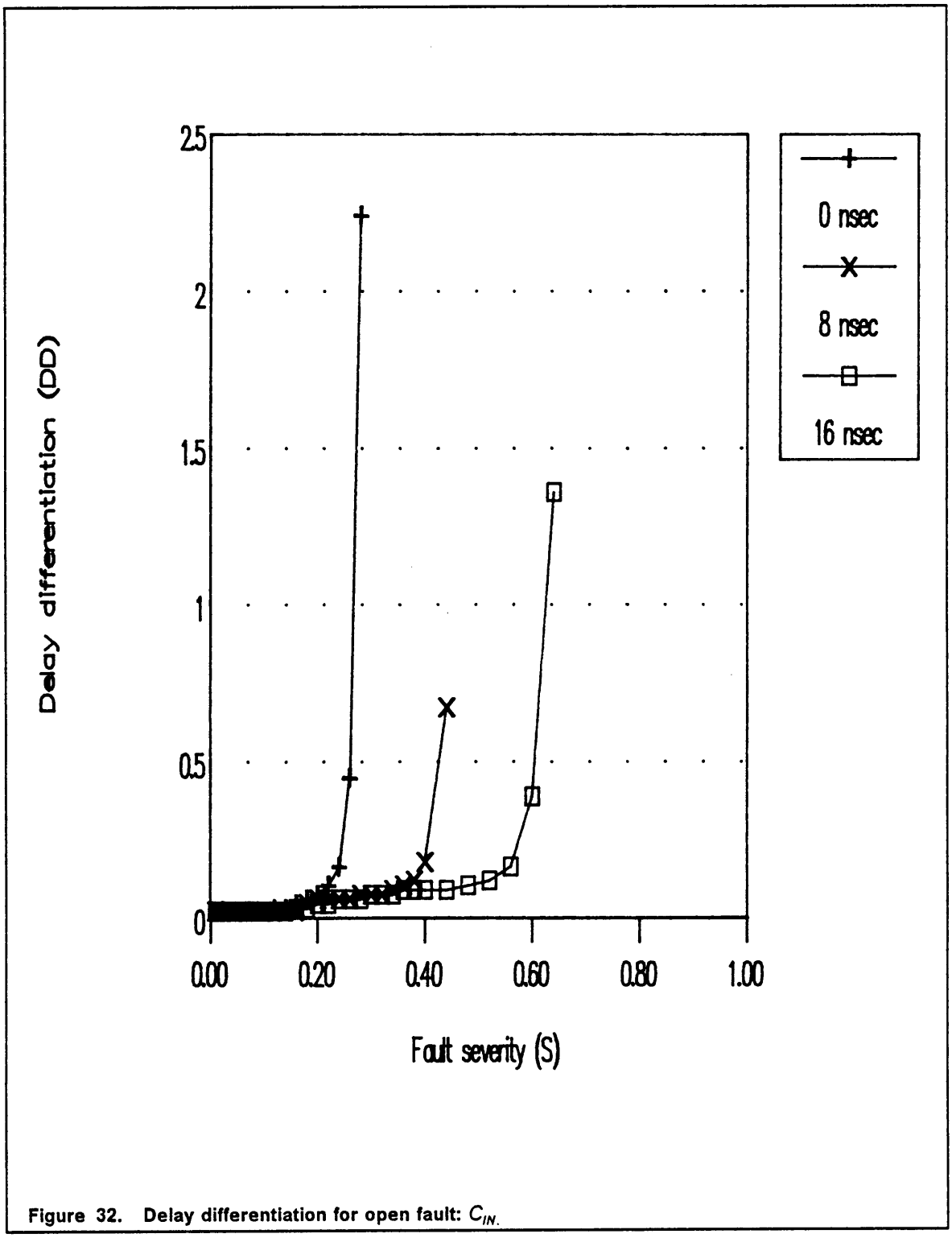

Figure 32. Delay differentiation for open fault: C_{IN}.

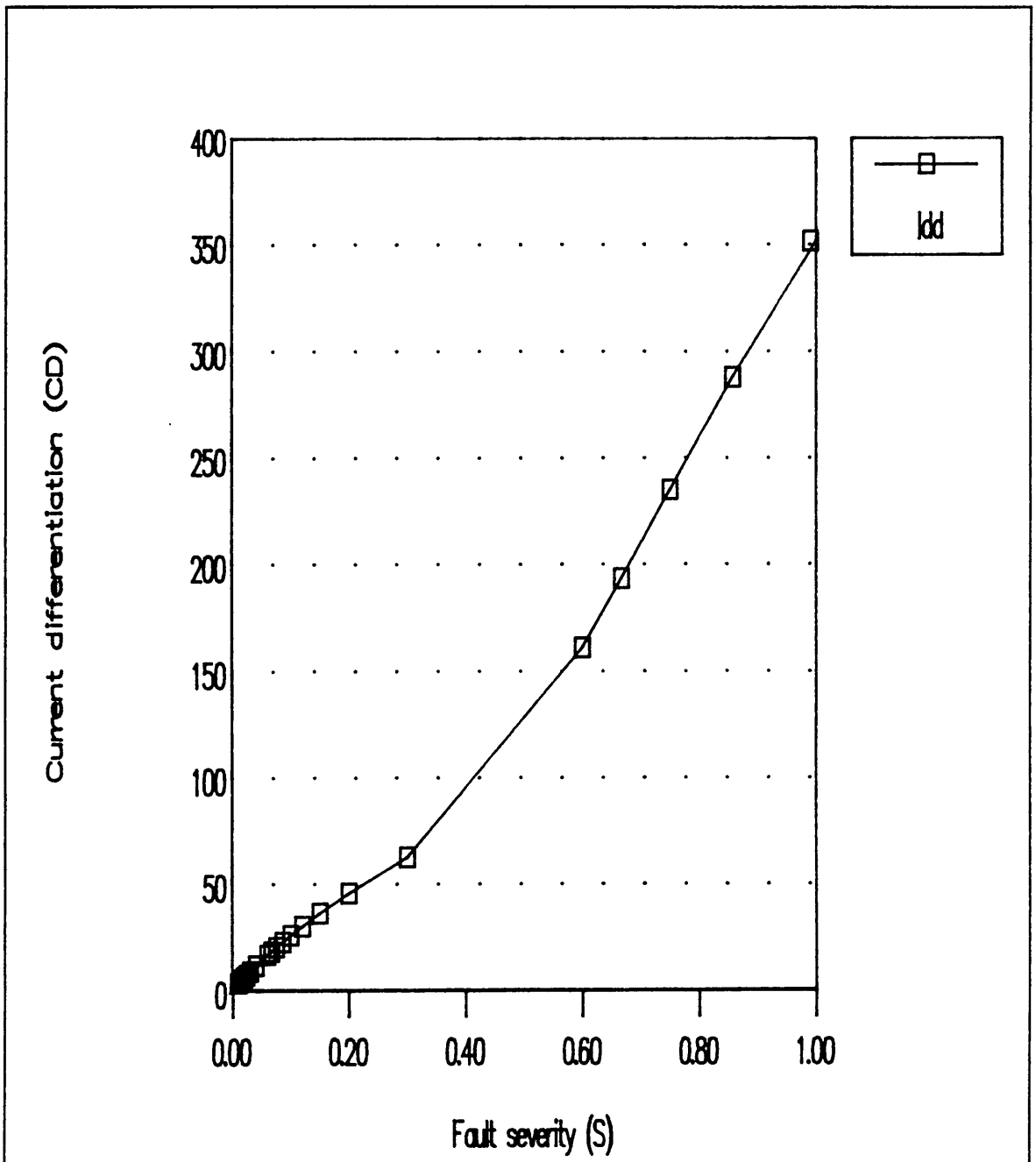

Figure 33. Current differentiation for short fault in bit-serial adder (FCMOS logic).

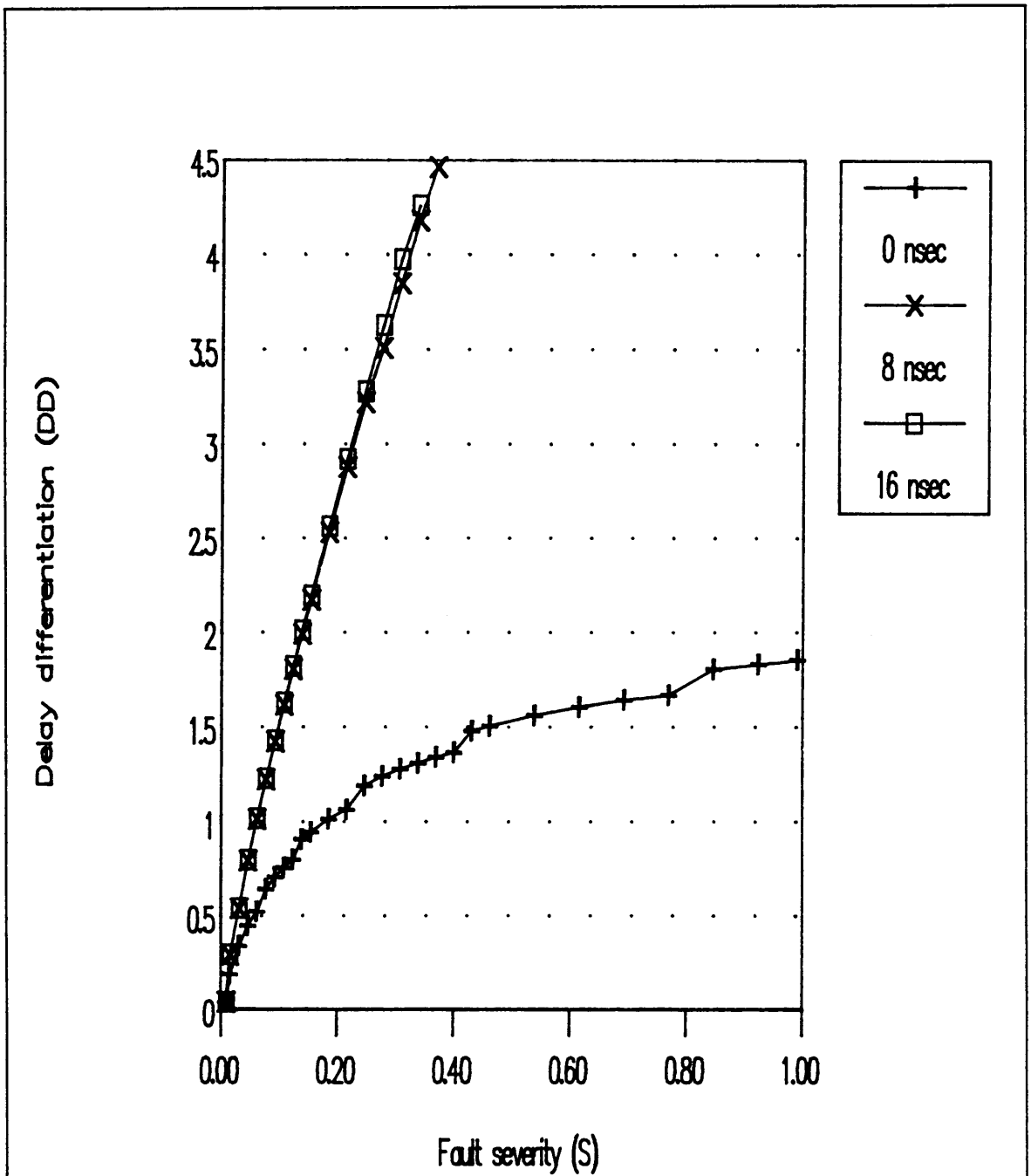

Figure 34. Delay differentiation for open fault: C_{OUT}.

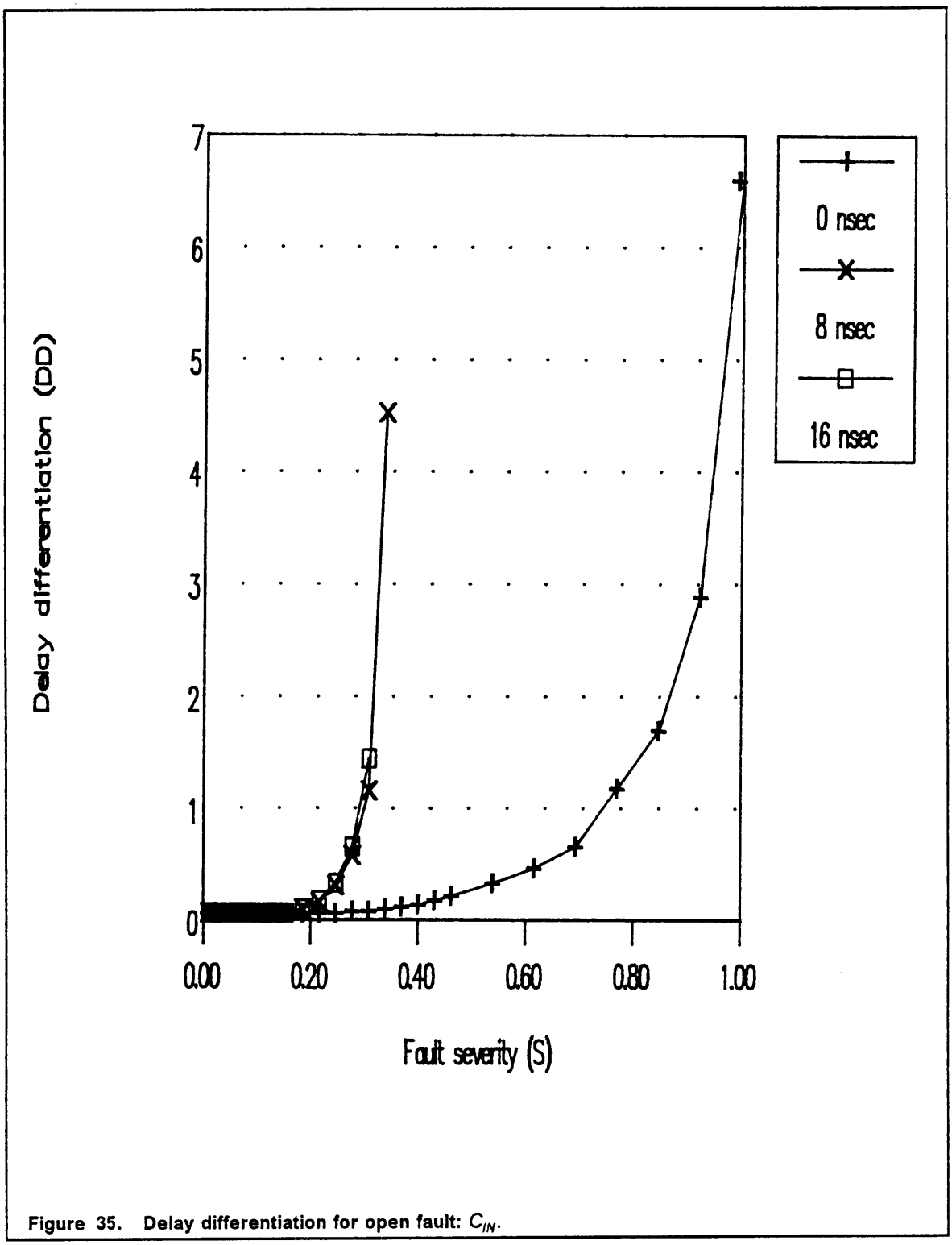

Figure 35. Delay differentiation for open fault: C_{IN}.

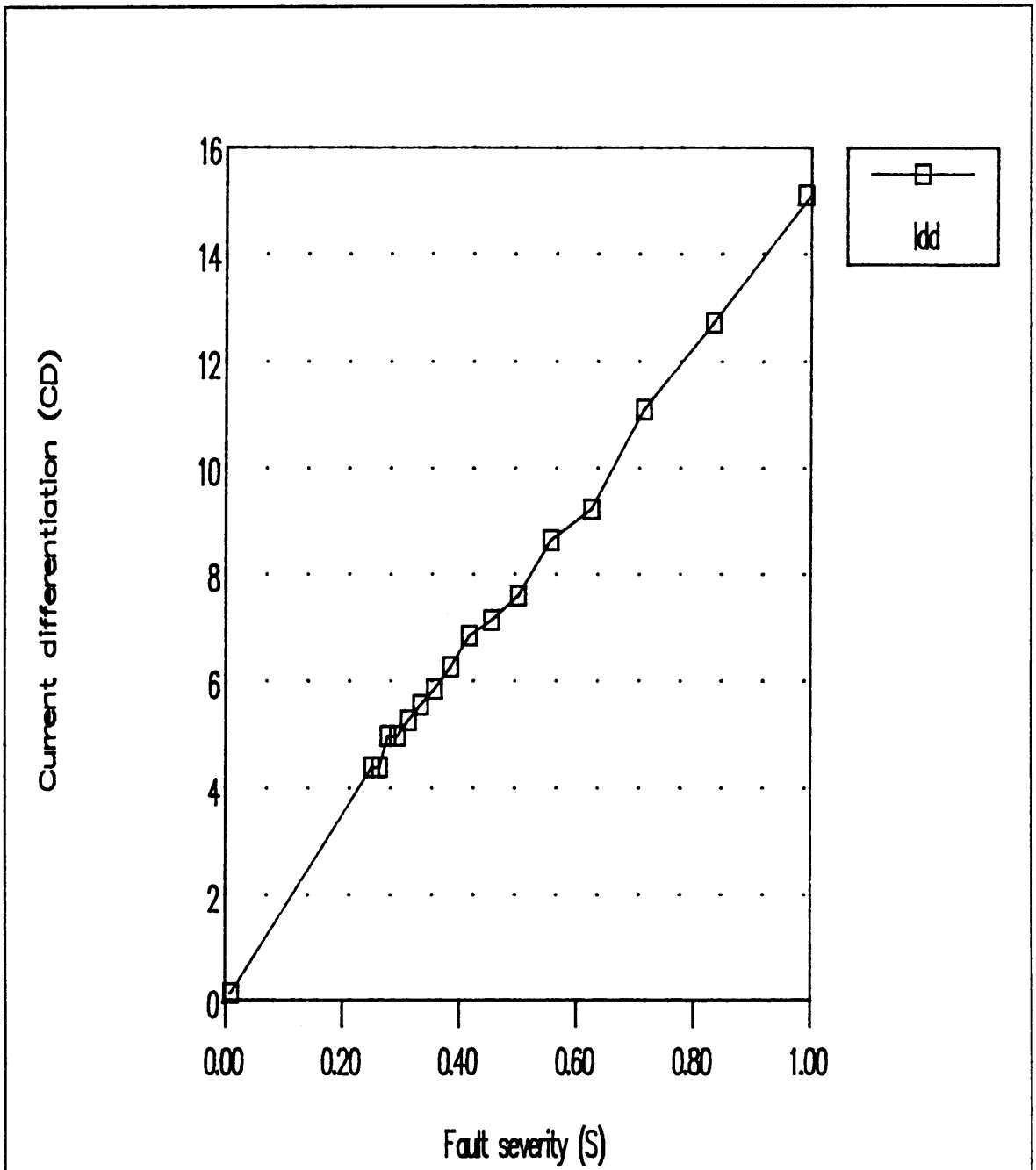

Figure 36. Current Differentiation for short fault in bit-serial adder (domino logic).

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