GENERALIZED AVERAGE-CURRENT-MODE CONTROL OF SINGLE-PHASE AC-DC BOOST CONVERTERS WITH POWER FACTOR CORRECTION

by

Konstantin P. Louganski

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Dr. Jih-Sheng Lai, Chairman
Dr. Yilu Liu
Dr. Kwa-Sur Tam
Dr. Douglas K. Lindner
Dr. Douglas J. Nelson

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Abstract

The dissertation presents a generalized average-current-mode control technique (GACMC), which is an extension of the average-current-mode control (ACMC) for single-phase ac-dc boost converters with power factor correction (PFC). Traditional ACMC is generalized in a sense that it offers improved performance in the form of significant reduction of the current control loop bandwidth requirement for a given line frequency in unidirectional and bidirectional boost PFC converters, and additional functionality in the form of reactive power control capability in bidirectional converters. These features allow using a relatively low switching frequency and slow-switching power devices such as insulated-gate bipolar transistors (IGBTs) in boost PFC converters, including those designed for higher ac line frequencies such as in aircraft power systems (360–800 Hz). In bidirectional boost PFC converters, including multilevel topologies, the GACMC offers a capability to supply a prescribed amount of reactive power (with leading or lagging current) independently of the dc load power, which allows the converter to be used as a static reactive power compensator in the power system.

A closed-loop dynamic model for the current control loop of the boost PFC converter with the ACMC has been developed. The model explains the structure of the converter input admittance, the current phase lead phenomenon, and lays the groundwork for development of the GACMC. The leading phase admittance cancellation (LPAC)

principle has been proposed to completely eliminate the current phase lead phenomenon and, consequently, the zero-crossing distortion in unidirectional converters. The LPAC technique has been adapted for active compensation of the input filter capacitor current in bidirectional boost PFC converters.

The dynamic model of the current control loop for bidirectional boost PFC converters was augmented to include a reactive power controller. The proposed control strategy enables the converter to process reactive power and, thus, be used as a reactive power compensator, independently of the converter operation as an ac-dc converter.

Multiple realizations of the reactive power controller have been identified and examined in a systematic way, along with their merits and limitations, including susceptibility to the ac line noise. Frequency response characteristics of reactive elements emulated by means of these realizations have been described.

Theoretical principles and practical solutions developed in this dissertation have been experimentally verified using unidirectional and bidirectional converter prototypes. Experimental results demonstrated validity of the theory and proposed practical implementations of the GACMC.

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Chapter 1

Introduction

1.1 Motivation

Single-phase ac-dc static power conversion involves shaping of a sinusoidal ac line voltage waveform into a dc voltage waveform with a relatively small ac component. Passive rectification based on traditional diode rectifiers with capacitive and inductive filters presents a simple and inexpensive solution [1]. These circuits, due to their principle of operation, draw nonsinusoidal and rich in harmonics current from the ac line. As an example, a diode bridge rectifier circuit with a capacitive filter draws line current in the form of narrow pulses, which occur at line voltage peaks. As the number of units of electronic equipment powered from the ac line increases every year, the problem of line current harmonics grows in its significance. Current harmonics lead to distortion of the line voltage waveform, increased rms current load, electromagnetic interference, neutral currents in three-phase systems, and adversely affect operation of transformers, electrical machines, reactive power compensators, and power system protection [2]. Significance of this problem has led to development of standards that place limits on current harmonics:

the International Electrotechnical Commission Standard IEC 61000-3-2 [3] and the IEEE/ANSI Standard 519 [4].

Another way to think about distortion of the line current waveform is in terms of the load power factor. Power factor k_p of a nonlinear load is a product of a displacement factor k_θ, which accounts for a phase shift between the voltage and current waveforms, and a distortion factor k_d, which is a measure of deviation of the current shape from sinusoidal [5]:

$$k_p = k_d\, k_\theta\,, \tag{1.1}$$

$$k_d = \frac{I_{1rms}}{I_{rms}}\,, \tag{1.2}$$

$$k_\theta = \cos\theta_1\,, \tag{1.3}$$

where I_{1rms} is the fundamental component of the line current, I_{rms} is the total line current, and θ_1 is the phase shift of the current fundamental relative to the sinusoidal line voltage.

Distortion factor is close to unity even for waveforms with noticeable distortion; therefore, it is not a very convenient measure of distortion for practical use. Distortion factor is uniquely related to another figure of merit: the total harmonic distortion (THD):

$$THD = \sqrt{\frac{{I_{rms}}^2 - {I_{1rms}}^2}{{I_{1rms}}^2}}\,. \tag{1.4}$$

$$k_d = \sqrt{\frac{1}{1+(THD)^2}}\,. \tag{1.5}$$

Although the degree of line current distortion can be characterized in terms of the distortion factor or the THD, harmonic standards impose absolute or relative limits on particular harmonics. As an example, Table 1.1 shows current harmonics limits specified by the IEC 61000-3-2 for Class D equipment, which includes personal computers, personal computer monitors, and television receivers with a specified power less than or equal to 600 W. The IEEE Standard 519 specifies limits on particular harmonics as well as on the THD of the current waveform (Table 1.2). Harmonic limits are given in percentage of the fundamental component of the load current.

Other agencies may find it necessary to impose additional harmonic restrictions for critical applications. The U.S. military was one of the first organizations to adopt a current harmonic regulation with a 3% limit [2]. Boeing and Airbus, the aircraft companies, adopted their own proprietary power quality standards for airborne equipment. These standards specify power quality requirements for a range of ac line frequencies, from 360 Hz to 800 Hz.

Significant reduction of current harmonics in single-phase circuits can only be achieved by using rectifiers based on switchmode power converters. These converters can be designed to emulate a resistive load and, therefore, produce very little distortion of the current [2]. By using pulse-width modulation or other modulation techniques, these converters draw a nearly sinusoidal current from the ac line in phase with the line voltage. As a result, the rectifier operates with very low current harmonic distortion and very high, practically unity power factor. This technique is commonly known as power factor correction (PFC). As a result of this research, the existing PFC technology based

TABLE 1.1 IEC 61000-3-2 HARMONIC LIMITS FOR CLASS D EQUIPMENT [3]

Harmonic order n	**Maximum permissible harmonic current per watt** mA/W	**Maximum permissible harmonic current** A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \leq n \leq 39$	3.85/n	See Table 1*

*Refers to Table 1 in IEC 61000-3-2.

TABLE 1.2 IEEE STANDARD 519 MAXIMUM ODD HARMONIC CURRENT LIMITS FOR GENERAL DISTRIBUTION SYSTEMS, 120 V TO 69 KV [4]

I_{SC} / I_L	**n < 11**	**11 ≤ n ≤ 17**	**17 ≤ n ≤ 23**	**23 ≤ n ≤ 35**	**35 ≤ n**	**THD**
< 20	4.0%	2.0%	1.5%	0.6%	0.3%	5.0%
20–50	7.0%	3.5%	2.5%	1.0%	0.5%	8.0%
50–100	10.0%	4.5%	4.0%	1.5%	0.7%	12.0%
100–1000	12.0%	5.5%	5.0%	2.0%	1.0%	15.0%
> 1000	15.0%	7.0%	6.0%	2.5%	1.4%	20.0%

on the boost converter topology with average-current-mode control was significantly improved. The proposed improvements allowed an extended range of operating conditions and additional functionality.

1.2 Overview of the Present State of Technology

PFC techniques can be broadly classified into passive and active [6]. Passive techniques utilize an input filter consisting of passive components (inductors and capacitors) to reduce line current harmonics caused by the diode rectifier [7]–[9]. However, improvements that can be achieved by this method are relatively limited. According to the above references, the THD could be reduced to less than 50% with a power factor around 0.9. Another drawback of the passive PFC technique is a relatively large size and weight of the filter inductor and capacitor. A passive filter design is difficult to optimize for universal line operation [6]. Although this solution can sometimes meet harmonic standard requirements, much better results can be obtained by using active PFC techniques based on switchmode power converters.

Early research on PFC converters dates back to 1980s [10]–[12]. The most significant contribution to classical PFC techniques in the form they are commercially used today was done by Unitrode Corporation designers in the late 1980s [13]–[15]. They popularized the concept of average-current-mode control (ACMC) for use in PFC converters as well as in other applications [15]. The ACMC was shown to be a better

choice for PFC converters compared with the previously known peak-current-mode control [16]. Unitrode (currently Texas Instruments) is a major developer and manufacturer of control integrated circuits for PFC converters, and its staff continues making contributions to the field [6], [17].

All basic switchmode power converter topologies such as boost, buck, buck-boost, and their variations can be used to realize active PFC techniques [6], [13], [18]. In high-voltage applications, multilevel topologies can be an option. All topologies can be configured for unidirectional as well as bidirectional power flow. At lower power ratings, MOSFETs are the switching power devices of choice because of their low conduction losses and high switching speed. For medium- and high-power applications, IGBTs can be used in PWM-controlled converters with switching frequency of up to 30 kHz. There are many integrated circuits (ICs) on the market that incorporate control functions for PFC converters and facilitate compact and cost-effective designs. Digital signal processors (DSPs) have been successfully used to control PFC converters [19]–[21]. Microcontrollers and DSPs can be used to realize traditional proportional-integral-derivative (PID) control laws as well as non-traditional control principles such as sliding-mode control, fuzzy logic, and neural networks [22]–[28]. One of the drawbacks of using microcontrollers and DSPs is significant effort that goes into software development.

A nonlinear control technique called one-cycle control [29] is among non-traditional control principles proposed for use with PFC converters. This is a constant-frequency, PWM-type of control, in which duty cycle of the power switch is not driven by the error between the regulated output and its reference. Instead, the control operates

such that “in each cycle the average value of a switched variable of the switching converter is exactly equal to or proportional to the control reference in the steady state or in a transient” [29]. In the buck converter example given in this paper, the switched variable is the voltage applied to the output L-C filter of the converter. The controller employs an integrator with reset and a comparator, which is set to the desired reference value for the switched variable. The control ensures that the average value of the switched variable achieves its desired reference value within one switching cycle, hence the name, one-cycle control. However, the control does not guarantee that the output voltage is equal to the average value of the switched variable if the esr of the filter components are taken into account. One-cycle control has been used in a boost PFC converter operating in discontinuous conduction mode [30] for relatively low power level applications. The converter requires no current sensing but still needs the output voltage control loop. The boost PFC converter operating in continuous conduction mode [31] requires line current sensing and output voltage feedback loop. The proposed controller eliminates the need for a multiplier and the current loop compensator in the traditional ACMC scheme at the expense of introducing two integrators with resets as part of the one-cycle controller. Overall, the proposed solution does not seem to be simpler than the ACMC. Since one-cycle control is nonlinear in nature, classical control theory cannot be used to analyze the system for closed-loop stability. Mapping theory [32] was used in [31] for stability analysis. It was reported that stability is guaranteed when the line voltage is lower than half of the output voltage. There is a potential for instability at light

load near the peak of the sine wave. Other applications of one-cycle control to PFC converters have been reported in [33] and [34].

A variation of the one-cycle control principle applied to control of the input current of a PFC converter is known as charge control [35]. PFC converters with discontinuous input current such as flyback [36] and buck [37] achieve higher quality input current waveforms with charge control than with peak-current-mode control because charge control acts upon the average value of the input current, which is required in PFC applications. Charge control has no advantage for use with the boost PFC converter because this type of converter has continuous input current, which is most naturally controlled with average-current-mode control.

The boost topology is by far more popular than others in PFC applications [6], [13]. The boost PFC converter draws continuous current from the line and, therefore, does not require much filtering, which is usually accomplished by an input filter capacitor. Other topologies such as buck, buck-boost, and flyback draw pulsed current and need much better input filter (design of higher-order input filters for PFC converters is described in [38]). Unlike the buck topology, the boost converter easily accommodates the input voltage range from zero to the line peak voltage. At power levels of up to a few hundred watts such as in computer power supplies and consumer electronics, the boost converter usually functions as a preregulator following a diode bridge, which rectifies the line sine wave. The boost preregulator produces at its output a coarsely regulated dc voltage with the magnitude that must be above the maximum line peak voltage for all

operating conditions. A downstream dc-dc converter can be used to step down this voltage according to the load requirements.

The boost converter can operate in continuous conduction mode (CCM), discontinuous conduction mode (DCM), or critical conduction mode (CRM). These names refer to the continuity of the inductor current within the switching cycle. The boost converter operating in DCM and CRM modes is usually easier to control, but it has higher peak-to-peak current ripple, which causes higher rms value of the inductor current, higher magnetic and conduction losses, and higher switching noise, which leads to increased filtering requirements. Therefore, these modes are restricted to relatively low power levels, while the CCM is used at medium and high power levels [6].

In a PFC converter, the control system is designed to shape the input current into a sinusoidal (or rectified sinusoidal) waveform to ensure low harmonic distortion of the line current and to adjust the magnitude of this current in order to maintain the output dc voltage at a specified level. The line voltage waveform is used as a reference for the converter input current. It is possible to use hysteretic control to force the current to follow the reference [39]; this type of control is attractive for lower power level converters operated in DCM and CRM [6]. The drawbacks of this type of control are variable switching frequency, which may lead to high switching losses and a switching noise spectrum that is more difficult to filter out. The ACMC provides better performance at medium and high power levels but requires more complicated control structure. It uses PWM control of the power switch whose duty cycle is determined by the current loop controller, which attempts to minimize the difference between the actual current and the

current reference derived from the line voltage waveform. The voltage loop controller adjusts the magnitude of the current loop reference signal in order to regulate the output dc voltage.

According to [6], current and voltage loop controllers are implemented as PI-type compensators, with the current loop bandwidth of approximately 10 kHz for the utility line frequency (50 or 60 Hz). This bandwidth requirement translates into the converter switching frequency of at least 50 kHz, with typical values approaching 100 kHz [13], [40]. Chapter 2 shows how to relax the bandwidth requirement by using the leading-phase admittance cancellation technique (LPAC). The LPAC method can be extended to cancel reactive current of the input filter capacitor as explained in Chapter 3. Based on converter the modeling and analysis results, a reactive power control principle is introduced in Chapter 4. Chapter 5 examines a number of reactive power controller realizations and their properties.

1.3 Dissertation Outline and Major Results

The dissertation presents development of the generalized average-current-mode control technique (GACMC) for single-phase ac-dc boost converters with power factor correction. The GACMC is an extension of the average-current-mode control (ACMC) technique. The traditional ACMC is generalized in a sense that the new control offers improved performance and additional functionality. The GACMC improves converter

performance compared with the traditional ACMC by allowing a significantly reduced current control loop bandwidth for a given line frequency in unidirectional and bidirectional boost PFC converters, which enables the converters to operate in an extended range of line frequencies for a given converter design. The GACMC provides additional functionality compared with the traditional ACMC in the form of reactive power control capability in bidirectional converters. These features of the GACMC allow using a relatively low switching frequency and slow-switching power devices such as insulated-gate bipolar transistors (IGBTs) in boost PFC converters, including those designed for higher ac line frequencies such as in certain aircraft power systems (360–800 Hz). In bidirectional boost PFC converters, including multilevel topologies, the GACMC offers a capability to supply a prescribed amount of reactive power (with leading or lagging current) independently of the dc load power, which allows the converter to be used as a static reactive power compensator in the power system.

The dissertation includes four relatively self-contained research topics based on the proposed modeling approach and dynamic analysis of the boost PFC converter with ACMC. Most of the theoretical development and experimental results included in this dissertation have been previously reported by the author in publications [41]–[44]. The subject of Chapter 2 is modeling, analysis, and improvement of the control structure of the unidirectional boost PFC converter. This chapter lays the groundwork upon which the rest of the dissertation research is founded. A closed-loop dynamic model of the boost PFC converter is newly derived from first principles. The reasons for the current phase lead and possible ways to eliminate it become readily apparent from the model. The

leading-phase admittance cancellation (LPAC) method is proposed, which allows operation without the current phase lead and the zero-crossing distortion at higher line frequencies (up to 800 Hz and above) with a standard converter designed for 60 Hz using the switching frequency less than 50 kHz. This method allows simple analog implementation and can be added to existing converters without their redesign. The method is load-invariant, line voltage-invariant, and is not sensitive to the boost inductance variation. The chapter suggests simple practical ways of adding the LPAC to the boost PFC converter designs based on commercial control ICs. The material in Chapter 2 has been reported by the author in [41].

Based on the modeling and analysis results developed for the unidirectional boost PFC converter, Chapter 3 examines the effect of the input filter capacitor on the total line current at higher line frequencies and the ways to mitigate this effect. It was found that the LPAC technique, which is used to cancel the inductor current phase lead in PFC boost converters designed for utility line frequency but operating at higher line frequencies, can be adapted (with some limitations imposed by topologies) to cancel the reactive current drawn by the input capacitor as well. Dynamic modeling of the converter has been used to determine conditions for reactive current cancellation and control circuit parameters required for that. Computer-aided analysis and experiments were used to verify the proposed method. It is shown how to achieve complete, load-invariant, line-frequency-invariant compensation of the input capacitor current in a bidirectional PFC boost converter (represented in this research by the full-bridge topology) using an adaptation of the LPAC technique. In a unidirectional PFC boost converter (represented by the

traditional diode-bridge circuit), the presence of uncontrolled rectifiers (diodes) in the line current path imposes limitations on the size of the filtering capacitor whose current can be compensated. However, a trade-off choice of filtering capacitors on the ac side and dc side of the bridge is possible, which allows unity-power-factor operation with substantial reduction but not complete elimination of the switching ripple in the line current. The results presented in Chapter 3 have been previously reported by the author in [42].

The modeling approach and the LPAC principle developed in Chapter 2 have been further employed in Chapter 4 to develop a bidirectional, multilevel ac-dc active front end converter with ACMC. A 20-kW single-phase multilevel active-front-end converter has been developed as an intelligent transformerless alternative to traditional line-frequency rectifiers to boost a medium-voltage ac source (2400 V rms) to a 4-kV dc distribution bus for subsequent power conversion. The converter utilizes developed in this dissertation generalized average-current-mode control scheme (GACMC), which features unity-power-factor operation and reactive power control capability. The GACMC incorporates the LPAC control technique developed in Chapter 2 for PFC boost converters. The LPAC allows a relatively low PWM carrier frequency of 10 kHz, appropriate for this power level, without negative consequences of the leading phase shift of the line current as observed in PFC boost converters with a low switching frequency to line frequency ratio. The low switching frequency reduces switching losses, increases converter efficiency, and allows utilization of insulated-gate bipolar transistors (IGBTs), which can only be used at a relatively low switching frequency, as switching power

devices in this application. An additional feature of the GACMC is the capability to supply a prescribed amount of reactive power (with leading or lagging current) independently of the dc load power, which allows the converter to be used as a static reactive power compensator in the power system. Reactive power source capability is a novel concept for bidirectional PFC converters, commonly known as active-front-end (AFE) converters, which allows them to some extent to cross the boundary with active filters for power quality improvement [45]. In this capacity, an AFE converter not only draws real power from the line without reducing power factor or creating current harmonics, but also is capable of correcting power factor deteriorated by the presence of reactive loads in the power system. This type of converter can help eliminate a static reactive power compensator or an active filter from a power system that the converter is part of depending on the nature of the system. Dynamic modeling of the current control loop has been used to determine possibility of reactive power control, and a simple practical implementation of a reactive power controller has been proposed. A scaled-down converter prototype was used to verify the concept. Experiments revealed good agreement with theory and simulation results. The material in Chapter 4 has been reported by the author in [43].

Reactive power controller for a single-phase active-front-end converter with ACMC introduced in Chapter 4 can be realized in multiple ways, each having their own advantages and drawbacks. In Chapter 5, we will take a close look at the ways to add a reactive power controller to the current control loop such that the converter can generate a specified amount of reactive power along with its intended use as an active-front-end.

The reactive power controller introduces a phase shift, leading or lagging, into the line current, thus emulating a capacitor or an inductor connected to the ac line. Therefore, the converter can be used as a reactive power compensator, at the same time supplying dc power to the load. A particular form of reactive power control for a multilevel AFE converter has been introduced in Chapter 4. This chapter examines other possible reactive power control realizations in a systematic way, along with their merits and limitations, including susceptibility to the ac line noise. A closed-loop dynamic model of the converter was used to derive a variety of possible forms of the reactive power controller and analyze their potential for use in different applications. Experimental data were obtained to verify the reactive power control concept and showed good agreement with theoretical predictions and simulation results. The material in Chapter 5 has been published by the author in [44].

Contributions of the dissertation can be summarized as follows:

- A closed-loop dynamic model for the current control loop of the boost PFC converter with ACMC has been developed. The model explains the structure of the converter input admittance, the current phase lead phenomenon, and lays the groundwork for development of generalized ACMC.
- The Leading Phase Admittance Cancellation principle has been proposed to completely eliminate the current phase lead phenomenon and, consequently, the zero-crossing distortion in unidirectional converters.
- The LPAC technique has been adapted for active compensation of the input filter capacitor current in bidirectional boost PFC converters.

- A reactive power control principle has been developed for bidirectional converters with ACMC. The proposed control strategy enables the converter to generate reactive power and, thus, be used as a reactive power compensator, independently of the converter function as an ac-dc converter.
- Multiple realizations of the reactive power controller have been identified and examined in a systematic way, along with their merits and limitations, including their susceptibility to the ac line noise. Frequency response characteristics of reactive elements emulated by means of these realizations have been described.

Chapter 2

Current Phase Lead Compensation in Single-Phase PFC Boost Converters with a Reduced Switching Frequency to Line Frequency Ratio

2.1 Introduction

The boost topology is a popular choice for a single-phase ac-dc preregulator with high power factor and low harmonic distortions of the ac line current. This converter employs a two-loop control system, with an inner "current" loop shaping the sinusoidal current drawn from the line, and the outer "voltage" loop maintaining the dc output voltage at the required level [6]. The boost converter operating in continuous current conduction mode (CCM) with average current mode control (ACMC) is a preferred choice for PFC converters with higher power rating. This chapter is focused on performance improvement of the current loop controller of the converter operating in CCM with ACMC.

The bandwidth of the current loop controller should be high enough to pass all significant harmonics of the rectified sine wave. For the utility line frequency (50-60 Hz), it is recommended to be around 10 kHz [6]. Because the control loop bandwidth may not

be larger than $^1/_5$ of the switching frequency, this requirement further translates into a switching frequency in excess of 50 kHz, with typical values approaching 100 kHz [13], [40]. In other words, with traditional current loop design, the switching frequency to line frequency ratio should be at least 1000, or the loop crossover frequency to line frequency ratio should be at least 150. If this ratio is much smaller, a zero-crossing distortion of the line current waveform appears due to the leading phase of the current relative to the line voltage. This leading phase is a result of control action of the current loop compensation scheme [46], [47]. A PFC converter with a zero-crossing distortion of the line current may not be able to meet harmonic distortion requirements.

At the utility line frequencies (50-60 Hz) and power level less than 1 kW, these requirements for frequency ratios usually do not present a problem. In some other applications, these ratios may be impossible or impractical to realize. For example, aircraft generator and its associated power system utilize much higher frequencies (360–800 Hz [48], [49]). Increasing the control loop bandwidth in order to avoid the zero-crossing distortion effect would require the switching frequency to be extended to hundreds of kilohertz, which would reduce converter efficiency and may be impractical. Another example is medium- and high-power (above 10 kW) single-phase PFC applications operating at the utility line frequency. These converters would greatly benefit from lower switching frequency (30 kHz or less). As a better alternative to using inefficient “brute-force” designs to comply with the above stated bandwidth requirement, it is proposed to make modifications to the standard current loop controller in order to eliminate the cause of the leading-phase distortion of the line current.

Among previously proposed methods to alleviate this problem are modification of the current reference signal [46], [47], [50], which is load-dependent and best implemented with DSP control, and various types of voltage feedforward schemes [51]–[54]. Some of these schemes use signal-by-signal division in the control law formula and are complicated for analog implementation [52]–[54]. A simple digital control solution is presented in [21]. An analog circuit based on two op-amps is suggested to implement a feedforward control law proposed in [51]. This law was shown to have some sensitivity to the boost inductance variation.

In this chapter, a closed-loop dynamic model of the boost PFC converter is newly derived from first principles. The reasons for the current phase lead and possible ways to eliminate it become readily apparent from the model. The leading-phase admittance cancellation (LPAC) method allows operation without the current phase lead and the zero-crossing distortion at 360-800 Hz with a standard converter designed for 60 Hz with the switching frequency less than 50 kHz. This method allows simple analog implementation and can be added to existing converters without their redesign. The method is load-invariant, line voltage-invariant, and is not sensitive to the boost inductance variation.

In order to appreciate possible benefits of elimination of the current phase lead and zero-crossing distortion, consider the closed-loop line-voltage-to-current transfer function of the boost converter approximated by a first-order low-pass filter with a given cutoff frequency (equal to the open-loop crossover frequency). Table 2.1 shows harmonic characteristics of the line current at 60 Hz line frequency. The harmonics were calculated

TABLE 2.1 HARMONIC DISTORTIONS VS. CURRENT LOOP BANDWIDTH

Crossover frequency	**300 Hz**	**600 Hz**	**1200 Hz**	**6 kHz**
f_{cr} / f_g	5	**10**	20	100
THD	8.85%	**3.52%**	1.37%	0.17%
phase shift	8.4º	**4.9º**	2.7º	0.6º
displacement factor	0.989	**0.996**	0.999	1.0
distortion factor	0.996	**0.999**	1.0	1.0
power factor	0.985	**0.996**	0.999	1.0
3rd harmonic	4.41%	**1.29%**	0.35%	0.02%
5th harmonic	3.64%	**1.20%**	0.35%	0.02%
7th harmonic	2.99%	**1.10%**	0.34%	0.02%
9th harmonic	2.50%	**1.00%**	0.33%	0.02%
11th harmonic	2.13%	**0.91%**	0.31%	0.02%
13th harmonic	1.85%	**0.82%**	0.30%	0.02%

by passing rectified line voltage waveform through the low-pass filter to obtain a rectified current waveform, then using it to reconstruct the ac current waveform. If the maximum odd harmonic limit is 4% and the THD limit is 5% (IEEE Standard 519), then current loop bandwidth of 600 Hz should provide a current waveform with acceptable quality. Consequently, the switching frequency does not have to be higher than 6 kHz. This control design corresponds to the ratio of the crossover frequency to the line frequency of only 10, and the switching frequency to the line frequency ratio of only 100. Although the closed-loop transfer function of the converter is not exactly a first-order low-pass filter, this example gives us an estimate of possible improvement.

2.2 System Modeling

Traditional design of a PFC boost converter utilizes a two-loop control structure (Fig. 2.1), with an outer voltage-regulating control loop providing reference to an inner current-shaping loop [6]. In practice, the dc link capacitance C is large enough such that it could be treated as a voltage source. Under this assumption, dc voltage V_o and the voltage loop compensator output V_c are constant values. Then, the dynamic model of the converter is described by the block diagram in Fig. 2.2. The power stage line-to-current and control-to-current transfer functions are

$$G_{iv}(s) = \frac{1}{r + s\,L} \quad \text{and} \quad G_{id}(s) = \frac{V_o}{r + s\,L}, \tag{2.1}$$

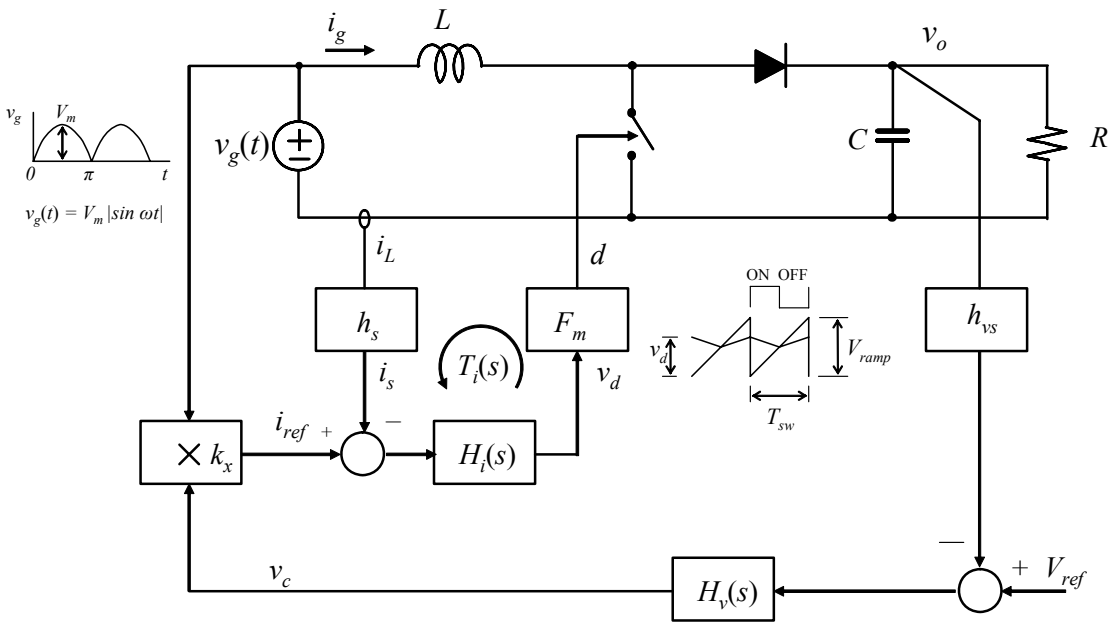


Figure 2.1 PFC boost converter control diagram.

(H_i – current loop compensator, H_v – voltage loop compensator, F_m – modulator gain, k_x – multiplier gain, h_s – current sensor gain, h_{vs} – voltage sensor gain).

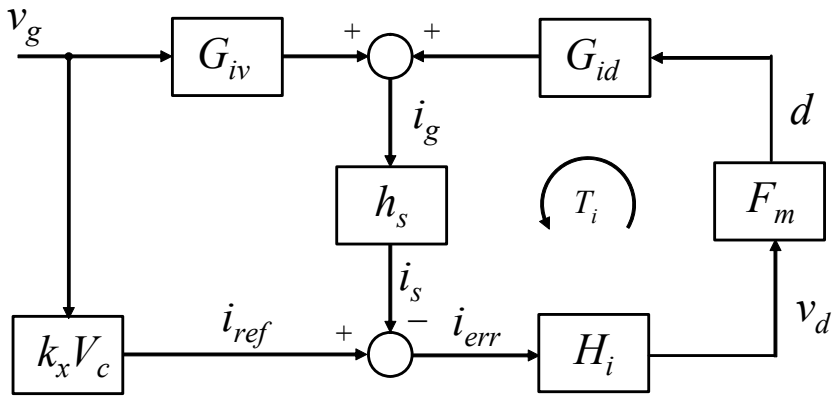


Figure 2.2 PFC boost converter current loop control diagram in terms of transfer functions.

(G_{iv} and G_{id} – power stage transfer functions, $k_x V_c$ – current reference gain).

where r is an equivalent resistance of the current path. This resistance does not noticeably affect closed-loop transfer functions because the current loop has very high low-frequency gain due to the integrator in $H_i(s)$ regardless of r. The compensator is a PI-type controller with the zero placed at or near the loop crossover frequency [6]:

$$H_i(s) = \frac{\omega_i\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)}. \tag{2.2}$$

The line voltage v_g is scaled down by the gain $k_x V_c$ to produce current reference i_{ref} for the control loop.

From Fig. 2.2, it is seen by inspection that current i_g is a sum of two terms:

$$i_g(s) = \frac{G_{iv}}{1+T_i} v_g(s) + \frac{G_{id}\, F_m\, H_i}{1+T_i} k_x V_c\, v_g(s). \tag{2.3}$$

Therefore, the closed-loop input admittance transfer function (which is similar to the generic form reported in [55]) is

$$Y(s) = \frac{i_g(s)}{v_g(s)} = \frac{G_{iv}}{1+T_i} + \frac{G_{id}\, F_m\, H_i}{1+T_i} k_x V_c, \tag{2.4}$$

or

$$Y(s) = G_{ivcl} + T_{icl}\, k_x V_c, \tag{2.5}$$

where

$$T_i = G_{id}\, F_m\, H_i\, h_s \tag{2.6}$$

is the loop gain transfer function, and

$$T_{icl} = \frac{G_{id}\, F_m\, H_i}{1 + T_i} \tag{2.7}$$

is the closed-loop control-to-current transfer function.

We can think of admittance $Y(s)$ as consisting of two components, or two branches $Y_1(s)$ and $Y_2(s)$, each drawing its own current from the ac line (Fig. 2.3). Below the crossover frequency, neglecting r,

$$Y_1(s) = G_{ivcl} = \frac{s}{V_o\, F_m\, h_s\, \omega_i \left(1 + \dfrac{s}{\omega_z}\right)} \tag{2.8}$$

and

$$Y_2(s) = T_{icl}\, k_x V_c = \frac{k_x V_c}{h_s} = Y_{CL0} = \frac{I_g}{V_g} = \frac{P_g}{V_g{}^2}\,. \tag{2.9}$$

Component $Y_2(s)$ is the closed-loop current-reference-to-current transfer function (current reference term), which provides desired input admittance magnitude with zero phase below crossover frequency of the loop gain T_i. This branch of the input admittance draws a current in phase with the line voltage, with the magnitude determined by V_c, which corresponds to the load power. Component $Y_1(s)$ is the closed-loop voltage-to-current transfer function (voltage term, or leading-phase admittance term), which has a 90º leading phase below the crossover frequency. This branch draws a leading-phase current, which is independent of the converter load and increases with the line frequency for a given current loop bandwidth. The magnitude of this current is low at 60 Hz but

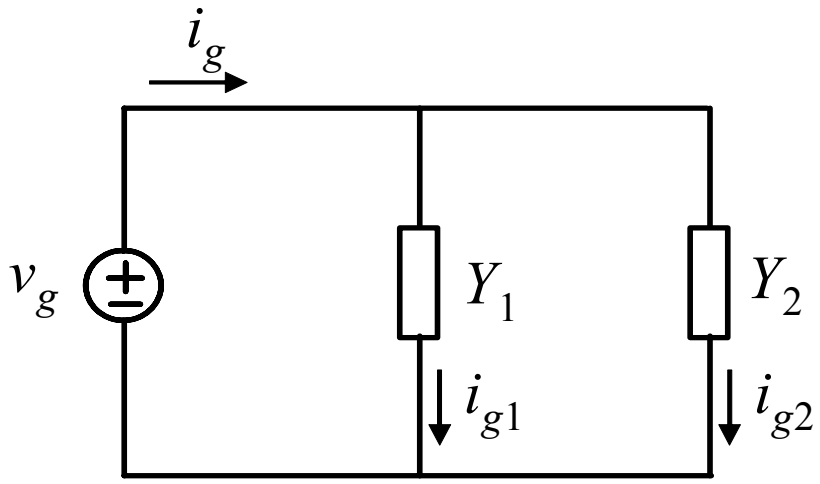


Figure 2.3 Closed-loop input admittance represented by two branches.

may become large enough in the frequency range of 360–800 Hz such that the phase of the total input admittance is no longer zero (Fig. 2.4), which is in agreement with results obtained in [50]. This is the reason why the current phase lead effect may be observed at these frequencies, which causes the zero-crossing distortion of the line current and increased harmonic content [46], [47], [50].

2.3 Current Phase Lead Compensation

2.3.1 Current Reference Correction

From the discussion above, it is clear that we need to compensate the effect of admittance component $Y_1(s)$ in order to eliminate the current phase lead and the resulting zero-crossing distortion. The current reference correction (CRC) method compensates for the effect of $Y_1(s)$ indirectly by using a corrective transfer function $K(s)$ in the current reference path (Fig. 2.5) so that

$$Y(s) = G_{ivcl} + T_{icl}\, k_x\, V_c\, K(s)\,. \tag{2.10}$$

$K(s)$ is determined from the condition $Y(s) = Y_{CL0}$ below the crossover frequency. From (2.8) and (2.9),

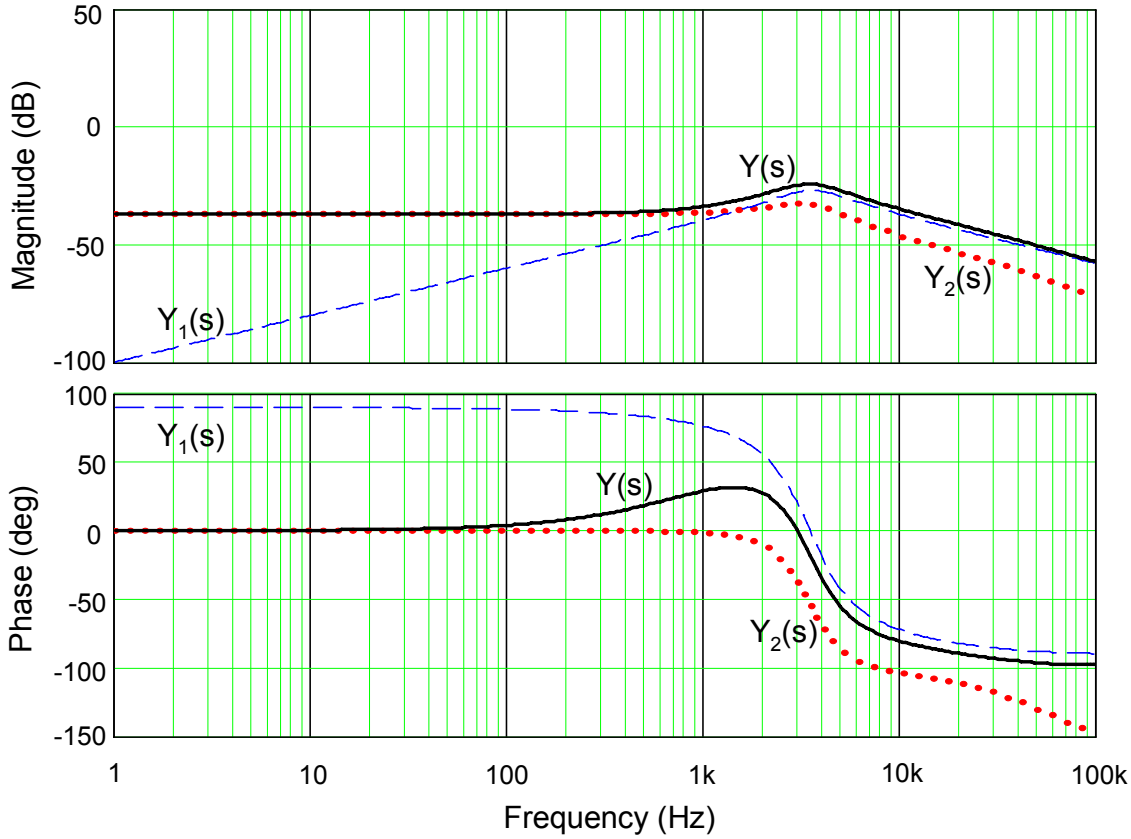


Figure 2.4 Closed-loop input admittance and its components.

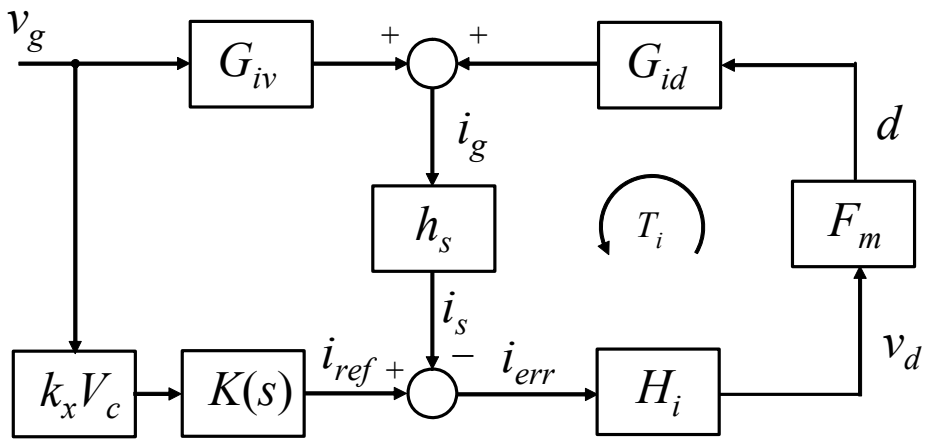


Figure 2.5 Current phase lead compensation using current reference correction.

$$Y(s) = \frac{s}{V_o F_m h_s \omega_i \left(1 + \frac{s}{\omega_z}\right)} + \frac{k_x V_c}{h_s} K(s) = Y_{CL0}\,, \tag{2.11}$$

from which

$$K(s) = \frac{1 + \frac{s}{\omega_{zk}}}{1 + \frac{s}{\omega_z}}, \tag{2.12}$$

where

$$\omega_{zk} = \left(\frac{1}{\omega_z} - \frac{1}{k_x V_c V_o F_m \omega_i}\right)^{-1}. \tag{2.13}$$

In Fig. 2.3, this is equivalent to creating a phase lag in the current drawn by $Y_2(s)$ such that it compensates the leading-phase current drawn by $Y_1(s)$. The results in Fig. 2.6 show that the frequency range of undistorted current operation is drastically extended for more than a decade. The expression for $K(s)$ is load-dependent (ω_{zk} is a load-dependent zero); therefore, $K(s)$ is best implemented using digital control. Adding a corrective transfer function into the current reference path was previously proposed in [46], which also suggested a load-invariant form of $K(s)$:

$$K(s) = \frac{1}{1 + s/\omega_z}\,. \tag{2.14}$$

However, simply neglecting ω_{zk} yields only a marginal improvement over uncompensated $Y(s)$ for given load conditions as shown in Fig. 2.6 (dotted line). Location

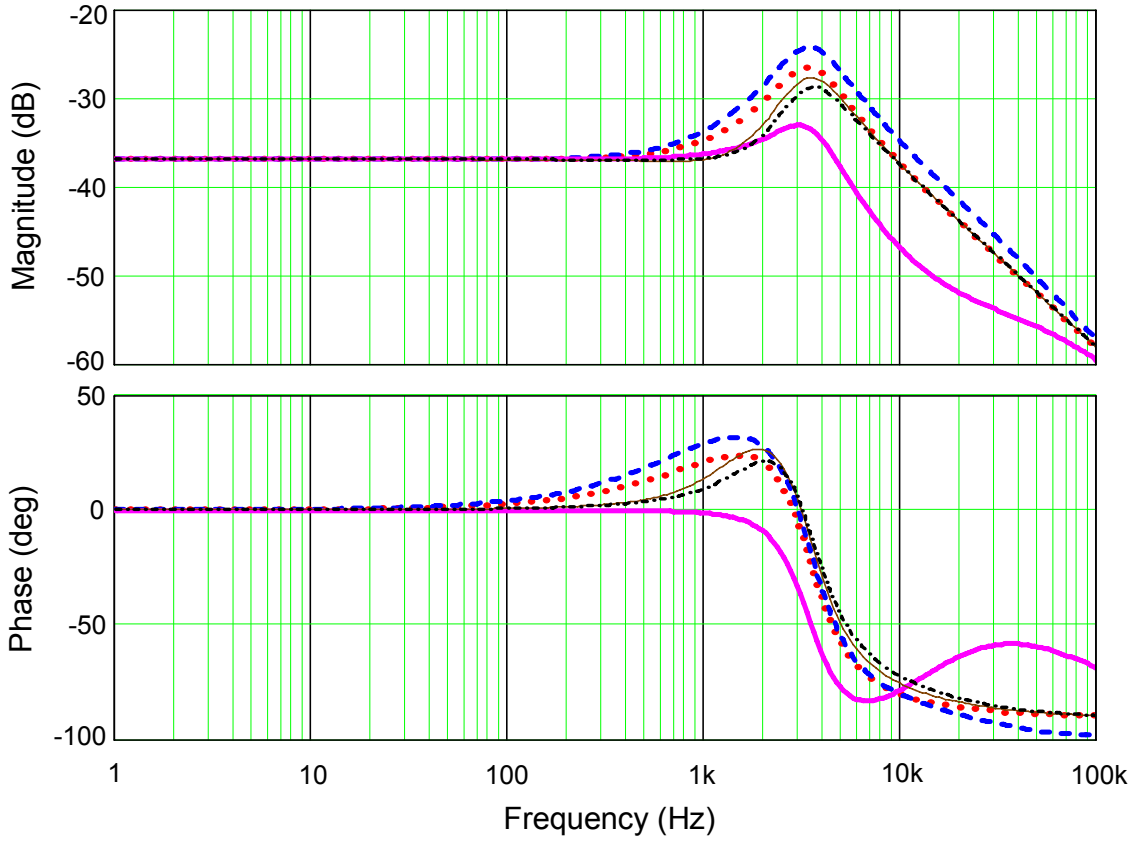


Figure 2.6 Closed-loop input admittance with current reference correction.

Dash—uncorrected, solid thick—exact formula (2.12),
dot—simple approximation (2.14), solid thin—better approximation (2.15),
dash-dot—double-pole approximation (2.16).

of ω_{zk} depends on the load and may be in the right- or left-half-plane, and the zero's effect may be significant. If an approximation in the form of (2.14) must be used, it is better to adjust location of the pole for predominant load conditions to yield the maximum benefit. Even better results can be achieved by adding a second pole or a zero. As shown in Fig. 2.6, better compensation is achieved using

$$K(s) = \frac{1}{1 + \dfrac{s}{0.4\,\omega_z}} \quad \text{(solid thin line)} \tag{2.15}$$

and

$$K(s) = \frac{1}{\left(1 + \dfrac{s}{0.8\,\omega_z}\right)^2} \quad \text{(dash-dot line).} \tag{2.16}$$

However, the best approach to eliminate the current phase lead and the resulting zero-crossing distortion is the load-invariant leading-phase admittance cancellation method described next.

2.3.2 Leading-Phase Admittance Cancellation

The two-component structure of the input admittance (2.4) suggests a natural way to eliminate phase lead in $Y(s)$ by adding a third component that cancels the effect of the first one. The leading-phase admittance cancellation (LPAC) method uses an additional term $Y_3(s)$ in the admittance equation to cancel the leading-phase term $Y_1(s)$. Then, the current reference term is left as the only one that determines the magnitude and phase of the line current. A new input from v_g with a transfer function $H_c(s)$ is introduced at the

summing junction in order to cancel the undesired voltage term in (2.4) as shown in Fig. 2.7 (solid line). This approach has an advantage of using the existing error amplifier input for LPAC implementation. Then,

$$Y(s) = G_{ivcl}(s) + T_{icl}(s)\, k_x V_c + T_{icl}(s)\, H_c(s). \tag{2.17}$$

$H_c(s)$ is determined from the condition $Y(s) = Y_{CL0}$ below the crossover frequency. Using (2.8) and (2.9),

$$H_c(s) = -\frac{1}{V_o\, F_m\, H_i(s)} = -\frac{s}{V_o\, F_m\, \omega_i \left(1 + \dfrac{s}{\omega_z}\right)}. \tag{2.18}$$

As an alternative, the new input can be introduced into the loop after $H_i(s)$ as shown in Fig. 2.7 (dash line):

$$Y(s) = G_{ivcl}(s) + T_{icl}(s)\, k_x V_c + \frac{G_{id}(s)\, F_m}{1 + T_i(s)} H_{c1}(s), \tag{2.19}$$

from which

$$H_{c1}(s) = -\frac{1}{V_o\, F_m}, \tag{2.20}$$

approximated as a static gain below the crossover frequency.

As shown in Fig. 2.8, addition of $H_c(s)$ or $H_{c1}(s)$ is equivalent to adding a new branch $Y_3(s)$, which draws a current opposite to the current of $Y_1(s)$ and, thus, cancels its effect at frequencies within the current loop bandwidth. The results in Fig. 2.9 demonstrate that the frequency range of undistorted current operation is drastically

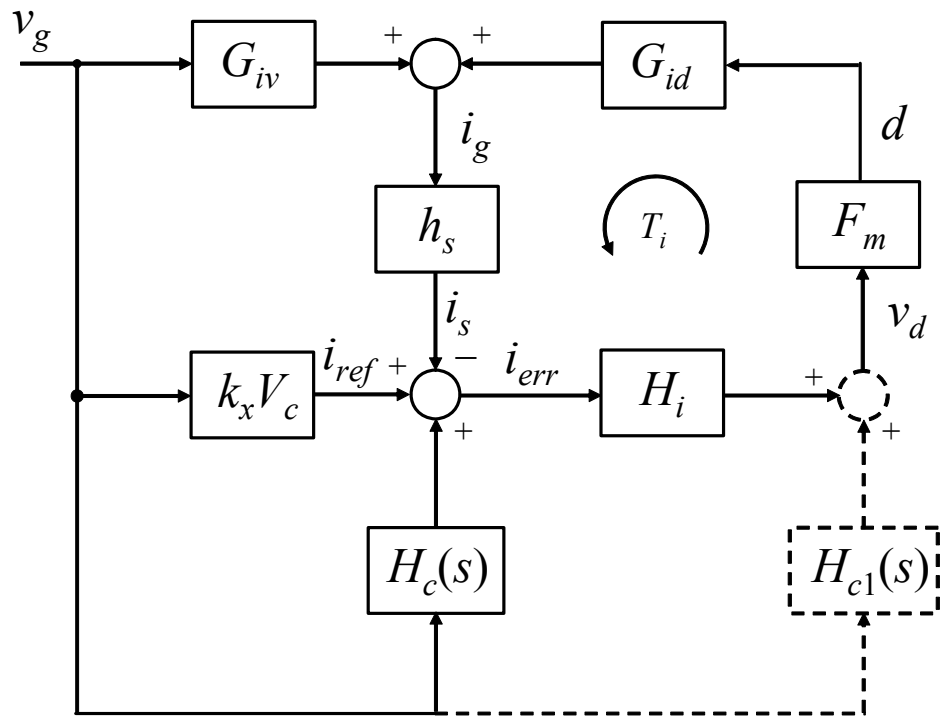


Figure 2.7 Two ways of implementing the leading-phase admittance cancellation for current phase lead compensation.

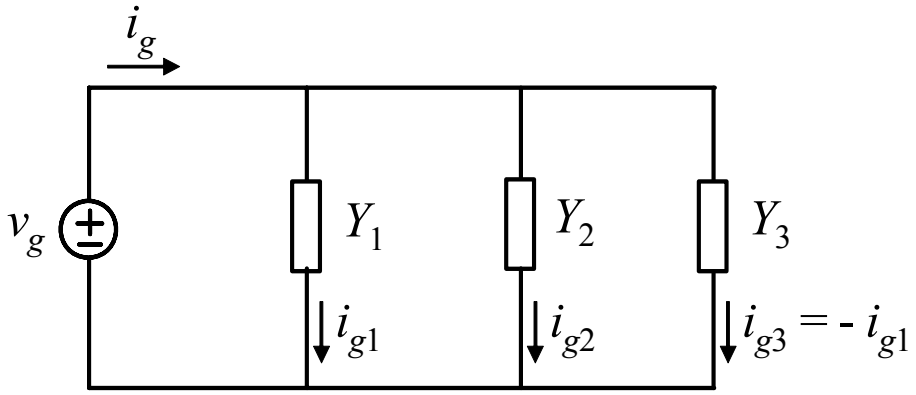


Figure 2.8 Elimination of the current phase lead by canceling the current in the leading-phase admittance branch.

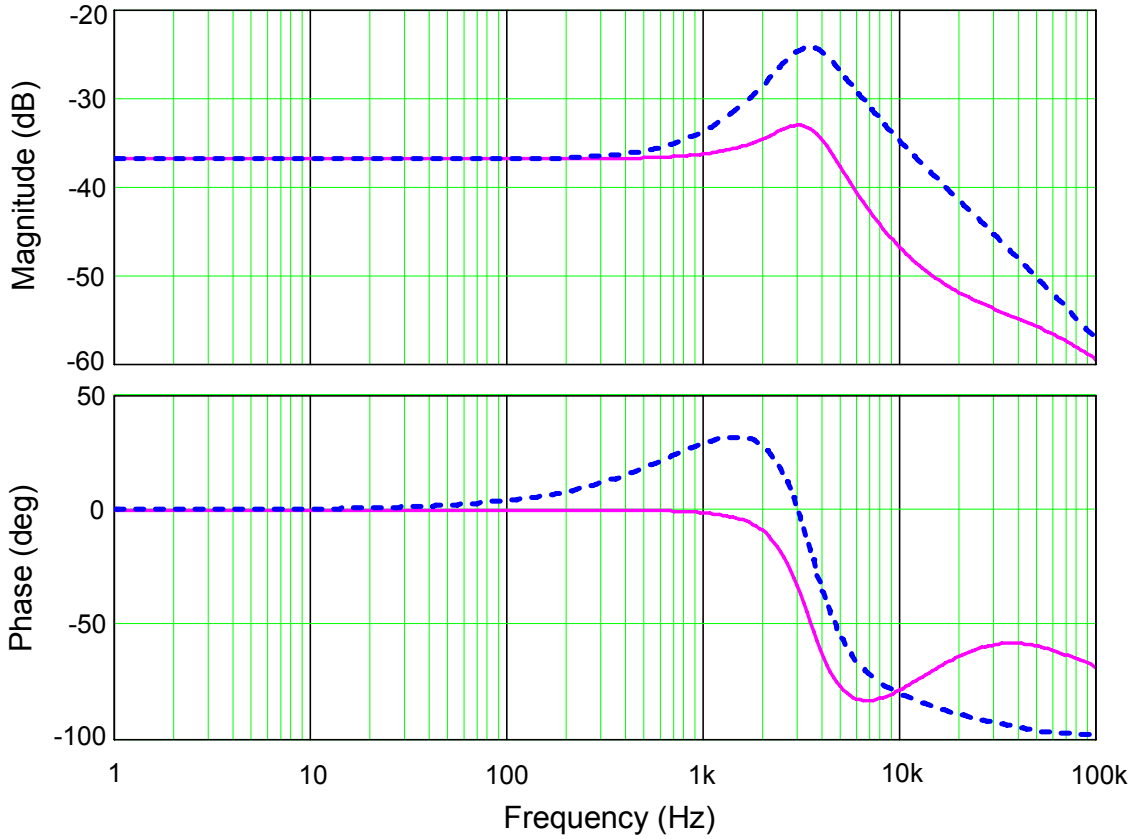


Figure 2.9 Closed-loop input admittance with leading-phase admittance cancellation. Dash—uncompensated, solid—LPAC-compensated.

extended for more than a decade. At 800 Hz, which is $^1/_5$ of the crossover frequency (4 kHz), the phase shift is less than 1°. Unlike $K(s)$ in the CRC method, $H_c(s)$ and $H_{c1}(s)$ are independent of load power.

2.3.3 Implementation of the LPAC

A generic implementation of the LPAC in a standard PFC control system is shown in Fig. 2.10. $H_c(s)$ is part of the compensator circuit; it is added to the system by means of an R_c-C_c network from the rectified line voltage to the negative input of the current loop amplifier. Assume for generality that the R_c-C_c circuit is connected to v_g through a gain h_c. Then,

$$H_c(s)\,H_i(s) = \frac{v_d(s)}{v_g(s)} = -\frac{h_c\left(R_f + \dfrac{1}{s\,C_{fz}}\right) \| \dfrac{1}{s\,C_{fp}}}{R_c + \dfrac{1}{s\,C_c}}, \tag{2.21}$$

$$H_c(s) = -\frac{C_c\,h_c}{C_{fp} + C_{fz}} \frac{s}{\omega_i\left(1 + \dfrac{s}{\omega_c}\right)}, \tag{2.22}$$

where

$$\omega_c = \frac{1}{C_c\,R_c}. \tag{2.23}$$

Comparing (2.22) with (2.18), we obtain

$$\omega_c = \omega_z, \qquad C_c = \frac{C_{fp} + C_{fz}}{V_o\,F_m\,h_c}, \quad \text{and} \quad R_c = \frac{1}{C_c\,\omega_z}. \tag{2.24}$$

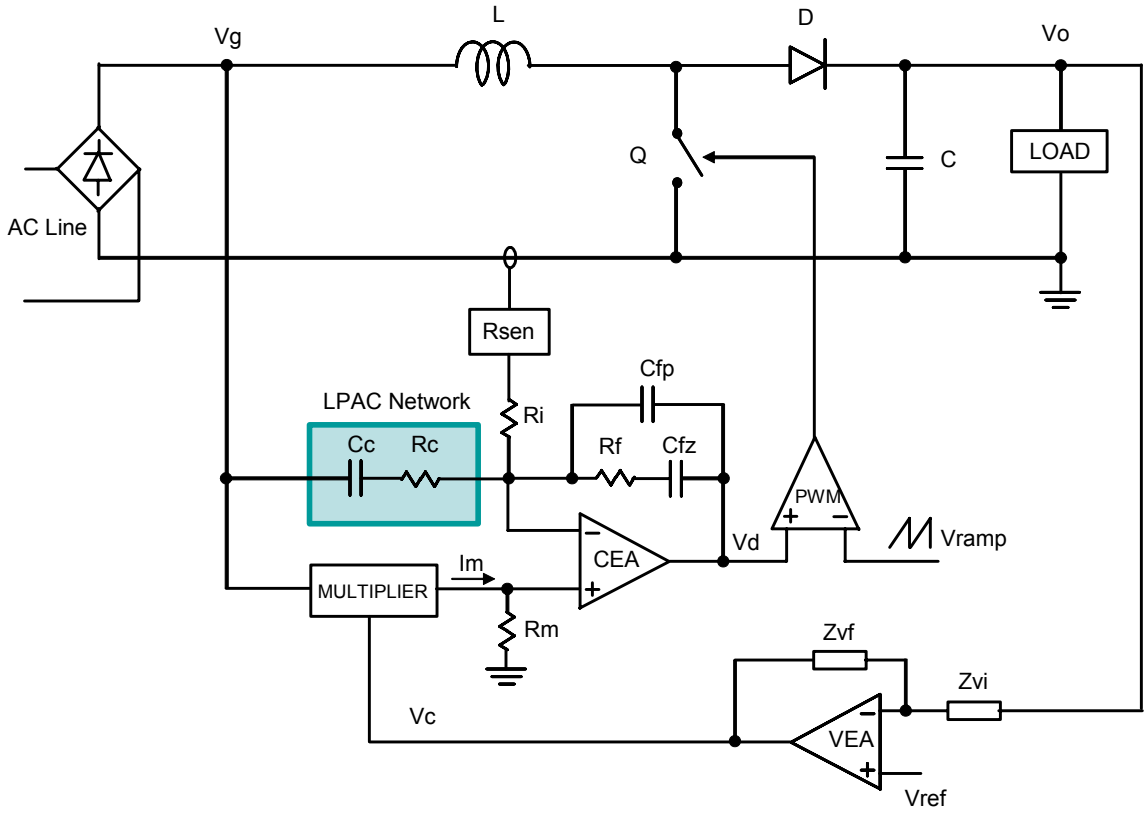


Figure 2.10 Generic implementation of the LPAC as part of the current loop compensator circuit.

The R_c-C_c circuit can be added to an existing converter without its redesign. In the simplest case, only two components (R_c and C_c) are needed. Fig. 2.10 shows how the LPAC can be implemented in a controller made of general-purpose components. A controller based on the UC3854 chip [56] would use the same way of connecting the LPAC network (Fig. 2.11). Another IC, UCC3817 [57], uses an additional inversion in the current loop and will require an inverted v_g signal to be applied to the R_c-C_c circuit (Fig. 2.12). Then, h_c is equal to the inverting amplifier gain. The inverting amplifier will need a negative supply voltage, which may be an undesirable requirement. An LPAC implementation shown in Fig. 2.13 does not require a negative supply voltage while preserving advantages of the UCC3817 such as the leading-edge modulation and higher noise immunity of the current amplifier. This circuit is based on using $H_{c1}(s)$ as shown in Fig. 2.7 (dash line) and requires breaking the connection between the error amplifier and the comparator. A new control IC with included LPAC functionality could possibly be created, which would integrate amplifiers A_1 and A_2 in the chip. The scaling factor of the voltage divider R_1-R_2 is determined by (2.20).

Single-phase PFC converters are usually designed with a universal "worldwide" voltage input. In order to maintain the same power drawn from the line regardless of the line voltage, the current reference is scaled down as the line voltage increases. This feature does not affect the LPAC design. The LPAC network is used to cancel the leading-phase current component, which does not depend on the load power. From Fig. 2.8, it is obvious that, as i_{g1} would change following a v_g change, so should i_{g3}. While i_{g2}, which represents the real power, has to be adjusted for a v_g change, i_{g3} does not.

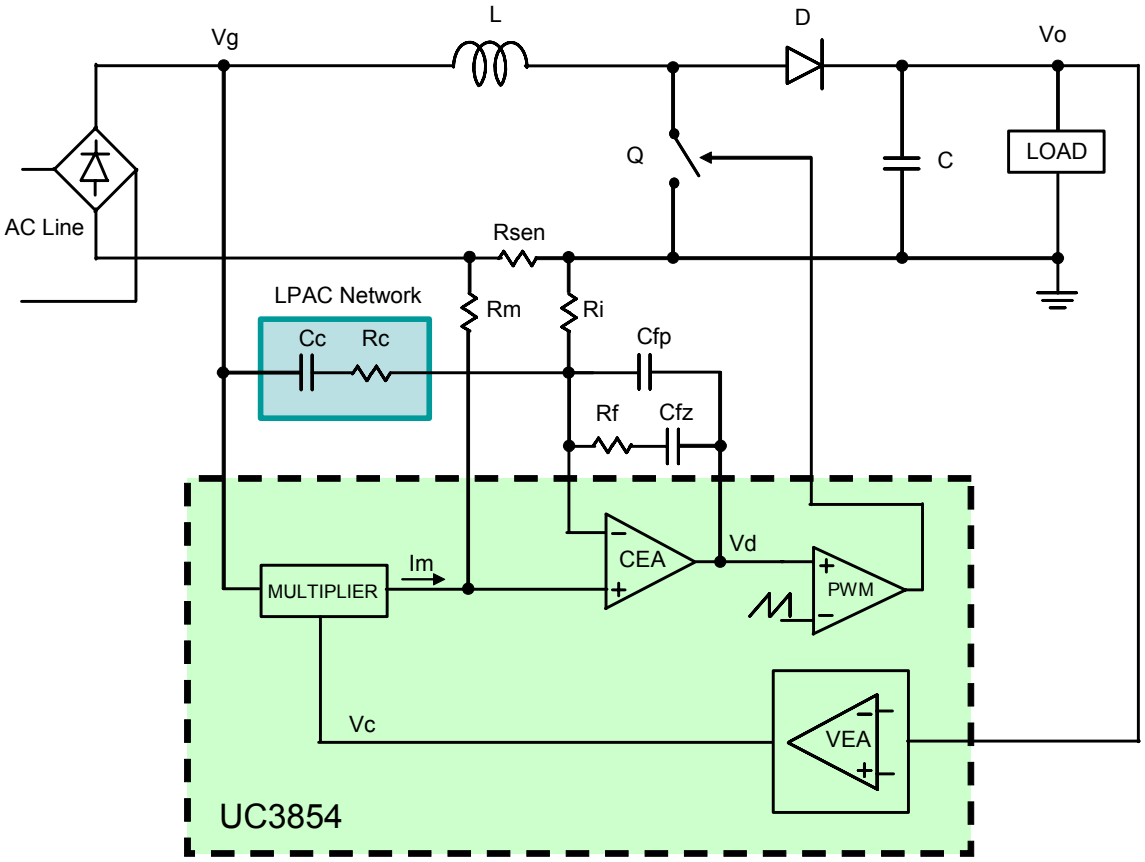


Figure 2.11 The LPAC implementation in the UC3854-based controller.

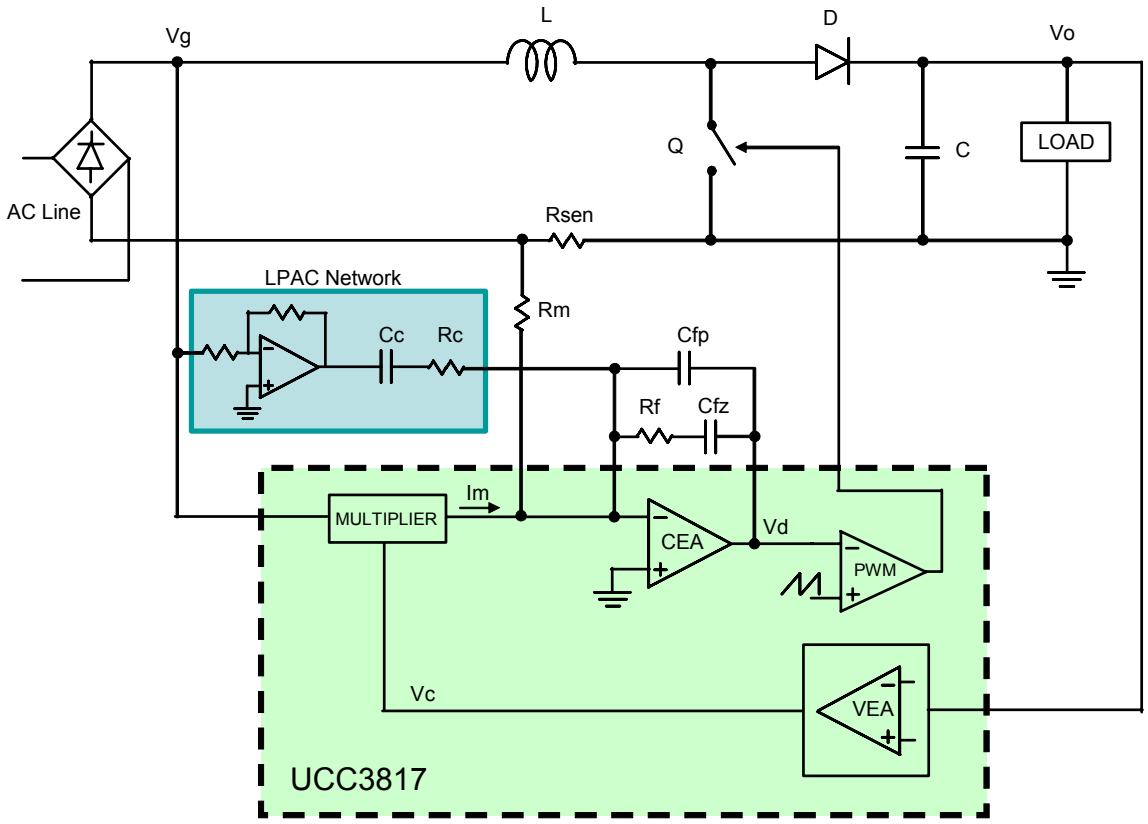


Figure 2.12 The LPAC implementation in the UCC3817-based controller.

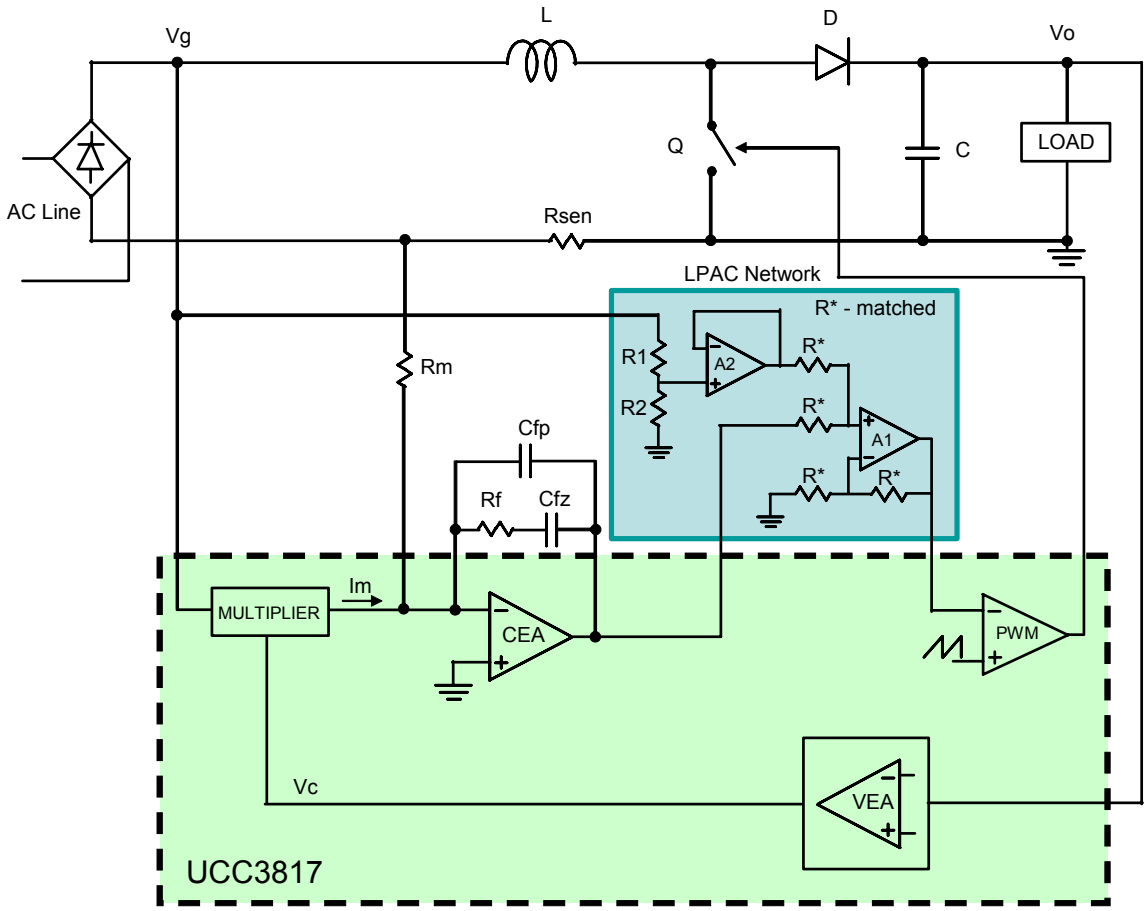


Figure 2.13 The LPAC implementation in the UCC3817-based controller without using a negative supply voltage.

2.4 Experimental Results

A PFC boost converter based on the UCC3817 Power Factor Preregulator IC was used to verify the LPAC method (Fig. 2.14). The bench setup was based on the UCC3817 Power Factor Preregulator Evaluation Board [40] with the LPAC circuit added as shown in Fig. 2.12. The current loop was designed with 4 kHz bandwidth. At 500 Hz line frequency, the phase lead and the zero-crossing distortion of the line current are observed, but they completely disappear when the LPAC circuit is enabled. The circuit was tested with different switching frequencies down to 35 kHz. At 60 Hz, there is no leading-phase distortion (Fig. 2.15 (a)), and the LPAC does not have any effect on the current. However, at higher line frequencies, the distortion becomes severe. Fig. 2.15 (b) and Fig. 2.15 (d) show the line current distortion when the frequency is increased to 500 Hz. The current phase lead does not depend on the switching frequency, and a higher switching frequency by itself does not alleviate the distortion. Fig. 2.15 (c) and Fig. 2.15 (e) indicate that the sinusoidal current shape with zero phase shift at 500 Hz is completely restored when the LPAC network is enabled, which is in agreement with the Bode plots in Fig. 2.9. While the converter was not tested at 800 Hz because of the ac source limitations, the Bode plots show that this design can operate up to 800 Hz without distortion when the LPAC is enabled. The experiment proved that it is possible to build a PFC converter for the aircraft ac frequency range (360–800 Hz) with a relatively low switching frequency and a high quality line current waveform.

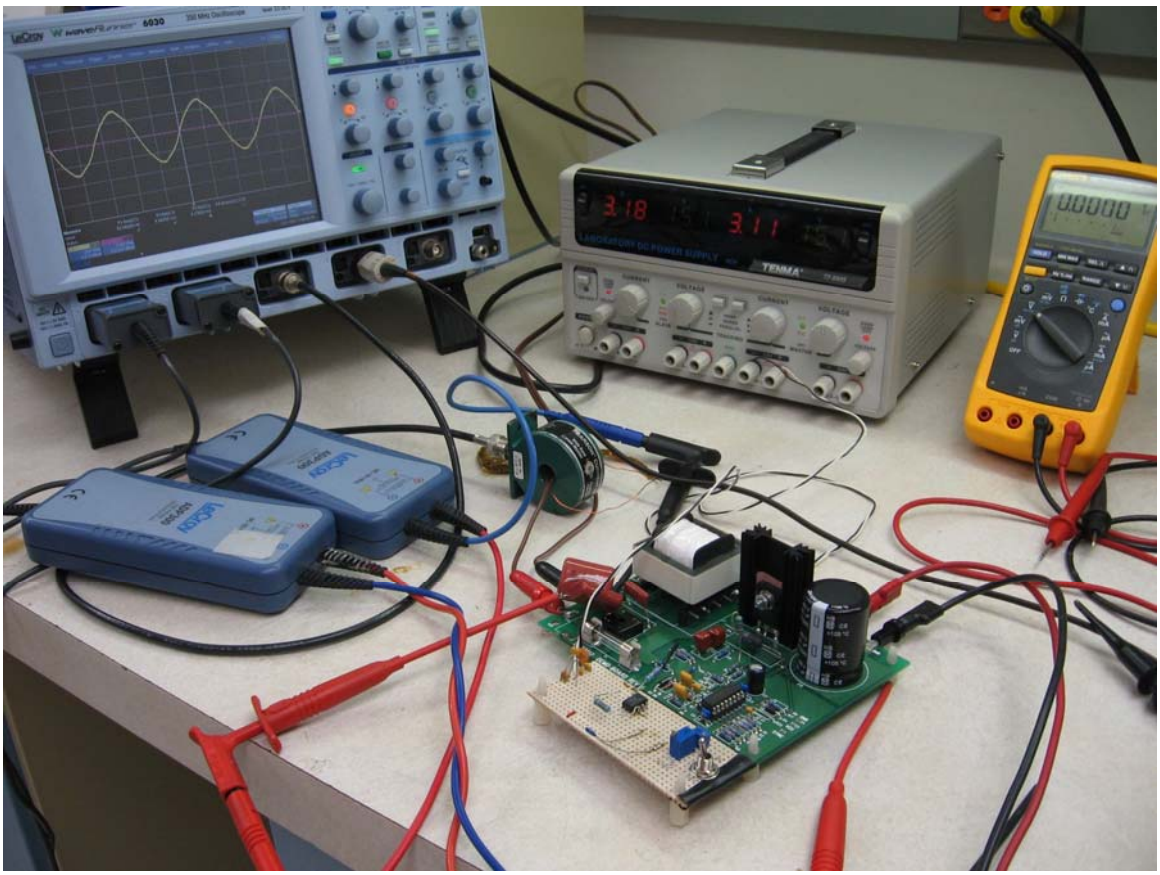


Figure 2.14 Experimental setup used to verify the LPAC method.

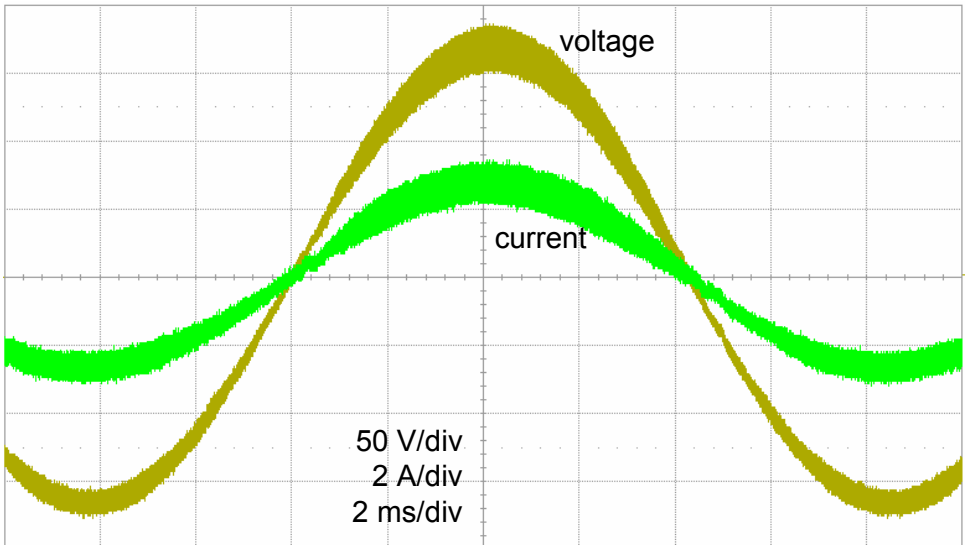


Figure 2.15(a) Experimental converter waveforms: f_{line} = 60 Hz, f_{sw} = 90 kHz, standard controller.

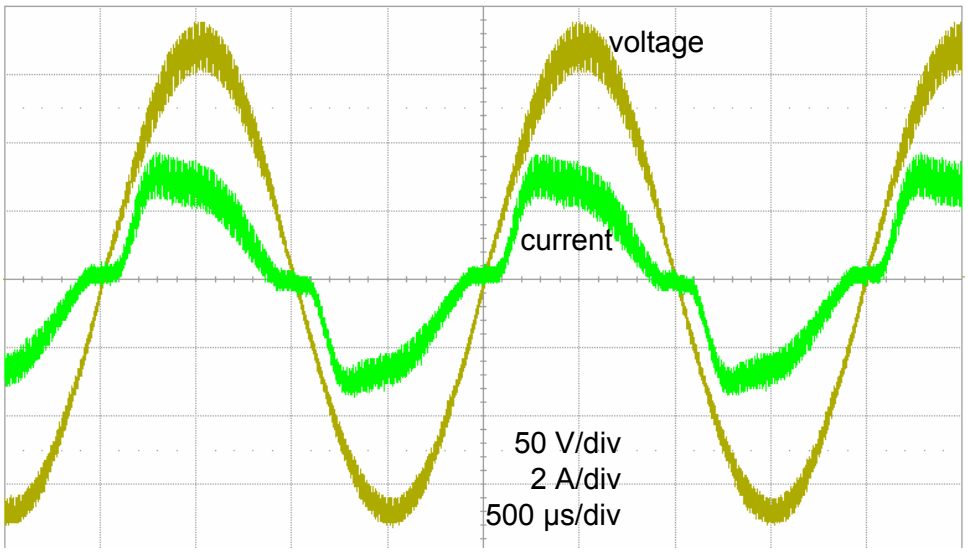


Figure 2.15(b) Experimental converter waveforms: f_{line} = 500 Hz, f_{sw} = 90 kHz, standard controller.

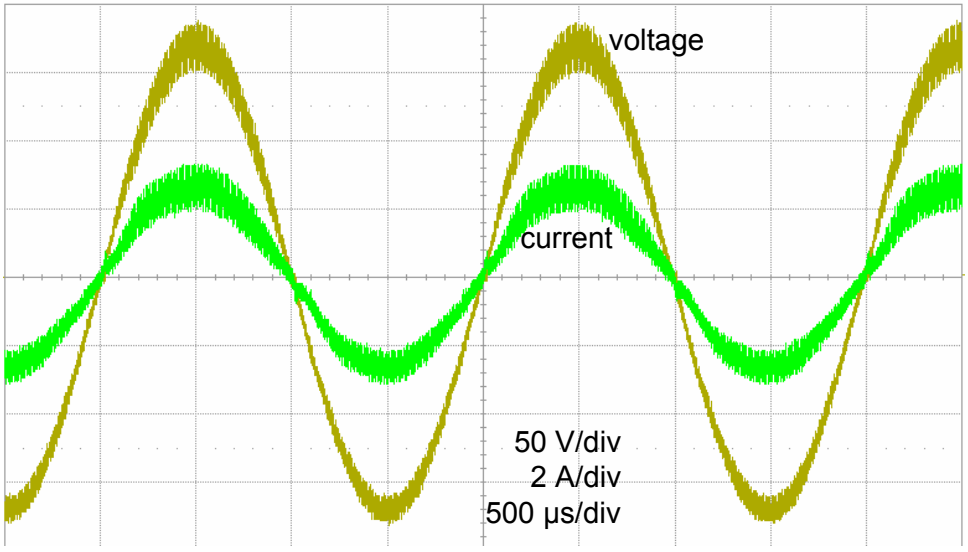


Figure 2.15(c) Experimental converter waveforms: f_{line} = 500 Hz, f_{sw} = 90 kHz, with LPAC.

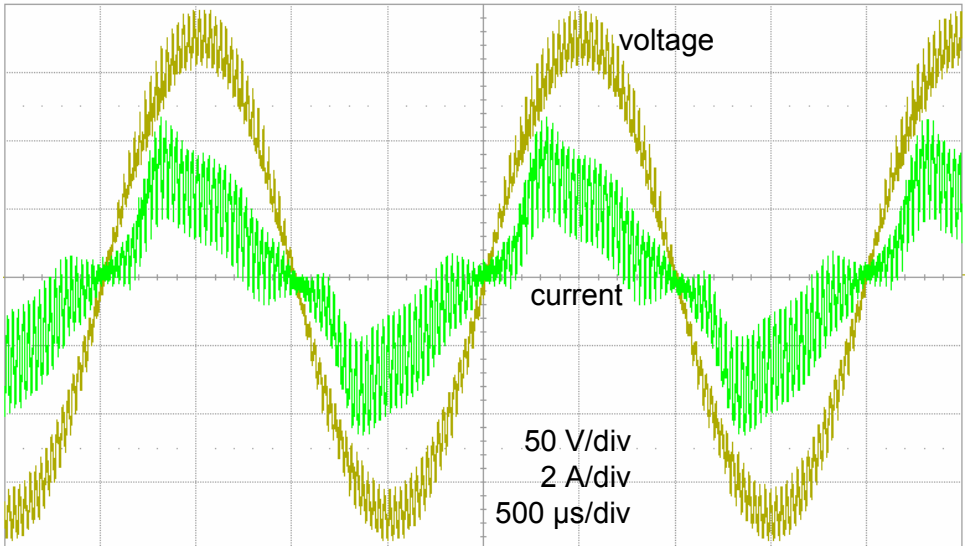


Figure 2.15(d) Experimental converter waveforms: f_{line} = 500 Hz, f_{sw} = 35 kHz, standard controller.

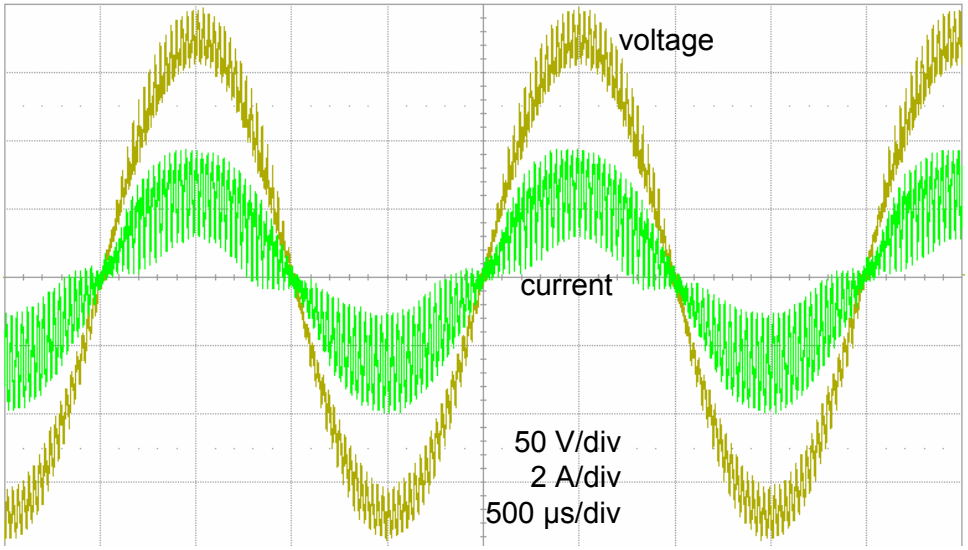


Figure 2.15(e) Experimental converter waveforms: f_{line} = 500 Hz, f_{sw} = 35 kHz, with LPAC.

2.5 Summary

The leading-phase admittance cancellation (LPAC) method has been proposed and developed for the single-phase PFC boost converter in order to eliminate the leading-phase distortion of the line current at higher line frequencies. This technique extends the allowable range of line frequencies from about $^1/_{150}$ of the current loop bandwidth with traditional design to about $^1/_5$ with the LPAC. This method can be used with any PFC boost converter but is especially useful in applications with higher line frequencies such as aircraft power systems (360–800 Hz) and in medium- and high-power (above 10 kW) single-phase PFC applications operating at the utility line frequency, which would benefit from a lower switching frequency (30 kHz or less). Unlike methods proposed in the past, the cancellation circuit added to the standard converter control system is load-invariant, line-voltage-invariant, and is not sensitive to the boost inductance variation. The LPAC method can be realized easily with only two passive components in the simplest case and can be applied to existing designs to extend their operating range of line frequencies or to lower their switching frequency in current operating conditions, thus improving the converter efficiency. The newly developed dynamic model of the system was used to determine component values of the LPAC network. Experimental results showed good agreement with simulation waveforms and confirmed effectiveness of the LPAC. It was shown theoretically and demonstrated experimentally that it is possible to build a PFC boost converter for the 360–800 Hz line frequency range with a relatively low switching frequency and high quality of the line current waveform.

Chapter 3

Active Compensation of the Input Filter Capacitor Current in Single-Phase PFC Boost Converters

3.1 Introduction

Single-phase ac-dc PFC boost converters operating in continuous current conduction mode (CCM) with average current mode control (ACMC) are often employed when a high power factor and low harmonic distortion of the line current are required. The two-loop control scheme used in these converters produces a sinusoidal line current in phase with the line voltage [6]. The converters can be based on a unidirectional or bidirectional topology [18]. An input filter capacitor at the ac line terminals is commonly used to provide a low-impedance path for the inductor current switching ripple in order to reduce propagation of the switching noise into the line [17], [40]. The required filtering capacitance is a function of the converter switching frequency and does not depend on the line frequency. However, this capacitor does affect the total current drawn from the line. Reactive current drawn by this capacitor is proportional to the line frequency. Because of this current, power factor of the converter is less than unity even if the converter without the filtering capacitor operates with unity power factor. At the utility line frequency (50–

60 Hz), this current is relatively small and does not cause noticeable power factor degradation. However, in applications with much higher line frequencies such as in aircraft power systems (360–800 Hz [46]–[49]), the input capacitor current becomes significant. For example, a 1.5-μF input capacitor typical for a 250-W converter [40] draws a current of only 68 mA from a 120-V, 60-Hz line but as much as 0.9 A at 800 Hz, which causes a 23° phase shift of the total current at full load and even larger phase shift at a lower load.

The leading-phase admittance cancellation technique (LPAC) introduced in Chapter 2 can be used to cancel the inductor current phase lead, which causes a zero-crossing distortion of the line current, in PFC boost converters designed for utility line frequency but operating at higher line frequencies such as 360-800 Hz [46], [47]. In this chapter, we will see how to adapt the LPAC method (with some limitations imposed by topologies) to cancel the reactive current drawn by the input capacitor as well. Dynamic modeling of the converter has been used to determine conditions for reactive current cancellation and control circuit parameters required for that. Computer-aided analysis and experiments were used to verify the proposed method. It is shown how to achieve complete, load-invariant, line-frequency-invariant compensation of the input capacitor current in a bidirectional PFC boost converter (represented in this research by the full-bridge topology) using an adaptation of the LPAC technique. In a unidirectional PFC boost converter (represented by the traditional diode-bridge circuit [17], [40]), the presence of uncontrolled rectifiers (diodes) in the line current path imposes limitations on the size of the filtering capacitor whose current can be compensated. However, a trade-

off choice of filtering capacitors on the ac side and dc side of the bridge is possible, which allows unity-power-factor operation with substantial reduction but not complete elimination of the switching ripple in the line current.

3.2 Bidirectional PFC Boost Converter

We will consider a bidirectional PFC boost converter based on the full-bridge topology operating in CCM with ACMC (Fig. 3.1). Following the modeling approach used in Chapter 2, the dc link voltage v_o and the voltage loop compensator output v_c can be considered constant if the dc link capacitance C is large enough. Then, the current loop dynamics is described by the control diagram in Fig. 3.2. The power stage line-to-current and control-to-current transfer functions for this topology are

$$G_{iv}(s) = \frac{1}{r + s\,L} \quad \text{and} \quad G_{id}(s) = \frac{2V_o}{r + s\,L}, \tag{3.1}$$

where r is an equivalent resistance of the current path. The compensator is a PI-type controller with the zero placed at or near the loop crossover frequency [6]:

$$H_i(s) = \frac{\omega_i\left(1 + \dfrac{s}{\omega_z}\right)}{s\left(1 + \dfrac{s}{\omega_p}\right)}. \tag{3.2}$$

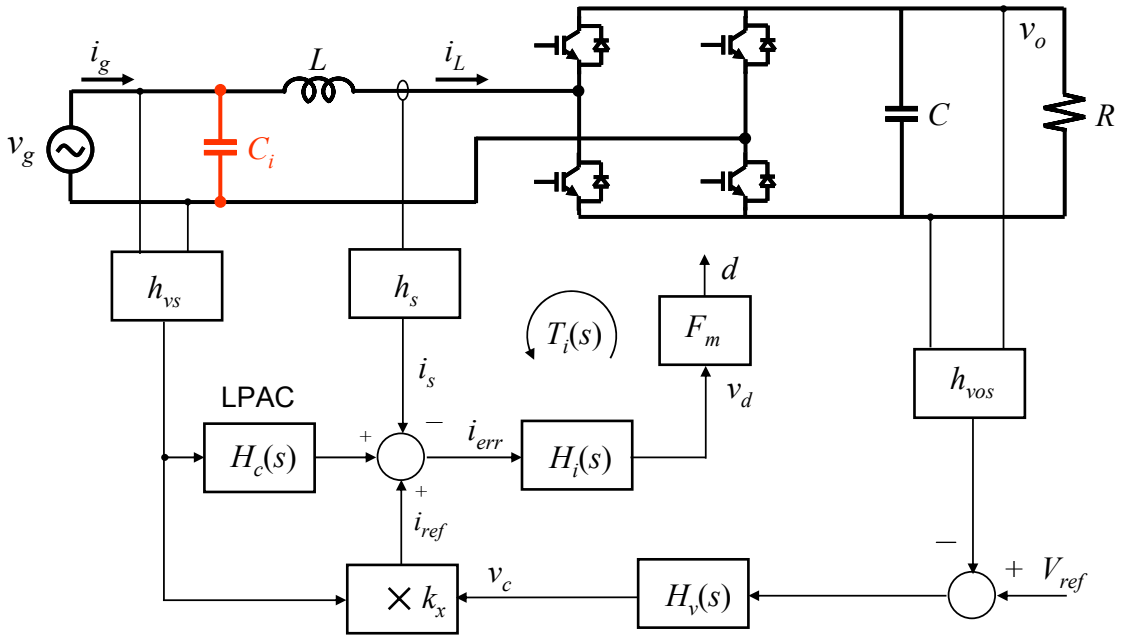


Figure 3.1 Full-bridge PFC converter with an input filter capacitor and LPAC.

H_i—current loop compensator, H_v—voltage loop compensator, H_c—LPAC transfer function, F_m—modulator gain, k_x—multiplier gain, h_s—current sensor gain, h_{vs} and h_{vos}—voltage sensors gain.

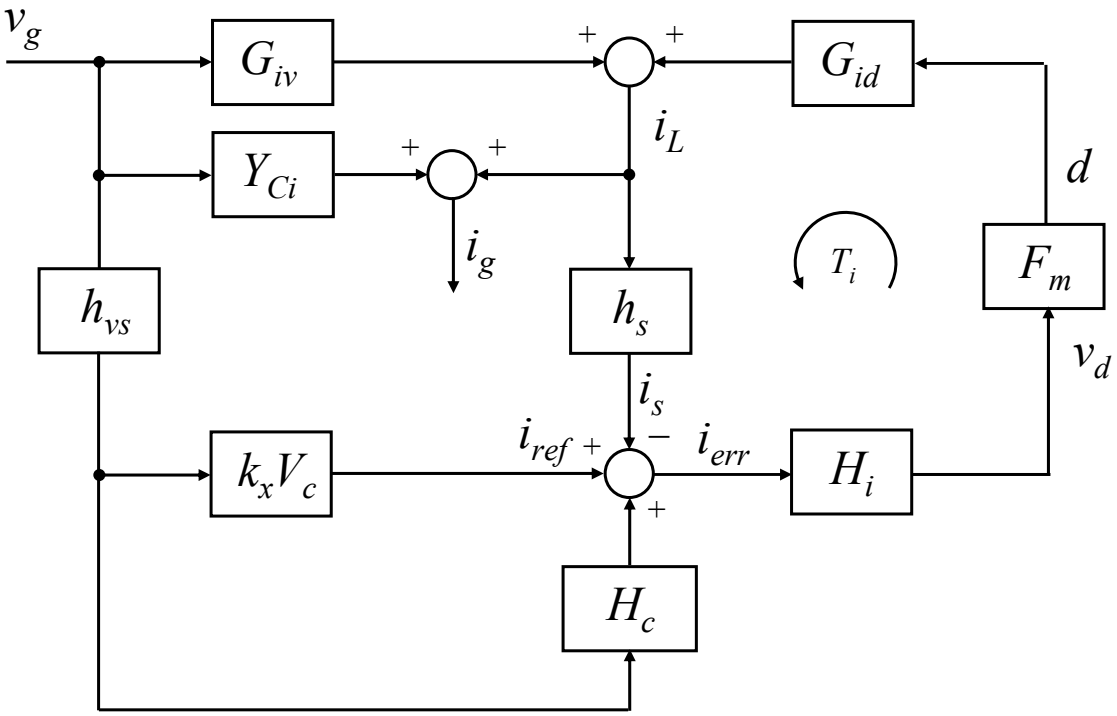


Figure 3.2 Current loop control diagram of the converter.

The converter uses the LPAC in order to eliminate the leading phase of the inductor current at higher line frequencies. From Fig. 3.2, the total input admittance of the converter is

$$Y(s) = \frac{i_g(s)}{v_g(s)} = \frac{G_{iv}}{1+T_i} + \frac{G_{id}\,F_m\,H_i}{1+T_i}\,k_x V_c\,h_{vs} + \frac{G_{id}\,F_m\,H_i}{1+T_i}\,H_c\,h_{vs} + Y_{Ci}\,, \tag{3.3}$$

where T_i is the current loop gain:

$$T_i = G_{id}\,F_m\,H_i\,h_s\,. \tag{3.4}$$

According to (3.3), the total input admittance of the converter can be represented by three admittance branches $Y_1(s)$, $Y_2(s)$, and $Y_3(s)$ and the input capacitor C_i (Fig. 3.3):

$$Y(s) = Y_1(s) + Y_2(s) + Y_3(s) + Y_{Ci}(s)\,. \tag{3.5}$$

Below the current loop crossover frequency, neglecting r,

$$Y_1(s) = \frac{s}{2V_o\,F_m\,h_s\,\omega_i\left(1+\dfrac{s}{\omega_z}\right)}, \tag{3.6}$$

$$Y_2(s) = \frac{k_x V_c\,h_{vs}}{h_s} = \frac{I_g}{V_g} = \frac{P_g}{{V_g}^2}, \tag{3.7}$$

$$Y_3(s) = \frac{H_c\,h_{vs}}{h_s} = -Y_1(s) = -\frac{s}{2V_o\,F_m\,h_s\,\omega_i\left(1+\dfrac{s}{\omega_z}\right)}, \tag{3.8}$$

$$Y_{Ci}(s) = s\,C_i\,. \tag{3.9}$$

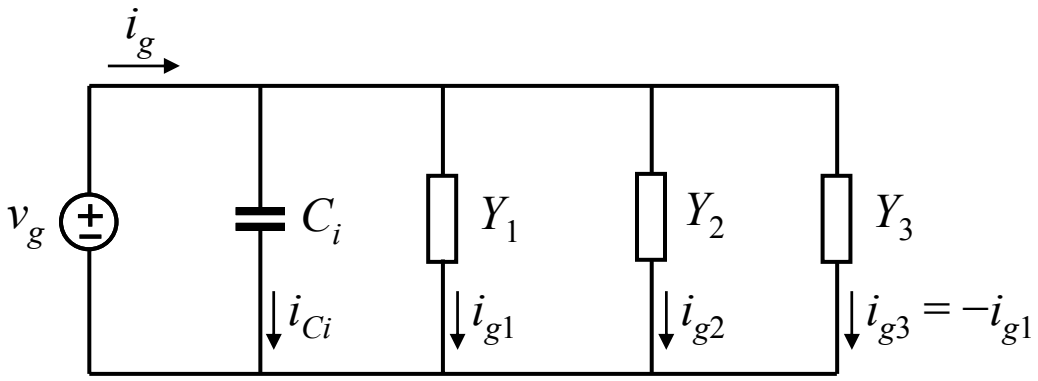


Figure 3.3 Input admittance of the converter with the input filter capacitor.

The LPAC term $Y_3(s)$ is used to cancel the effect of the leading-phase term $Y_1(s)$. From (3.8), the LPAC transfer function is

$$H_c(s) = -\frac{s}{2V_o F_m h_{vs} \omega_i \left(1 + \frac{s}{\omega_z}\right)}. \tag{3.10}$$

With ω_z located at the crossover frequency and the upper limit of the line frequency range being at least five times below the crossover frequency as in Chapter 2, the effect of the pole in $Y_1(s)$ can be neglected. Then, the effect of the leading-phase term $Y_1(s)$ can be viewed as created by a capacitor, which can be lumped with C_i to be cancelled together by $Y_3(s)$ within the line frequency range. The LPAC should use the canceling transfer function in the form

$$H_c(s) = -\left(Y_1(s) + Y_{Ci}(s)\right)\frac{h_s}{h_{vs}}, \tag{3.11}$$

which results in

$$H_c(s) = -\frac{1 + 2V_o F_m \omega_i C_i h_s}{2V_o F_m h_{vs}} \frac{s}{\omega_i \left(1 + \frac{s}{\omega_z}\right)}. \tag{3.12}$$

Comparing (3.12) with the circuit realization for $H_c(s)$, which is used in the converter implementation (Fig. 3.4), we can obtain component values for the cancellation network:

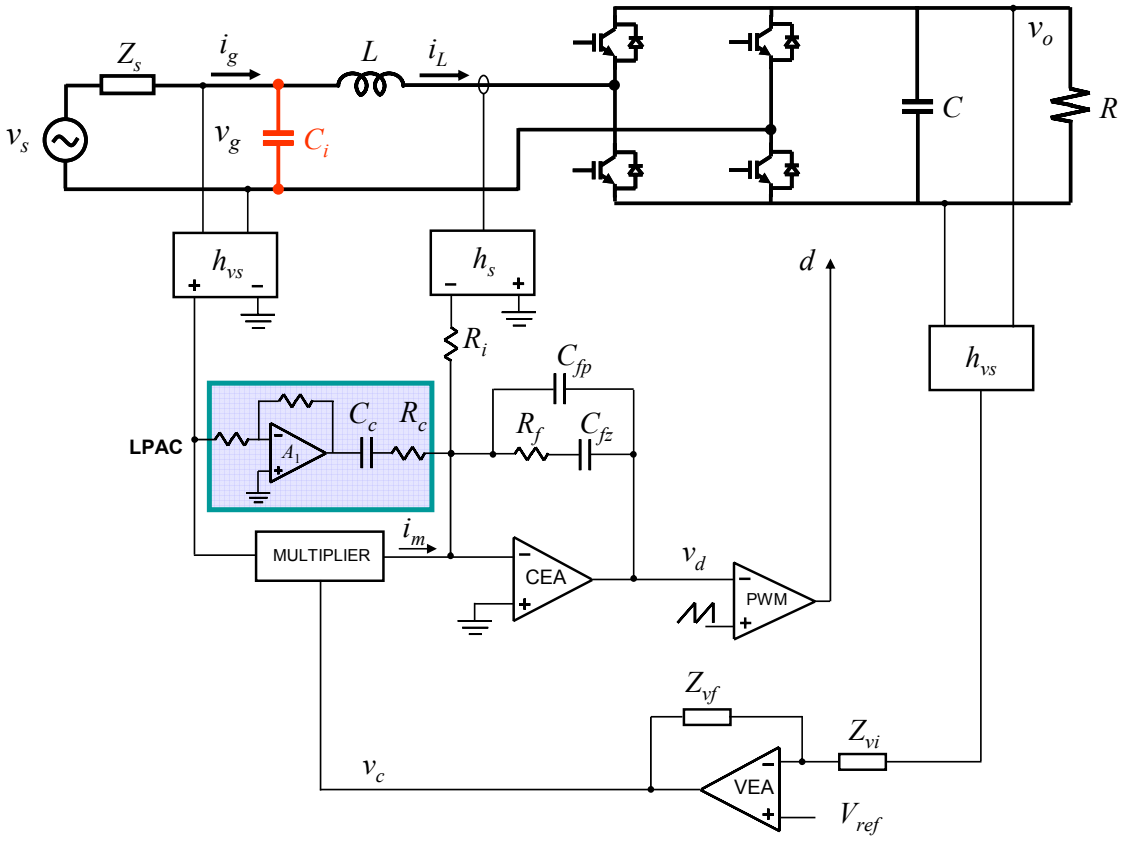


Figure 3.4 Implementation of the bidirectional PFC converter.

$$C_c = \frac{C_{fp} + C_{fz}}{2 V_o F_m h_c h_{vs}} \left(1 + 2 V_o F_m \omega_i C_i h_s\right) \tag{3.13}$$

and

$$R_c = \frac{1}{C_c \omega_z}, \tag{3.14}$$

where h_c is gain of the LPAC network amplifier A_1 (Fig. 3.4). Expressions (3.13) and (3.14) show that the achieved compensation of C_i current is load-invariant and line-frequency-invariant. If an input capacitor is not used, or its current is not intended to be cancelled by the LPAC, letting $C_i = 0$ in (3.13) results in an expression for C_c that is equivalent to (2.24).

Converter operation was analyzed using a PSpice simulation model based on the converter circuit diagram (Fig. 3.4). Fig. 3.5 shows waveforms of the converter with a standard two-loop controller (without the LPAC) designed for the utility line frequency and operating at 500 Hz. The inductor current i_L has a phase lead due to the leading-phase input admittance term $Y_1(s)$. The total current i_g has additional phase lead due to the reactive current drawn by the input capacitor. A phase shift of the total current results in deterioration of the converter power factor. If the leading-phase term $Y_1(s)$ is cancelled by the LPAC, the inductor current is in phase with the line voltage (Fig. 3.6). However, the reactive input capacitor current still causes phase shift of the total current i_g and non-unity power factor operation. The LPAC can be used to cancel C_i current as well such as the total current is in phase with the line voltage (Fig. 3.7), and the converter truly operates with unity power factor. The LPAC causes the inductor current to acquire a phase lag, which cancels the phase-leading current of the input capacitor. The total current

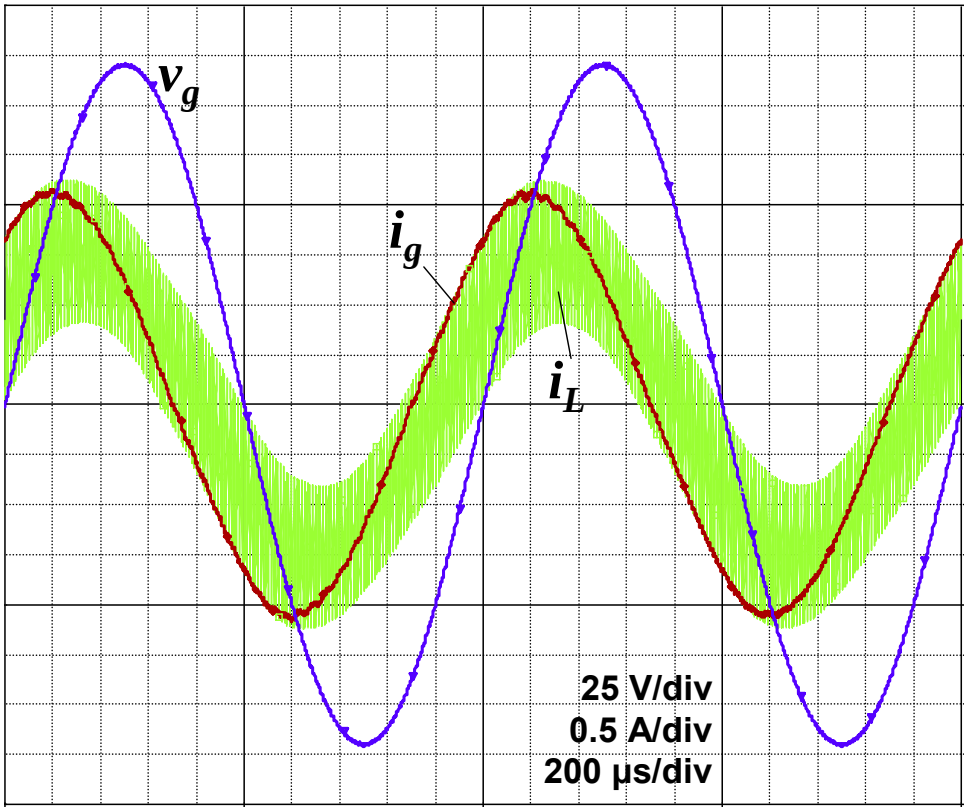


Figure 3.5 Bidirectional PFC converter operation with a standard controller (without LPAC).

f_{ac} = 500 Hz, f_{sw} = 90 kHz, C_i = 1.5 µF, P_o = 100 W.

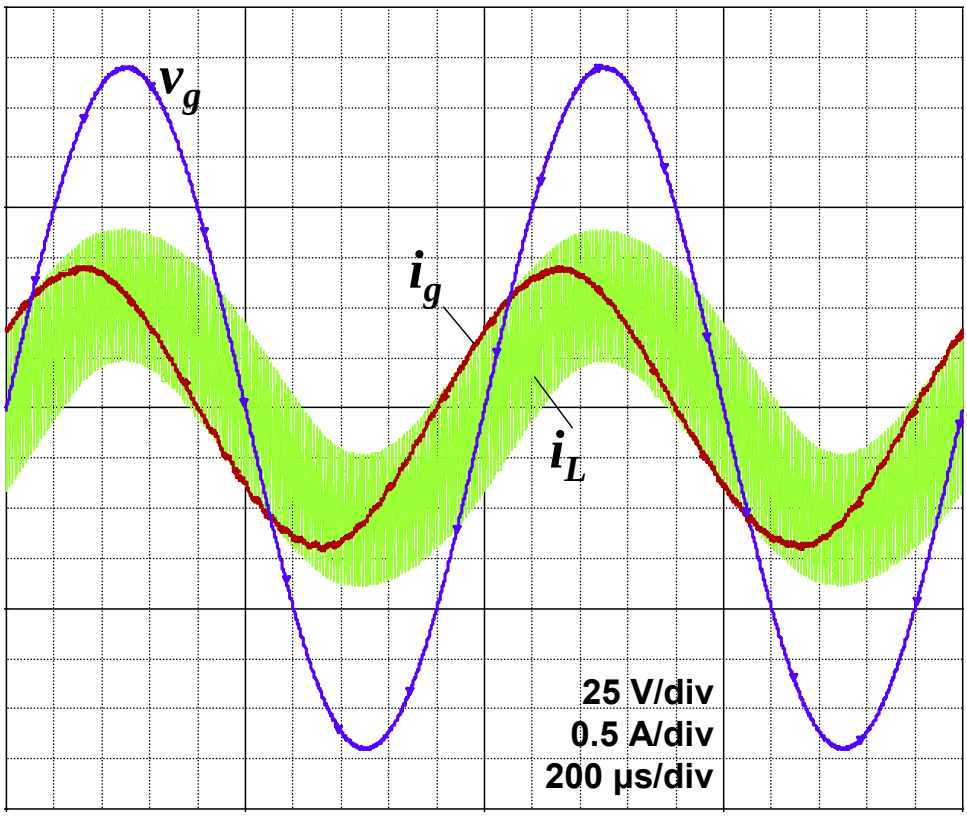


Figure 3.6 Bidirectional PFC converter operation with LPAC-compensated inductor current.

f_{ac} = 500 Hz, f_{sw} = 90 kHz, C_i = 1.5 µF, P_o = 100 W.

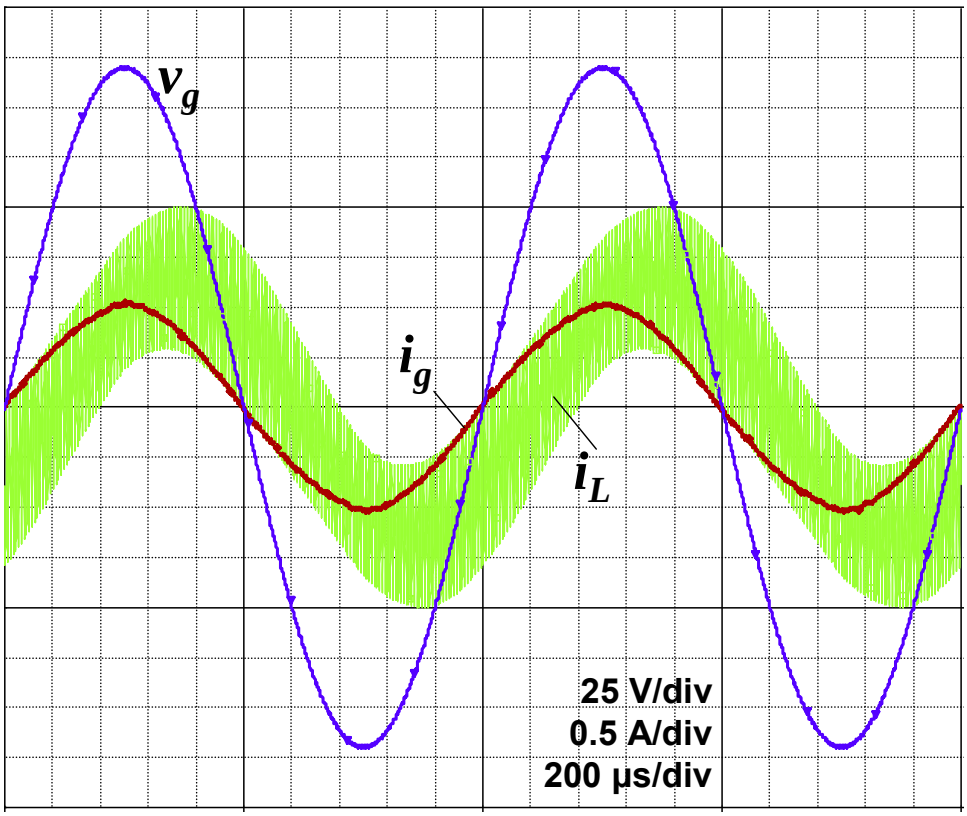


Figure 3.7 Bidirectional PFC converter operation with LPAC-compensated total current.

f_{ac} = 500 Hz, f_{sw} = 90 kHz, C_i = 1.5 µF, P_o = 100 W.

magnitude in Fig. 3.7 is substantially reduced compared with Fig. 3.5 and 3.6 because the total current no longer contains a reactive component.

3.3 Unidirectional PFC Boost Converter

The unidirectional PFC boost converter (Fig. 3.8 and 3.9) has the same control structure as the bidirectional converter (Fig. 3.1), but the power circuit uses a diode bridge rectifier and a single-switch boost converter. Under an assumption that the dc link capacitance C is large enough, v_o and v_c can be considered constant, and the current loop dynamics is described by the control diagram in Fig. 3.2, where $h_{vs} = 1$. Besides that, there is a difference in the power stage transfer functions:

$$G_{iv}(s) = \frac{1}{r + sL} \qquad \text{and} \qquad G_{id}(s) = \frac{V_o}{r + sL}, \tag{3.15}$$

where r is an equivalent resistance of the current path. According to the control diagram (Fig. 3.2), the total input admittance of the converter is described by (3.3), in which expressions for $Y_1(s)$ and $Y_3(s)$ take the following forms:

$$Y_1(s) = \frac{s}{V_o F_m h_s \omega_i \left(1 + \dfrac{s}{\omega_z}\right)}, \tag{3.16}$$

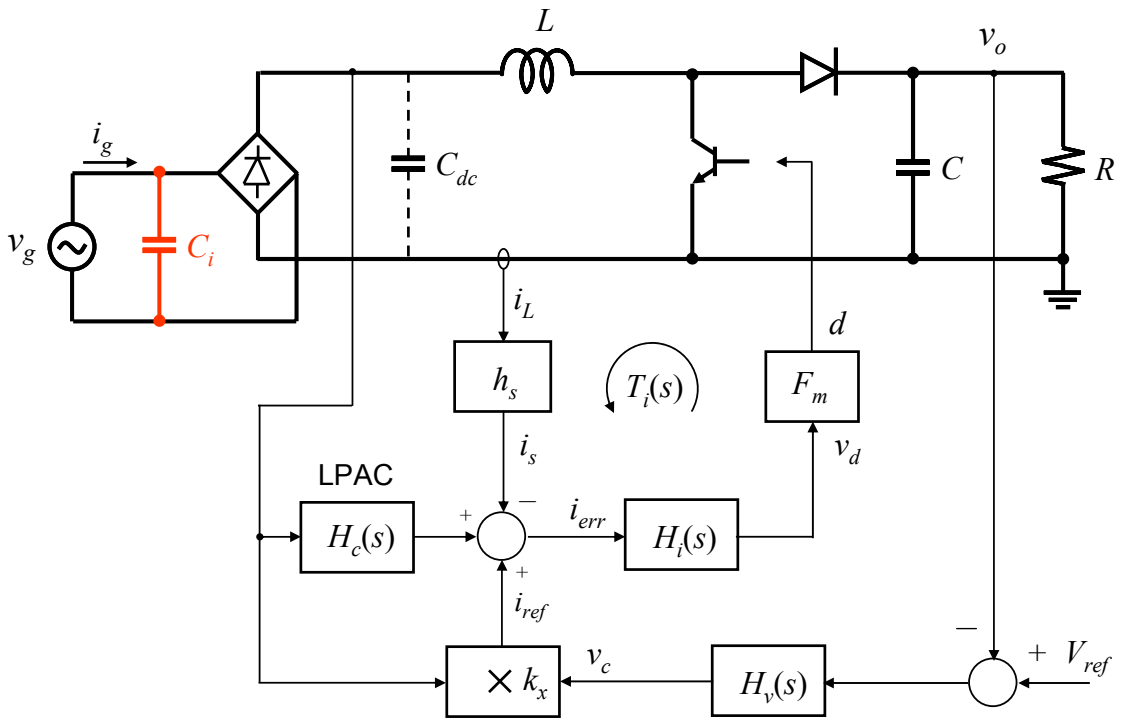


Figure 3.8 Unidirectional PFC boost converter with an input filter capacitor and the LPAC.

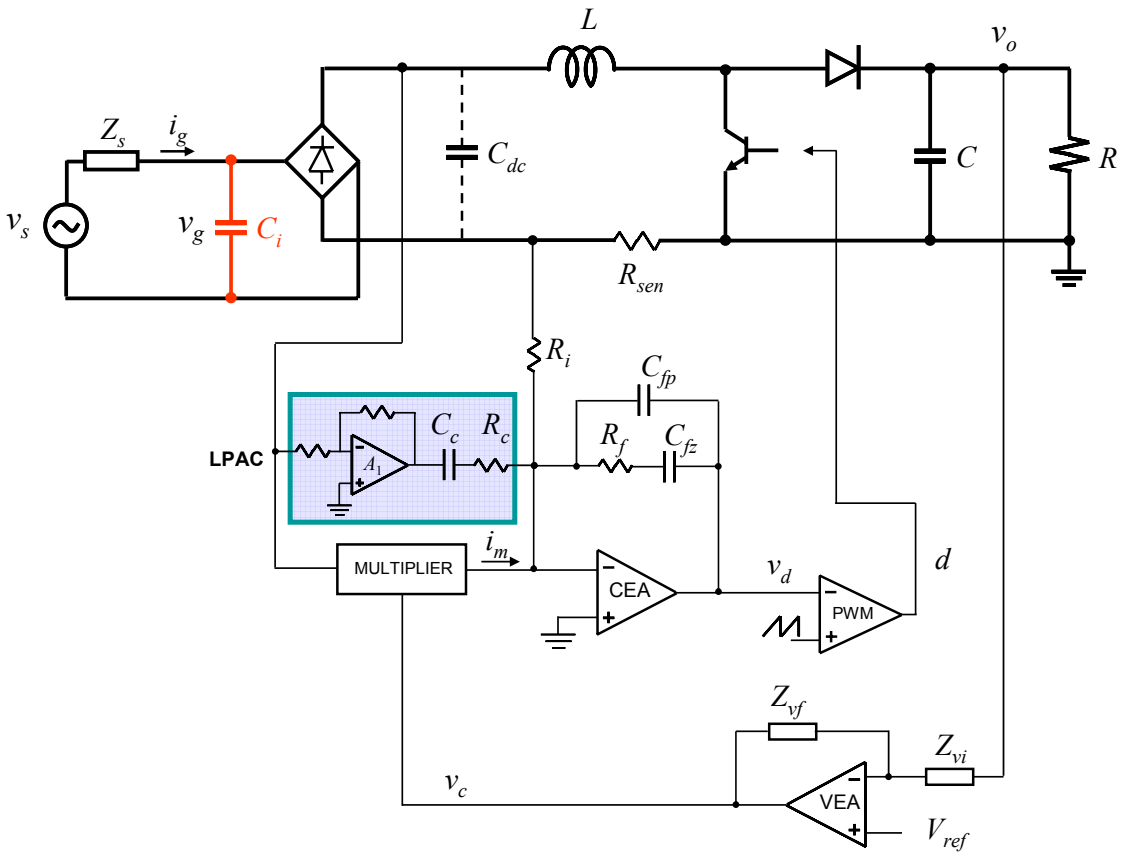


Figure 3.9 Implementation of the unidirectional PFC boost converter.

$$Y_3(s) = \frac{H_c}{h_s} = -Y_1(s) = -\frac{s}{V_o\, F_m\, h_s\, \omega_i \left(1 + \dfrac{s}{\omega_z}\right)}. \tag{3.17}$$

and the LPAC transfer function is (according to Chapter 2)

$$H_c(s) = -\frac{s}{V_o\, F_m\, \omega_i \left(1 + \dfrac{s}{\omega_z}\right)}. \tag{3.18}$$

Using the LPAC to cancel the input capacitor current, according to (3.11), will require the transfer function

$$H_c(s) = -\frac{1 + V_o\, F_m\, \omega_i\, C_i\, h_s}{V_o\, F_m} \frac{s}{\omega_i \left(1 + \dfrac{s}{\omega_z}\right)}, \tag{3.19}$$

which is realized with the following component values for the LPAC network:

$$C_c = \frac{C_{fp} + C_{fz}}{V_o\, F_m\, h_c} \left(1 + V_o\, F_m\, \omega_i\, C_i\, h_s\right) \tag{3.20}$$

and

$$R_c = \frac{1}{C_c\, \omega_z}, \tag{3.21}$$

which are similar to the ones obtained for the bidirectional converter. If $C_i = 0$, equation (3.20) is reduced to (2.24).

The method of using the LPAC for the input capacitor current cancellation in the unidirectional converter and expressions for C_c and R_c are very similar to the ones for the

bidirectional converter. Besides a subtle difference in expressions for C_c, however, there is a major difference between the bidirectional and unidirectional topologies: the latter has uncontrolled rectifiers (diodes) in the ac line current path. As explained in [46], the diode bridge causes a zero-crossing distortion of the inductor current whenever it is not in phase with the line voltage. This is demonstrated in simulation results using a PSpice model based on the converter circuit diagram in Fig. 3.9. Fig. 3.10 shows waveforms of the converter with a standard two-loop controller (without the LPAC) designed for the utility line frequency and operating at 500 Hz (inductor current i_L is measured on the ac side of the bridge, which makes it easier to compare i_g and i_L waveforms). The leading-phase admittance component causes a leading phase of the inductor current and the zero-crossing distortion due to the diode bridge. The total line current i_g has an additional phase lead because it includes reactive current drawn by C_i. The LPAC can be used to eliminate the zero-crossing distortion of the inductor current (Fig. 3.11). However, the input capacitor current remains uncompensated, which results in a phase shift of the total current; thus the converter operates with a less-than-unity power factor. In a bidirectional converter, this phase shift was compensated by adding an appropriate phase lag to the inductor current i_L as discussed above. The unidirectional converter does not allow this solution. An inductor current phase shift, whether it is leading or lagging, causes a zero-crossing distortion due to the diode bridge. This effect is demonstrated in Fig. 3.12, where an attempt is made to use the LPAC to compensate the input capacitor current according to (3.19–3.21). The inductor current phase lag created by the LPAC causes a severe zero-crossing distortion and unacceptable current waveforms.

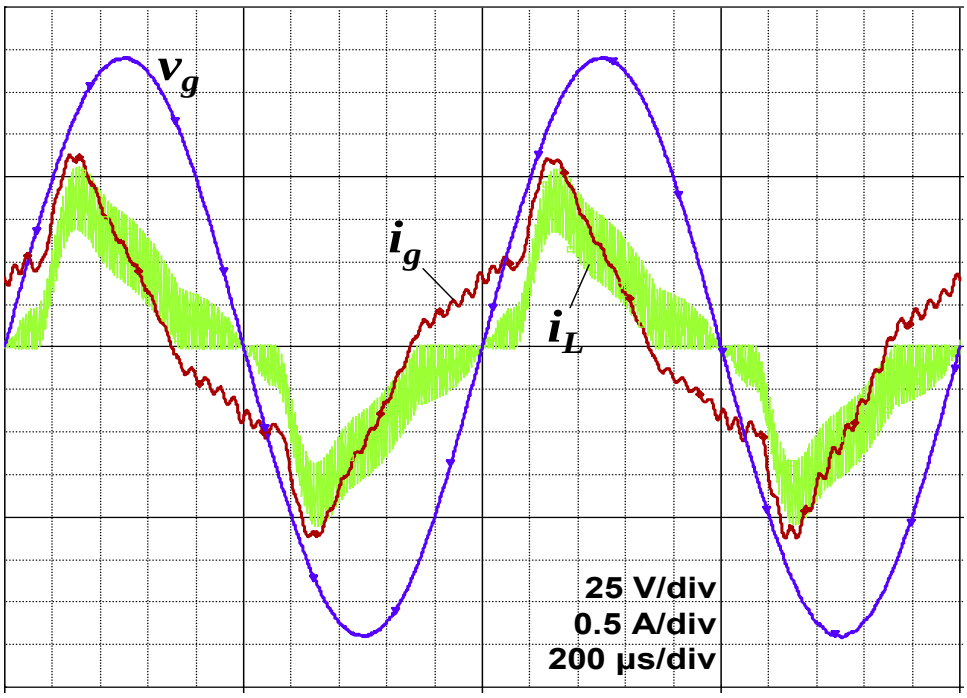


Figure 3.10 Unidirectional PFC converter operation with a standard controller (no LPAC).

f_{ac} = 500 Hz, C_i = 1.5 µF, P_o = 100 W.

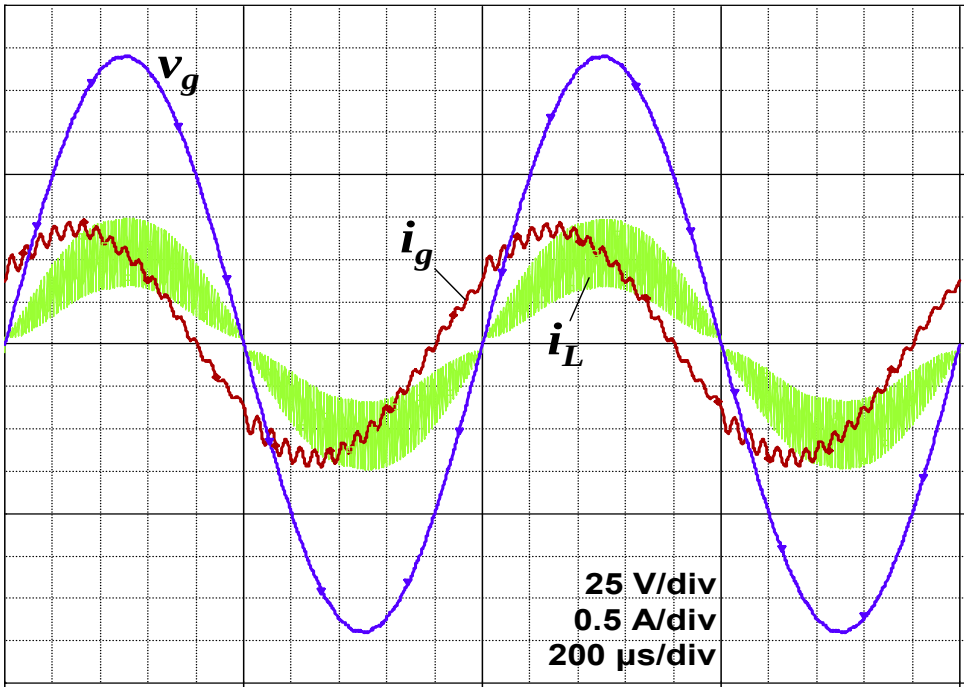


Figure 3.11 Unidirectional PFC converter operation with LPAC-compensated inductor current.

f_{ac} = 500 Hz, f_{sw} = 90 kHz, C_i = 1.5 µF, P_o = 100 W.

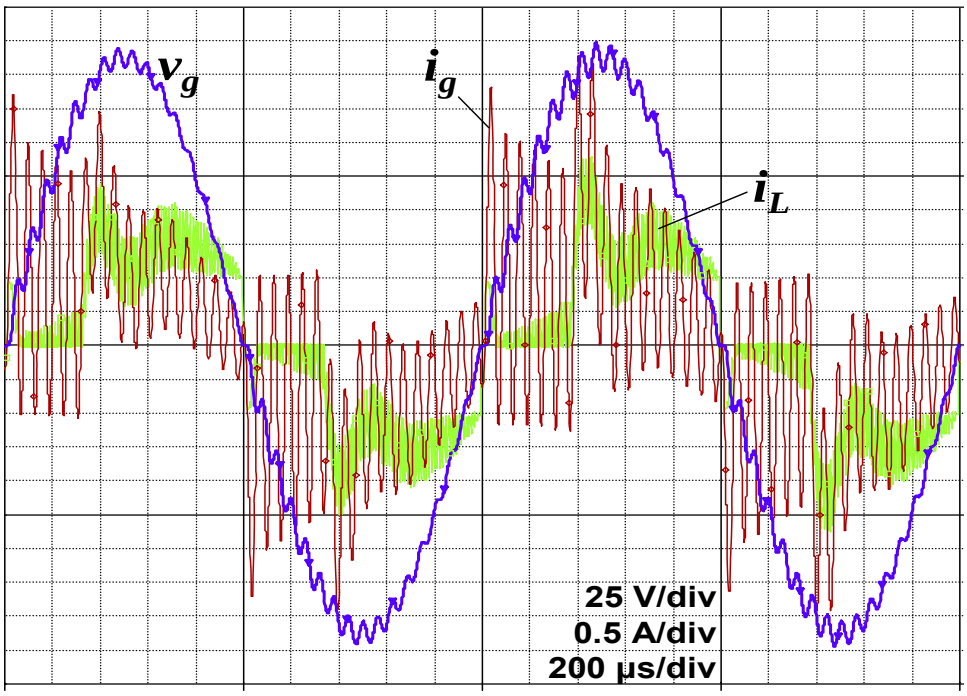


Figure 3.12 Unidirectional PFC converter, an attempt to compensate both inductor current and C_i current.

f_{ac} = 500 Hz, C_i = 1.5 µF, P_o = 100 W.

PFC boost converters may be designed with a filtering capacitor C_{dc} on the dc side of the bridge (Fig. 3.8 and 3.9). C_{dc} is used to reduce excessive noise at the input of the multiplier, although it is not intended to filter the switching ripple entirely. Some of the inductor ripple current can be bypassed by C_{dc}. A small C_{dc} would draw reactive current from the line as if this capacitor were placed on the ac side of the bridge [48]. Since C_{dc} and the inductor are not separated by the bridge, an inductor current with an appropriate lagging phase can be used to cancel the reactive current of C_{dc} (as suggested in [48]). However, there is a limitation on the size of this capacitor. A large C_{dc} would act as an energy storage element for the diode rectifier and may cause "flat spots" and additional distortion of the line current around the zero crossings [17]. Simulations showed that a large C_{dc} causes excessive overshoot at zero crossings and ringing in current waveforms (Fig. 3.13) since the closed-loop system is underdamped [46]. The ringing is excited at zero crossings due to inductor current discontinuity. Using simulation analysis and testing of the converter prototype, it was found that a possible trade-off solution could be to use smaller filtering capacitors both at the ac and dc side of the bridge at the expense of somewhat increased ripple in the line current. Waveforms in Fig. 3.14 were produced with 0.1-μF capacitors instead of the original 1.5-μF ac-side capacitor. The line current ripple is small, the inductor current ripple (measured on the ac side) is reduced, and there is no current phase shift. For a given value of C_{dc}, the LPAC can be designed according to (3.20) and (3.21), where $C_i = C_{dc}$. It follows from these equations that the LPAC network parameters are load-independent and line-frequency

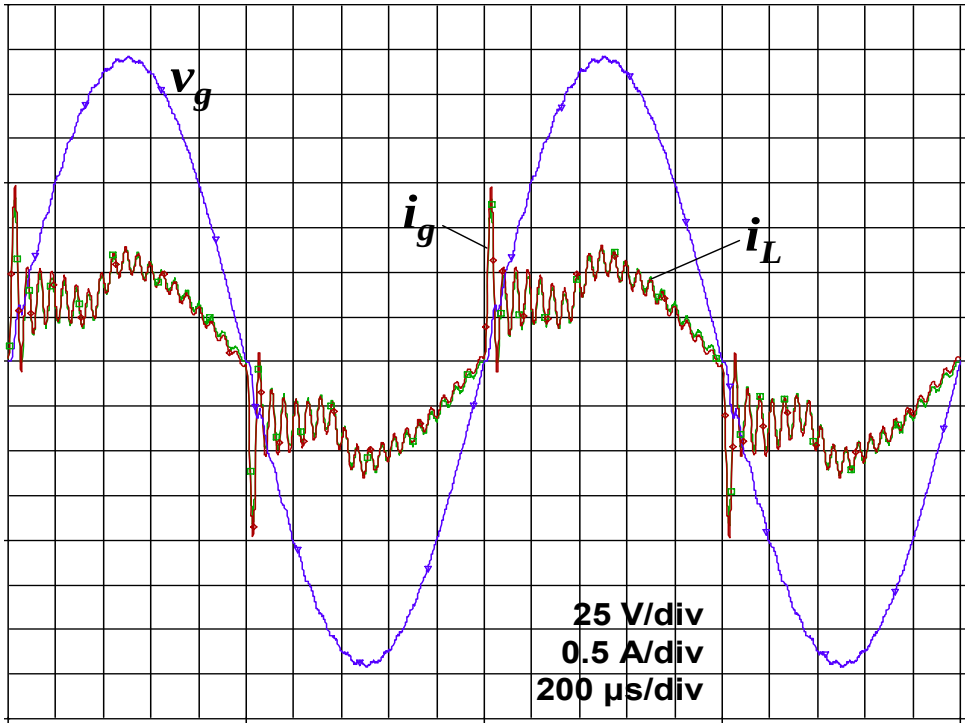


Figure 3.13 Unidirectional PFC converter, LPAC-compensated with a large C_{dc}. f_{ac} = 500 Hz, C_i = 0.1 µF, C_{dc} = 1 µF, P_o = 100 W.

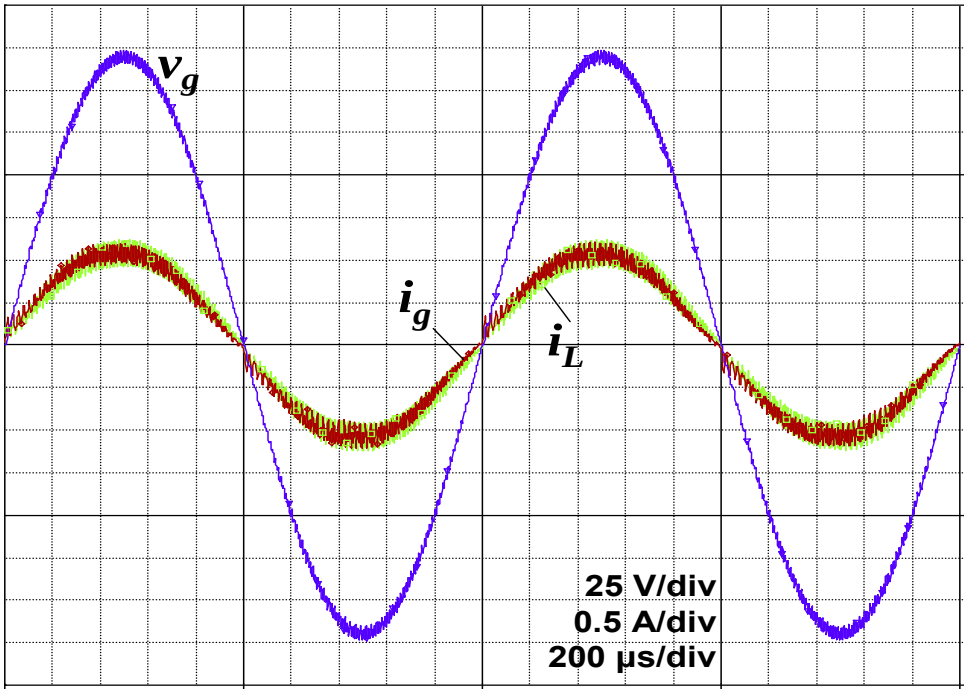


Figure 3.14 Unidirectional PFC converter, LPAC-compensated unity-power-factor operation.

f_{ac} = 500 Hz, C_i = 0.1 µF, C_{dc} = 0.1 µF, P_o = 100 W.

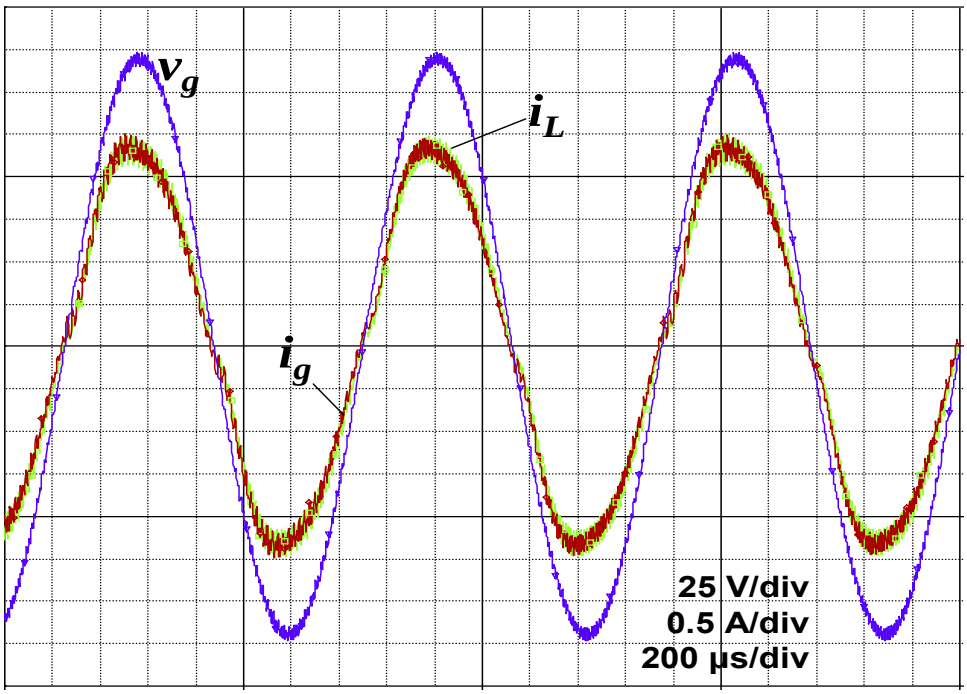


Figure 3.15 Unidirectional PFC converter, LPAC-compensated unity-power-factor operation.

f_{ac} = 800 Hz, C_i = 0.1 µF, C_{dc} = 0.1 µF, P_o = 200 W.

independent. This is demonstrated in Fig. 3.15 obtained with the same as in Fig. 3.14 converter design operating with a double load at the line frequency of 800 Hz.

3.4 Experimental Results

The unidirectional PFC boost converter prototype used to verify the results in Chapter 2 (Fig. 2.14) was used to verify the simulation results. The experiments confirmed the major features of the waveforms obtained by simulation. Experimental waveforms of the converter operating with a standard controller (Fig. 3.16) and with an LPAC-compensated inductor current (Fig. 3.17) match simulation waveforms in Fig. 3.10 and 3.11 very well. It is noticeable that simulation produced somewhat more oscillatory line current waveforms, while in the experimental setup the oscillations are more damped. This difference is prominent in Fig. 3.12 and 3.18, which demonstrate an attempt to compensate C_i current by introducing a phase lag in the inductor current. Current overshoot at zero crossings in a converter with a large C_{dc} (Fig. 3.13) is prominent in the testing results as well (Fig. 3.19). Fig. 3.20 confirms simulation waveforms obtained with a trade-off choice of filtering capacitors C_i and C_{dc} (Fig. 3.14).

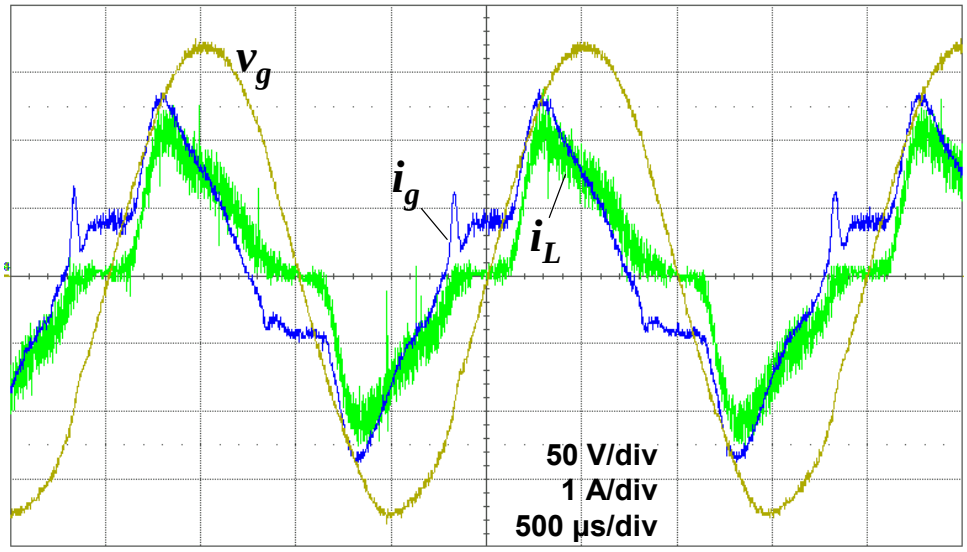


Figure 3.16 Experimental waveforms of the unidirectional PFC converter operation with a standard controller (no LPAC).

f_{ac} = 500 Hz, C_i = 1.5 µF, P_o = 120 W.

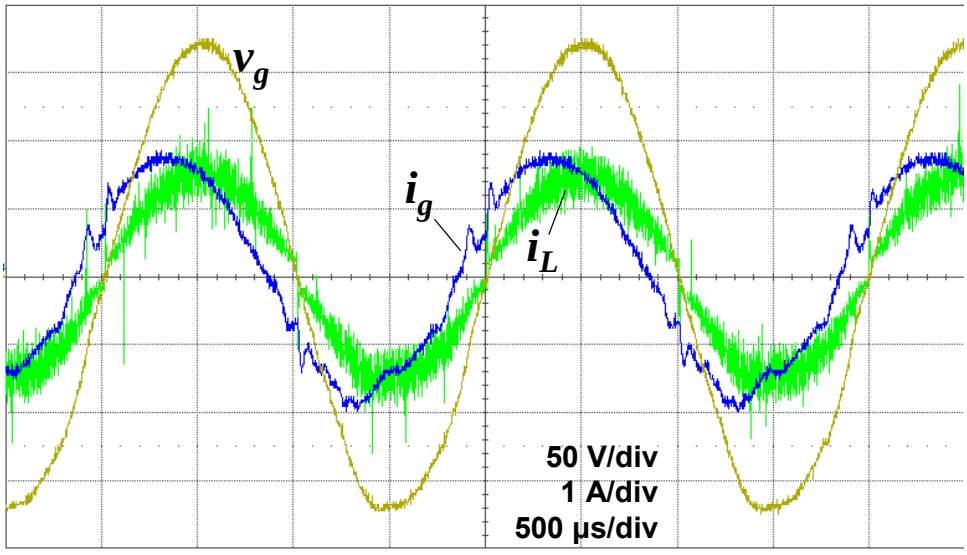


Figure 3.17 Experimental waveforms of the converter with LPAC-compensated inductor current.

f_{ac} = 500 Hz, C_i = 1.5 µF, P_o = 120 W.

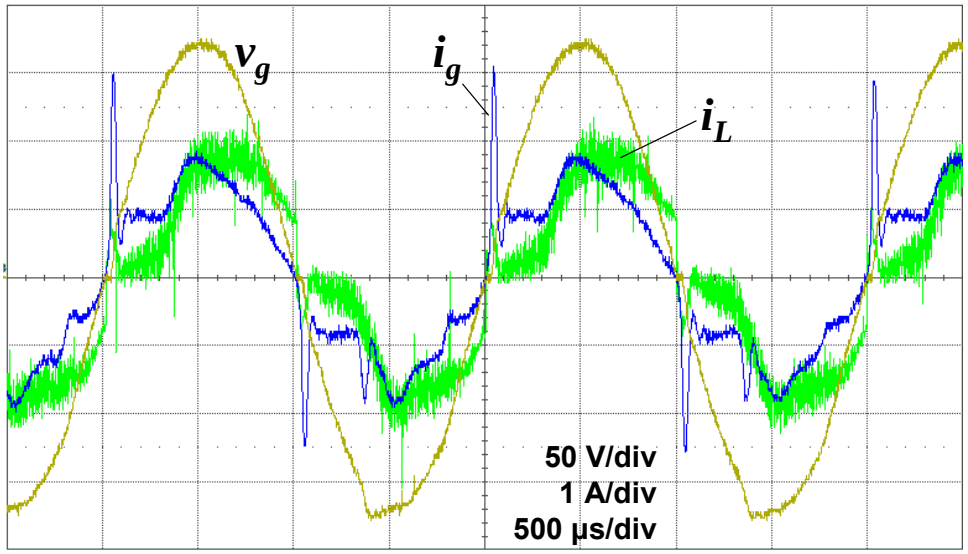


Figure 3.18 Experimental waveforms of the converter, an attempt to compensate both inductor current and C_i current.

f_{ac} = 500 Hz, C_i = 1.5 µF, P_o = 120 W.

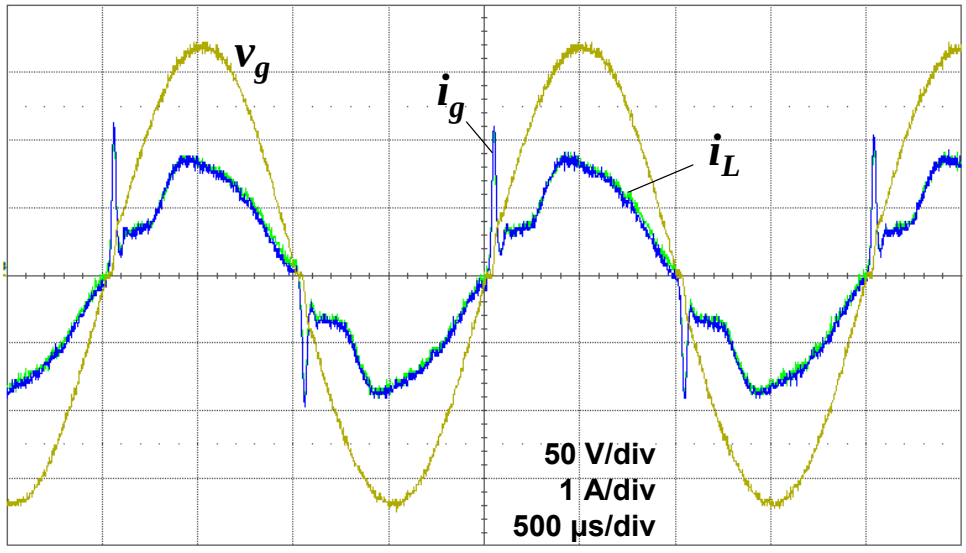


Figure 3.19 Experimental waveforms of the converter, LPAC-compensated with a large C_{dc}.

f_{ac} = 500 Hz, C_i = 0.1 µF, C_{dc} = 1 µF, P_o = 120 W.

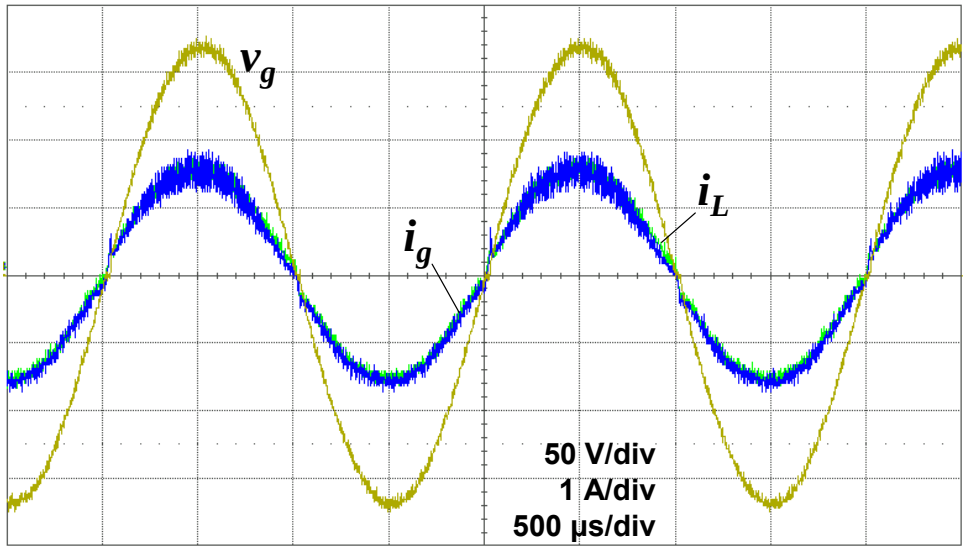


Figure 3.20 Experimental waveforms of the converter, LPAC-compensated, operation with unity power factor.

f_{ac} = 500 Hz, C_i = 0.1 µF, C_{dc} = 0.1 µF, P_o = 120 W.

3.5 Summary

At higher line frequencies such as in certain aircraft power systems (360–800 Hz), reactive current drawn by the input filter capacitor of a PFC converter from the ac line becomes significant, which leads to a decreased power factor even if the inductor current is in phase with the line voltage. This chapter presents a method that allows cancellation of the input capacitor current using the LPAC technique introduced in Chapter 2. Closed-loop dynamic models for the bidirectional and unidirectional PFC boost converters were used to derive conditions for cancellation of the capacitor current and expressions for component values of the LPAC network. The method was verified by computer simulations using PSpice simulation software. Simulation results for the unidirectional converter were confirmed by testing of a converter prototype. Bidirectional converters allow complete, load-invariant, line-frequency-invariant cancellation of the input capacitor current and provide unity power factor under all operating conditions. Unidirectional converters allow substantial reduction but not complete elimination of the switching ripple in the line current. Under these conditions, the converter achieves unity power factor with no phase shift of the line current, with load-invariant and line-frequency-invariant component values of the LPAC network.

Chapter 4

A Single-Phase Multilevel Active-Front-End Converter with Reactive Power Control

4.1 Introduction

Bidirectional active-front-end (AFE) switchmode ac-dc power converters are used in single-phase power systems in order to avoid current harmonics and power factor deterioration resulting from use of diode rectifiers. The AFE converters are designed to draw sinusoidal current from the ac line in phase with the line voltage. The converters employ a bidirectional, usually full-bridge or multilevel, power circuit topology [18]. A multilevel topology reduces voltage stress on semiconductor devices by sharing full voltage between several devices and allows building power converters for voltage ratings of several kilovolts and higher [58], [59]. Average current mode control (ACMC), which uses the line voltage waveform as a reference for the line current [6], can be successfully used in AFE converters to provide operation with unity power factor.

A 20-kW single-phase multilevel active-front-end converter has been developed as an intelligent transformerless alternative to traditional line-frequency rectifiers to boost a medium-voltage ac source (2400 V rms) to a 4-kV dc distribution bus for subsequent

power conversion. The three-level diode-clamped (neutral-point clamped) boost rectifier topology makes the converter suitable for high-voltage power distribution applications. The converter utilizes a form of proposed in this dissertation generalized average-current-mode control scheme (GACMC), which is an improvement upon the traditional ACMC. The GACMC features unity-power-factor operation achieved at a lower than allowed by the ACMC switching frequency, and reactive power control capability. The GACMC incorporates the leading-phase admittance cancellation technique (LPAC) developed for PFC boost converters in Chapter 2. The LPAC allows a relatively low PWM carrier frequency of 10 kHz, appropriate for this power level, without negative consequences of the leading phase shift of the line current as observed in PFC boost converters with a low switching frequency to line frequency ratio as described in earlier chapters. The low switching frequency reduces switching losses and increases converter efficiency. An additional feature of the GACMC is a capability to supply a prescribed amount of reactive power (with leading or lagging current) independently of the dc load power, which allows the converter to be used as a static reactive power compensator in the power system. Possible applications include all-electric ship and similar power systems, residential power distribution networks, etc.

Reactive power source capability is a novel concept for AFE converters, which allows them to some extent to cross the boundary with active filters for power quality improvement [45]. In this capacity, an AFE converter not only draws real power from the line without reducing power factor or creating current harmonics, but is also capable of correcting power factor deteriorated by the presence of reactive loads in the power

system. This type of converter can help to eliminate a static reactive power compensator or an active filter from a power system that the converter is part of depending on the nature of the system.

This chapter presents theoretical development and design of the AFE converter with the features described above. Dynamic modeling of the current control loop has been used to determine possibility of reactive power control, and a simple practical implementation of a reactive power controller has been proposed. A scaled-down converter prototype was used to verify the concept and demonstrated good agreement with theory and simulation results.

4.2 Converter Modeling And Control

4.2.1 Modeling and Control for Unity Power Factor

The converter employs a multilevel boost rectifier topology (Fig. 4.1) and multilevel sinusoidal PWM technique with triangular carriers. The converter control structure is based on traditional two-loop control for PFC boost converters [6], with an outer dc voltage-regulating control loop providing reference to an inner current-shaping loop. The power stage line-to-current and control-to-current transfer functions are derived from the converter average model in Fig. 4.2. Using the modeling approach from Chapter 2, we assume that the dc link capacitors are large enough, which results in constant

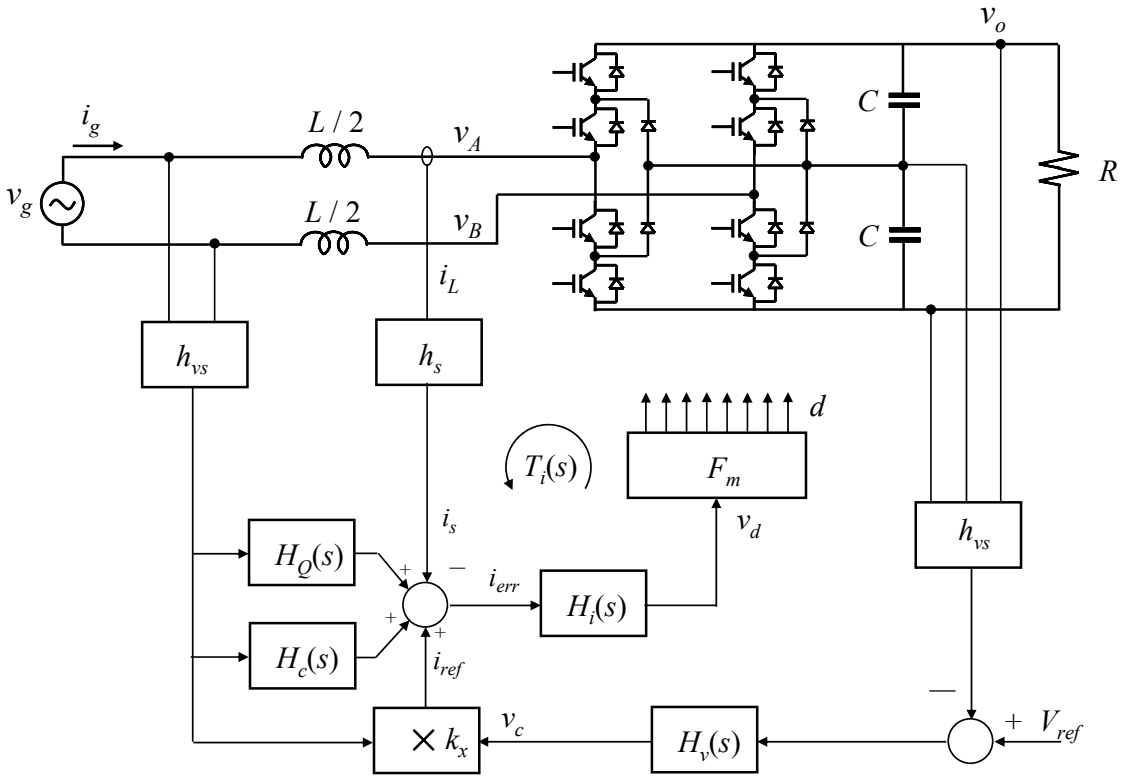


Figure 4.1 The AFE converter and its control system.

H_i—current loop compensator, H_v—voltage loop compensator, F_m—modulator gain, k_x—multiplier gain, h_s—current sensor gain, h_{vs}—voltage sensor gain.

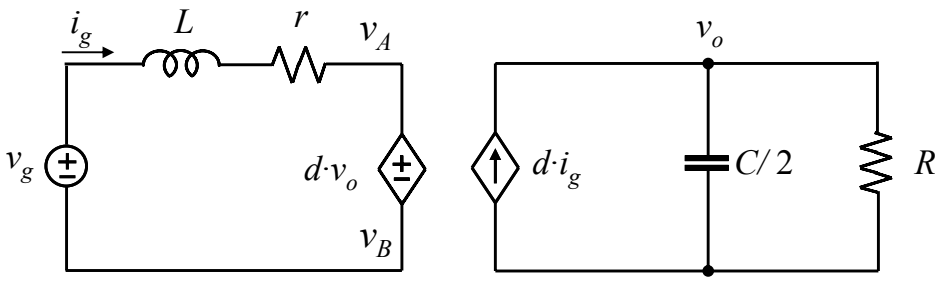


Figure 4.2 Average model of the AFE converter.

values for dc voltage V_o and the voltage loop compensator output V_c in Fig. 4.1. Then, the line current equation is

$$i_g(s) = \frac{1}{r + s\,L}\, v_g(s) - \frac{V_o}{r + s\,L} d(s), \tag{4.1}$$

from which the power stage transfer functions are

$$G_{iv}(s) = \frac{1}{r + s\,L} \quad \text{and} \quad G_{id}(s) = -\frac{V_o}{r + s\,L}. \tag{4.2}$$

The voltage- and current-loop compensators are PI-type controllers. The principles of voltage loop controller design for a PFC boost converter are well known [6]; the focus of this research is on the current loop control. The current loop compensator has its zero placed at or near the loop crossover frequency [6] and has a transfer function:

$$H_i(s) = \frac{\omega_i \left(1 + \dfrac{s}{\omega_z}\right)}{s\left(1 + \dfrac{s}{\omega_p}\right)}, \tag{4.3}$$

where ω_i, ω_z, and ω_p are the current loop compensator gain, zero, and pole, respectively. The converter duty cycle is determined as

$$d = F_m\, v_{da}, \qquad F_m = \frac{1}{V_{tr}}, \tag{4.4}$$

where F_m is the modulator gain, v_{da} is the modulator input signal, and V_{tr} is the PWM carrier magnitude. This is not a duty cycle of a particular switch but rather a variable used in the average model to describe operation of the power stage as a whole. Compared with the model for a single-switch PFC boost converter developed in Chapter 2, the transfer function $G_{id}(s)$ has a negative sign, which requires the current loop compensator output signal to be inverted before it enters the PWM modulator. Otherwise, the models are mathematically identical, and all the modeling results obtained in Chapter 2 apply to this converter.

The converter operates in continuous current mode with ACMC. The LPAC technique described above is used to reduce the current loop bandwidth requirement (and the corresponding switching frequency). Traditional ACMC scheme allows the converter to draw sinusoidal line current in phase with the line voltage provided that the current loop bandwidth is high enough (around 10 kHz [6]), which requires a switching frequency in excess of 50 kHz; too high for a converter with this power rating. A lower switching frequency and bandwidth in a single-switch PFC boost converter would result in a leading phase of the line current and a zero-crossing distortion of the current waveform. While a bidirectional AFE converter would not have a zero-crossing distortion under these conditions, the line current would still have a load-dependent leading phase and would make unity-power-factor operation impossible. The converter uses the GACMC to overcome this problem by adding an LPAC network with transfer function $H_c(s)$ to the traditional ACMC scheme:

$$H_c(s) = -\frac{s}{V_o F_m h_{vs} \omega_i \left(1 + \frac{s}{\omega_z}\right)}. \tag{4.5}$$

As suggested in Chapter 2, the LPAC network is realized as a C_c-R_c network (Fig. 4.3), where

$$C_c = \frac{C_{fp} + C_{fz}}{V_o F_m h_{vs}}, \quad \text{and} \quad R_c = \frac{1}{C_c \omega_z}. \tag{4.6}$$

4.2.2 Reactive Power Control

Another feature of the GACMC is a reactive power controller ($H_Q(s)$ in Fig. 4.1), which introduces a specified amount of phase shift (leading or lagging) in the line current waveform independently of the dc load. Therefore, the converter can supply a specified amount of reactive power (capacitive or inductive) to the power system and can be used as a static reactive power compensator in addition to its intended use as an AFE converter.

As shown above, the closed-loop input admittance of a PFC boost converter with LPAC can be viewed as a sum of partial admittances:

$$Y(s) = Y_1(s) + Y_2(s) + Y_3(s), \tag{4.7}$$

where $Y_1(s)$ is the leading-phase component caused by the line voltage, $Y_2(s)$ is the current reference component responsible for the real power transfer, and $Y_3(s)$ is the LPAC component, which cancels $Y_1(s)$ at the line frequency. The reactive power

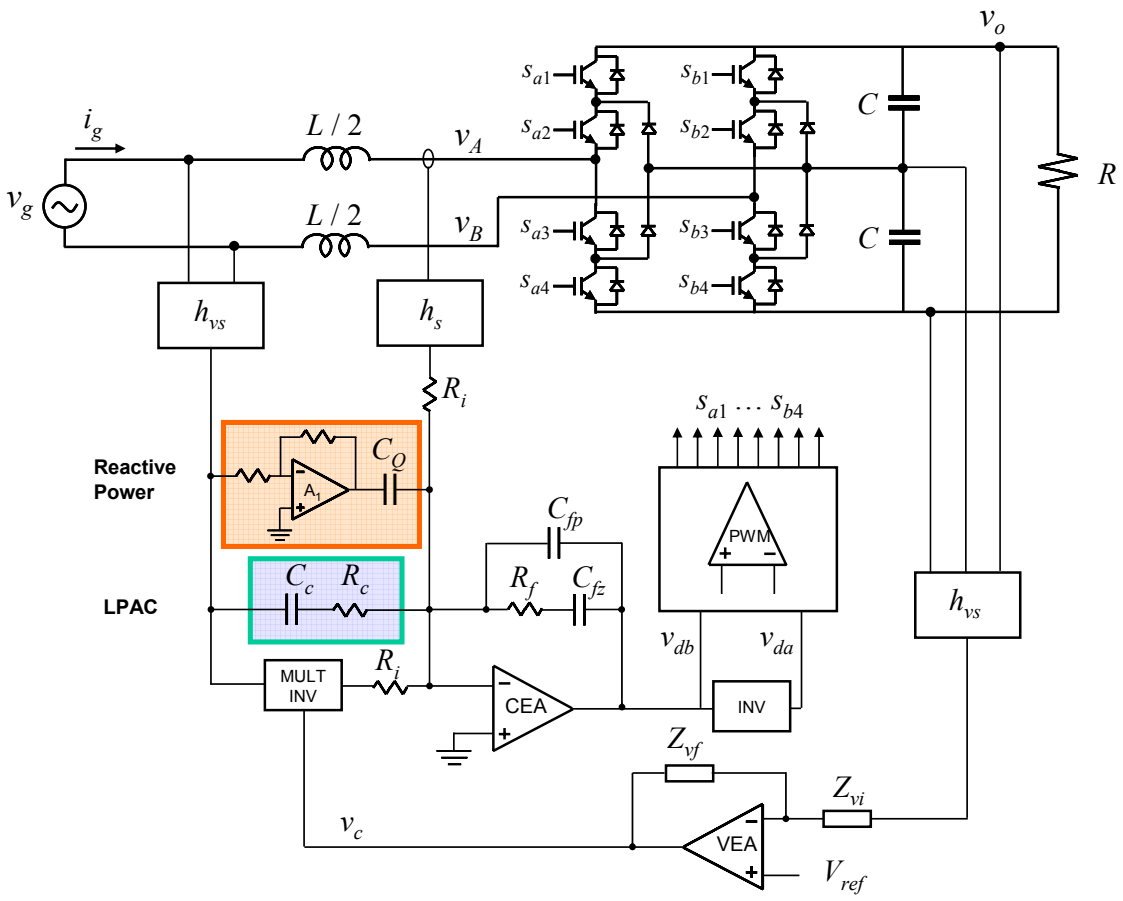


Figure 4.3 Implementation of the AFE converter control system.

controller in the GACMC scheme adds another input admittance component $Y_Q(s)$ (Fig. 4.4) such that

$$Y(s) = Y_1(s) + Y_2(s) + Y_3(s) + Y_Q(s)\,. \tag{4.8}$$

The reactive power controller allows emulating a capacitance C_{YQ} connected to the ac line in order to produce reactive power Q if

$$Y_Q(s) = s\,C_{YQ}\,, \qquad C_{YQ} = \frac{Q}{2\pi\, f_g\, V_g{}^2}\,. \tag{4.9}$$

Alternatively, an inductance L_{YQ} connected to the ac line is emulated if

$$Y_Q(s) = \frac{1}{s\,L_{YQ}}\,, \qquad L_{YQ} = \frac{V_g{}^2}{2\pi\, f_g\, Q}\,. \tag{4.10}$$

In both cases, the reactive power produced is

$$Q = V_g{}^2 \left|Y_Q\right|. \tag{4.11}$$

Because $Y_3(s)$ cancels $Y_1(s)$ at the line frequency, the effective input admittance of the converter is

$$Y(s) = \frac{P_g}{V_g{}^2} + Y_Q(s)\,, \tag{4.12}$$

where P_g is the real power drawn from the line, and $Y_Q(s)$ in the form of (4.9) or (4.10) determines the reactive power according to (4.11).

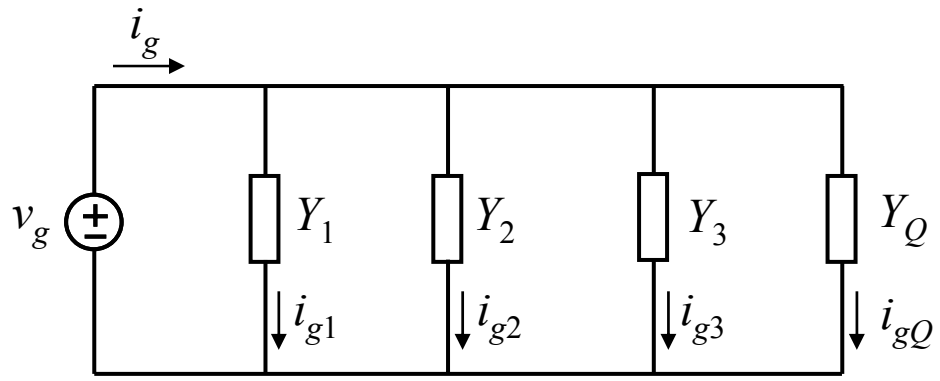


Figure 4.4 Input admittance components of the AFE converter with reactive power control.

Fig. 4.5 shows the PFC boost converter current loop control diagram with added reactive power controller $H_Q(s)$. An alternative implementation of the reactive power controller in the form of $H_{Q1}(s)$ is possible but will not be discussed here. From Fig. 4.5,

$$Y(s) = \frac{i_g(s)}{v_g(s)} = \frac{G_{iv}}{1+T_i} + \frac{G_{id}\,F_m\,H_i}{1+T_i} k_x V_c\, h_{vs} + \frac{G_{id}\,F_m\,H_i}{1+T_i} H_c\, h_{vs} + \frac{G_{id}\,F_m\,H_i}{1+T_i} H_Q\, h_{vs}, \quad (4.13)$$

where T_i is the current loop gain:

$$T_i = G_{id}\,F_m\,H_i\,h_s. \quad (4.14)$$

Similarly to the analysis in Chapter 2, the first and the third terms in (4.13) cancel each other, and the second term accounts for the real power drawn from the line. Then, below the current loop crossover frequency,

$$H_Q(s) = \frac{h_s}{h_{vs}} Y_Q(s). \quad (4.15)$$

Considering (4.9), in order to emulate a capacitance C_{YQ},

$$H_Q(s) = \frac{h_s C_{YQ}}{h_{vs}} s. \quad (4.16)$$

The reactive power controller is implemented as an h_Q-C_Q network (Fig 4.3), where h_Q is gain (positive or negative) of amplifier A_1, which can be configured as inverting or noninverting. From Fig. 4.1 and 4.3,

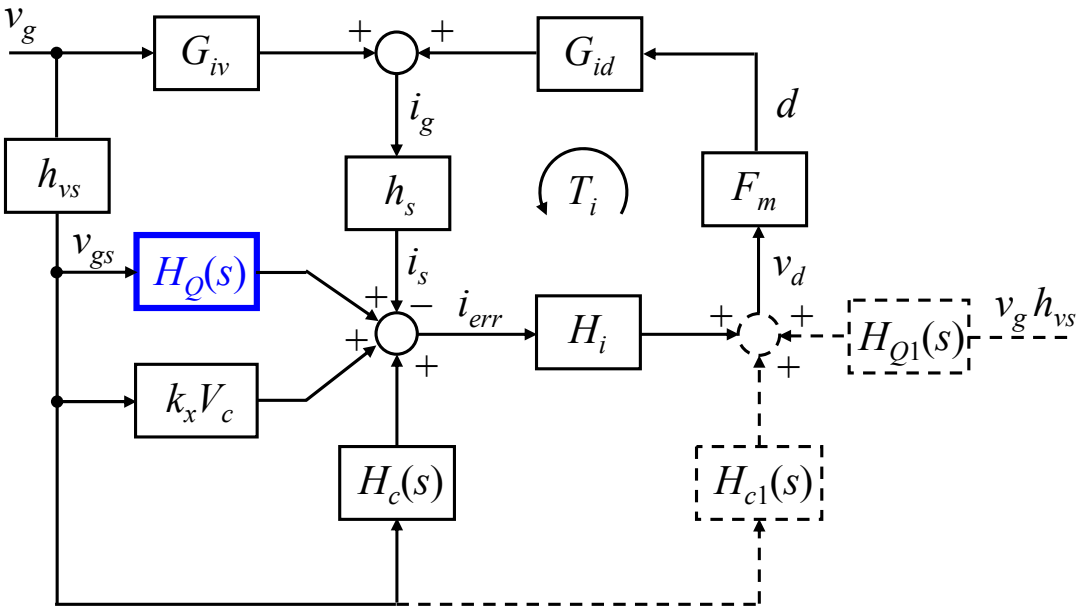


Figure 4.5 AFE converter current loop control diagram with alternative implementations of the reactive power controler.

$$H_Q(s)\,H_i(s)=\frac{v_d(s)}{v_{gs}(s)}=-\frac{h_Q\,C_Q}{C_{fp}+C_{fz}}\,\frac{1+\,s/\omega_z}{1+\,s/\omega_p}\,. \tag{4.17}$$

Taking into account (4.3), (4.9), and (4.16), we obtain:

$$H_Q(s)=-\frac{h_Q}{\omega_i}\,\frac{C_Q}{C_{fp}+C_{fz}}\,s\,, \tag{4.18}$$

$$h_Q C_Q=-\frac{h_s C_{YQ}\,\omega_i}{h_{vs}}\left(C_{fp}+C_{fz}\right), \tag{4.19}$$

$$h_Q C_Q=-\frac{Q\,h_s\,\omega_i\left(C_{fp}+C_{fz}\right)}{V_g{}^2\,2\pi\,f_g\,h_{vs}}\,. \tag{4.20}$$

Amplifier A_1 (Fig. 4.3) has to be inverting in order to emulate capacitance C_{YQ} (reactive power Q with leading current phase).

At the line frequency f_g, effective input admittance of the converter emulating capacitance C_{YQ}, according to (4.12), is

$$Y(j\,2\pi\,f_g)=\frac{P_g}{V_g{}^2}+j\,2\pi\,f_g\,C_{YQ}\,. \tag{4.21}$$

If amplifier A_1 is configured as noninverting, the sign of $H_Q(s)$ will change, and so will the sign of reactive part of the input admittance. According to (4.13) and (4.16),

$$H_Q(s)=-\frac{h_s C_{YQ}}{h_{vs}}\,s\,, \tag{4.22}$$

$$Y(j2\pi f_g) = \frac{P_g}{V_g^{\,2}} - j2\pi f_g C_{YQ}\,. \tag{4.23}$$

The converter will be operating with reactive power of the same magnitude but with a lagging reactive current, thus emulating an inductor connected to the ac line. Effective value of the inductance is obtained from the equation:

$$2\pi f_g C_{YQ} = \frac{1}{2\pi f_g L_{YQ}}, \tag{4.24}$$

from which

$$L_{YQ} = \frac{1}{(2\pi f_g)^2 C_{YQ}}\,. \tag{4.25}$$

4.3 Converter Design

Fig. 4.3 and 4.6 show details of the converter implementation. The control system relies on voltage and current sensors h_{vs} and h_s to sense the line voltage, line current, and the dc voltage (the sensor gains for v_g and v_o can be different). The voltage loop compensator (VEA) adjusts the magnitude of the line current through the multiplier (MULT) in order to maintain the required dc voltage as load conditions change. The current reference signal derived from the line voltage waveform and adjusted in

magnitude by the voltage control loop is supplied through an inverting output of the multiplier to the negative input of the current loop amplifier (CEA). Other inputs of CEA come from the current sensor h_s, the LPAC network C_c-R_c, and the reactive power controller A_1-C_Q.

The current loop amplifier and the inverting buffer (INV) provide input signals v_{da} and v_{db} for multilevel PWM. The modulator uses a set of comparators and digital logic to produce gate driving signals $s_{a1}\ldots s_{b4}$ from the input signals v_{da} and v_{db} and PWM carrier signals v_{tr1} and v_{tr2}, as shown in Fig. 4.6 and Table 4.1. The gate driving signals are carried to the respective device gate drivers in the high-voltage part of the converter through fiber-optic links.

The converter design includes a number of protection functions such as power device overcurrent and overtemperature protection, dc link overvoltage and undervoltage protection, and dc link voltage imbalance protection.

Fig. 4.7 and 4.8 show simulated waveforms of the converter operating with 20 kW real power and 10 kVA reactive power with leading and lagging phase of the current, respectively. The reactive power is controlled independently of the real power, which is determined by the converter load.

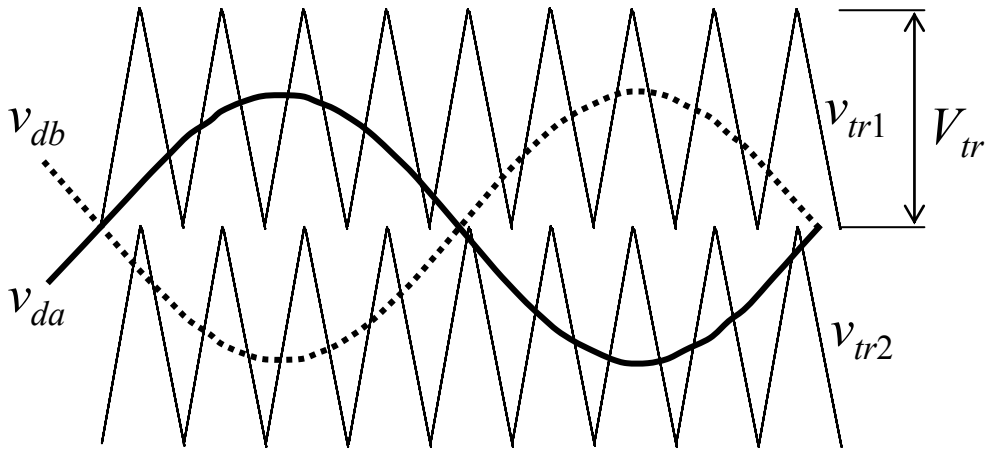


Figure 4.6 Multilevel PWM modulator input and carrier signals are used to produce gate driving signals.

TABLE 4.1 GATE DRIVING SIGNALS

s_{a1}	$v_{da} - v_{tr1}$
s_{a2}	$v_{da} - v_{tr2}$
s_{a3}	$\overline{v_{da} - v_{tr1}}$
s_{a4}	$\overline{v_{da} - v_{tr2}}$
s_{b1}	$v_{db} - v_{tr1}$
s_{b2}	$v_{db} - v_{tr2}$
s_{b3}	$\overline{v_{db} - v_{tr1}}$
s_{b4}	$\overline{v_{db} - v_{tr2}}$

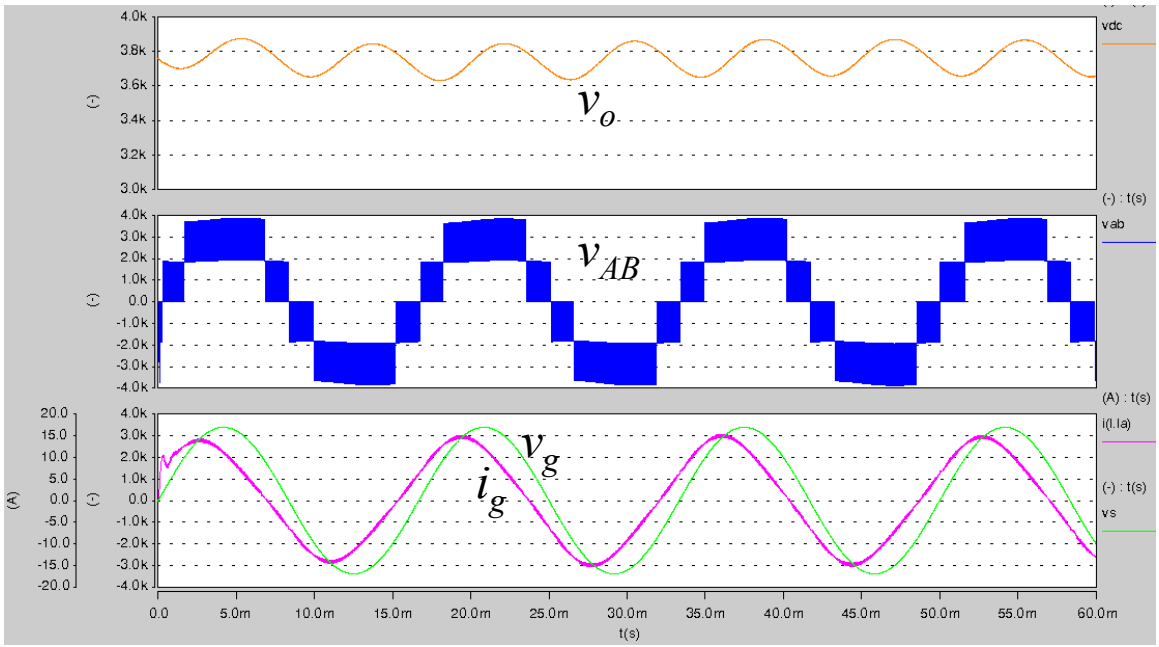


Figure 4.7 The AFE converter operation with 20 kW real power and 10 kVA reactive (leading phase) power.

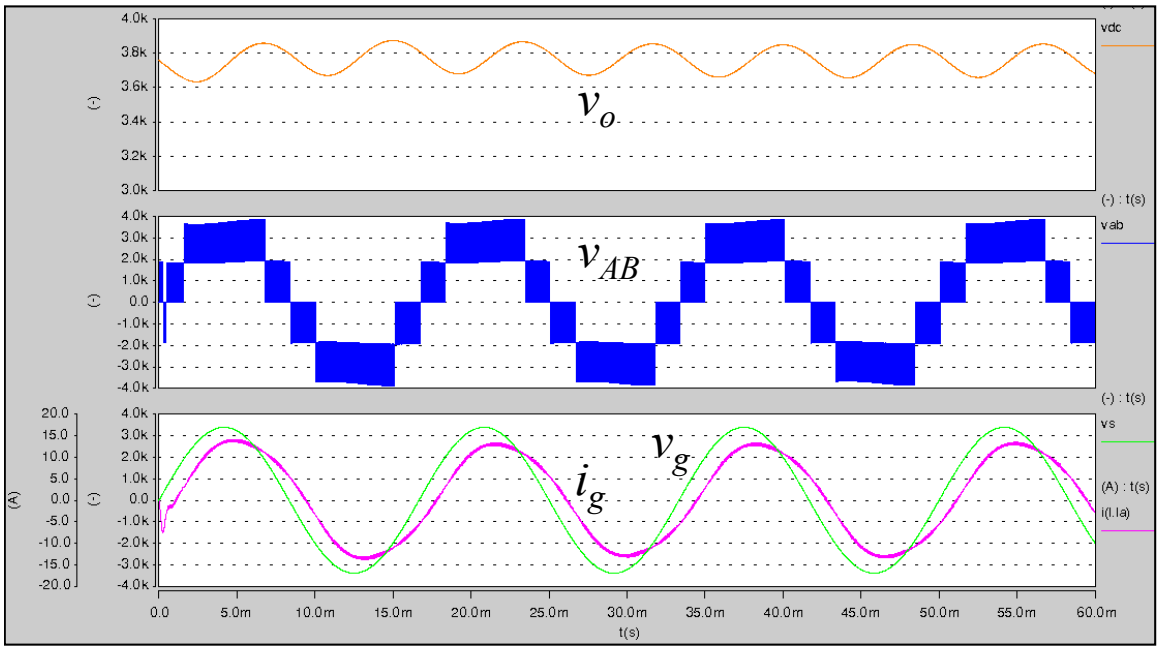


Figure 4.8 The AFE converter operation with 20 kW real power and 10 kVA reactive (lagging phase) power.

4.4 Experimental Results

A scaled-down 240-V ac input, 376-V dc output version of the converter shown in Fig. 4.9 was used to verify the concepts presented in this chapter (converter parameters are given in the Appendix). The prototype was implemented using low-voltage insulated-gate bipolar-junction transistors (IGBTs). A separate low-voltage control board provided gating signals to the IGBTs through fiber optic links. The laboratory setup was powered from the utility grid, and a load bank was used as a dc load for the converter. Experiments showed effectiveness of the LPAC in removing the line current phase lead and, thus, ensuring unity-power-factor operation of the converter. Without the LPAC, the current phase lead is observed (Fig. 4.10). The current phase lead becomes more prominent at lower load levels, which follows from analysis in Chapter 2. The LPAC removes the current phase lead and ensures unity-power-factor operation of the converter at all load levels (Fig. 4.11). The reactive power controller was used to introduce a phase shift of the line current of up to 30°, thus producing reactive power of 0.86 kVA, which is 58% of the real power processed by the converter (1.44 kW). The converter was used to generate reactive power with both leading (Fig. 4.13) and lagging (Fig. 4.14) phase of the line current. Operation with reactive power does not cause any adverse effects on processing of the real power and is a fully transparent process for the load. However, semiconductor devices and passive power components have to be rated for the line current including its reactive component if the converter is to be used for reactive power generation. The experimental waveforms showed good agreement with theoretical predictions and simulation results.

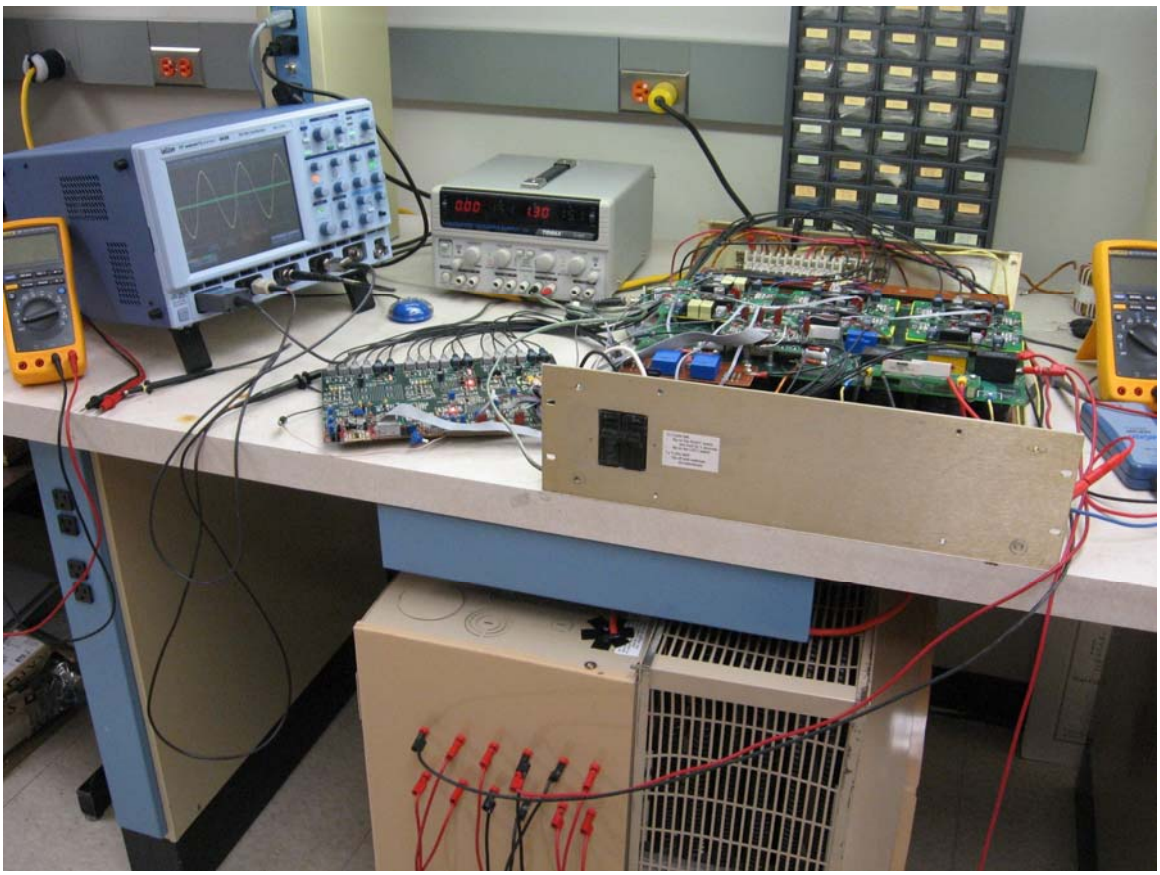


Figure 4.9 Experimental setup used to verify the reactive power control principle.

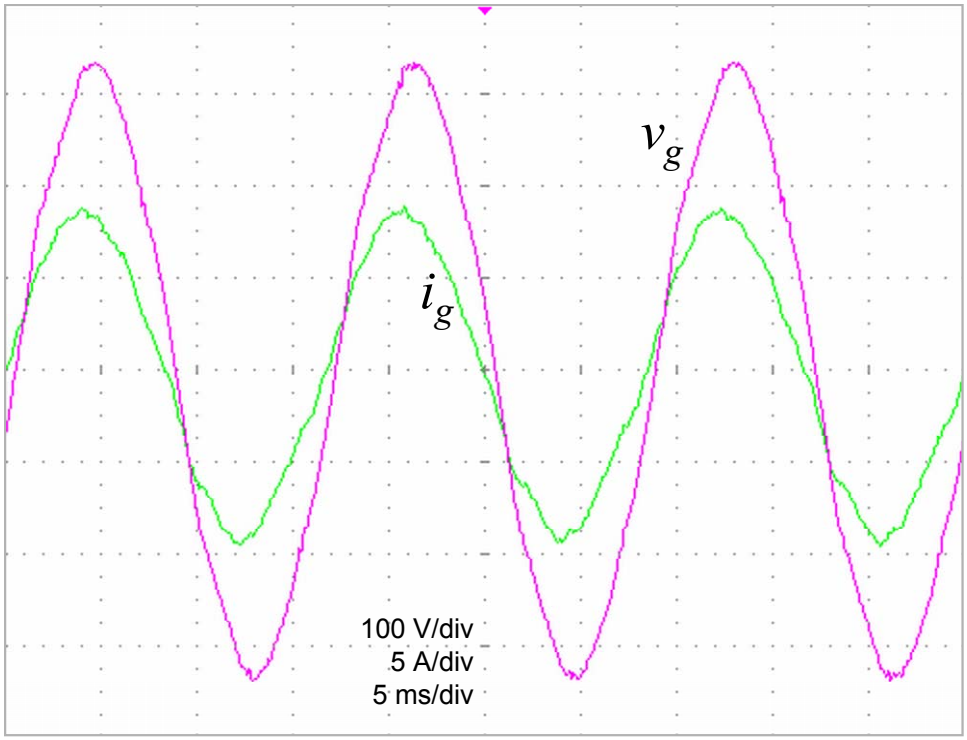


Figure 4.10 The AFE converter operating without LPAC has a leading phase of the line current.

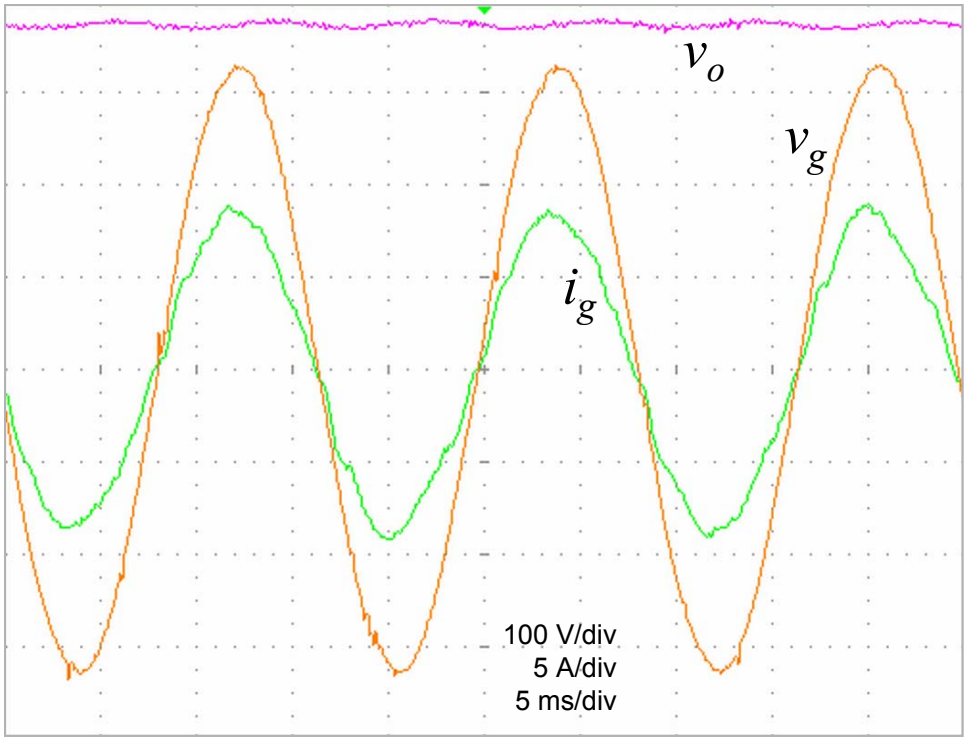


Figure 4.11 Unity-power-factor operation of the converter operating with LPAC enabled.

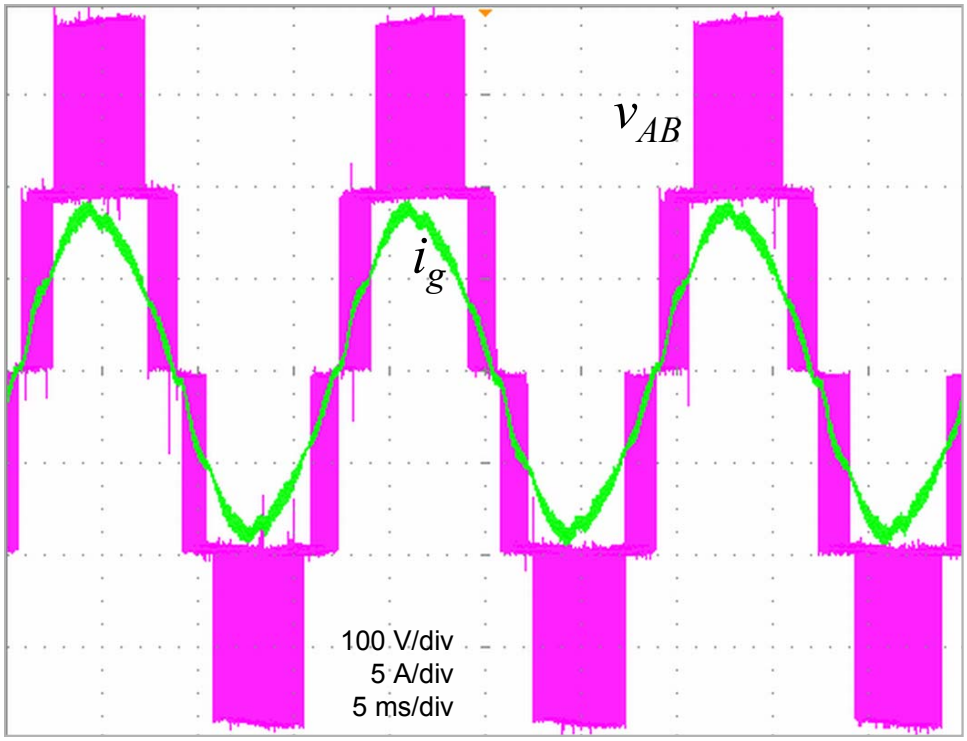


Figure 4.12 Current and voltage waveforms of the converter operating with unity power factor.

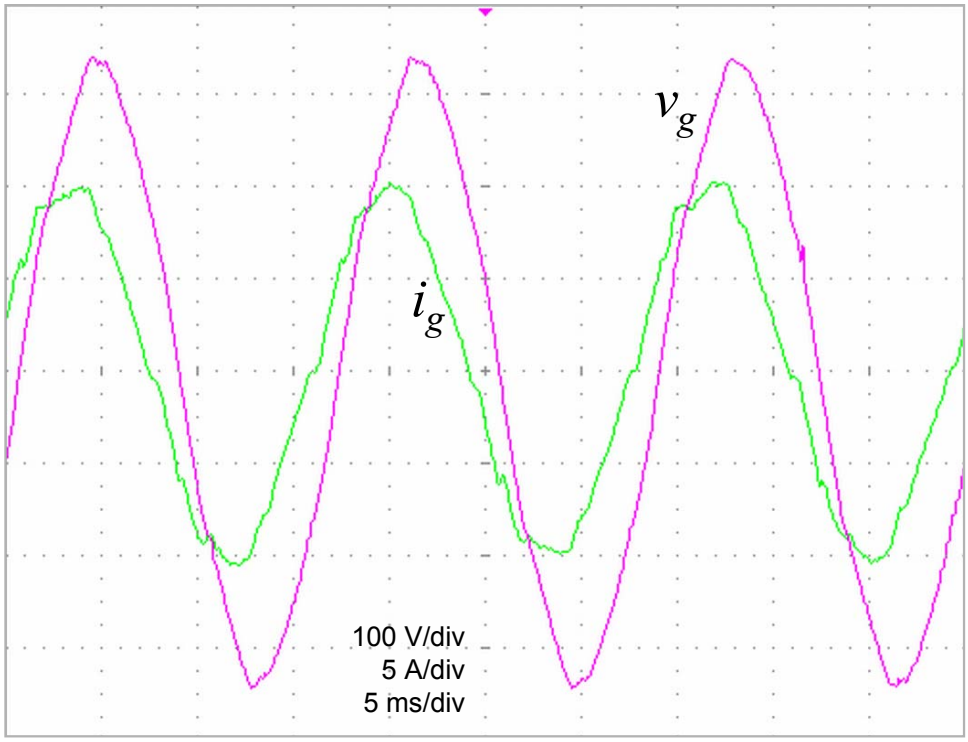


Figure 4.13 Converter operation with 1.44 kW real power and 0.86 kVA reactive power (leading phase).

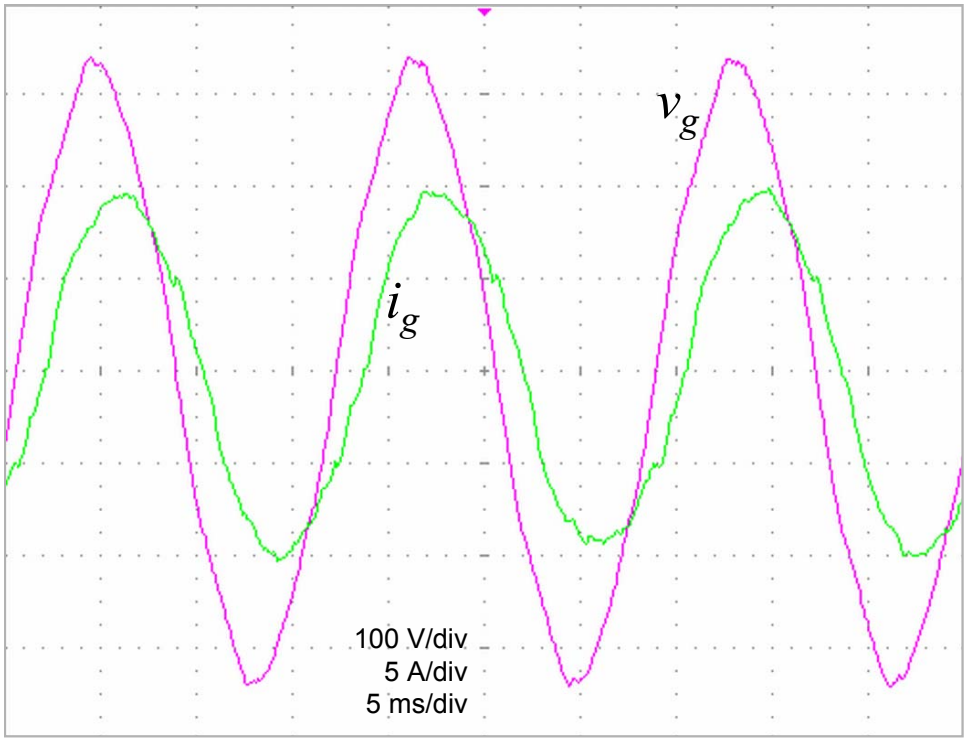


Figure 4.14 Converter operation with 1.44 kW real power and 0.86 kVA reactive power (lagging phase).

4.5 Summary

This chapter presents development of a 20-kW single-phase multilevel active-front-end converter as a high-performance alternative to traditional line-frequency rectifiers. The converter uses a newly introduced generalized average-current-mode-control scheme, which offers advanced features such as the LPAC compensation and the reactive power control. The LPAC method, developed earlier for single-phase PFC boost converters, allows a low 10-kHz switching frequency, which reduces switching losses and increases converter efficiency, without the line current phase shift inherent to the traditional average-current-mode control when a low switching frequency is used. The newly proposed reactive power controller allows the converter to be used as a static reactive power compensator in the power system independently of its function as an ac-dc converter. This work presents theoretical basis for reactive power control using dynamic modeling of the current loop and a simple implementation of the reactive power controller. This method does not require extra power components or modifications of the converter power circuit and achieves reactive power control entirely by means of the controller action as part of the GACMC. The concepts presented in this chapter were verified by testing of a converter prototype, which successfully demonstrated both unity-power-factor operation and reactive power control capability. The multilevel topology and low switching frequency operation are well suited for a medium-voltage (2.4 kV) or distribution-system-voltage (13.8 kV) level converter, which can be implemented with high-voltage IGBTs or high-voltage silicon carbide devices.

Chapter 5

Reactive Power Control Realizations in Single-Phase Active-Front-End Converters

5.1 Introduction

Single-phase active-front-end (AFE) ac-dc converters provide unity power factor with low harmonic distortions and can be used in residential power distribution networks and most home appliances [18]. The two-loop control scheme developed for PFC boost converters operating in continuous current conduction mode (CCM) with average current mode control (ACMC) can be successfully used in AFE converters as discussed in Chapter 4. This control structure, with an outer voltage-regulating loop providing a reference for an inner current-shaping loop [6], can be used to control reactive power processed by the converter by creating a phase shift between the line voltage and line current if the power stage topology allows that. PFC boost converters are limited to one-quadrant operation. They operate with unity power factor but do not allow a phase shift and, therefore, are not suitable for reactive power control. The AFE converters use the full-bridge topology capable of four-quadrant operation, which allows a phase shift and reactive power flow.

This chapter describes the ways to add a reactive power controller to the current control loop such that the converter can generate a specified amount of reactive power along with its intended use as an active-front-end. The reactive power controller introduces a phase shift, leading or lagging, into the line current, thus emulating a capacitor or an inductor connected to the ac line. Therefore, the converter can be used as a reactive power compensator, at the same time supplying dc power to the load. Reactive power source capability is a novel concept for AFE converters, which allows them to some extent to cross the boundary with active filters for power quality improvement [45]. A particular form of reactive power control for a multilevel AFE converter has been described in Chapter 4. In this chapter, we examine other possible reactive power control realizations in a systematic way, along with their merits and limitations, including susceptibility to the ac line noise. A closed-loop dynamic model of the converter was used to derive a variety of possible forms of the reactive power controller and analyze their potential for use in different applications. Experimental data were obtained to verify the reactive power control concept and showed good agreement with theoretical predictions and simulation results.

5.2 Reactive Power Control

The AFE converter is based on the full-bridge topology (Fig. 5.1) operating in CCM with ACMC and utilizing the two-loop control structure developed for PFC boost

converters [6]. A multilevel topology can be an option for high-voltage applications. In this control scheme, the outer dc voltage-regulating loop adjusts the magnitude of the sine wave derived from the line voltage and provided as a reference to the inner current-shaping control loop. The system modeling is based on an assumption that the dc link capacitance C is high enough such that the dc voltage ripple is small as it is in practical implementations. Therefore, the dc link voltage V_o and the voltage loop controller output V_c can be considered constant values in steady-state operation. Then, the power stage transfer functions for the full-bridge converter are

$$G_{iv}(s) = \frac{1}{r + sL} \quad \text{and} \quad G_{id}(s) = \frac{2V_o}{r + sL}, \tag{5.1}$$

where r is an equivalent resistance of the current path. The voltage- and current-loop compensators are PI-type controllers. The voltage loop control is designed according to the guidelines for PFC boost converters [6]. The current loop compensator has a transfer function:

$$H_i(s) = \frac{\omega_i\left(1 + \frac{s}{\omega_z}\right)}{s\left(1 + \frac{s}{\omega_p}\right)}, \tag{5.2}$$

where ω_i, ω_z, and ω_p are the current loop compensator gain, zero, and pole, respectively. The zero is placed at or near the current loop crossover frequency.

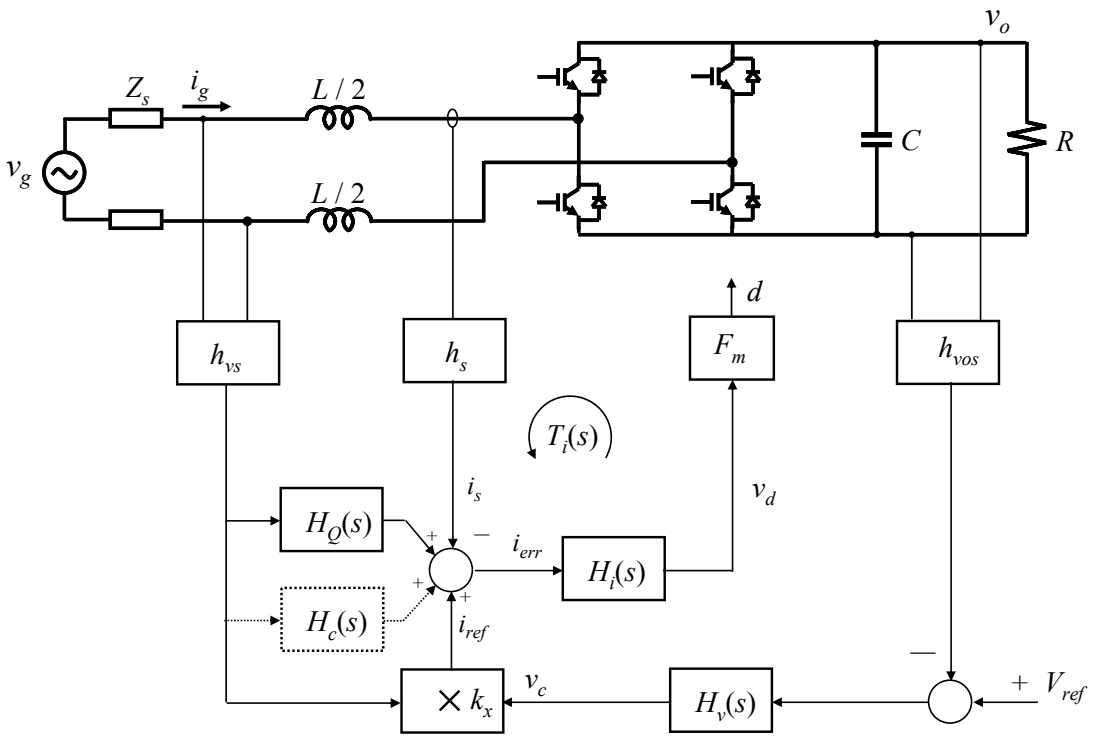


Figure 5.1 AFE converter control system.

H_i—current loop compensator, H_v—voltage loop compensator, H_Q—reactive power controller, H_c—LPAC controller, F_m—PWM modulator gain, k_x—multiplier gain, h_s—current sensor gain, h_{vs}—voltage sensor gain

If the current loop bandwidth is not high enough with respect to the line frequency (much less than 10 kHz for the utility line frequency of 60 Hz [6]), the line current will have a leading phase shift, which is a property of this control scheme, as discussed in previous chapters. This phase shift can be eliminated with an optional leading-phase admittance cancellation (LPAC) network $H_c(s)$ or $H_{c1}(s)$ (Fig. 5.2).

Reactive power control is achieved by injecting a control signal from the reactive power controller $H_Q(s)$ into the current loop at the summing junction of the error amplifier (Fig. 5.1). From the current loop control diagram (Fig. 5.2), the closed-loop input admittance of the converter is

$$Y(s) = \frac{i_g(s)}{v_g(s)} = \frac{G_{iv}}{1+T_i} + \frac{G_{id}\,F_m\,H_i}{1+T_i} k_x V_c\, h_{vs} + \frac{G_{id}\,F_m\,H_i}{1+T_i} H_c\, h_{vs} + \frac{G_{id}\,F_m\,H_i}{1+T_i} H_Q\, h_{vs}, \quad (5.3)$$

where T_i is the current loop gain:

$$T_i = G_{id}\,F_m\,H_i\,h_s. \quad (5.4)$$

The third term in (5.3) is designed to cancel the first term, and the second term determines the real power drawn from the ac line. The fourth term is admittance created by the reactive power controller $H_Q(s)$. Below the crossover frequency of the current loop, this term reduces to

$$Y_Q(s) = \frac{h_{vs}}{h_s} H_Q(s), \quad (5.5)$$

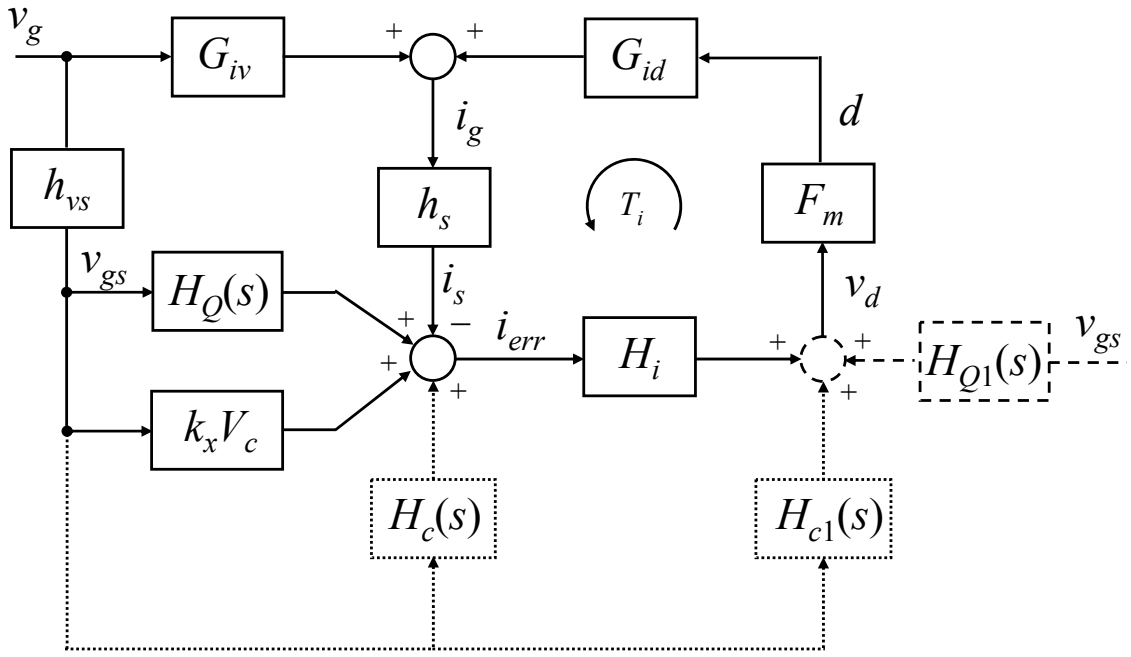


Figure 5.2 AFE converter current loop control diagram with alternative implementations of reactive power control.

where $Y_Q(s)$ is the admittance component created by the reactive power controller according to the reactive power command. In order to produce leading-phase reactive power Q, the reactive power controller has to emulate a capacitance connected to the ac line terminals so that $Y_Q(s) = sC_{YQ}$. The capacitance value should be

$$C_{YQ} = \frac{Q}{V_g^{\,2}\, 2\pi f_g}. \tag{5.6}$$

Then,
$$H_Q(s) = \frac{h_s}{h_{vs}} C_{YQ} s. \tag{5.7}$$

Below the crossover frequency, (5.3) reduces to

$$Y(s) = \frac{P_g}{V_g^{\,2}} + C_{YQ}\, s. \tag{5.8}$$

Fig. 5.3 shows $Y(s)$ of the converter operating with real power of 1.3 kW and leading-phase reactive power (solid line). At 60 Hz, the line current has a leading phase shift of 37°, and the reactive power is 1 kVA. The emulated capacitance is constant over the range of frequencies (frequency-invariant) if $H_Q(s)$ is defined by (5.7). This is important in applications with varying line frequency such as certain aircraft power systems [48], [49]. The phase plot shows that, if $H_Q(s)$ in (5.7) is implemented with the negative sign, the admittance phase will change its sign as well (dotted line), and the converter will emulate an inductance at any given frequency. This inductance, however, will be dependent on the line frequency. The emulated inductance and capacitance are related by the equation:

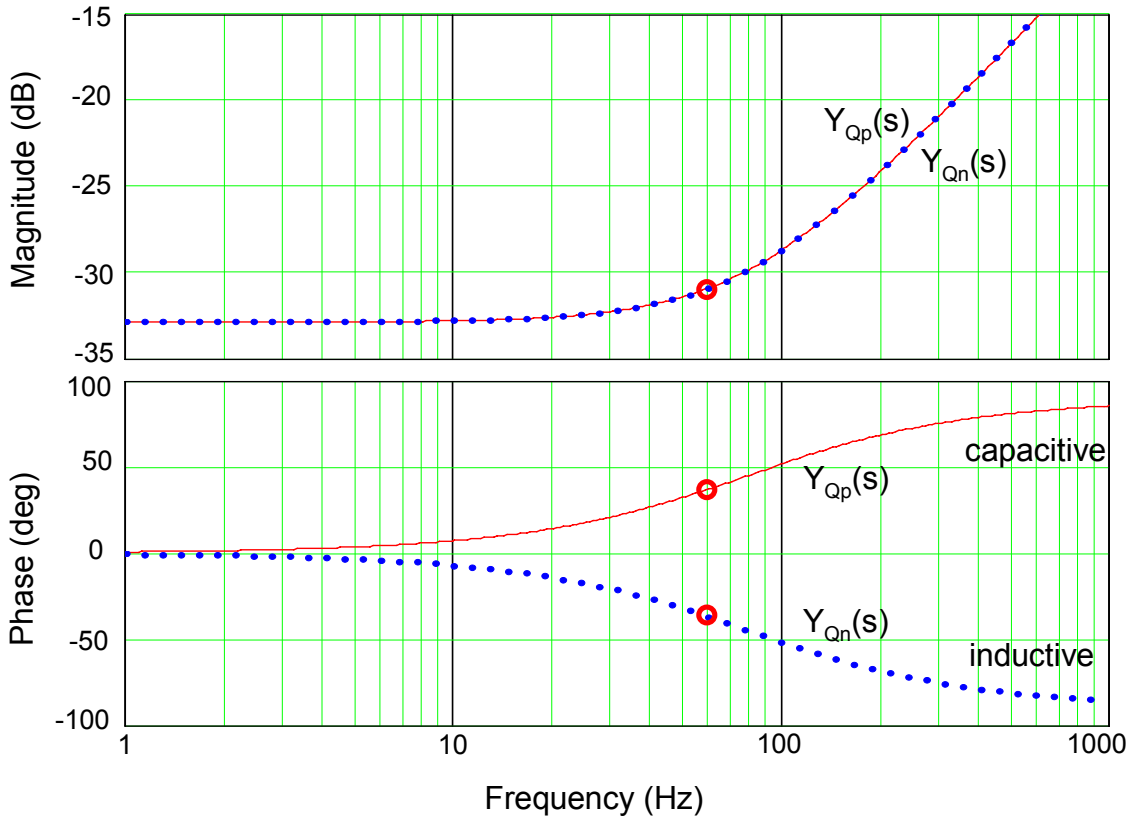


Figure 5.3 Converter input admittance with $H_Q(s)$ defined by (5.7).

$$2\pi f_g C_{YQ} = \frac{1}{2\pi f_g L_{YQ}}, \tag{5.9}$$

from which

$$L_{YQ} = \frac{1}{(2\pi f_g)^2 C_{YQ}}. \tag{5.10}$$

A frequency-invariant inductance for generating lagging-phase reactive power Q can be emulated by using a reactive power controller in the form

$$H_Q(s) = \frac{h_s}{h_{vs}} \frac{1}{s L_{YQ}}, \tag{5.11}$$

where

$$L_{YQ} = \frac{V_g^{\,2}}{2\pi f_g Q}. \tag{5.12}$$

Then,

$$Y(s) = \frac{P_g}{V_g^{\,2}} + \frac{1}{s L_{YQ}}. \tag{5.13}$$

Fig. 5.4 shows $Y(s)$ of the converter with emulated inductance operating with 1.3 kW of real power and lagging-phase reactive power (solid line). At 60 Hz, the line current has a lagging phase shift of 37°, and the reactive power is 1 kVA. The emulated inductance is constant over the range of frequencies (frequency-invariant) if $H_Q(s)$ is defined by (5.11). The phase plot shows that, if $H_Q(s)$ in (5.11) is implemented with the negative sign, the admittance phase will change its sign as well (dotted line), and the converter will emulate a capacitance at any given frequency. This capacitance, however,

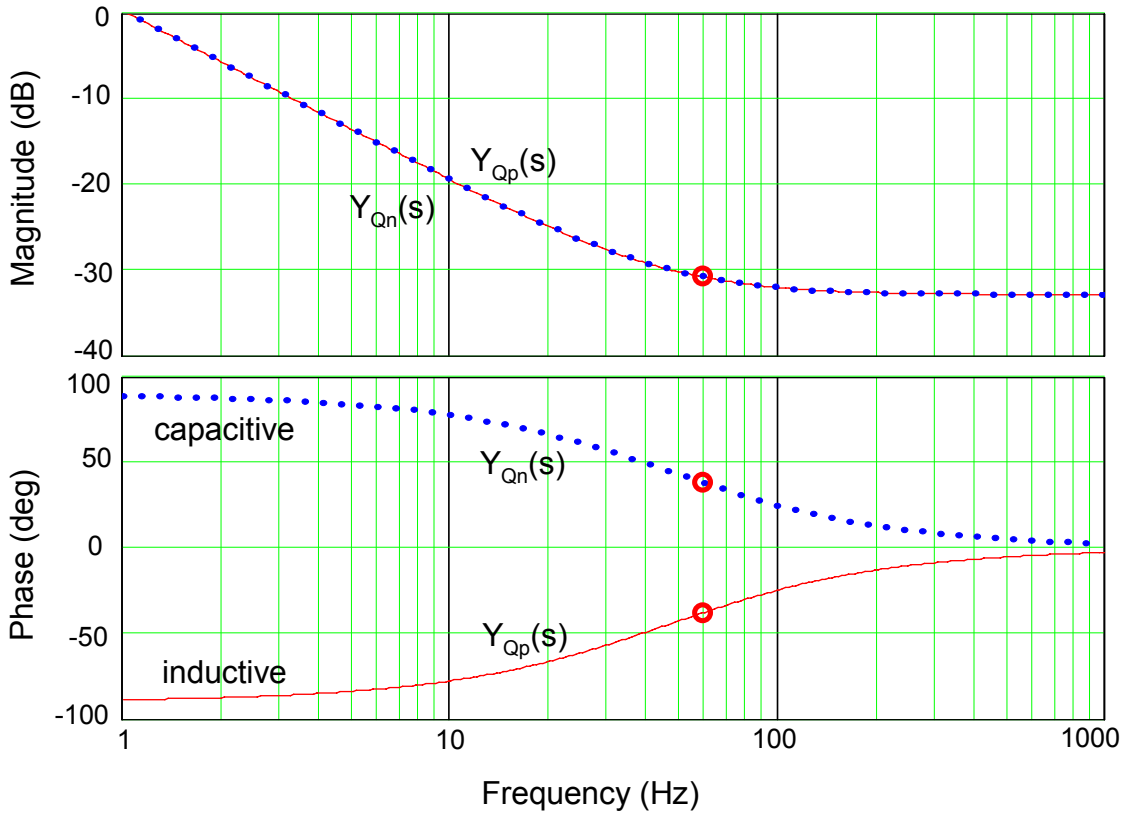


Figure 5.4 Converter input admittance with $H_Q(s)$ defined by (5.11).

will be dependent on the line frequency. The relationship between the emulated capacitance and inductance at a given line frequency is determined by (5.9).

The capacitance C_{YQ} and inductance L_{YQ} are emulated only at the line frequencies within the current loop bandwidth. Beyond the crossover frequency, the emulated reactive elements change their nature. If the line voltage has harmonics extending beyond the current loop bandwidth, these harmonics will be applied to a reactive element of a different kind than the line voltage fundamental. As follows from (5.3), the input admittance created by the reactive power controller over a range of frequencies is

$$Y_Q(s) = \frac{T_i(s)}{1+T_i(s)} \frac{h_{vs}}{h_s} H_Q(s). \tag{5.14}$$

If $H_Q(s)$ is determined by (5.7), then impedance of the emulated capacitance is given by

$$Z_Q(s) = \frac{1+T_i(s)}{T_i(s) C_{YQ} s}. \tag{5.15}$$

Fig. 5.5 shows an impedance plot of the capacitance (solid line) obtained with $H_Q(s)$ as determined by (5.7). The converter emulates a capacitance with a constant value C_{YQ} at frequencies up to the crossover frequency, above which the emulated element becomes inductive. It is interesting to note that the frequency response of the emulated capacitance resembles frequency response of real capacitors. If $H_Q(s)$ in (5.7) is taken with the negative sign, the impedance phase is inverted (dotted line). The emulated element becomes a frequency-dependent inductance below the crossover frequency and a frequency-dependent capacitance above the crossover frequency.

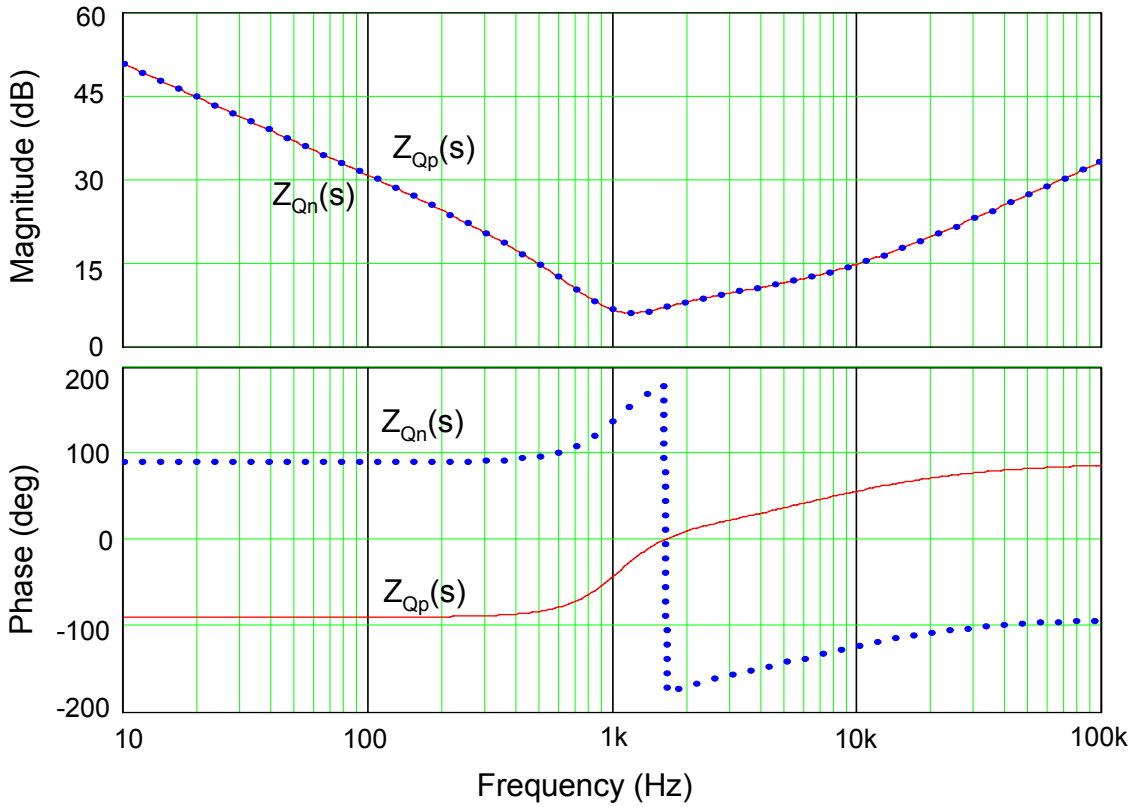


Figure 5.5 Impedance of capacitance C_{YQ} obtained with $H_Q(s)$ defined by (5.7).

If $H_Q(s)$ is determined by (5.11), the converter emulates an inductance, whose impedance is

$$Z_Q(s) = \frac{1 + T_i(s)}{T_i(s)} L_{YQ}\, s \ . \tag{5.16}$$

An impedance plot (Fig. 5.6) of the emulated inductance (solid line) has a slope of 20 dB/dec below the current loop crossover frequency. Above that frequency, the slope increases and becomes 60 dB/dec above the compensator pole ω_p, where the emulated reactive element behaves as a frequency-dependent capacitance. If $H_Q(s)$ in (5.11) is taken with the negative sign (dotted line), the emulated element acts as a frequency-dependent capacitance below the crossover frequency and a frequency-dependent inductance (with a slope of 60 dB/dec) above ω_p. One must remember the frequency limit of equations (5.15) and (5.16) imposed by the average model from which they were derived.

Another point in the current loop where the reactive power control signal could possibly be applied is the PWM modulator input, which is also used by an alternative implementation of the LPAC $H_{c1}(s)$ (Fig. 5.2). For an alternative form of the reactive power controller $H_{Q1}(s)$ applied to this input, equation (5.3) takes the form:

$$Y(s) = \frac{i_g(s)}{v_g(s)} = \frac{G_{iv}}{1 + T_i} + \frac{G_{id}\, F_m\, H_i}{1 + T_i} k_x V_c\, h_{vs} + \frac{G_{id}\, F_m\, H_i}{1 + T_i} H_c\, h_{vs} + \frac{G_{id}\, F_m}{1 + T_i} H_{Q1}\, h_{vs}\,, \tag{5.17}$$

Then,
$$H_{Q1}(s) = \frac{h_s}{h_{vs}} H_i(s)\, Y_Q(s)\,. \tag{5.18}$$

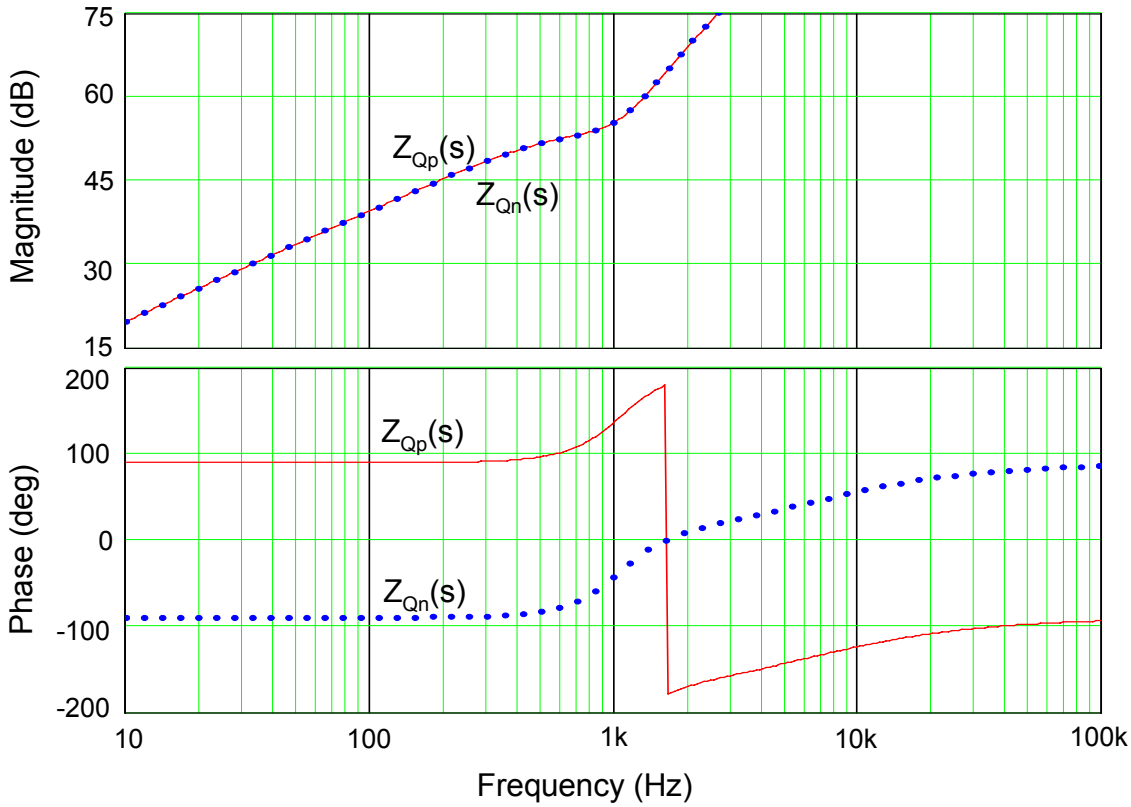


Figure 5.6 Impedance of inductance L_{YQ} obtained with $H_Q(s)$ defined by (5.11).

Since the reactive power control signal enters the loop after the compensator in the signal flow path within the loop, $H_i(s)$ has to be added to the reactive power controller transfer function as (5.18) demonstrates. This solution is impractical because $H_i(s)$ has high gain at the line frequency and is intended for operation within the closed loop. Used in an open-loop configuration, the compensator circuit will saturate its amplifier and lose its transfer function.

5.3 Controller Realizations

According to (5.7) and (5.11), the reactive power controller circuit should take a form of a differentiator or an integrator, respectively. Fig. 5.8 and 5.9 show possible reactive power controller realizations. Transfer functions and design equations for these realizations are summarized in Table 5.1. The circuit in Fig. 5.8(a) contains a differentiator explicitly; the one in Fig. 5.8(b) forms a differentiator when connected to the compensator. Circuits in Fig. 5.9 are developed according to the same principle. These realizations can be used in place of $H_Q(s)$ in the converter circuit diagram in Fig. 5.7. Realization in Fig. 5.8(b) has been used in the converter described in Chapter 4. Reactive power level is controlled by adjusting the amplifier gain h_Q, which can be positive or negative. It was found that the realization in Fig. 5.9(b) requires impractically small h_Q / L_Q ratio for realistic converter parameters; therefore, it presents only

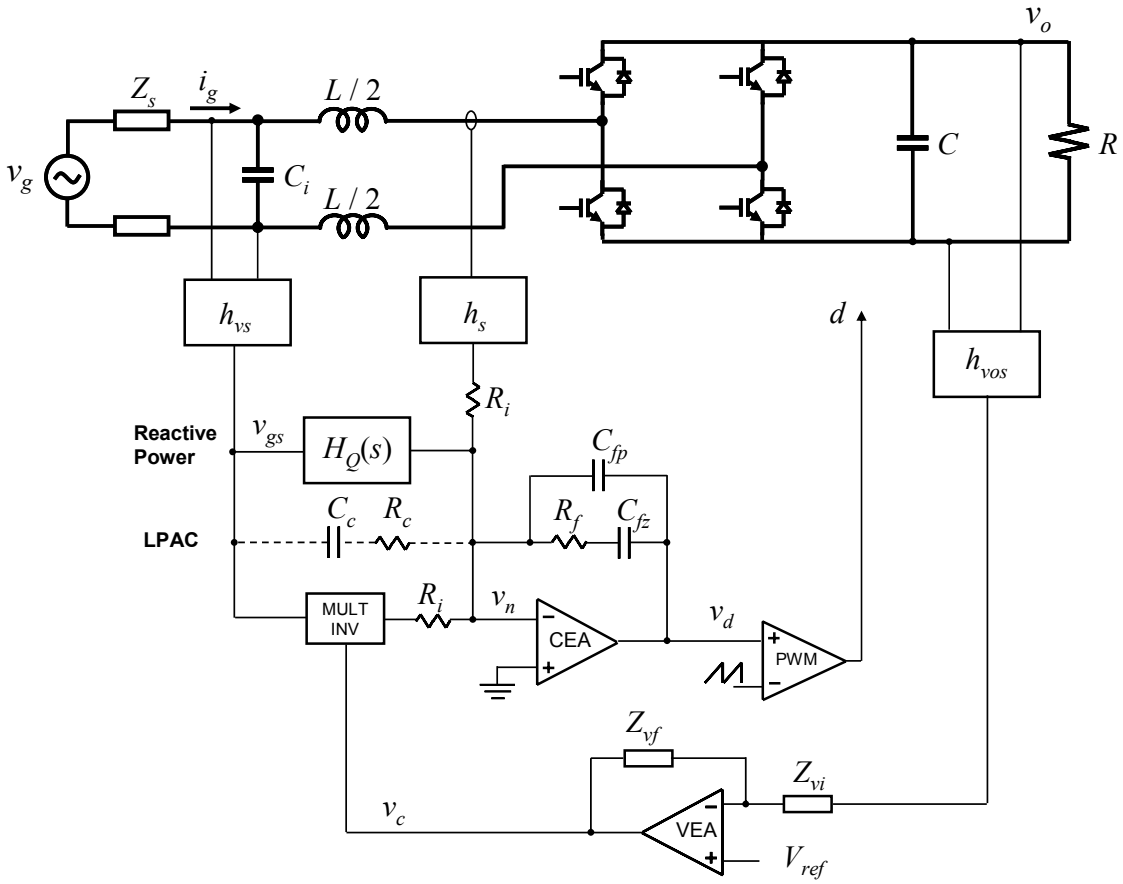
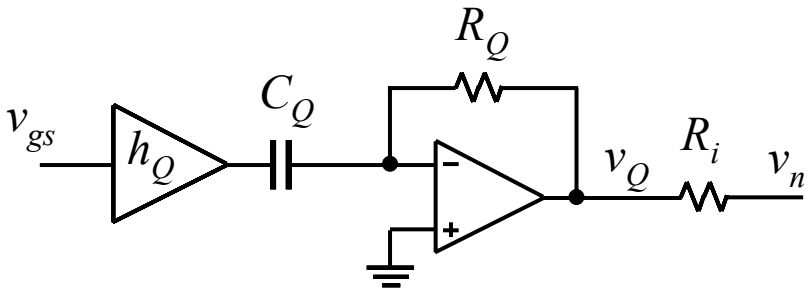
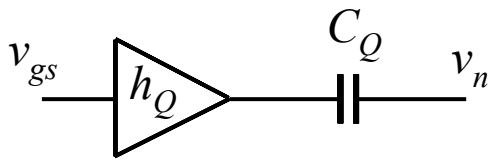


Figure 5.7 Implementation of the converter control system.

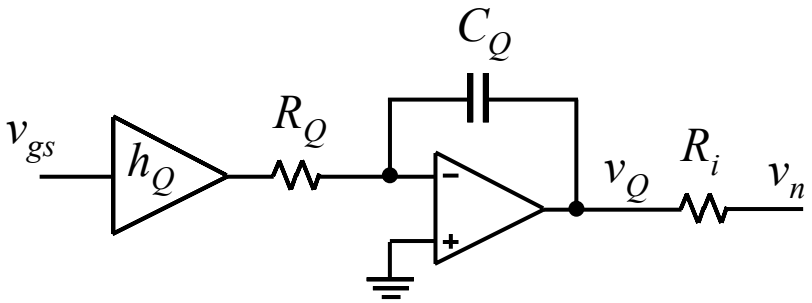


(a)

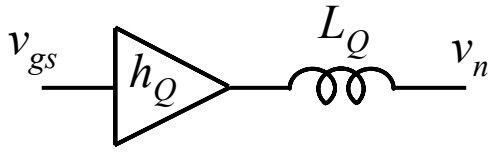


(b)

Figure 5.8 Realizations of $H_Q(s)$ in the form of (5.7).



(a)



(b)

Figure 5.9 Realizations of $H_Q(s)$ in the form of (5.11).

TABLE 5.1 REACTIVE POWER CONTROLLER REALIZATIONS

	Realization	h_Q	Frequency-invariant element	Frequency-dependent element	$H_Q(s)$	Design Equation
1	Fig. 8(a)	$h_Q > 0$	positive C	negative L	$h_Q R_Q C_Q s$	$h_Q R_Q C_Q = \frac{h_s}{h_{vs}} C_{YQ}$
		$h_Q < 0$	negative C	positive L		
2	Fig. 8(b)	$h_Q < 0$	positive C	negative L	$-\frac{h_Q C_Q}{\omega_i (C_{fp} + C_{fz})} s$	$-h_Q C_Q = \frac{h_s}{h_{vs}} C_{YQ} \omega_i (C_{fp} + C_{fz})$
		$h_Q > 0$	negative C	positive L		
3	Fig. 9(a)	$h_Q > 0$	positive L	negative C	$\frac{h_Q}{s C_Q R_Q}$	$\frac{h_Q}{C_Q R_Q} = \frac{h_s}{h_{vs} L_{YQ}}$
		$h_Q < 0$	negative L	positive C		
4	Fig. 9(b)	$h_Q < 0$	positive L	negative C	$-\frac{h_Q}{s \omega_i (C_{fp} + C_{fz}) L_Q}$	$-\frac{h_Q}{L_Q} = \frac{h_s \omega_i (C_{fp} + C_{fz})}{h_{vs} L_{YQ}}$
		$h_Q > 0$	negative L	positive C		

theoretical interest. The other realizations can be conveniently implemented and have been experimentally verified.

5.4 Noise Performance

Because reactive power controller transfer function in the form (5.7) contains a differentiator, this controller is susceptible to noise present in the ac line voltage, particularly switching noise of the converter as well as any other noise coming from the line. This noise is amplified as it propagates from v_g to v_d through $H_Q(s)$ (Fig. 5.2) and may disrupt operation of the PWM modulator. The current loop compensator transfer function includes an integrator, which provides attenuation of the noise coming through the compensator. However, the differentiator in $H_Q(s)$ defined by (5.7) cancels the effect of this integrator; thus the noise coming through $H_Q(s)$ to v_d is not attenuated well and may be amplified instead. At high frequencies, the reactive power control signal path has the transfer function:

$$\frac{v_d(s)}{v_g(s)} = h_{vs}\, H_Q(s)\, H_i(s) = \frac{h_s\, C_{YQ}\, \omega_i\, \omega_p}{\omega_z}, \tag{5.19}$$

which shows that there is no gain roll-off at high frequencies in this signal path.

On the other hand, reactive power controller in the form (5.11) is based on the integrator, which suppresses noise. The high-frequency transfer function of the reactive power control signal path is

$$\frac{v_d(s)}{v_g(s)} = h_{vs}\, H_Q(s)\, H_i(s) = \frac{h_s\, \omega_i\, \omega_p}{\omega_z\, L_{YQ}\, s^2}. \tag{5.20}$$

This form of reactive power control has a 40 dB/dec gain roll-off at high frequencies and, therefore, provides much better noise performance.

When form (5.7) is used, simulation analysis and experiments using the setup described in the next section showed that presence of the switching noise at the line terminals may cause irregular PWM operation of the modulator and distortions of the line current waveform. In order to avoid noise effects, a good filtering of the sensed line voltage signal may be required. In our experiments, a 2nd order band-pass filter tuned to the line frequency provided an improvement of the line current waveform as long as the line frequency is constant. In systems with varying or "wild" frequency [48], [49], good filtering may be problematic, and one may have to use a phase-locked loop or other solutions suitable for varying line frequency.

5.5 Experimental Results

A multilevel AFE converter prototype (Fig. 4.9) used to test the reactive power control concept presented in Chapter 4 was utilized to verify reactive power controller realizations developed in this chapter. The converter operated from a 208-V ac line and provided 376 V to the dc bus load. Fig. 5.10 demonstrates waveforms of the converter operating with 4 kVA leading-phase reactive power while supplying 2.6 kW to the load. In Fig. 5.11, the reactive power processed by this converter has a lagging phase. Reactive power controller realization in Fig. 5.9(a) used in these tests provided clean, noise-free waveforms. Fig. 5.12 demonstrates the effect of noise coming from the line through the reactive power controller and affecting operation of the PWM modulator. Realization in Fig. 5.8(a), which is susceptible to noise, was used in this test. The noise in the current waveform causes additional noise in the voltage waveform, which aggravates the problem. The noise level in the current waveform produced with this realization can be reduced by better filtering of the line voltage signal used for the reactive power control.

The converter with reactive power control can supply reactive power without processing any real power. In this capacity, the converter can be used as an adjustable reactive power compensator. Fig. 5.13 shows the converter operation with 3 kVA leading-phase reactive power and no real power. The reactive power has a lagging phase in Fig. 5.14.

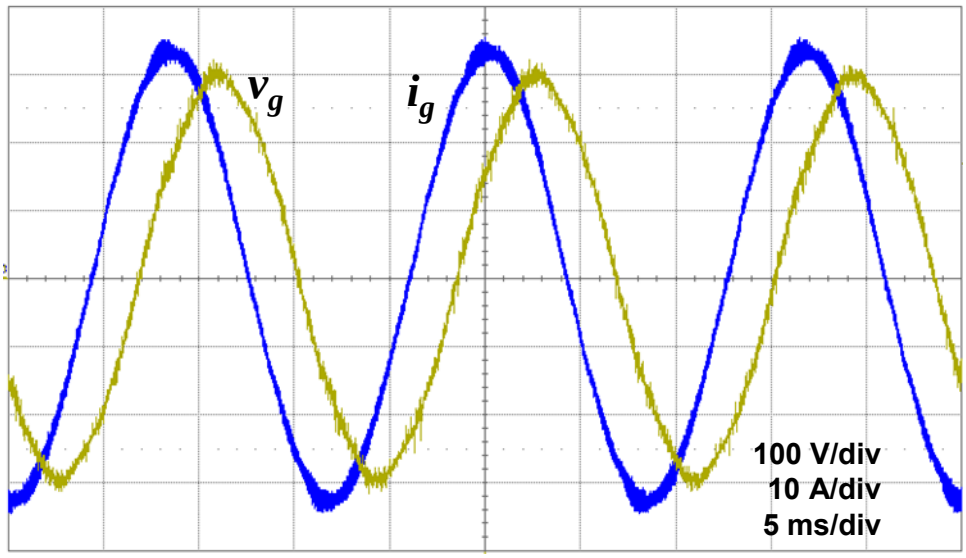


Figure 5.10 Experimental waveforms of the converter operating with leading-phase reactive power. $H_Q(s)$ is realized as in Fig. 5.9(a).

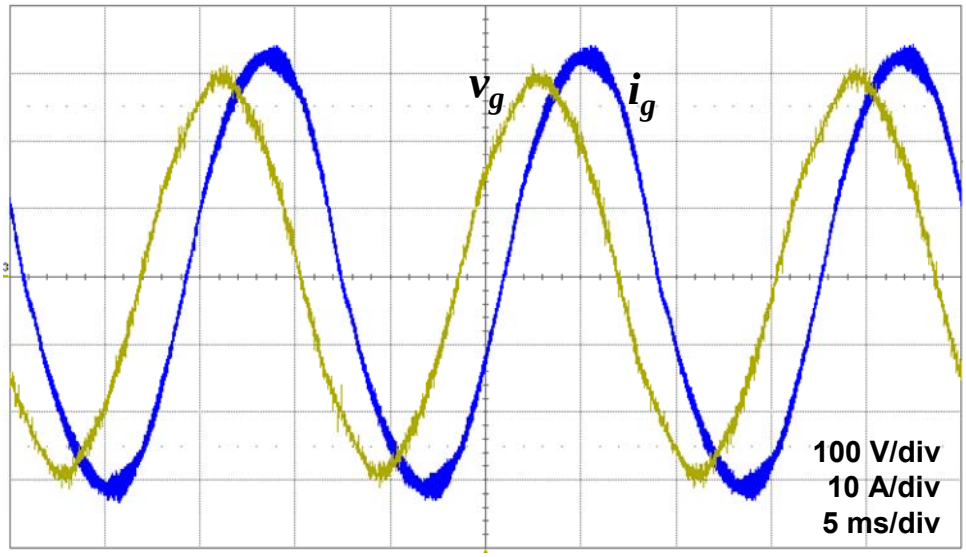


Figure 5.11 Experimental waveforms of the converter operating with lagging-phase reactive power. $H_Q(s)$ is realized as in Fig. 5.9(a).

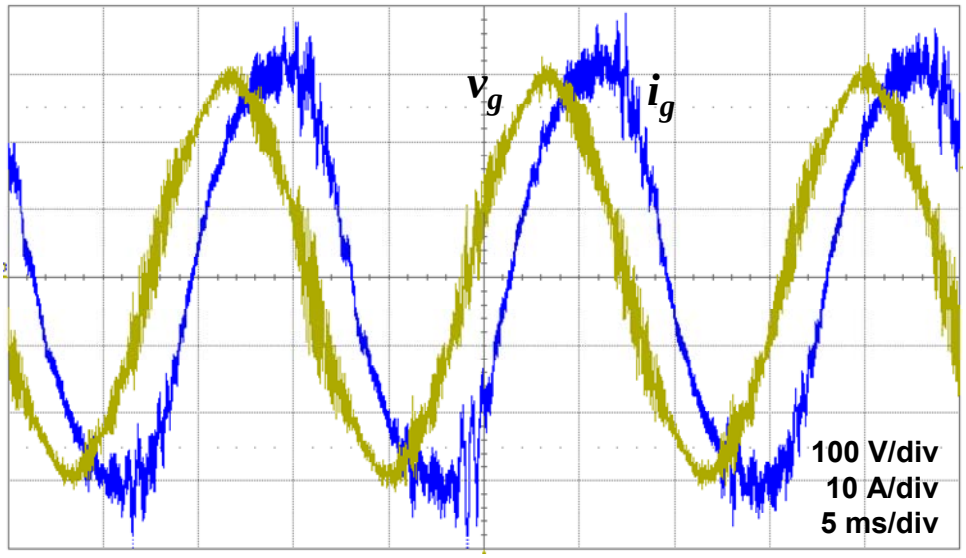


Figure 5.12 Current waveform distortion due to noise in the ac line voltage. $H_Q(s)$ is realized as in Fig. 5.8(a).

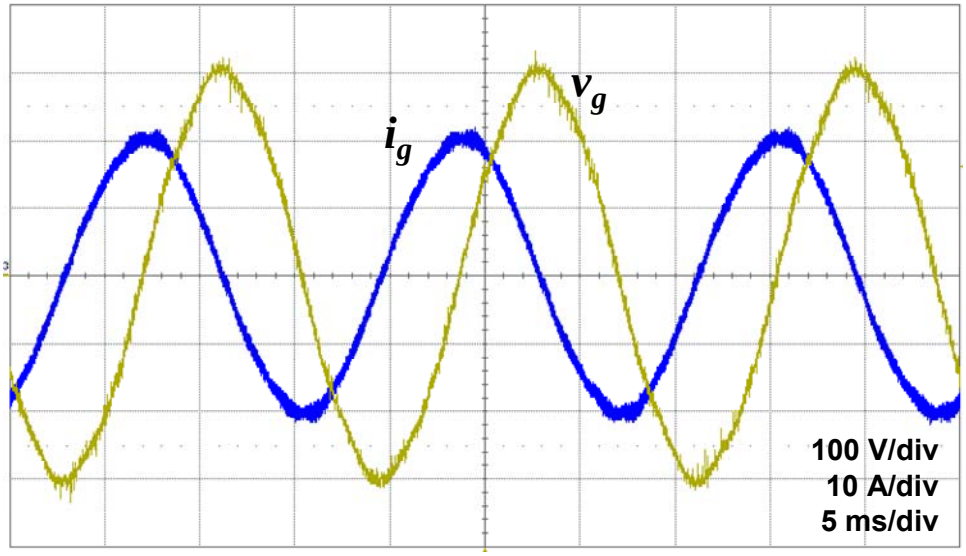


Figure 5.13 Experimental waveforms of the converter operating with leading-phase reactive power (no real power).

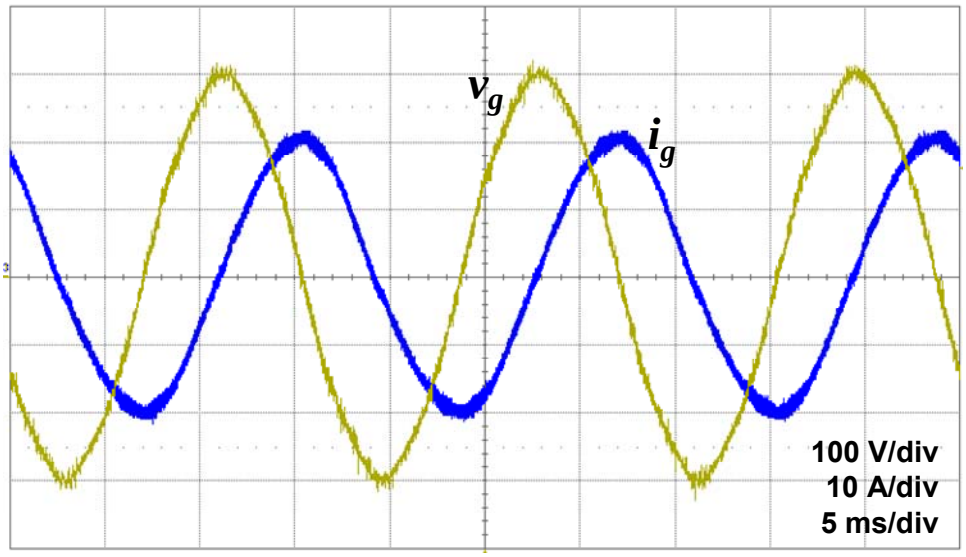


Figure 5.14 Experimental waveforms of the converter operating with lagging-phase reactive power (no real power).

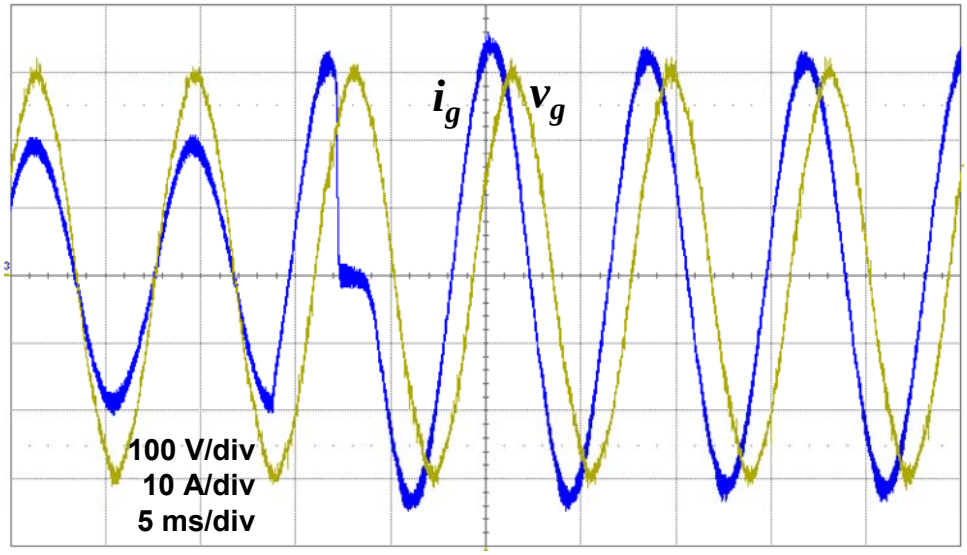


Figure 5.15 Step response to the reactive power command.

Dynamic performance of reactive power control is very good due to high bandwidth of the current loop. Fig. 5.15 displays the converter response to a step change in the reactive power command. Initially, the converter operated with no reactive power. Transition to the commanded level of reactive power occurred within one line cycle.

The experimental results are in a good agreement with theoretical predictions and simulation waveforms.

5.6 Summary

This chapter presents development of a methodology and implementation techniques for adding reactive power control to single-phase AFE converters operating with ACMC. Reactive power source capability allows the AFE converters to be used as reactive power compensators in addition to their function as ac-dc converters or without processing real power. The converters can operate and perform reactive power control at different line frequencies or at varying line frequency. Reactive power control can be realized in multiple ways by adding a suitable controller to the current control loop. This chapter presents a comprehensive study of reactive power control realizations in a single-phase AFE converter, along with their merits and limitations, including susceptibility to the ac line noise. Different forms of the reactive power control were derived in a systematic way by using closed-loop dynamic modeling of the converter, and their potential for use in certain applications was discussed. It is possible to use reactive power

control to provide emulation of a frequency-invariant capacitance or inductance, which may be necessary in applications with varying line frequency such as in certain aircraft power systems. Analysis and simulation results were supported by experiments.

Chapter 6

Conclusions

The dissertation summarizes research work that culminated in development of the generalized average-current-mode control (GACMC), which is an extension of the average-current-mode control for boost PFC converters. The GACMC significantly extends the allowable range of line frequencies for a given current loop bandwidth, or, in other words, significantly reduces the current loop bandwidth requirement for a given line frequency. The GACMC also offers additional functionality—reactive power control capability for bidirectional PFC boost converters.

Initially, the leading-phase admittance cancellation (LPAC) method has been developed for the single-phase PFC boost converter in order to eliminate the leading-phase distortion of the line current at higher line frequencies. This technique extends the allowable range of line frequencies from about $^{1}/_{150}$ of the current loop bandwidth with traditional design to about $^{1}/_{5}$ with the LPAC. This method is useful in applications with higher line frequencies such as aircraft power system (360–800 Hz) and in medium- and high-power (above 10 kW) single-phase PFC applications operating at the utility line frequency, which would benefit from a lower switching frequency. The LPAC method is

load-invariant and line-voltage-invariant. It can be realized easily with only two passive components in the simplest case and can be applied to existing designs. The newly developed dynamic model of the system provided theoretical foundation of this method and design equations for component values of the LPAC network. Experimental results showed good agreement with simulation waveforms and confirmed effectiveness of the LPAC.

The LPAC technique was further utilized for cancellation of the input filter capacitor current, which becomes significant at higher line frequencies such as in aircraft power systems (360–800 Hz). It was found that the LPAC network can be further tuned to do additional job—to cancel the reactive current of the input capacitor in a bidirectional boost PFC converter. Closed-loop dynamic models for the bidirectional and unidirectional PFC boost converters were used to derive conditions for cancellation of the capacitor current and design formulas for component values of the LPAC network. The method was verified by computer simulations and experimentally. Bidirectional converters allow complete, load-invariant, line-frequency-invariant cancellation of the input capacitor current and provide unity power factor under all operating conditions. Unidirectional converters allow substantial reduction but not complete elimination of the switching ripple in the line current. Under these conditions, the converter achieves unity power factor with no phase shift of the line current, with load-invariant and line-frequency-invariant component values of the LPAC network.

Based on the insights gained from modeling of the boost PFC converter with ACMC and LPAC, a reactive power control technique was proposed. This technique

allows a bidirectional PFC boost converter (active front end topology) to generate a prescribed amount of reactive power with a leading or lagging phase independently of the primary function of the converter as an ac-dc PFC rectifier. This technique was utilized in the development of a 20-kW single-phase multilevel active-front-end converter as a high-performance alternative to traditional line-frequency rectifiers. The converter uses the LPAC compensation to allow a low 10-kHz switching frequency, which reduces switching losses and increases converter efficiency, without the line current phase shift inherent to the traditional average-current-mode control when a low switching frequency is used. The reactive power controller allows the converter to be used as a static reactive power compensator in the power system independently of its function as an ac-dc converter. This work presented a theoretical basis for reactive power control using dynamic modeling of the current loop and a simple implementation of the reactive power controller. This method does not require extra power components or modifications of the converter power circuit and achieves reactive power control entirely by means of the controller action as part of the GACMC. This concept was verified by testing of a scaled-down converter prototype, which successfully demonstrated both the unity-power-factor operation and reactive power control capability.

Further research revealed that there are multiple ways to implement the reactive power control by adding a suitable controller to the current control loop, with certain ways being more advantageous in certain applications. The dissertation presents a comprehensive study of reactive power control realizations in a single-phase active-front-end (AFE) converter, along with their merits and limitations, including susceptibility to

the ac line noise. Reactive power control can be realized in multiple ways by adding a suitable controller to the current control loop. Different forms of reactive power control were derived in a systematic way by using closed-loop dynamic modeling of the converter, and their potential for use in certain applications was discussed. It is possible to use reactive power control to provide emulation of a frequency-invariant capacitance or inductance, which may be necessary in applications with varying line frequency such as in certain aircraft power systems. Analysis and simulation results were supported by experiments. Dynamic performance of reactive power control is very good due to high bandwidth of the current loop. Experiments showed that transients due to a change in the commanded level of reactive power usually take no longer than one line cycle.

The converter can operate with real power only, reactive power only, or any combination of these. However, if the reactive power control capability is used, the converter power circuit components must be rated for the full power including its reactive component. Reactive component of the line current causes additional losses in the power circuit components, which should have appropriate current ratings. The inductor esr will dissipate more power due to reactive current; therefore, the inductor has to be properly sized. On the other hand, the dc link capacitor is not affected by the LPAC and reactive power control because the ripple current flowing through the capacitor is determined only by the real power processed by the converter. The voltage ratings of power components are not affected by the LPAC and reactive power control. Therefore, the maximum real and reactive power processed by the converter are limited by the current ratings of the power circuit components.

Closed-loop stability of the current loop is determined by the loop-gain transfer function $T_i(s)$ (2.6), which is ensured to be stable by proper design of the current loop compensator $H_i(s)$ (2.2). The LPAC and the reactive power controller do not factor in the loop-gain transfer function $T_i(s)$ and, therefore, do not affect the current loop stability. The converter remains stable once the LPAC and the reactive power controller are added. The LPAC and the reactive power controller do not factor in the voltage loop signal path (Fig. 2.10, 3.1, 4.1, 5.7) and, therefore, do not affect the voltage loop stability. The converter performance characteristics are not particularly sensitive to the values of the LPAC and reactive power controller components; no more than to the values of other power and control circuit components. No fine adjustments of the LPAC and reactive power controller components are necessary. Analysis and experiments showed that the closest standard values of resistors and capacitors can be used in the LPAC and the reactive power controller without any noticeable degradation of the converter performance.

Major achievements of this work:

- A closed-loop dynamic model for the current control loop of the boost PFC converter with ACMC has been developed. The model explains the structure of the converter input admittance, the current phase lead phenomenon, and lays the groundwork for development of generalized ACMC.
- The Leading Phase Admittance Cancellation principle has been proposed to completely eliminate the current phase lead phenomenon and, consequently, the zero-crossing distortion in unidirectional converters.

- The LPAC technique has been adapted for active compensation of the input filter capacitor current in bidirectional boost PFC converters.
- A reactive power control principle has been developed for bidirectional converters with ACMC. The proposed control strategy enables the converter to generate reactive power and, thus, be used as a reactive power compensator, independently of the converter function as an ac-dc converter.
- Multiple realizations of the reactive power controller have been identified and examined in a systematic way, along with their merits and limitations, including their susceptibility to the ac line noise. Frequency response characteristics of reactive elements emulated by means of these realizations have been described.

Possible directions for further research:

- Investigate input filter design considerations for converters with the GACMC and effect of the GACMC on input filter–converter interaction.
- Study the effect of the dc voltage ripple on converter operation and possible ways to reduce this ripple in converters using the GACMC.
- Investigate possibilities of using other types of compensators in the current control loop.

Appendix

Converter Parameters

Chapter 2

L = 1 mH, R_{sen} = 0.33 Ω, F_m = 0.25, $R_m = R_i$ = 4 kΩ, R_{fz} = 3.3 kΩ, C_{fp} = 820 pF,

C_{fz} = 12 nF, C_c = 2.7 nF, R_c = 20 kΩ, h_c = 0.054, V_o = 385 V.

Chapter 3

V_g = 120 V, V_o = 385 V, L =1.31 mH, h_s = 0.315, h_{vs} = 1, F_m = 0.25, R_i = 4.02 kΩ,

R_{fz} = 3.3 kΩ, C_{fp} = 820 pF, C_{fz} = 12 nF, C_c = 2.7 nF, R_c = 20 kΩ, L_s = 60 μH,

R_s = 0.05 Ω, f_{sw} = 90 kHz.

Chapter 4

V_g = 240 V, V_o = 376 V, L = 2.82 mH, C = 3000 μF, h_s = 0.333, h_{vs} = 0.01, F_m = 0.1,

R_i = 10 kΩ, R_{fz} = 15.8 kΩ, C_{fp} = 1.5 nF, C_{fz} = 10 nF, C_c = 27 nF, R_c = 5.9 kΩ, C_Q = 33 nF,

h_Q = 3.9.

Chapter 5

V_g = 208 V, V_o = 376 V, L =2.82 mH, C = 1500 μF, h_s = 0.333, h_{vs} = 0.01, F_m = 0.1,

R_i = 10 kΩ, R_f = 15.8 kΩ, C_{fp} = 1.5 nF, C_{fz} = 10 nF, C_c = 27 nF, R_c = 5.9 kΩ,

C_Q = 220 nF, R_Q = 10 kΩ, f_{sw} = 10 kHz.

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Vita

The author, Konstantin P. Louganski, was born in Tuapse, Russia in 1964. He received his Electrical Engineer's (B.S.) degree in Electromechanics from Rostov State University for Transportation Technology, Rostov-on-Don, Russia in 1986 and his M.S. in Electrical Engineering degree from Virginia Polytechnic Institute & State University in 1999.

From 1999 to 2002, he worked on development of electronic control for diesel engines at Cummins, Inc. in Columbus, Indiana. In August 2002, he started his Ph.D. program at Virginia Polytechnic Institute & State University (Virginia Tech) pursuing his study and research in the field of power electronics. As a graduate research assistant, he worked on a number of power conversion projects including dc-dc converters, inverters, power factor correction, and multilevel converters. His current research interests involve power converter topologies and control, power factor correction, and alternative energy applications. He is a Student Member of the IEEE Power Electronics Society and the IEEE Industry Applications Society.