

Fabrication Refinements of Advanced Packaging Techniques for Medium-Voltage
Wirebond-less Multi-Chip Power Modules

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ABSTRACT

Three growing power electronics applications have massive requirements for properly operating their medium-voltage and high-voltage systems: electric transportation, renewable energy, and the power grid. Their needs include dense power systems with higher efficiency and higher voltage and current devices. This requires devices with higher switching frequencies to lower the size of the passives in the converter and devices that can withstand higher operating temperatures as components move closer together to improve power densities. Devices that achieve higher switching speeds and lower specific on-state resistances also reduce losses.

Wide bandgap devices (WBG) like silicon carbide (SiC) have a higher bandgap, higher electric field strength, higher thermal conductivity, and lower carrier concentration than silicon (Si). This allows for higher temperature operation, faster switching, higher voltage blocking, and lower power losses, directly meeting the requirements of the previously noted applications. However, the current packaging schemes are limiting the ability of SiC to operate in these applications by applying packaging schemes used for Si. Therefore, it is critical to use and refine advanced packaging techniques so that WBG devices can better operate and meet the growing demands of these power electronic applications.

Low-inductance, wirebond-less, high-density, scalable modules are possible due to advanced packaging methods. While beneficial to the operation and design, these techniques introduce new challenges to the fabrication process. This requires refinement

to improve the yield of sandwich-structure modules with wirebond-less interconnects. For this module, encapsulated, silver-sintered substrates reduce the peak electric field within the package, improving the partial discharge inception voltage to meet insulation requirements. It is essential to have a uniform bondline between the substrates to achieve all bond connections and improve reliability. Silver sintering is also used to attach the molybdenum (Mo) post interconnects. These interconnects allow for sandwich-structure modules with low inductances; however, they have tolerance variation from manufacturing and bondline thicknesses, which become problematic for multi-chip power modules with an increased number of die and posts. The variation results in tilt, causing some posts to disconnect altogether. Additionally, soldering MCPMs involves a large thermal mass that the soldering reflow profile from a datasheet does not account for.

Ultimately, these fabrication concerns can result in misalignment or disconnected post interconnects to the top substrate. Post interconnect planarity and alignment are vital for this multi-chip power module to avoid open or shorted connections that can derate switch positions. This thesis aims to refine each packaging step in assembling a wirebond-less, multi-chip power module. The bond uniformity of silver (Ag) sintering is addressed in dried preform and wet paste cases. The soldering methods are explored and improved by creating a modified reflow profile for large thermal masses and introducing pressure to reduce bondline variation and voiding content. The entire sandwich structure module is analyzed in a statistical tolerance analysis to understand which component introduces the most variation and height mismatch, providing insight as to which packaging techniques need further control to improve the yield of multi-chip power modules.

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GENERAL AUDIENCE ABSTRACT

The electrification of many systems worldwide has increased the need for compact, efficient power electronics. Their applications span electric transportation, renewable energy systems, grid applications, and data centers, to name a few medium-voltage applications. Wide bandgap (WBG) semiconductors can outperform silicon in these applications, offering higher temperature robustness, higher efficiency performance, and higher voltage capabilities. The faster switching will reduce the size and weight of the converters containing these devices. However, using typical packaging schemes such as wirebonds will limit the potential of WBG devices in these applications.

Advanced packaging techniques have been developed to increase the electric field strength, reduce the power loop inductances, reduce electromagnetic interference from fast-switching transients, and improve the power densities of multi-chip power modules for medium voltage and current applications. However, these packaging techniques are not trivial to implement and have resulted in a low yield of these modules.

This thesis aims to refine each packaging step in assembling a wirebond-less, multi-chip power module. The bond uniformity of silver sintering is addressed in cases of dried preform and wet paste. The soldering methods are explored and improved by creating a modified reflow profile for large thermal masses and introducing pressure to reduce bondline variation and voiding content. The entire sandwich structure module is analyzed in a statistical tolerance analysis to understand which component introduces the most

variation and height mismatch, providing insight as to which packaging techniques need further control to improve the yield of multi-chip power modules.

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Chapter 1 Introduction

1.1 Background

Power electronics has shifted from the long-standing use of silicon (Si) devices to exploring the capabilities that wide bandgap (WBG) devices can offer for the field. The inherent properties of WBG devices, namely silicon carbide (SiC), allow them to outperform Si in several applications, as noted in Figure 1. The critical electric field is higher than Si, making SiC the top contender for medium-voltage and high-voltage applications. This increase in critical electrical field is accompanied by a size reduction of the chip, thus, reducing the gate area and ultimately lowering the gate charge. This is key for device operation at higher frequencies, allowing for lower on-state resistance, minimizing switching losses, and opening the door for applications that require efficient power conversion [1]–[4]. The high operating temperature combined with the high thermal conductivity allows SiC to have improved high-temperature performance while being more feasible to cool than Si devices [3], [5].

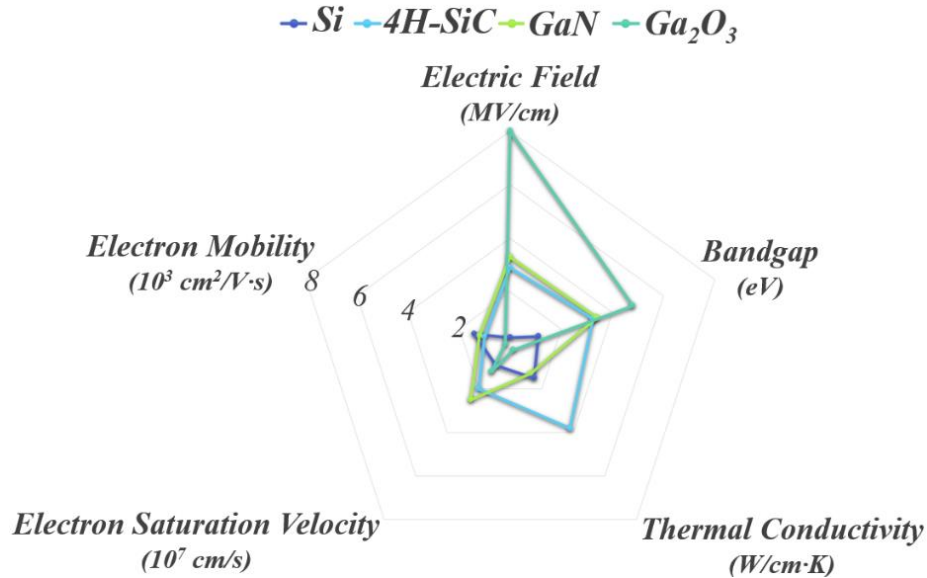


Figure 1: Comparison of key characteristics of different semiconductor devices [6][7].

Various power devices have utilized Si as the foundation of power electronics, ranging from field-effect transistors (FET), bipolar-junction transistors (BJT), and gate bipolar junction transistors (IGBT). Si transistors have been extensively reviewed in academic research, the most extensive being the Si IGBT [5]–[7]. While these power modules have proved reliable and durable for low and medium voltages and high currents and have seasoned experts on their operation, growth, and manufacturability, these modules have quite a few limitations. As discussed previously, the switching speed of Si devices will limit these modules for the demands of efficient power conversion. Additionally, the maximum voltage rating of these modules' plateaus is 6.5 kV, rendering these modules useless for high-voltage applications such as renewable energy grid interfaces and all-electric ships [7]–[9]. Joining Si IGBT power modules in series to increase the rated blocking voltage can rectify this issue; however, this solution introduces many challenges, mainly concerning voltage stability and developing complicated control schemes [9]–[11]. Furthermore, to meet safety and reliability requirements, the modules in series or parallel need to be isolated and heavily derated, increasing the footprint of the converter and decrementing the overall power density [12].

However, this same argument can apply to the medium- and high-voltage SiC modules with lower current capabilities. The devices and modules need to be connected in parallel for these modules to reach the current levels that Si IGBTs have. Paralleling SiC devices or modules can introduce similar problems that the series of IGBTs present, now regarding current imbalances, but the same increased control complexity and lower power density from derating [11], [13], [14]. Additionally, the increased switching speed, compounded by the proximity of connected modules, can present unforeseen EMI concerns

that require careful consideration and testing [15]. These challenges have led to a growing interest in parallel devices within the package to increase power densities, uncomplicate the controls, and target reduced imbalances.

Nonetheless, the medium- and high-voltage SiC MOSFET application space has flourished despite these challenges for high-current applications. Commercially and academically developed packages highlight the promising potential that SiC and wide bandgap devices have during operation. It is essential to identify the current packaging layouts and materials used to successfully fabricate multi-chip power modules to explore the challenges of fabricating these modules given their voltage requirements and the increased complexity as the number of devices and components in these modules rises.

1.2 Survey of Multi-Chip Power Module Packaging Techniques

1.2.1 Overview of the Typical Packaging Components and Schemes

It has become apparent from the characteristics of WBG semiconductors that they can meet the demands of applications today for power electronics for high voltage, high current, high temperature, fast switching, high efficiency, and low losses. However, these devices cannot operate under all these conditions independently. The packaging of the devices is necessary to interface the device characteristics for use with the external world for these applications. The packaging of the device provides the enclosure to allow the device to reliably perform electrically, thermally, and mechanically. It involves understanding the physics, chemistry, and material science of all the components in a package to optimize the electrical and thermal. It can significantly impact the devices' performance, size, cost, and reliability [16].

The conventional power module package is shown in Figure 2. It consists of a substrate attached to a baseplate with a thermal interface material. The baseplate's function is to dissipate heat generated from the package during operation. The substrate, typically an inorganic ceramic, provides mechanical support and electrical connections for the devices based on the substrate patterning. A common ceramic substrate is direct bonded copper (DBC), which consists of two copper layers with a ceramic sandwiched in-between for insulation and rigidity. There are also active metal brazing (AMB) substrates with silicon nitride and copper, which provide even more mechanical robustness than DBCs with less coefficient of thermal expansion (CTE) mismatch and better heat dissipation. This work focuses on a direct-bonded aluminum (DBA) type, which has better thermal performance than DBC and AMB substrates but slightly worse CTE than AMB.

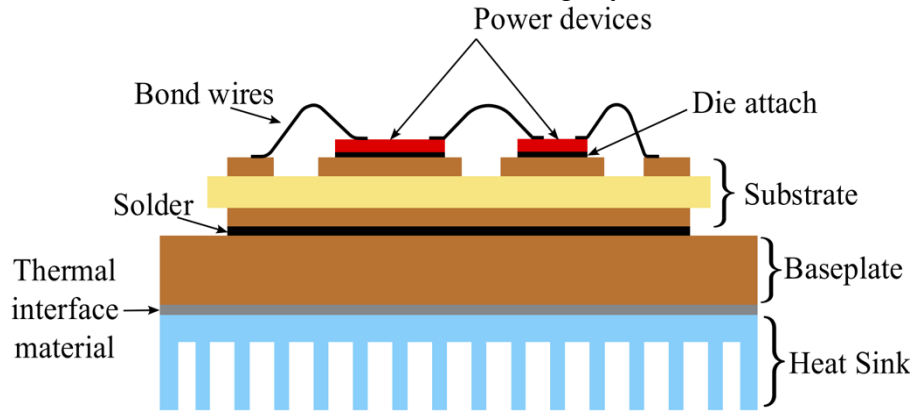


Figure 2: Conventional power module packaging scheme with crucial components labeled [16].

The semiconductors are attached to the substrate using a die attach material such as epoxy, solder, and sinter. Conductive epoxy is less common for power electronics applications due to its limited thermomechanical performance. Soldering can be in the form of paste, preform, or wire and has been a conventional die attach method since the beginning of power electronics. Recently, methods have shifted to silver sintering

techniques for a more reliable bond with higher thermal conductivity and less voiding content.

Interconnects form the connections within the package from the devices to terminals or other devices. These interconnects are typically wirebonds for the bare device, but some devices are compatible with flip-chip or ball grid array (BGA) interconnect methods. Methods to eliminate wirebonds within a package and replace them with more reliable interconnects have been investigated and will be a focus of this work.

Terminals are what allow the devices to interface with external applications. These can range from screw terminals, pins, springs, clamps, and more. These terminals can be permanently attached to their external environment, such as a gate driver or bus bar, for better attachment reliability, or they are clamped so that the package can be removed and serviced.

The encapsulation is crucial for improving electrical insulation for medium- and high-voltage modules. However, it is also beneficial to protect the device and internals of the package from the environment and thermomechanical shocks. The encapsulants are dielectric materials ranging from tolerant silicone gels to rigid epoxy molding compounds. The encapsulants are held within a plastic module housing material, or in some cases, the encapsulation material can be the entire device housing.

1.2.2 Current Challenges of Package Interconnects for Medium-Voltage Multi-Chip Power Modules

Multi-chip power modules (MCPMs) enable the series and paralleling of devices to achieve higher voltages and currents, respectively. Modules have reached up to 10 kV for SiC devices, but only a few hundred amps compared to high current Si IGBT

modules[17], [18]. It is important to lay out the module to reduce parasitic imbalances and the magnitude of the parasitics overall since SiC devices are more sensitive to imbalances and the magnitudes of parasitics due to the fast-switching nature of these devices [19].

The substrate of multi-chip power modules needs to be sized to have adequate heat spreading and reduce thermal coupling between chips. This can result in large substrates where the path between devices and the package terminals that interface with the gate driver and busbar becomes longer. The most common interconnect method across these substrates is the aluminum (Al) wirebond. Al wirebonds are cost-effective and have thoroughly developed manufacturing processes [20]. Wirebonds require pads to bond to laterally, increasing the substrate surface size and decreasing the power density [21]. The lengths of the wires increase to connect across the MCPM, increasing the parasitic inductance and force on the necking point, degrading the reliability and module performance [22], [23]. Additionally, wirebonds have low reliability for stressful thermomechanical environments. They are one of the significant causes of failure at elevated temperatures, which is not promising for WBG devices operating at higher temperatures than their Si counterpart [24]. Cracking and bending fatigue accumulates, and the wirebonds fail open once reaching their fusing current [22], [25], [26].

Wirebonds have a large inductance, and wirebonds across multi-chip power modules also introduce parasitic imbalances. It has known with Si IGBT wirebonded multi-chip modules that the overshoot can be almost 3.5 times greater than the rated value, significantly increasing losses [27]. With fast-switching SiC devices, higher losses compounded with imbalanced parasitics in multi-chip power modules can have catastrophic effects during converter-level operation and even during a double-pulse test

of the package [28], [29]. This results in slowing the switching speeds to control the EMI and reduce the impact of parasitics, an undesirable result from attempting to package WBG devices as if they were traditional Si. Even though there are many concerns with using wirebonds for a multi-chip power module, especially for high voltage, it is the interconnect method used for commercial 10 kV power modules. These modules have 18 devices and parasitic inductances ranging from 16-37 nH, which is unideal for SiC 10 kV switching [29]. A promising variety of alternatives have been researched to address the consequences that wirebonds introduce for multi-chip power modules (Figure 3). The options include advanced wirebonding materials, flip-chip modules, pressure contacts, and vertical, three-dimensional interconnects.

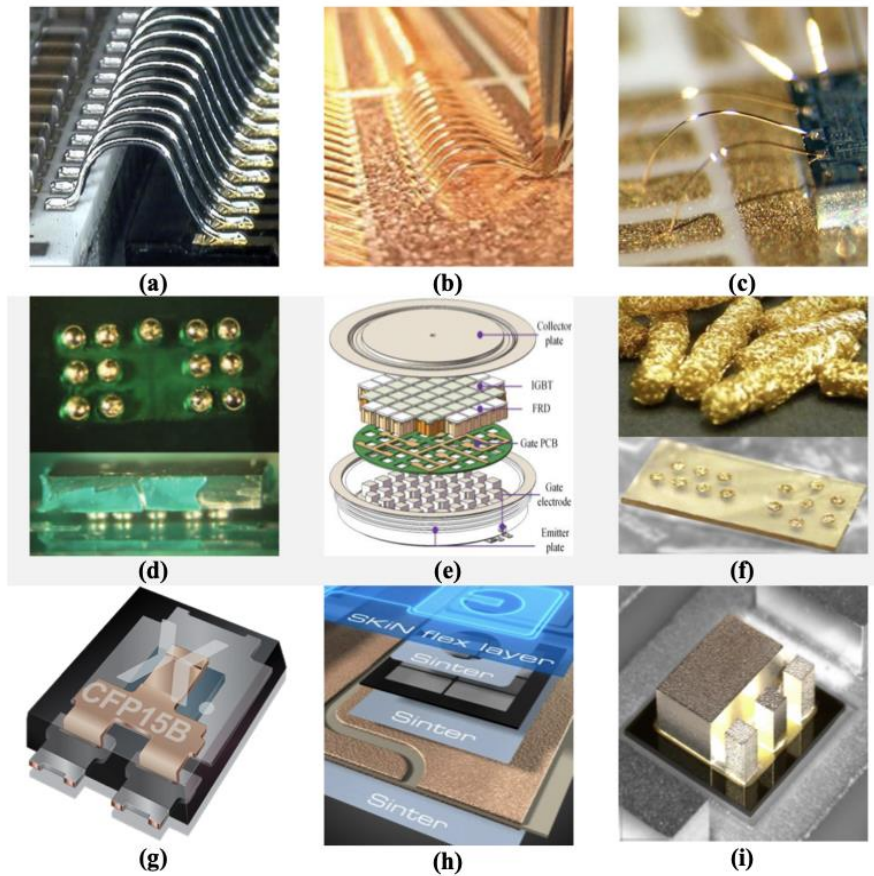


Figure 3: Various interconnects including (a) Al wirebonds [30] (b) Cu wirebonds [31] (c) Au wirebonds [32] (d) Flip-chip solder bumps [33] (e) Press-pack [34] (f) Fuzz buttons [35] (g) Cu clips [36] (h) Flexible PCB [37] and (i) Metal posts [21].

Industry companies such as ABB, Siemens, Heraeus, and Danfoss have employed advanced wirebonding techniques and materials in power modules [38]. While it would be beneficial to analyze the module layout and impact of the wirebonds on the overall parasitics and parasitic imbalances, the inside details of the modules are usually protected. The interconnect methods can still be investigated. Materials instead of aluminum have increased the reliability of wirebonds [20], [38], [39]. Copper wirebonds have better power cycling results over aluminum and high electrical and thermal conductivity. While improvements to the bonding process have been made, there is a risk of damaging the device during bonding due to the hardness of copper to the fragile die surface [38], [39]. Additionally, the oxidation of copper cannot be ignored even at lower temperatures, which can complicate manufacturability [20], [38]. Gold wirebonds are resilient to corrosion, highly conductive, and easily adhere to many typical metal surfaces in the package, making it an easy choice in terms of performance. Still, the cost of gold (Au) is not always feasible for large-scale production of packages [38], [39]. Thus, there has been more effort in improving the performance of copper (Cu) and aluminum wirebonds rather than transitioning to gold.

Even though changing the materials of the wirebonds can provide better electrical performance and, in some instances, reduce the parasitic inductance slightly, it does not address the overall problem that multi-chip power modules face with imbalanced parasitics [27]. To reach higher currents, many devices are still connected parallel; thus, many wirebonds are still within the module. The layout becomes the primary method to reduce the parasitic influences of the wirebonds [40]. Wirebonds also eliminate any potential for double-sided cooling, which is essential to the future cooling of WBG devices [20].

Changing the material of the wirebonds or layouts to reduce parasitic inductance is therefore deemed a workaround for this analysis and not a solution.

Flip-chip bonding is an interconnect method that inherently reduces parasitic inductances. Flip-chip bonding consists of solder balls (or bumps) distributed across the device, which solder directly to the substrate pads. This vertical interconnect method results in a lower profile package and minimized area needed for lateral wirebond connections, improving the overall power density of the module [33],[41]. The solder bumps create a layer between the device's backside and the substrate, improving thermomechanical reliability and reducing CTE mismatch between the die and the substrate [38], [41]. However, there are still drawbacks to this interconnect technology for medium-voltage power modules. It also proves difficult for medium-voltage devices, given creepage and clearance requirements and requiring underfills with high dielectric strength to reduce the peak electric field between the chip and the substrate, and the highest voltage module (6.5 kV) had only undergone a leakage current experiment to verify operation [42].

Another interconnect which proves more promising for the overall interconnect reliability and performance for multi-chip power modules is accomplished by applying pressure. Press-packs utilize pressure contacts with dry spacers to form connections across arrays of devices. The technology reduces CTE mismatch by utilizing molybdenum spacers to interface between the die and the terminals. There is improved reliability for medium-voltage and high-power applications since the dry contact eliminates common failure mechanisms of mechanical bonding seen with wirebonds and solder [43]–[45]. They also allow the interconnects to take on a new responsibility within the package: heat transfer.

This newfound technique paves the way for double-sided cooling as the topside of the devices can now have a large interconnect to conduct heat efficiently [43].

However, these successful press-packs for Si are not always translatable to WBG devices like SiC. SiC devices have notably less area for their contacts [45], [46], and the press-pack relies on a dry contact, needing tight tolerances to ensure even contact across all devices and also ensuring there are no potential gaps, which are difficult to control given surface roughness of different components [43]. Dry contacts also restrict the encapsulates that can be used, requiring complicated gas insulation methods with lower breakdown strength than silicone gels [47].

It was noted earlier how impactful the parasitics are for SiC devices. While press-pack modules can improve the magnitude and symmetry compared to wirebonded modules, press-pack modules tend to have a large form factor. Most of the modules cannot be insulated from the heat sink, and thus the inductance of the main power loop is still large [43], [44]. Additionally, while the layout of the devices can be symmetrical to aid in balancing, the actual contact strength relies on even pressure distribution [48]. Uneven distribution will result in disconnected devices, resulting in imbalanced current sharing, imbalanced thermal performance, imbalanced mechanical stresses, and overcurrent failures [34], [49].

Finally, 3-D interconnects led the way in producing multi-chip power modules that minimize the overall footprint by creating vertical packages. The interconnection can remain short, allowing for a decrease in inductance while allowing the spacing to be adjusted to accommodate high voltages by determining the clearance in vertical structures and reducing the peak electric field [50]. They also allow heat dissipation through the

topside of the device and open the door for more reliable double-sided cooling methods. Larger contact areas of 3-D interconnects decrease thermal and electrical resistance and increase the current-carrying capability. These 3-D interconnects include clips, pins, flexible circuit boards, PCB embedding, and metal posts.

Fuzz buttons are a dry contact used in press-packs instead of spacers. They act as a low-profile interconnect with compliance benefits and low parasitic inductances. Their compliance allows for more uniform pressure distribution than the rigid contacts in typical press-packs. Their small size also helps with adaption to the smaller size pads of SiC devices. However, these do not allow thermal conduction through them like metal posts do for double-sided cooling. Insulation is also a concern due to their low profile, and medium- and high-voltage packages need further insulation. The fuzz buttons were packaged with 1.2 kV devices but never experimentally verified. The typical insulation techniques are incompatible with fuzz buttons since they cannot be potted without degrading their flexible nature, and the alternative of hermetically sealed packages is costly [35], [46], [51].

More typical 3-D interconnects of metal posts have been utilized and are the main focus of this work. Mo posts enable low inductance designs and create sandwich-structure modules with high power density and good thermal conductivity for double-sided cooling [52], [53]. This is attractive for WBG devices due to the higher operating temperature than Si. Mo also has a low CTE (4.9 ppm/C) that is quite similar to SiC devices (3.7) as well as the aluminum nitride (AlN) substrates (5.3) [50], [54], [55].

These Mo post interconnects have been demonstrated in various modules [29], [52]–[54]. [54] utilizes Mo posts sintered to the die and substrates on one side of the double-sided cooled package and soldered to the other. Even though the CTE between the

substrate and interconnect selection reduces by choosing Mo posts, other materials in the package still dominate the thermomechanical stresses, and the failures manifest in the post bond. To reduce the thermomechanical stresses, a combination of Cu and Mo posts is needed, as well as the removal of the copper heat sinks. While this improved the thermomechanical reliability, the heat spreading of the package was sacrificed as the bonds of the post interconnects could not withstand the CTE of a Cu baseplate.

Similar work using only copper posts machined in a bridge-shape sought to improve a module's thermomechanical reliability and overall thermal cycling lifetime. During cycling, cracks still propagated in the bondline, indicating unresolved CTE mismatch between the interconnect and die. The complex shape of the interconnect further introduces fabrication and tolerance challenges and cost of manufacturability concerns [56]. Additionally, the wet contact choice of solder introduces thermomechanical stresses since there is a CTE mismatch to the copper post that significantly degrades during thermal cycling, which motivates the use of Mo [57].

Changing post materials from Cu to Mo has improved the CTE. However, more advanced material syntheses are investigated to improve compliance, one of the drawbacks of the rigid post interconnect. [58] explored a Cu-Mo-Cu gradient post to have improved CTE mismatch with Mo and the conductivity of the post with Cu. This module was only demonstrated as a single IGBT device. [59], [60] explored Mo-Cu and Mo plated with Au to reduce the CTE mismatch and create; however, the cost of these advanced material interconnects is a notable concern. Different interconnect shapes have also been explored for alleviating thermomechanical stresses at the bondlines [57]. Making an X-shaped or octagon-shaped post relieved stresses in simulation, but the better-performing shape in

FEM analysis had worse reliability in the experiment, questioning the benefits of these complex post shapes. Additionally, these are for very short heights, and the stress reduction would not apply at the spacing required for medium-voltage operation.

The use of metal posts for medium-voltage power modules is limited to research [38]. It is important to investigate why these metal post interconnects are confined to modules from academia and their associated fabrication challenges, especially for the future of MCPMs.

1.3 Multi-Chip Power Module Overview and Motivations for Fabrication Refinements for Wirebond-Less Multi-Chip Power Modules

While the typical packaging scheme in Figure 2 is deemed “typical,” that does not mean it should remain the best practice for the future of power electronics. Based on the advancements in interconnect technology, it is clear that the typical packaging schemes are not enough for the demands of power electronics applications today. It is impossible to achieve high voltage, high temperature, fast switching, and low loss power modules using these packaging schemes developed for Si devices regarding WBG devices. Advanced packaging techniques and designs are required to fabricate MCPMs for WBG devices such as SiC.

Improvements in packaging technologies have increased the feasibility of medium-voltage SiC modules through low-inductance designs and electrical insulation techniques to achieve high-speed switching without significant overshoot [21], [61]–[63]. Additionally, without balancing parasitics, the paralleling of multiple die becomes challenging. The complications of connecting modules to increase the current or voltage

rating within the converter have been discussed. Paralleling devices within the package are more attractive for higher power densities.

Figure 4(a) compares two commercial 10 kV MCPMs that utilize wirebond interconnects. Wirebonds need lateral pads to bond to while maintaining creepage and clearance requirements, resulting in large substrates and modules with significant power loop inductances. Figure 4(b) references two modules fabricated in the Center for Power Electronic Systems (CPES) that utilize Mo post interconnects between the die and the substrate. As shown, the shift from wirebonds to Mo posts allows for dense designs and vertical sandwich-structure modules with higher power density and lower parasitic inductances.

For SiC, the devices themselves can reach higher voltages than Si, but the paralleling of devices allows SiC to finally compete with the current ratings of Si IGBTs [64]. However, for proper operation, the module layout must be designed to balance parasitics between devices[65]. If the parasitics are imbalanced, the devices experience higher overshoots, higher losses, higher temperatures, and risk module failure [27], [65], [66]. The fabrication of these multi-chip power modules (MCPMs) is not trivial, and the next section will provide further insight into the design and fabrication of the MCPM from [50].

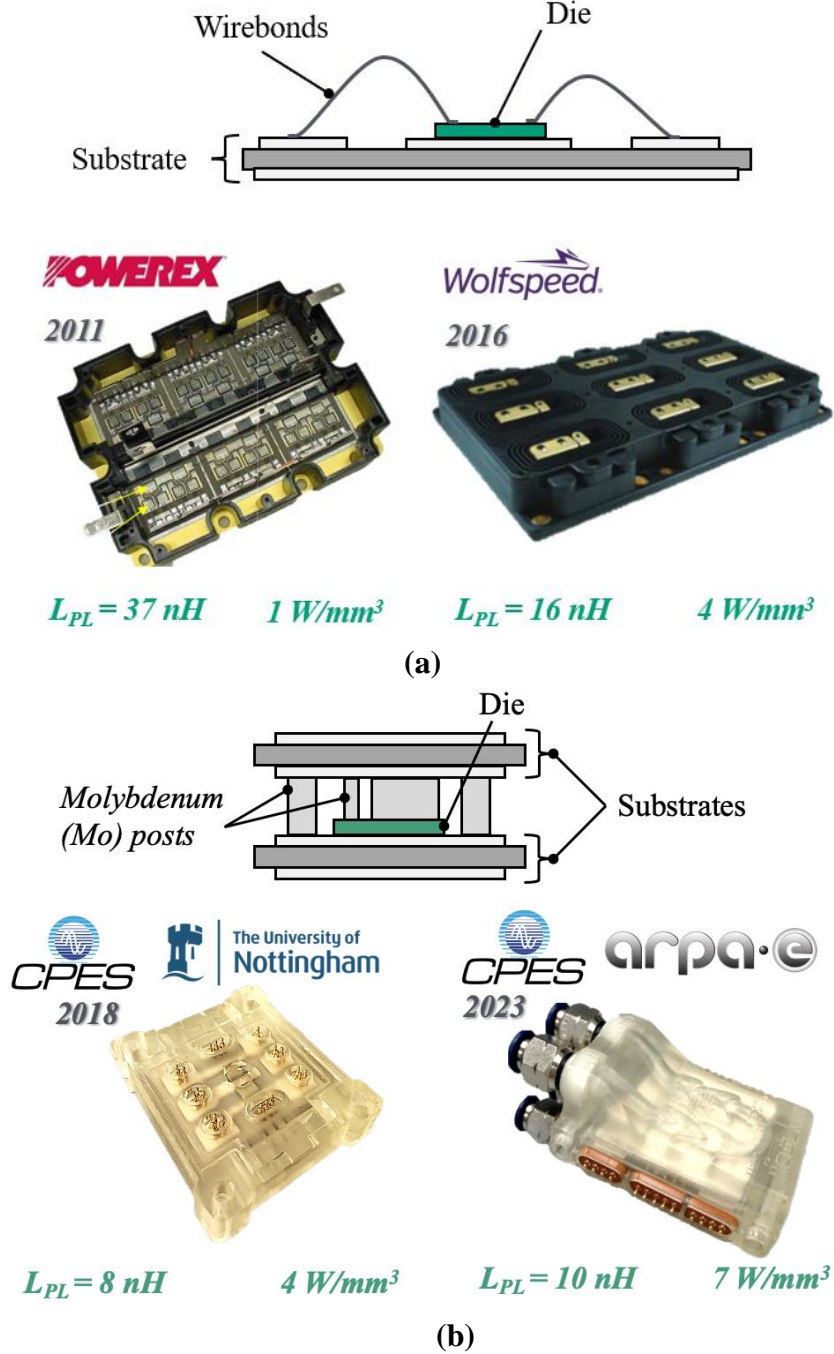


Figure 4: (a) Commercial 10 kV modules with wirebonds and their respective power loop inductance and power density [17], [18]. (b) CPES 10 kV modules with Mo post interconnects, and their respective parasitic inductance and power density improved from the wirebonded modules [29], [53].

1.3.1 Multi-Chip Power Module Overview

The MCPM that will be the focus of this work is a medium-voltage, SiC, sandwich-structure, half-bridge power module developed by DiMarino at Virginia Tech Center for

Power Electronic Systems [29] (Figure 5). Medium-voltage SiC devices enable modules with simpler control schemes, improved power density, and higher efficiency than modules that require series connections to reach 10 kV blocking voltages [67]. The module utilizes a symmetrical layout of the devices, which aids in balancing parasitics and promotes even current-sharing across devices [65]. Because of this, the modules can ideally scale from one die per switch position to multiple die per switch position. Overall, the module design in Figure 6 utilizes stacked, pressure-assisted silver sintered substrates, Mo post interconnects, silver sinter die attach, and spring-pin terminals. The module is populated with 13 kV SiC devices from the National Institute of Advanced Industrial Science and Technology (AIST). The details of these devices are in Table 1. This section will detail the design and advanced packaging techniques used to fabricate the MCPM.

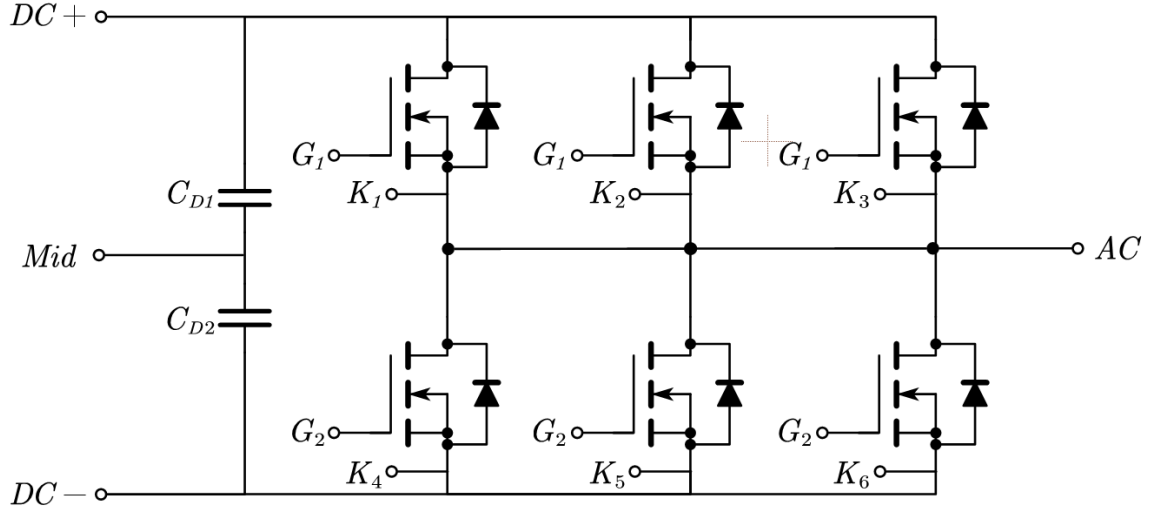


Figure 5: Half-bridge circuit schematic of the MCPM in Figure 6 with six devices, separate kelvin connections, and embedded decoupling capacitors.

Table 1: AIST 13 kV SiC MOSFET Device Specifications.

$V_{TH,MAX}$	Size	$R_{DS,on}$	$I_{D,MAX}$	V_{TH}	Backside Metallization	Frontside Metallization
13 kV	$6.94 \times 6.94 \times 0.35 \text{ mm}^3$	705 m Ω	5 A	3.4 V	Gold	Silver

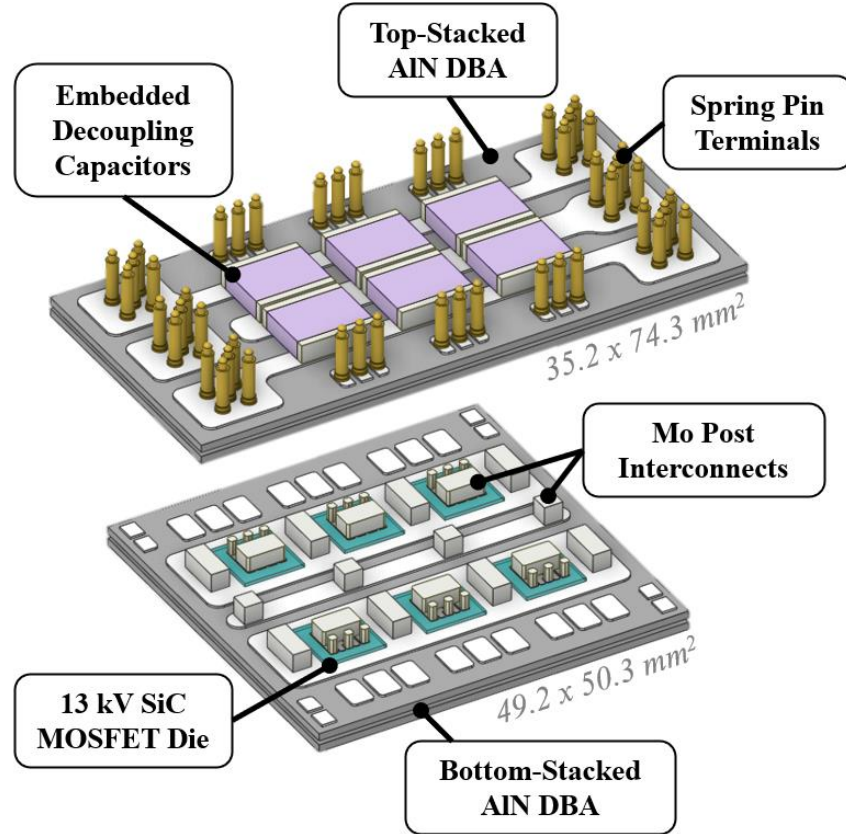


Figure 6: Medium-voltage, multi-chip power module with stacked aluminum nitride, direct-bonded aluminum substrates, silver sinter bonds, molybdenum post interconnects, embedded decoupling capacitors, and spring pin terminals.

The fabrication process is broken down step-by-step in Figure 7. Two AlN DBA substrates are sintered under pressure for the bottom and top substrates. Encapsulated, stacked substrates with the midplane connecting to half of the maximum potential reduce the peak electric field seen by the triple points, increasing the PDIV to 16.8 kV [50]. Vias within the ceramic connect the aluminum pads electrically. This substrate design is crucial for the medium-voltage operation of 10 kV-13 kV SiC MCPMs.

One of the critical components of the package design is the metal Mo posts interconnects for the gate, kelvin source, power source, drain, and midplane connections. Post interconnects attached using silver sintering within sandwich-structure modules enable low inductance, power-dense modules that allow double-sided cooling [52], [54].

While this module does not utilize double-sided cooling, the posts still enable the dense sandwich-structure module with low parasitics. This design is crucial to switch silicon carbide at high voltages with low overshoot. These posts are sintered to the die and the substrate using pressure-less silver sintering.

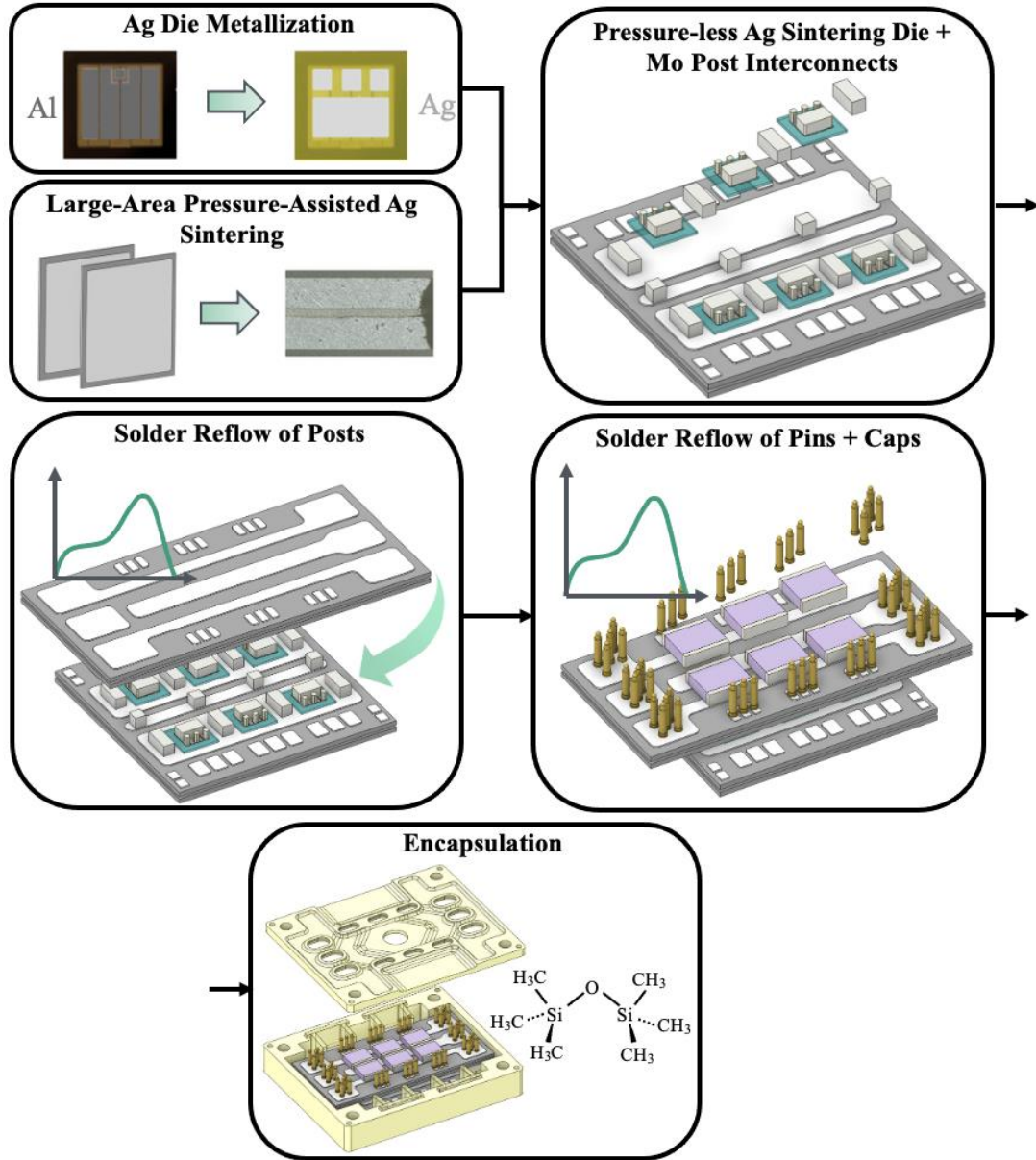


Figure 7: Fabrication process for the multi-chip power module in [50].

Nano-silver sinter paste is chosen to attach the posts to the die and the die to the substrate due to the low voiding and high thermal conductivity over typical solder alloys.

This is crucial since the SiC MOSFETs' drain side is the direct thermal path for conducting heat away from the device [68]. Silver sintering is also beneficial for building multi-chip, sandwich structure modules fabricated in sequential steps since the melting temperature of a sintered bond is 960 °C, and the sintering temperature of the paste is 250 °C. Using nano-silver sinter paste allows for the post interconnects to the die, the post interconnects to the substrate, and the die themselves to all be attached in separate steps without any bond degradation, easing the manufacturing process.

Three MOSFETs per switch position are symmetrically attached on the bottom DBA using pressure-less nano-silver sintering with additional posts for current conduction. The symmetrical layout of the devices and Mo posts allows for balanced parasitics and an easily scalable design.

The top substrate connects to the molybdenum posts by pressure-assisted soldering. Solder is chosen for this connection because the top substrate is not in the thermal path; thus, the high thermal conductivity of sinter paste is unnecessary. Soldering the top substrate also allows for compliance between all the posts since it is not as rigid an attachment method as sintering. This is beneficial for relieving any thermomechanical stresses the module may see during operation [50].

The terminals of the module are gold spring pins. Spring pins are beneficial for balancing parasitics with ease of symmetrical layout. The pins compress to the field-graded busbar, sealing off the module from the air and reducing the in-air peak electric field, allowing for 6 mm spacing between pads [69]. Next to the spring pins, the module has embedded decoupling capacitors, which reduce the parasitic inductance seen by the devices during switching and lowering voltage overshoot. The capacitors also allow faster

switching by connecting to an integrated common-mode screen to reduce EMI from these transients. The module is encapsulated in a silicone gel within a high-temperature resin housing through multiple degassing and curing steps to ensure a void-less enclosure [50].

In summary, these advanced packaging techniques allow for the successful design of medium voltage modules that have low inductance, reduced EMI, high PDIV, and paralleled SiC devices for higher current operation. However, while the techniques are necessary, their fabrication is not trivial, and it can introduce concerns about yield and manufacturability for these dense, sandwich-structure MCPMs with post interconnects.

1.3.2 Motivation for Fabrication Refinements of Multi-Chip Power Modules

The advanced packaging techniques of the module, displayed in Figure 8, enable low-inductance, high-density, scalable modules. They also introduce new challenges to the fabrication process, requiring refinement to increase the yield of sandwich-structure modules with wirebond-less interconnects.

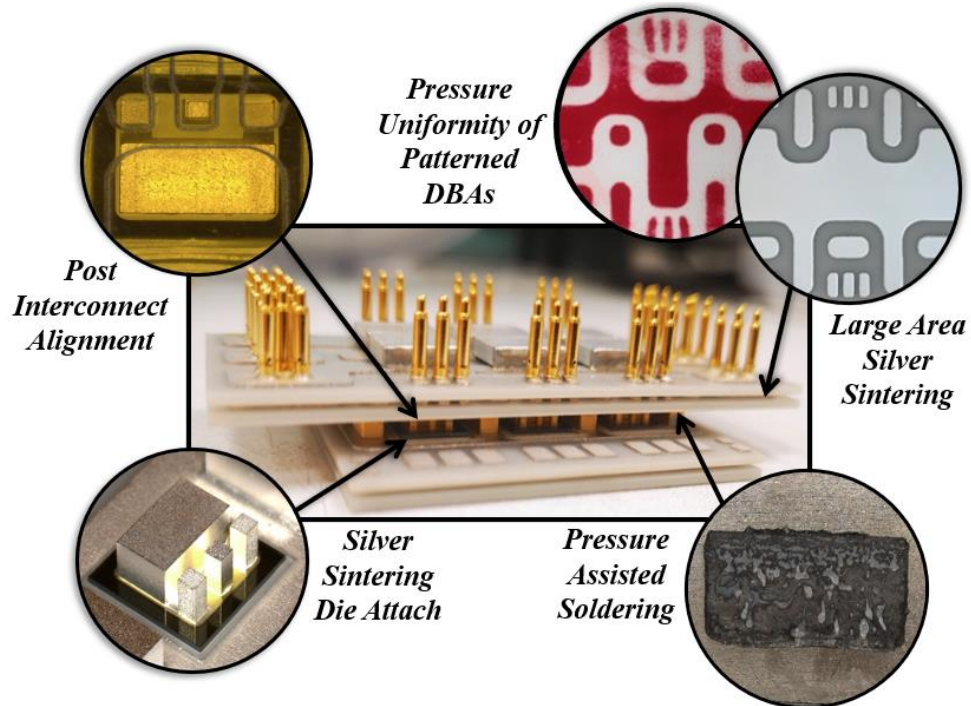


Figure 8: Advanced packaging techniques and fabrication refinements developed for MCPMs.

Encapsulated silver-sintered stacked substrates are used in medium-voltage packages to relieve the peak electric field at triple points, increasing the PDIV and module reliability [50]. Uniformity of the bondline in these stacked substrates is critical to the thermomechanical reliability of the package as well as ensuring electrical connections are sufficiently made. Unlike solder, which melts during reflow and smoothly coalesces to form a bond between two connections, any defects in the silver sinter bond before sintering will remain after the bond is formed, even during a pressure-assisted sintering process [70]. The sinter paste will not coalesce or bridge any gaps between connections, meaning the bondline must be determined precisely.

Post interconnects attached using silver sintering within sandwich-structure modules enable low inductance, power-dense modules that allow for double-sided cooling [52], [54]; however, machined post interconnects have non-negligible tolerances, which become more problematic as the number of posts scales up with increasing die in parallel for current scalability. Even if the post heights are identical, package assembly processes and attachment methods can tilt the posts. The phase change of the solder and unpredictable outgassing of solder flux during reflow can tilt the posts or render connections useless [71]. Alternatively, when the posts are placed in the sinter paste for the die interconnect attach, the bondline thickness can vary if placed with a different amount of pressure every time, creating a mismatch in the heights. The tilt can cause some of the smaller gate and kelvin posts to disconnect altogether.

Additionally, soldering MCPMs involve a large thermal mass for which the typically soldering reflow profile was not created. Temperatures and ramp rates need to be

scaled to reduce void creation and complete reflow; however, with increased temperatures and times to heat the large thermal mass, there is a chance for de-wetting the solder [72].

Ultimately, these fabrication challenges lead to misalignment or disconnected post interconnects. For an MCPM, post interconnect planarity and alignment are crucial to avoid gate-source shorts or missed connections that can render switch positions useless and limit current capability. This does not solely arise from the post interconnects themselves, but every layer in a sandwich-structure module can contribute to non-idealities and non-uniformity. Therefore, every step and every component in the assembly procedure is critical to analyze and understand its impact on the module fabrication, and refinement is paramount to achieving current scalability and improving yield for MCPMs.

1.4 Research Objectives and Thesis Organization

Advanced packaging techniques enable low-inductance, high-density, scalable modules. They also introduce new challenges to the fabrication process, requiring refinement to increase the yield of sandwich-structure modules with wirebond-less interconnects. These advanced packaging techniques are required to elicit the benefits that WBG devices can offer if packaged correctly. The yield of these sandwich-structure modules requires an investigation into every step of the assembly procedure. However, it also requires an investigation into the core of the module components and how their manufacturability as a part contributes to the overall assembly, traditionally done with a statistical tolerance analysis. Every step and every component is critical, and refinement is paramount to achieving current scalability and improving yield for MCPMs.

In the next chapter, the refinement analysis will start with the pressure-assisted sintering of the patterned MCPM substrates and develop a process for repeatable bondline

uniformity as well as analyzing the warpage of the substrates during the process. Chapter 3 will investigate the benefits of pressure-assisted soldering to improve bond quality in the power and signal loops and the necessary steps to solder large thermal masses properly. A statistical tolerance analysis of the assembly process is conducted in Chapter 4 to understand the manufacturability of the module by bridging the refinements and the components together, quantifying the yield of the modules from a statistical lens. In Chapter 5, the fabrication and testing of a multiple scaled-down version of the MCPM with two die per switch position verifies the functionality of the refinements. The MCPM is fabricated using the refinements and conclusions drawn from the statistical tolerance analysis. Finally, Chapter 6 will provide a summary, conclusion, and key takeaways for future works.

Chapter 2 Fabrication Challenges and Refinements of Sintering in Wirebond-less Multichip Power Modules

2.1 Introduction

The base of the MCPM is the substrate, which, when patterned, provides the electrical connections for the power module. As more die are connected in parallel, the substrates grow in length to ensure no thermal coupling and to route more electrical connections. As mentioned, these substrates are stacked and bonded using pressure-assisted silver sintering to reduce the peak electric field seen at the triple points within the module to operate above 10 kV [50].

This section will investigate necessary refinements to the sintering process to create strong, uniform, reliable bonds, not only for the substrates but also for the die-attach and post-attach to the substrates. The bond is vital for reducing the thermal resistance of the module as well as extracting the heat from the drains of the vertical SiC devices. Thus, silver sinter paste provides a low-voiding, highly reliable, and more thermally conductive solution to extract heat from WBG devices [73]. Non-uniform bondlines result in poor bond quality, resulting in bonds that will not perform reliably over time and eventually fail. Each sintered bond layer for the substrates, die, or posts can impact the planarity of the entire module, whether due to uneven bondlines from the placement of posts or substrate warpage that occurs from the pressure-assisted sintering process.

While larger bond areas need pressure applied during sintering to obtain a high bond strength, smaller bond areas can typically be sintered without pressure using a nano-silver paste [68], [73]. The Mo post interconnects are attached to the die in this manner, as well as the die and other posts to the substrate, as shown previously in Figure 7. However,

using post interconnects introduces two main challenges: (1) proper alignment to the small pads of SiC, and (2) ensuring planar connections by controlling the uniformity of the sinter bondline. Defects or excessive paste application introduces tilt across the post and die, shorts the gate and source, or causes paste migration onto the field grading. It is essential to refine these fabrication steps for the MCPM to improve yield since the substrate is the base of the module, and the silver sintering of the die and interconnects is vital for the functionality of WBG devices in advanced packages.

2.2 Pressure-Assisted Large-Area Sintering Methodology of Patterned Substrates for Multichip Power Modules

While the die and posts can be sintered without pressure and still have strong bonds, large-area bonds tend to require pressure. Sintering has many benefits over soldering, such as high thermal conductivity, lower voiding content, and better thermal cycling capabilities. However, pressure-assisted sintering elicits further benefits. Much work has been done to investigate the impact of pressure while sintering, especially for large areas such as substrates. The following section will detail the previous work with pressure-assisted sintering involving sinter paste, sinter preform, and the benefit of nano-silver sinter over micro-silver sinter.

2.2.1 Previous Work on Pressure-Assisted Large-Area Sintering of Plain Substrates

As noted, stacking substrates aids in relieving the peak electric field around the triple points of a package by connecting the middle metal to the mid potential. Soldering such a large area would create large voids and disrupt the main thermal path for the bottom substrate connected to the drain of the devices. Thus, bonding with silver sinter paste is essential to ensure low voiding and the benefits of increased thermal conductivity.

Pressure-sintering of micro-silver paste was explicitly investigated as a more reliable attachment for large-area bonding as compared to a baseline of solder, in this instance, to bond a 50.8x50.8 mm² substrate to a copper baseplate and improve heat extraction compared to typical thermal interface materials [74]. The sintering pressure and temperature are not provided for the bonding step of the substrate to the Cu baseplate. Thermal cycling results show that the bonding of the micro-silver paste still outperformed solder by 1000 cycles, giving enough evidence to explore the benefits of silver sintering for the packaging of WBG devices that experience higher temperatures, even close to the melting and reflow temperature of many solders.

Micro-silver paste requires pressures greater than 40 MPa for sintering below 300 °C. This pressure would not be feasible to bond the substrates for this MCPM since the vias in the AlN ceramic will crack at pressures greater than 3 MPa [70], [75]. Even if used for die attach, most SiC devices cannot experience 40 MPa without cracking. Thus, micro-silver paste would not be suitable as a pressure-assisted die attach method and is unsuitable for the pressure-sintering of substrates with vias.

Since micro-silver sintering required high processing temperatures and high pressures that were not feasible for manufacturing these MCPMs, nano-silver sintering has become a feasible replacement to allow for silver sintering at lower temperatures (240-280 °C) and without pressure to achieve high bond strengths still [68], [73], [76]. Different substrates and metallization combinations were explored with different sintering times to achieve the highest shear strength possible. Overall, nano-silver allowed for exceptional shear strengths at low temperatures and minimal to no pressure compared to micro-silver paste.

The University of Nottingham [77] tested the difference between pressure and pressure-less sintering with nano-silver paste of two plain, Si_3N_4 substrates sized 40x40 mm², with 0.3 mm of copper and 1 mm of ceramic, similar size to the DBA 1-DBA 2 of the MCPM that is the focus of this work. Each substrate had a screen-printed layer of silver sinter paste dried before sintering two substrates without pressure and two substrates with 3 MPa at 250 °C for 20 minutes. Profilometer scans show that the pressure-assisted sintered substrates have a consistent bondline thickness, while substrates without pressure resulted in a sloped bondline. This was due to squeezing out of the paste while overlaying the substrates, creating a non-uniform bondline during the sintering process. The paste in the pressure-less bond was concentrated in the center, having many voids as large as 400 µm at the edges. The significant voiding is a result of the wet screen-printing process. The pressure-assisted sintered bondline exhibits only 80 µm voids.

While the nano-silver paste is more reliable than solder when bonding large areas, the drawbacks to screen printing large amounts of paste must be addressed. There is a high likelihood of uneven bondline thickness, which can create concentrated stresses as some regions of the bond now have higher resistances [77], [78]. While the paste oozing during screen printing and sintering cannot short connections on plain substrates, it can lower the PDIV of the module if it oozes onto the ceramic since the creepage requirements of the substrate were carefully designed [61]. When it comes to patterned substrates, the oozing of the paste could quickly short many different connections, rendering the MCPM useless. This work motivates the use of pressure-assisted sintering and to explore the use of silver preform. Preform controls the bondline thickness, reduces voiding, and reduces the risk of shorting pads.

A final study compared the benefits of nano-silver paste to nano-silver preform to improve the bond's reliability and ease the concerns of oozing paste from a wet screen-printing process while bonding two substrates. In [62], two 49.2 x 23.1 mm² substrates are sintered together with nano-silver paste and nano-silver preform. Like previous methods, the paste is screen-printed and dried before undergoing a sintering profile at 250 °C at 1 MPa for 30 minutes. In contrast, the preform is pre-dried on a polyimide carrier film, eliminating the need for the drying step. The preform is then stamp transferred to the substrate at 1 MPa for 60 seconds at 140 °C. The substrates are then sintered at 3 MPa for 90 seconds at 250 °C.

C-SAM images show that the preform stamp-transferred bond is more uniform than the screen-printed bond. The screen-printed sintered substrates had two times higher surface roughness than preform-sintered substrates after 500 thermal cycles. Additionally, from a manufacturability perspective, the processing time is shortened from 30 to 3 minutes since the screen printing and drying steps are no longer needed. Nano-silver preform can achieve a strong, reliable, uniform bond at low pressures (3 MPa) compared to micro-silver sintering (40 MPa), which needs a drying process and sintering.

The larger, patterned substrate is missing from these main works regarding the sintering of substrates. Patterned substrates are required to route the electrical connections to the many paralleled die in multi-chip power modules. Additionally, while there are studies documenting the warpage of substrates to baseplates during pressure sintering, soldering, or thermal cycling, there is little work done on how these high-pressure sintering processes between substrates impact the warpage of the substrate. This concept can significantly impact the planarity of sandwich-structure MPCMs. The following

subsections will explore these concerns using the substrates for MCPMs shown in Figure 9 and Figure 10.

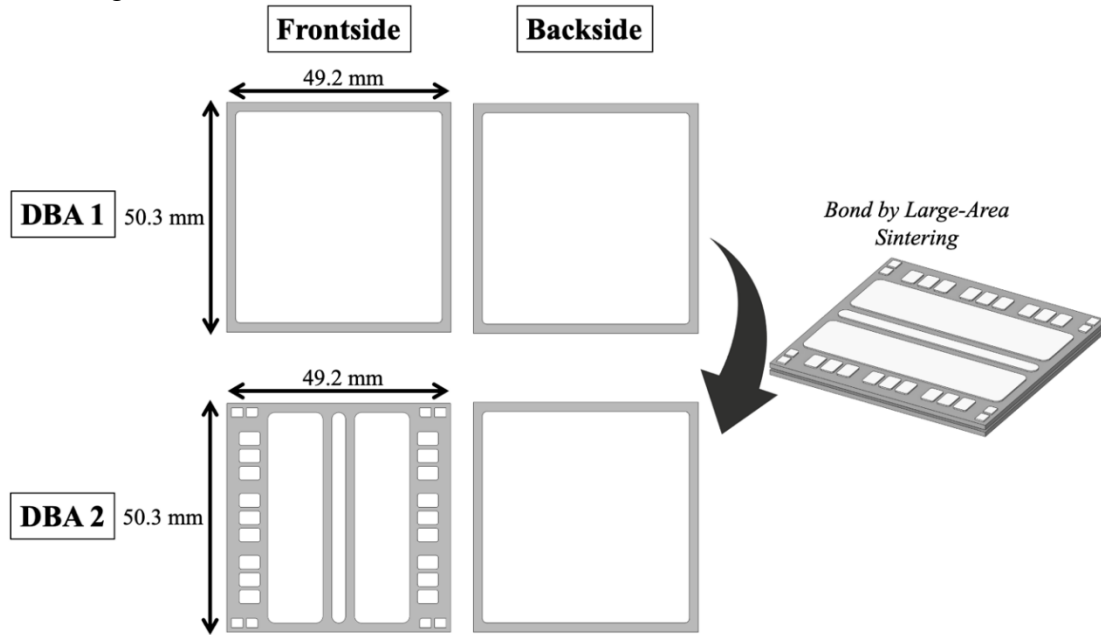


Figure 9: DBA 1 and DBA 2 sizing, patterning, and stacking method.

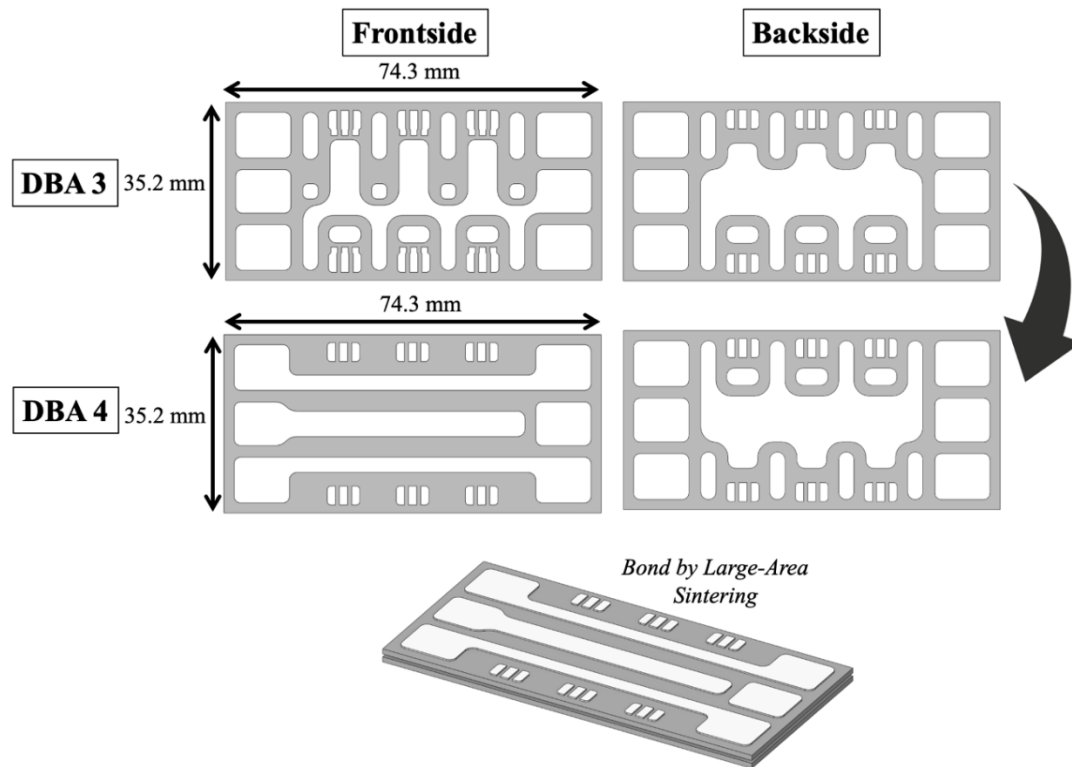


Figure 10: DBA 3 and DBA 4 sizing, patterning, and stacking method.

2.2.2 Challenges of Pressure-Assisted Large-Area Sintering of Patterned Substrates

As mentioned, [62] made great strides in understanding the reliability performance of nano-silver preform and developing a method to sinter large-area substrates without cracking their vias (Figure 11). Across a larger substrate, silver sinter preform can control the bondline thickness and improve voiding better than silver sinter paste. However, the substrates utilized in [62] to demonstrate the large-area sintering was not patterned and were less than twice the size of the substrates used in the MCPM. Larger, patterned substrates have many crevices and complex patterns, especially for MCPMs. These intricacies introduce new challenges to the previous large-area sintering process.

When using the method detailed in [62] to stamp transfer silver preform to a bare substrate, the pressure-sensitive film indicates that some of the preform may be transferred to unwanted spots on the ceramic and may not be sufficiently transferred to all of the aluminum pads, as shown in Figure 12. Even with a smaller patterned substrate, the methodology in [62] still had trouble achieving a uniform transfer. Transferring the silver preform to the ceramic could result in a short circuit between adjacent pads or decrease the PDIV. Conversely, suppose the silver preform is not evenly transferred to the Al pads. In that case, it can create open connections and non-uniform bondlines because some substrate areas will not have silver preform.

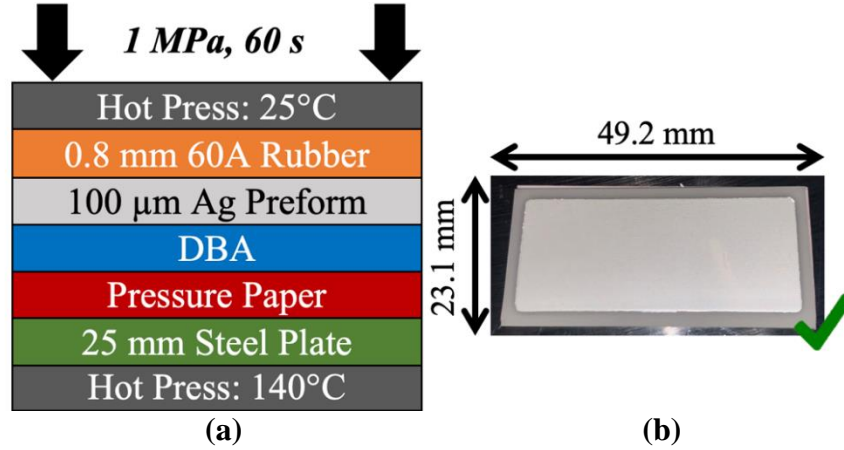


Figure 11: (a) Previous method developed for large-area sintering of substrates by stamp transferring Ag preform and (b) successful transfer with that method on a smaller, plain substrate.

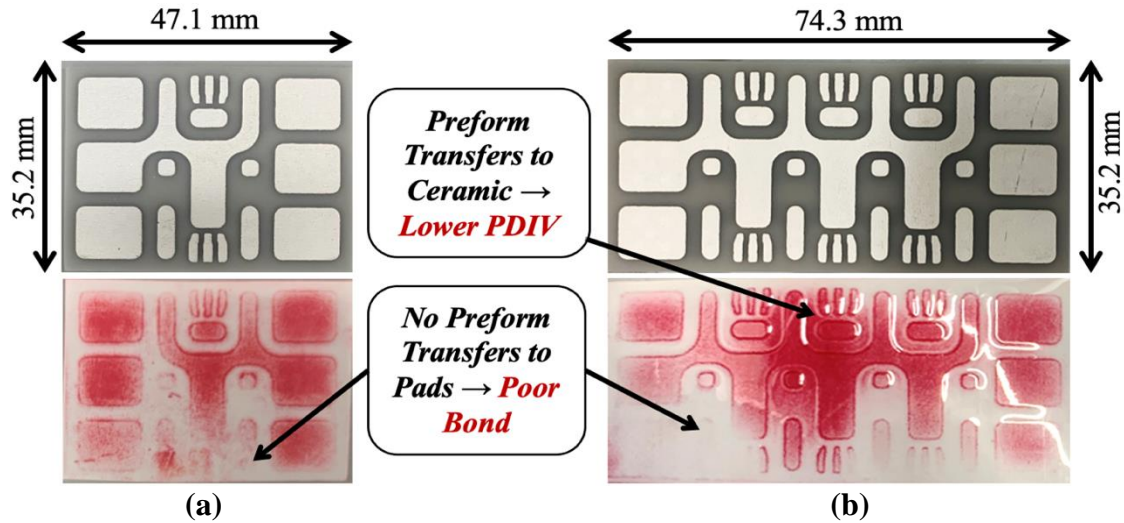






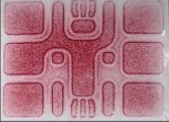





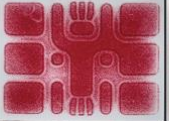

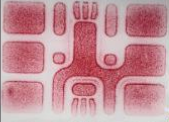








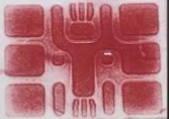


Figure 12: (a) Non-uniform, two-die patterned substrate's pressure paper using the Ag preform stamp-transfer method developed for small, plain substrates. (b) Non-uniform, MCPM patterned substrate's pressure paper indicating a non-uniform preform transfer using the previous methods detailed.

2.2.3 A New Method for Pressure-Assisted Large-Area Sintering of Patterned Substrates

The larger, patterned substrate for an MCPM requires a new stamp-transfer process for successful preform transfers. The materials and methodology in [62] were used as a starting point. An experiment uses the substrate in Figure 12(a) to test different pressures from 1-2 MPa, durations from 60-90 seconds, rubber thicknesses of 0.8 and 1.6 mm, and

rubber durometer-shore hardness classifications of medium-soft (40A), medium (50A), and medium-hard (60A). Testing different rubber hardness classifications and thicknesses is paramount because how the rubber deforms considerably impacts even pressure distribution across the large-area substrate and creviced patterns. Analysis of the resultant pressure-sensitive film in Table 2 indicates the success of each test in achieving a uniform transfer. The near-ideal transfer was achieved with 0.8 mm medium-hard (60A) rubber under a pressure of 1.5 MPa for 90 seconds with dark coloring on the Al pads and minimal coloring on the ceramic.

Table 2: Evaluation of Pressure Sensitive Film with Pressure Varying From 1-2 MPa, Time From 60-90 Seconds, Thicknesses Varying From 0.8-1.6 mm, and Rubber Durometers of Medium-Soft, Medium, and Medium-Hard.

Pressure + Time →				
Rubber Hardness + Thickness ↓	1 MPa 60 s	1.5 MPa 90 s	2 MPa 60 s	2 MPa 90 s
40A, 0.8 mm				
40A, 1.6 mm				
50A, 0.8 mm				
50A, 1.6 mm				
60A, 0.8 mm				
60A, 1.6 mm				

The new transfer process (1.5 MPa, 90 seconds, 60 A rubber, 0.8 mm thick) was tested on the larger MCPM substrate using the stack-up in Figure 13(a). The new process improved the pressure distribution and allowed the successful transfer of silver preform to the substrate, as seen in Figure 13(b). The process was successfully repeated on eight MCPM samples and seven of the smaller patterned substrates, each showing a significant improvement over the pressure paper results from the prior method seen in Figure 12, and all had successful, uniform silver preform transfers.

A mylar stencil further de-risks the transfer step to prevent any preform from transferring to the ceramic. The mylar stencil is 100 μm thick, so it sits well below the 300 μm thick aluminum pads and does not interfere with bond uniformity during the transfer process. The substrates were sintered according to the profile determined in [62] at 3 MPa for 90 seconds at 250 $^{\circ}\text{C}$ since the substrate performed reliably in thermal cycling tests.

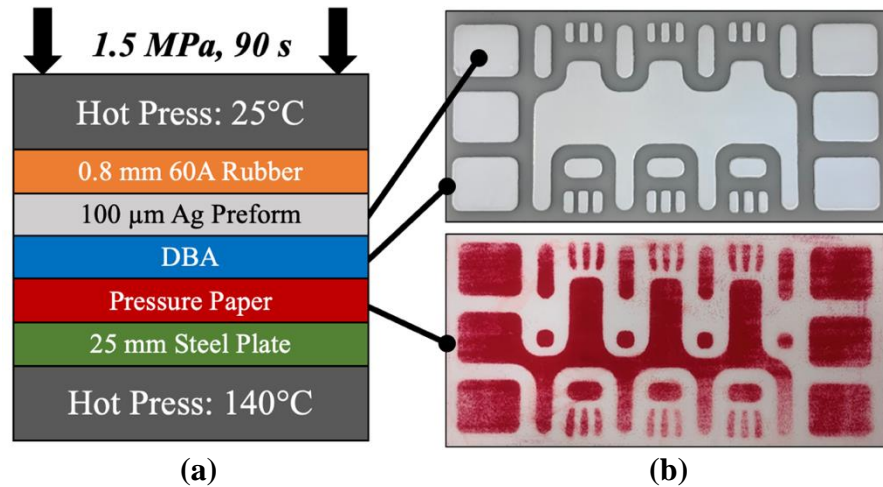


Figure 13: (a) New transfer method with 1.5 MPa, 90 s, and 0.8 mm 60A (medium) rubber and (b) successful transfer of preform to substrate showing uniform pressure paper.

2.3 Analysis of Substrate Warpage during Pressure-Assisted Large-Area Sintering

The previous section details a successful method of repeatedly transferring silver preform to patterned substrates using a stamp-transfer method. This new method improves the bondline uniformity. Reliability testing was conducted on large-area sintered DBA substrates in [62] and demonstrated improved performance of substrates with silver sinter preform over screen-printed silver sinter paste. The work done in [62] does not detail any analysis of the substrate warping after undergoing the large-area sintering process. This detail could explain why the modules built faced yield problems when trying to solder the top posts to the top stacked substrate, assuming they did not end planar. Investigating and understanding if the substrate warpage impacts the non-planarity of the posts in sandwich-structure modules is essential.

A literature review was conducted on potential causes of warpage to large-area substrates, some from the studies on the sintering bond quality in the previous section, but some did not provide details about the substrate warpage. The literature review focused on the impacts of temperature, heat, pressure, and the CTE mismatch of materials with substrates of similar sizes to this MCPM but varied thicknesses. Very few studies detail the effect of pressure-assisted large-area sintering of similar substrates; thus, work detailing the impact of sintering and soldering of substrates to baseplates and the impact of thermal cycling of substrates were added to the review to understand the general behavior of substrate warpage.

Work of large-area soldering and sintering substrates to baseplates was analyzed to see the impact of bonding dissimilar materials under an intense heating profile on substrate

warpage. Since the baseplate is typically thicker in the substrate, and in these cases copper, it dominates the final substrate warpage. Due to its high CTE, when the copper baseplate cools from a peak temperature, it will shrink, pulling the bonded substrate into a convex shape [79]–[81]. The magnitude of the warpage is dependent on many parameters, such as the thickness, CTE, and Young’s Modulus. However, the work mainly focuses on the thickness of the substrate and baseplate and the CTE mismatch between the two [81], [82]. [79] concluded that the thinner baseplates were more susceptible to warping since they were not as stiff as thicker substrates. This induced more warping in the substrate during the solder reflow profile. Additionally, reducing the CTE mismatch between the baseplate material and substrate material decreased the magnitude of convex warpage at room temperature [81], [83].

Pre-bending the substrates aided in reducing the final warpage magnitude of these substrates. Two works approach this with opposite methods [79], [84]. By matching the same shape (i.e., concave baseplate and concave substrate), the bond is more reliable than a planar substrate and a warped baseplate. However, no effort is made to analyze the overall warpage of the substrate. [84] pre-bends the baseplate convexly so the expected concave behavior of warping becomes planar instead, reducing the warpage of the overall substrate.

From the baseplate sintering and soldering analysis, three concepts examine the behavior of sintered substrates: The material with the dominating CTE will control the direction of the warpage, the thinner materials tend to warp more drastically, and pre-bending of the materials can change the final warpage of the materials. What is missing from these works and how it relates to sintering stacked substrates is the application of

pressure, the difference between the thickness of the ceramic and the thicknesses of the metal, and the idea of similar materials with similar CTEs but with different patterns.

The symmetry of the metal patterning can impact the final substrate warpage [81]. This work does not use pressure and is used solely to understand temperature impacts. If the substrate had uneven patterning on both sides, the warpage was more intense due to imbalanced metal. This patterning can also influence the concavity of the substrates warping [82]. Additionally, symmetrical metal showed much less thermomechanical stresses during thermal cycling. While Si_3N_4 DBC has a much more significant CTE mismatch than the MCPM substrates (AlN DBA), the overall behavior is still essential to analyze to find trends for these patterned substrates.

In [75], the simulation utilized the MCPM substrates in this work and simulated pressure-sintering. In this simulation, the substrates warped only a few microns. However, experimentally, the warping was a few orders of magnitude higher. The work noted that 10 kN (about 4 MPa) resulted in the cracking of the vias within the substrates and was not carried forward with the different samples sintered. This cracking can alter the final warpage results and may not represent actual warping behavior. Thus, it is vital to understand the impact of the aluminum pad pattern in terms of the CTE mismatch with the ceramic. This work is the closest available to this work but needs to explain the phenomena behind the minimal warpage in the simulation and the extreme warpage seen in the experiment. Additionally, the pressure applied was too high because it caused cracks in the substrate and the vias. Nonetheless, results were used as a baseline to understand the warping of MCPM substrates with complex patterns.

Simulations were conducted with ANSYS Workbench transient thermal and static structural to better understand the phenomena seen in literature with substrate warpage when applied to these large MCPM substrates. After the transfer process is completed from the last section, the hot plate temperatures are raised to 200 °C for the top hot plate and 250 °C for the bottom plate. The stack-up in Figure 14 is the same as the substrates sintered in [62] and is constructed by cutting the rubber covered with a layer of Kapton to the same size as the substrates being sintered.

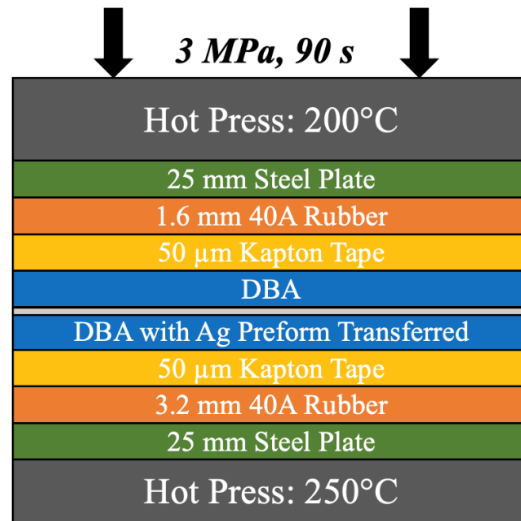


Figure 14: Stack-up for the pressure-assisted sintering of large-area substrates in a pneumatic hot press.

Once placed between the hot plates, the pressure increases to 3 MPa within 30 seconds, holds for 90 seconds, and is immediately released. In the simulation, the two temperature profiles are ramped to their maximum to emulate the substrate meeting the hot plates until reaching bonding temperature (250 °C), then held for 90 seconds before cooling to room temperature with natural convection. The overall profile for the pressure and temperature is shown in Figure 15.

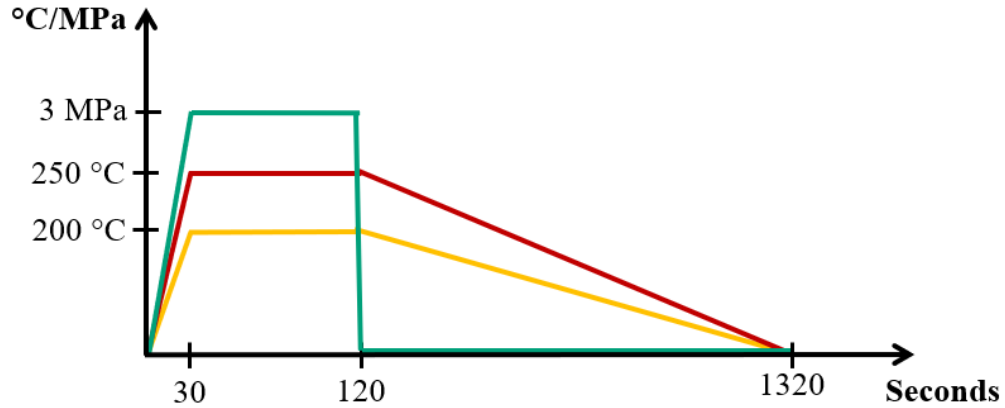


Figure 15: Hot press pressure profile (green), bottom hot plate temperature profile (red), and top hot plate temperature profile (yellow) for the ANSYS thermomechanical simulation of pressure-assisted silver sintering of stacked substrates.

The geometry was simplified only to include the bottom hot plate as a fixed support, and the pressure was applied directly to the substrate. The substrate is a frictional contact with the bottom hot plate to allow it to deform correctly. The simulation conditions are detailed in Table 3. The boundary conditions for the substrates are noted in Figure 16 only for DBA 1-DBA 2 but are the same for DBA 3-DBA 4. The meshing for each is in Figure 17 and Figure 18, respectively. The meshing of the sintered silver layer was not refined to save computational time since it will not contribute to the overall warpage as much as the bulk metal materials.

Table 3: ANSYS Workbench Simulation Parameters.

Top Hot Plate	200 °C
Bottom Hot Plate	250 °C
Pressure	3 MPa
Total Profile Time	1320 seconds
Ramp to Temperature + Pressure	30 seconds
Hold Temperature + Pressure	90 seconds
Cooling	20 minutes to 25 °C
Substrate Contacts	Merged Bodies
Substrate to Hot Plate Contact	Frictional (0.2)
Weak Springs	On
Surface Effect	On

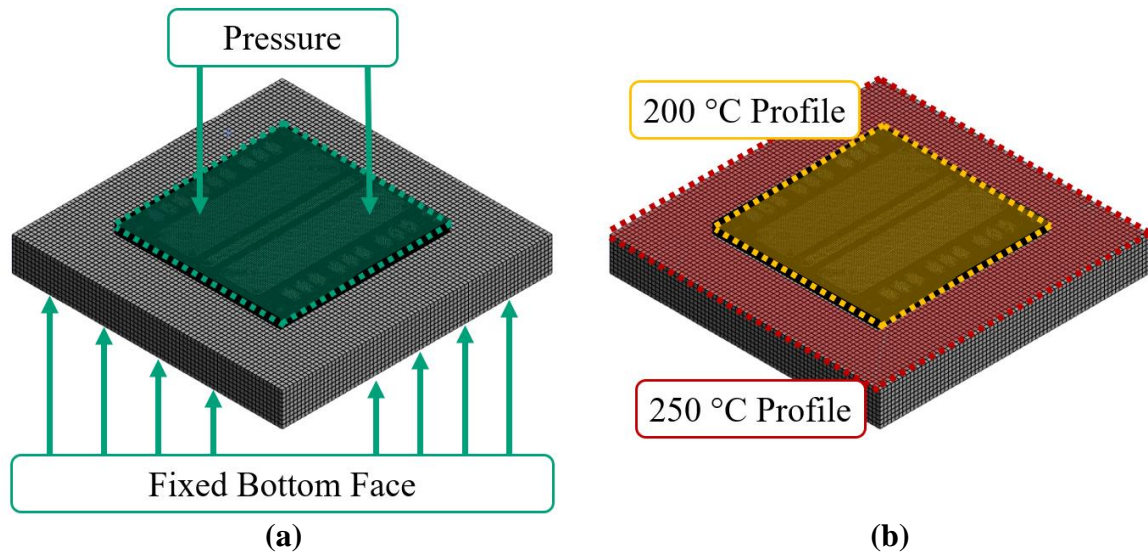


Figure 16: (a) Pressure boundary conditions for DBA 1-DBA 2. (b) Temperature boundary conditions for DBA 1-DBA 2.

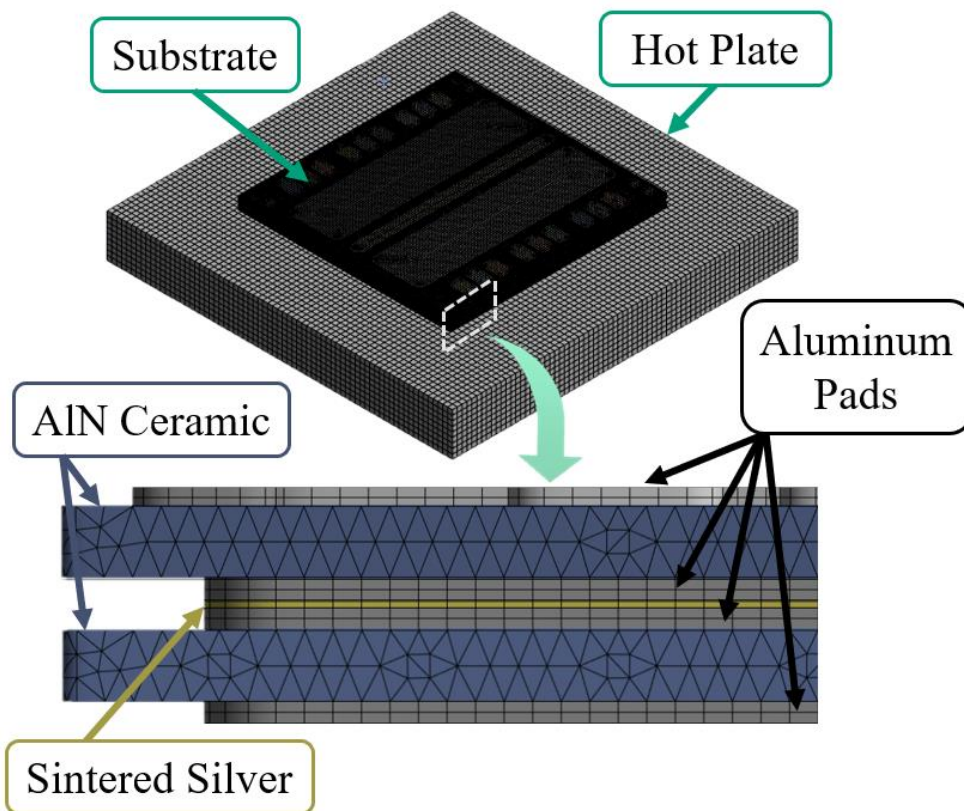


Figure 17: Meshing for DBA 1-DBA 2 thermomechanical simulation.

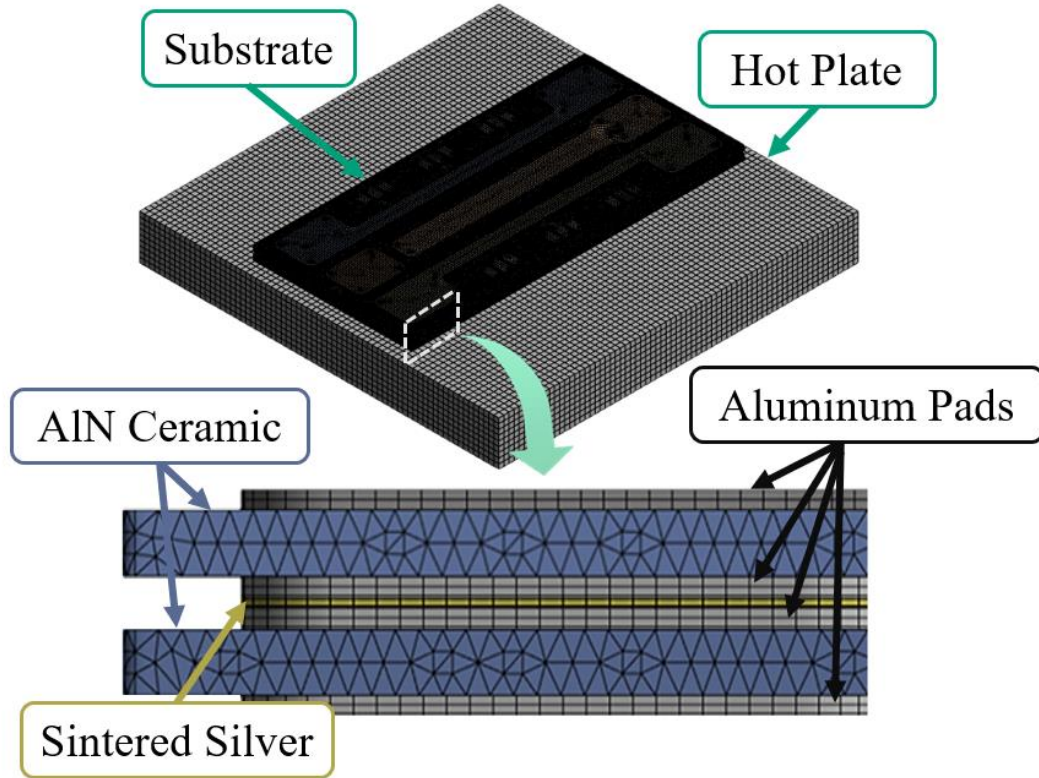


Figure 18: Meshing for DBA 3-DBA 4 thermomechanical simulation.

The simulation results show that both substrate warp convexly, with a magnitude of $12.2\ \mu\text{m}$ for DBA 1-DBA 2 and $12.4\ \mu\text{m}$ DBA 3-DBA 4. This is influenced by the patterning of the substrate geometry, which for both substrates, there is more metal on the backside of each stacked substrate, as noted in Table 4. Thus, the amount of metal shrinking dominates the concavity during the cooling process [74], [82].

Table 4: MCPM Substrate Metal Patterning Surface Areas as Referenced in Figure 9 and Figure 10.

DBA Pattern Location in Figure 9 and Figure 10	Metal Surface Area (mm^2)
DBA 4 Frontside	2670.18
DBA 4 Backside	3149.14
DBA 3 Backside	3149.14
DBA 3 Frontside	2987.19
DBA 2 Frontside	3319.43
DBA 2 Backside	4238.19
DBA 1 Backside	4238.19
DBA 1 Frontside	4238.19

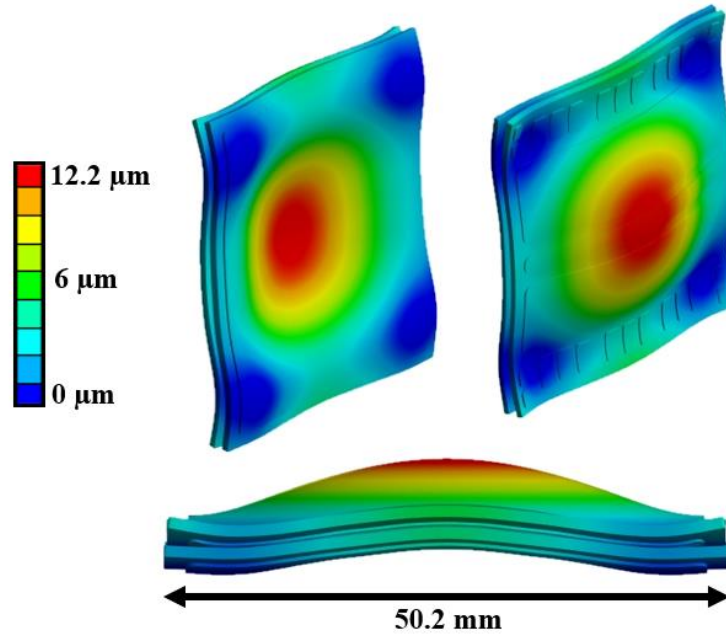


Figure 19: DBA 1-DBA 2 ANSYS thermomechanical deformation results.

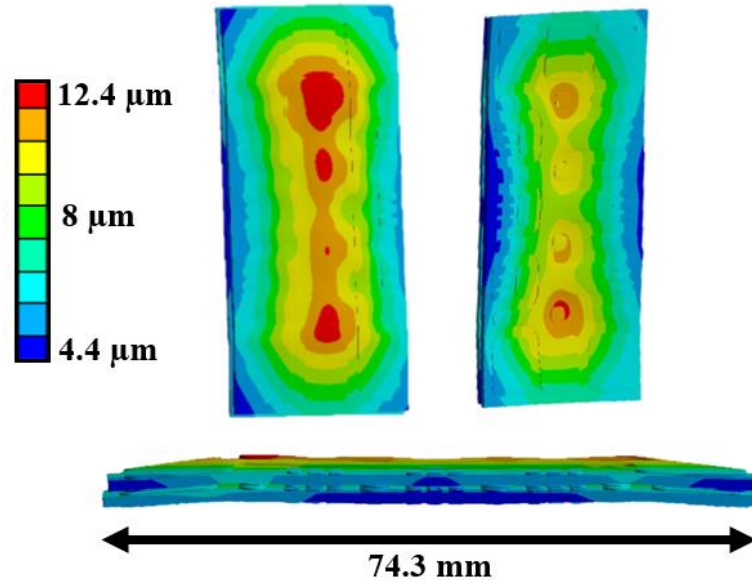


Figure 20: DBA 3-DBA 4 ANSYS thermomechanical deformation results.

The slight rise in deformation magnitude at the corners of the substrate is believed to be caused by the only sharp corners in the geometry at those locations having much higher localized stresses than in reality. While these corners were slightly rounded to mitigate this effect, future simulations should sweep different radii of curvature to understand the impact.

While the simulation simulates two substrates starting perfectly planar, the experiment shows that few substrates start planar. The experiment will provide insight into whether different initial substrate warpages impact the final warpage. Five samples of each MCPM substrate (DBA 1-DBA 2 and DBA 3-DBA 4) were analyzed to understand where the substrate warpage arose. First, each substrate was scanned using a Bruker DekTak contact profilometer at the locations detailed in Figure 21 for DBA 1 and DBA 2 and Figure 22 for DBA 3 and DBA 4. The shapes of the substrates before sintering varied and were paired in multiple manners: similar curvatures, opposite curvatures, and a mix of planar and non-planar to analyze the impact on the final warpage. Table 5 summarizes the amount of warpage and shape for each type of substrate before sintering. Some substrates have a slope across their metal pads, which is believed to be from uneven polishing during the substrate synthesis rather than due to a reduction in the ceramic thickness.

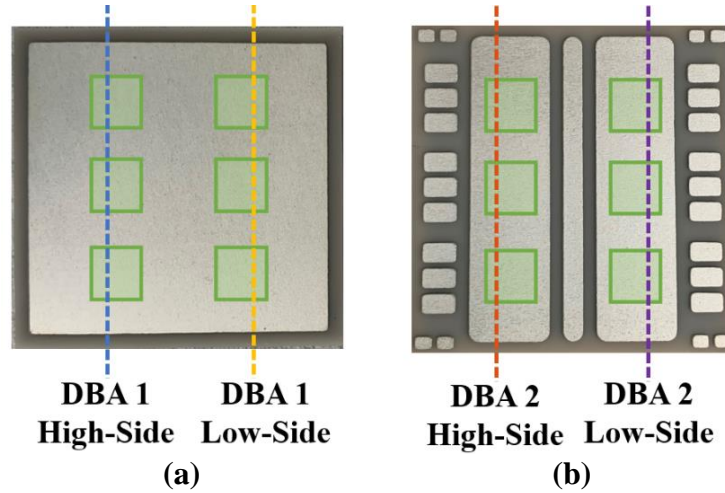


Figure 21: MCPM substrates with their approximate scan locations for (a) DBA 1 high-side (blue) and low-side (yellow) and (b) DBA 2 high-side (orange) and low-side (purple), as well as approximate locations of the die in green. The color of the lines corresponds to the graphs in Table 5.

In Figure 14, the rubber was cut to the size of the substrate to help distribute the pressure uniformly. A squeegee applies a Kapton tape layer to minimize air bubbles and avoid creating non-uniform pressure areas. The substrates are placed on each other, with the preform-transferred side on the bottom facing upward. For sintering, the profile previously mentioned for the simulation was used (3 MPa, 90 seconds), with the pressure applied by a Carver hydraulic hot press.

After sintering, the samples were scanned again using the scan locations in Figure 21 and Figure 22. The substrates showed consistent warpage across a group of samples, but they differed from the simulation. For DBA 1-DBA 2, the substrates warped in a concave-up direction, with the maximum warpage being $-26.8\text{ }\mu\text{m}$. For DBA 3-DBA 4, the substrates warped concave-down, with a maximum warpage of $43.5\text{ }\mu\text{m}$. In most cases, regardless of the initial warpage shapes, the end warpage shape was the same.

After contacting the substrate manufacturer, DOWA METALTECH, it was understood that the aluminum has a specific stress-strain curve that could only be obtained under a non-disclosure agreement. The manufacturing of the substrates most likely impacted the stress-free state of the aluminum, which can affect the behavior of the substrate during the simulation, and, therefore, the final warpage shape. This can explain the discrepancy between the DBA 1-DBA 2 simulation and the experimental results. Performing the simulations again with the proper stress-strain curve may give a more accurate simulation result to model the effects of aluminum metal patterning on the warpage, matching the experimental.

Table 6: Pressure-Assisted Sintering Substrate Warpage Results Showing Pre-Sintered Substrates (Light Blue and Light Red) to Post-Sintered Substrates (Dark Blue and Dark Red). DBA 1 and DBA 3 are Shades of Blue, While DBA 2 and DBA 4 are Shades of Red.

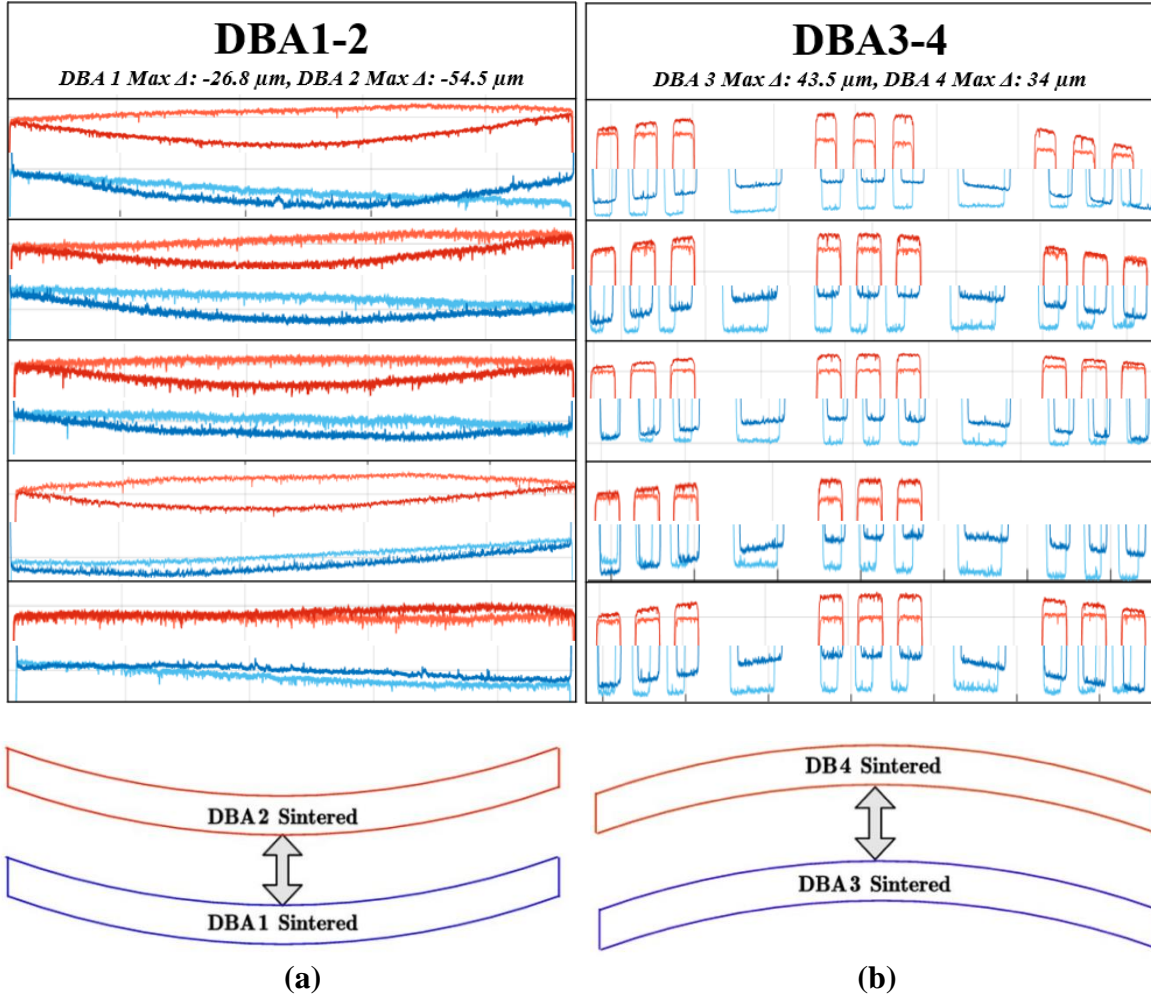


Figure 23: Behavior summary of the substrate warpage after the pressure-assisted large-area sintering process, showing DBA 1 to DBA 2 warping concavely and DBA 3 to DBA 4 warping convexly.

Future work regarding the substrate warpage of large-area sintered MCPM substrates should work to understand the manufacturing processes that contribute to the warpage before sintering. Additionally, the large-area sintered patterned substrates should undergo thermal cycling to understand the reliability compared to plain substrates. Cooling under pressure can be explored to reduce the warpage of the substrates. This was undesirable for manufacturability purposes since the Carver Hydraulic hot press takes over

eight hours to cool between sintering samples; therefore, the samples were removed each time from the press and left to cool to room temperature with a slight pressure applied from two smaller steel plates.

2.4 Pressure-Less Nano-Silver Sintering of Molybdenum Post

Interconnects

Once the substrates have been sintered, the interconnects and die can be attached. The MCPM interconnects comprise of Mo posts with 100-200 nm of titanium (Ti) and 200-500 nm of silver metallization. Mo posts reduce the CTE mismatch with SiC and have lower parasitic inductance than wirebonds. They allow for power-dense, sandwich structure modules that enable double-sided cooling [50], [53]. There are 36 different posts, and their sizes are listed in Table 7. The kelvin, gate, and source posts are shorter to account for the thickness of the die and be the same height as the DBA and midplane posts when sintered to the substrate.

Table 7: Post Names and Sizes in the MCPM.

Post Name	Post Size
Kelvin Source Post	1 x 1 x 2.13 mm ²
Gate Post	1 x 1 x 2.13 mm ²
Power Source Post	5.2 x 3 x 2.13 mm ²
DBA Post	6 x 2.5 x 2.5 mm ²
Midplane Post	2.5 x 2.5 x 2.5 mm ²

While sintering offers many improvements over soldering, attaching these small posts to the die small die pads with sinter paste is not trivial. Additionally, sinter paste does not coalesce to its respective pads since sintering is a solid-solid diffusion process, exhibiting no self-planarizing like molten solder. While solder paste can typically be dispensed or easily screen printed and melt to form a wetted contact with the whole metal surface, the sinter paste must either be carefully dipped or very finely screen-printed to

ensure a complete, proper bond. Any defects or contaminates in the sinter bondline will remain after sintering; thus, any post tilt cannot be corrected.

When these posts are then placed, the paste can ooze. With the small pad sizes of SiC, especially the medium-voltage MOSFETs having a gate pad of 0.36-1 mm², any misalignment of the post and sinter paste oozing will result in a gate-source short. Alternatively, the paste can ooze onto the field-grading of the device. Especially since these posts are placed by hand, this can create misalignment, planarity issues, and shear forces on the post, resulting in disconnected devices or module failure.

To control the oozing of the sinter paste and ensure proper alignment to avoid gate-source shorts, a die bonder can be repurposed as a post-placement tool. While the aspect ratio of the posts is much higher than a typical device, adjusting the pick-and-place tool head can allow for the adapted use for the taller posts. The die-bonder utilizes beam splitting to overlay two images: the die's surface and the post's bottom. This way, the posts are accurately aligned, and potential tilt from placement is mitigated. There is also a force gauge on the die bonder, so when a post is placed, the oozing of the paste can be controlled by setting the force limit.

The Mo post interconnects are placed in two steps. First, a bare die and four posts (two kelvin, one gate, and one source posts) are cleaned in a sonicator using acetone, isopropyl, then deionized water in consecutive steps. The posts are hand-dipped into NBE Tech silver sinter paste, as shown in Figure 24. The dipping bond uniformity is essential to mitigate any voids and defects. However, any non-uniformity at the edge will be corrected as the post is placed, and the slight pressure helps the paste ooze and coalesce out from under the bond, but not as much as to ooze onto the field grading. The posts are placed

onto the $6.94 \times 6.94 \times 0.35 \text{ mm}^3$ device using a die bonder. The posts placed by hand in Figure 25(a) are compared to those placed with the die bonder in Figure 25(b), exhibiting controlled bondlines and no post tilt. Once placed, the posts are sintered to the die using the profile in Figure 26.

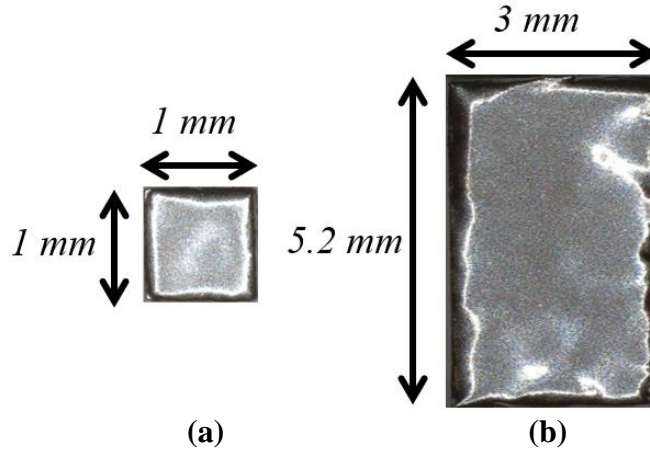
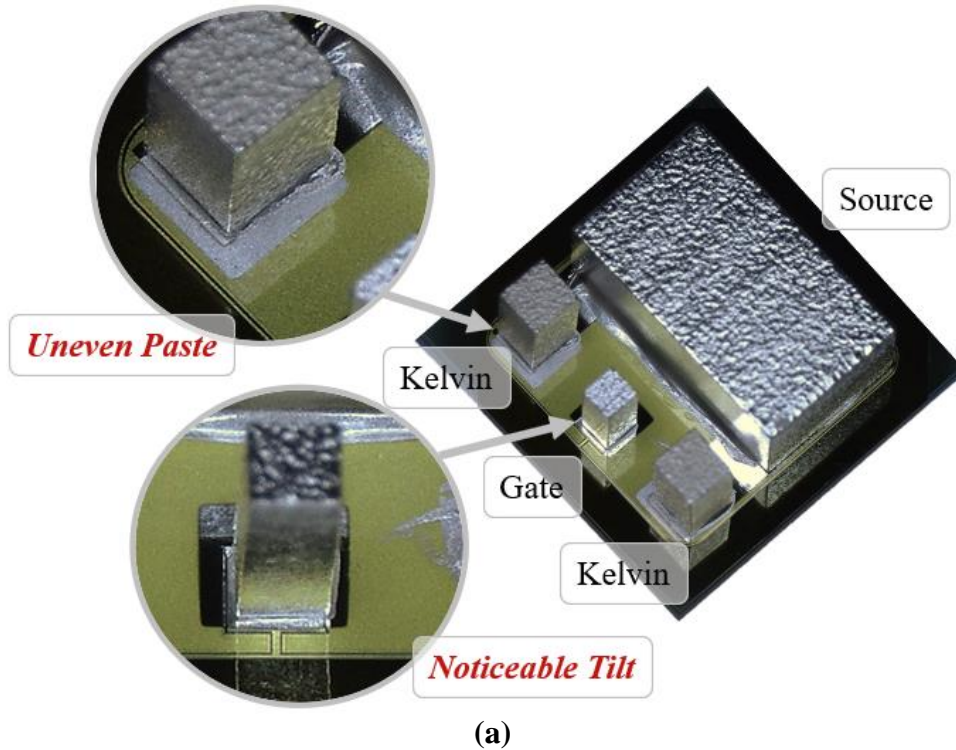
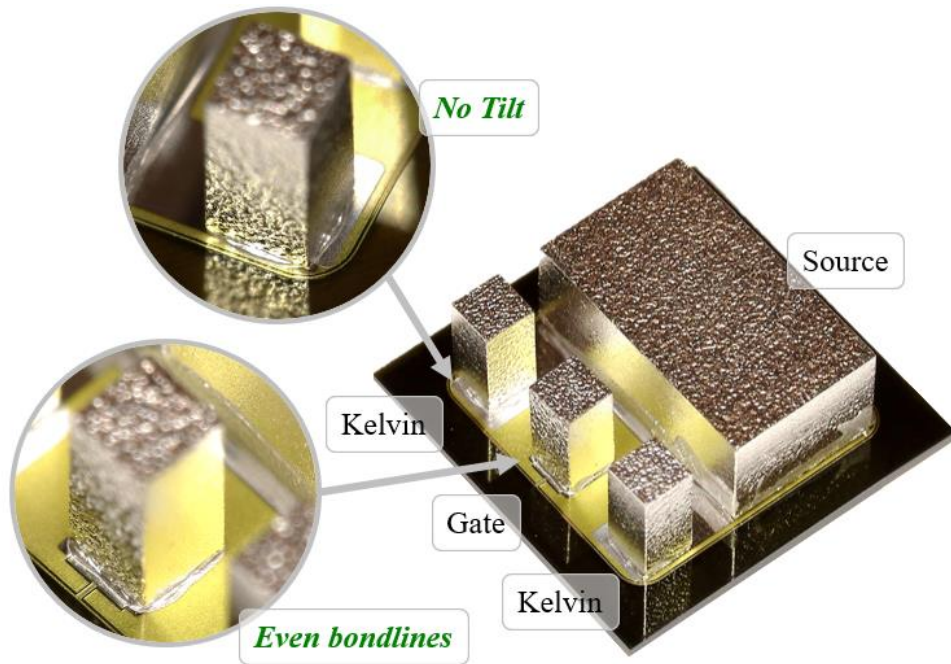


Figure 24: Nano-silver paste hand-dipped kelvin post (a) and source post (b).





(b)
Figure 25: (a) Mo post interconnects (2 kelvin, 1 gate, and one source) on the SiC device placed by hand. (b) Mo post interconnects placed with the die bonder, highlighting the hand-dipped silver sinter bondlines.

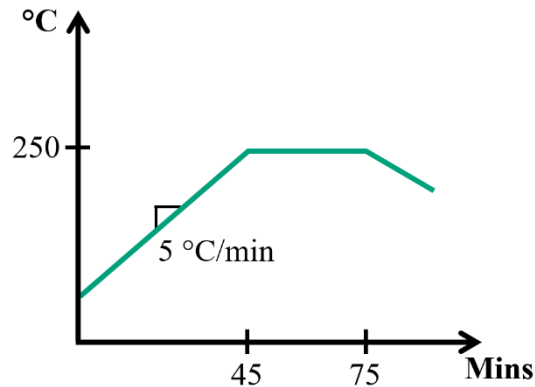


Figure 26: NBE Tech pressure-less silver sinter paste heating profile.

Once the posts are placed on six die, the next set is ready to be sintered to the substrate along with the die. Silver sintering is crucial for die attachment since the drain of the device is the main heat-extracting path, and silver sintering has better thermal conductivity and lower voiding contact than solder. The backside of the devices is gold, so important consideration is paid to the sintering time. Silver tends to diffuse faster than gold,

and limiting the Kirkendall voiding at the boundary between the materials is crucial to preserve the bond quality [73].

2.5 Pressure-Less Nano-Silver Sintering for Die Attach

Kyocera's CT2700R7S silver sinter paste was used for the die attach due to the formula's compatibility with gold metallization. Shear tests have ranged from 14-18 MPa with these sized die with gold metallization, which is acceptable given the large contact area of the die compared to the posts [29]. A 50 μm stainless-steel stencil with the die and post pattern is used to screen print the sinter paste to the DBA (Figure 27). The cutouts for the posts and die have a 200 μm extended perimeter from their nominal size.

When lifting the stencil after screen-printing, ridges can form at the edges of the paste due to its high viscosity, which can tilt the posts or die if placed on top of them. This is a significant adjustment for the sintering screen-printing process since defects in the bondline during this screen-printing process will remain. Additionally, since the ridges around the stencil cutout are thicker once lifting the stencil, they can easily crawl up the sides of the devices and lower the PDIV of the module, potentially shorting the drain and source. Therefore, ensuring uniform bondlines with no ridges or bumps from contamination or application is essential. Once the paste is screen printed, the six die, eight DBA posts, and four midplane posts are placed either by hand or with the die bonder and sintered accordingly with the profile in Figure 28.

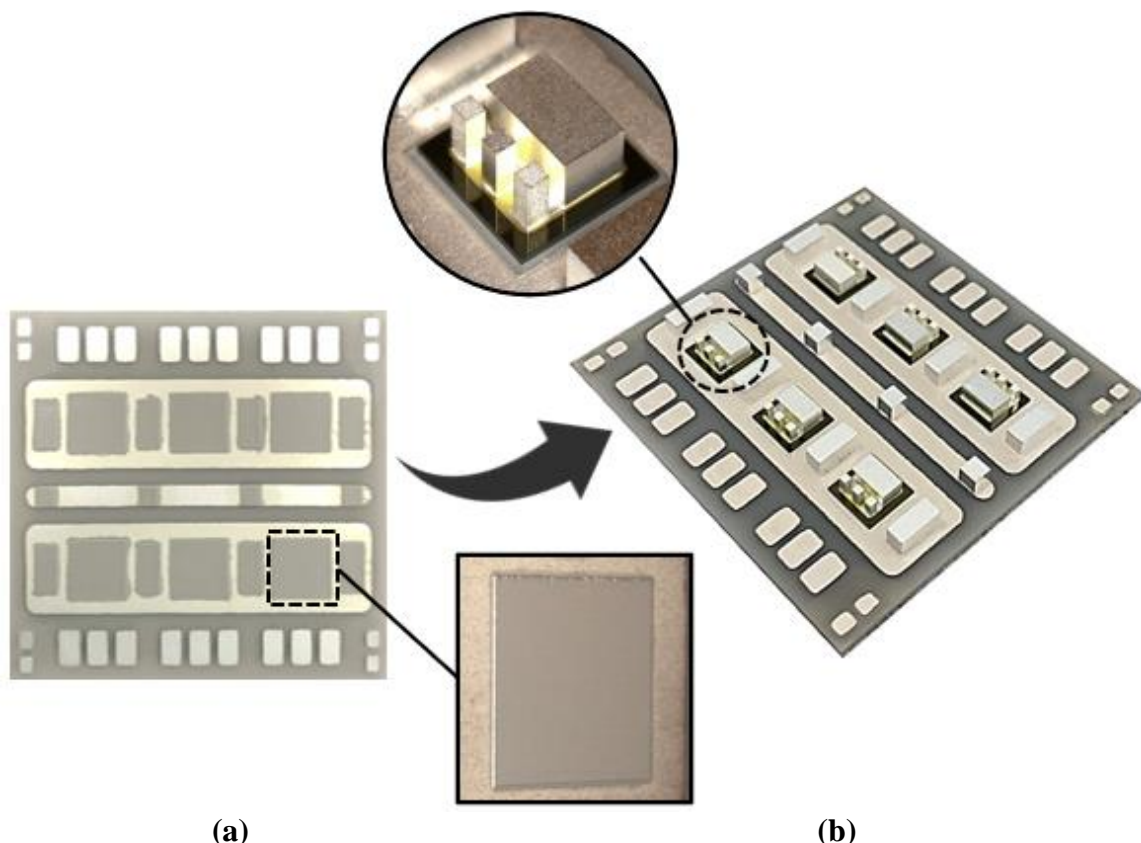


Figure 27: (a) Screen printed sinter paste on DBA 2 with a clear image of a uniform, defect-less screen print, and (b) all die and posts placed on the substrate in the paste, highlighting the die placement with no paste on the sides of the die or the field grading.

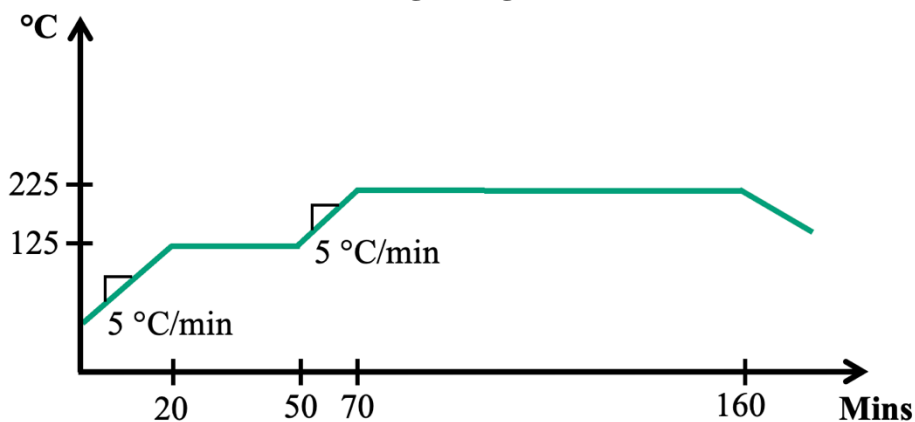


Figure 28: Kyocera pressure-less silver sinter paste heating profile.

2.6 Summary

A new process was developed to ensure uniform, repeatable transfers of silver preform to patterned MCPM substrates. Silver preform is more reliable for bonding large

areas when compared to silver sinter paste as well as solder. Previous work had yet to explore the transfer process for larger, patterned MCPM substrates, which proved to be more challenging to have successful silver preform transfers. The new process uses a thinner rubber with a higher durometer (from 1.6 mm and 40A to 0.8 mm, 60A), uses a higher pressure (from 1 MPa to 1.5 MPa), and for a longer time (from 60 seconds to 90 seconds). The process was repeated for eight patterned MCPM substrates and smaller patterned substrates for a two-die module, each having a uniform, successful transfer.

Not only was the transfer process improved, but the warpage of the substrates from this pressure-assisted sintering process was analyzed. It is important to note that the substrates' patterning will influence their warping based on the various CTE mismatches at different locations as the substrates grow and shrink from the heating and cooling stages. This warpage will be used to further investigate the planarity analysis of the sandwich-structure MCPM in Chapter 5.

Once the substrates were sintered, the post and die attach methods were evaluated. Since these are smaller areas than the substrates, the advancements in nano-silver paste have allowed pressure-less sintering. Instead of placing the posts by hand, a die bonder was adapted to accurately place the posts utilizing beam-splitting to prevent misalignment while also controlling even oozing of the bondline for a single post.

Chapter 3 Fabrication Challenges and Refinements of Soldering in Wirebond-less Multichip Power Modules

3.1 *Introduction*

While Mo post interconnects allow for advanced packages with low parasitic inductances, they can also introduce challenges for soldering. Their alignment is crucial when soldering the top substrate, and it is difficult to align all 36 posts since the view is restricted. Not only can their alignment across a substrate prove challenging, but their vertical tolerance to the top substrate is also a concern. Machined posts have tolerances that accumulate as they populate more across the module with paralleled devices. While the tolerances are inherent to the posts, their attachment processes can introduce more planarity challenges. The solder reflow profile involves the outgassing of flux, which can be volatile and uncontrolled. This can introduce non-uniform bondlines and displace the substrate, causing tilt across the posts and potentially disconnecting them altogether. The non-uniformity compounds if the sinter bondline of the posts has any defects or tilt.

Even if the assembly processes are entirely controlled, the solder reflow profile for an MCPM does not match the profile from the manufacturer. The ramp rates and temperatures must adjust to reflow all 36 bonds properly while ensuring enough soaking time and time above liquidus to minimize voiding content. However, more than simply scaling the temperature and time is required as there is a risk of de-wetting the solder if the accurate reflow profile is not followed.

The spring pin terminals are also soldered, but in a convection reflow oven, and these small pins can be easily tilted and displaced from the flux outgassing. The terminals

allow the devices to interface with external systems. If attached crookedly, the pins can easily break off and leave no method of interfacing the device with the system.

The alignment of the Mo posts to the top substrate is first investigated before soldering the large thermal mass of the MCPM. A new profile is determined to reflow the MCPM properly. A pressure-assisted soldering method is explored to reduce tilt and improve the connection reliability between the posts and the top substrate. Once the module is soldered together, the spring pin terminals are attached.

3.2 Alignment of Molybdenum Post Interconnects Before Soldering

With four Mo posts per device and the additional DBA and midplane posts on the substrate, soldering the top substrate of a six-die module requires perfect alignment of 36 posts of varying sizes. Misalignment can result in either a gate to kelvin source short or an open gate or kelvin source connection. Not only will this lower the current rating of the module, but one misaligned post can create planarity and alignment issues for other posts in the module, potentially disconnecting more devices. The size of the post interconnect pads for each post are in Figure 29.

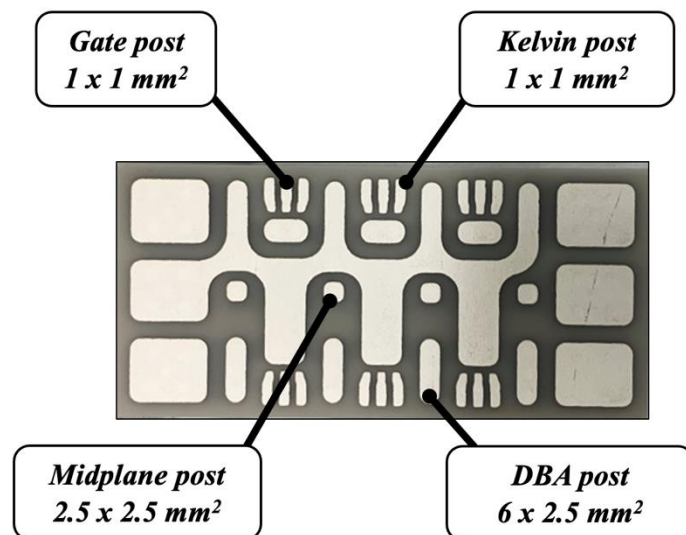


Figure 29: DBA 3 substrate pattern with callouts to specific pads that posts align to (post sizes are noted below post name).

Checking the alignment of sandwich structure modules can be difficult since the bottom view of the top substrate is restricted during fabrication. To ease the blind alignment, a glass slide with a 50 μm layer of Kapton tape engraved (using the VLS laser engraver) with the substrate pattern was placed atop the devices, as seen in Figure 30. The patterned glass slide allows a clear view of the posts and their landing pads on the top substrate to verify their alignment before the soldering step. Not only does this de-risk the fabrication of the module moving forward, but it also helps validate the fabrication of the previous steps.

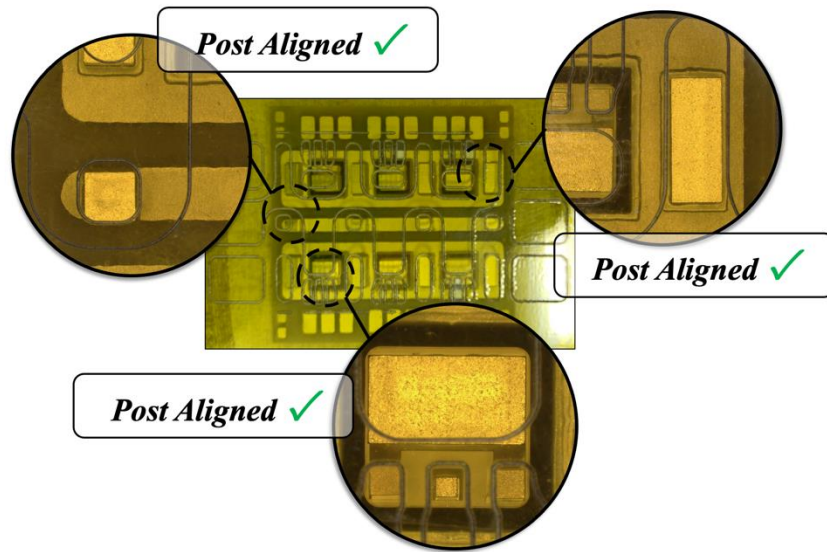


Figure 30: Glass slide with etched DBA pattern overlaid onto post interconnects to verify successful alignment for soldering.

3.3 Soldering of Multi-Chip Power Modules with Large Thermal Masses

Once the devices and posts have been aligned and sintered to the bottom substrate, the top substrate is attached by solder reflow. Soldering is chosen for this step to allow for some thermomechanical relief compared to rigid sinter bonds and also to allow for a more compliant bond than sinter paste [29]. MCPMs with vertical sandwich structures have large thermal masses, which are not typically accounted for in the soldering profile datasheets.

An inappropriate heating profile can cause incomplete reflow and high voiding content [72], [85], [86]. Incomplete reflow profiles will result in disconnected devices, and de-wetting can have the same outcome as the solder can no longer bridge the connection from the post to the pad on the substrate. High voiding content can significantly affect the signal and power paths since voiding increases the thermal resistance of the bond and the reliability over time [86], [87]. Each substrate also has different metal patterning, resulting in uneven heat flow paths during the soldering profile, and some bonds can reflow at different times.

A tin-silver alloy (WS-D440 Sn96.3/Ag3.7) promotes adhesion to the silver metallization of the Mo post interconnects and the DBAs and was dispensed on top of the posts (Figure 31(a)). Silver alloys are also known to have higher wettability and higher reflow temperatures, aiding in the reduction of voids by lowering the surface tension of the solder [88]–[91]. A thermocouple was then attached at the location of the solder joint of the module in Figure 31(b). The temperature and ramp rates of the hot plates were varied (in grey) until the thermocouple temperature plotted in green in Figure 32 matched the manufacturer-recommended profile for Sn96.3/Ag3.7 solder plotted in dashed light green.

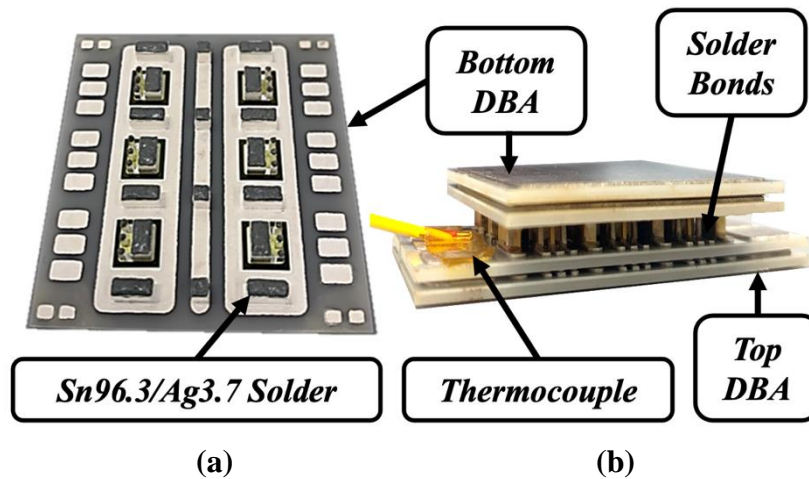


Figure 31: (a) Solder paste on the sintered Mo posts. (b) The bottom DBA flipped onto the top DBA with a thermocouple at the solder joint.

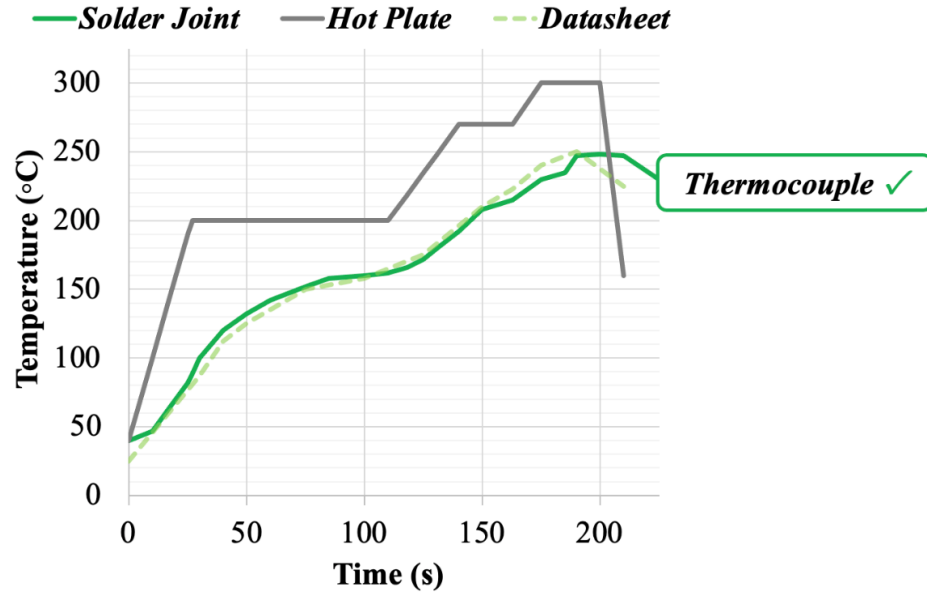


Figure 32: Sn96.3/Ag3.7 solder-reflow profile of stack-up where the temperature at the solder joint location in the MCPM matches the recommended soldering profile.

3.4 Pressure Soldering Techniques for Molybdenum Post Interconnects in Multi-Chip Power Modules

Post interconnects compound the soldering challenges of MCPMs. The posts have a 50 μm height tolerance which can result in open connections (e.g., if one post is shorter than the others, there may not be enough solder to make electrical contact with the substrate). Additionally, when the solder reflows, the outgassing of the flux results in uneven bondlines, points of high thermomechanical stress, and high bond resistance [71], [92], [93]. The tilt can be so drastic that it may disconnect smaller area bonds altogether. This is vital for MCPMs with many small post connections for every gate and kelvin connection. Even a slight tilt can disconnect the 1 x 1 mm² bond areas of these posts, making the MCPM non-functional.

3.4.1 Pressure-Assisted Soldering Methodology

Voids occur from the gaseous flux bubbles that remain in the bondline during reflow. As these voids form, they can displace solder and tilt the posts. Extensive work has been done to understand the chemistry and physics behavior of solder voids and how they impact die tilt, heat transfer, and electrical bond quality, mostly surrounding the Young-Laplace equation and the ideal gas law [71], [72], [86], [94]. Equation (1) relates the pressure inside the bubble (P_b) to the sum of the atmospheric pressure (P_a) and the pressure due to surface tension (σ), which also depends on the radius (r). It explains the pressure difference across two fluids due to surface tension (i.e., solder and gaseous flux). Equation (2) is famously known as the ideal gas law, which indirectly relates pressure (P) and volume (V) to the amount of gas (n), the ideal gas constant (R), and the temperature (T).

$$P_b = P_a + 2 \frac{\sigma}{r} \quad (1)$$

$$PV = nRT \quad (2)$$

Effectively reducing voids during reflow typically requires a pressure gradient. This is traditionally accomplished under a vacuum, facilitating the void escape by lowering the atmospheric pressure outside the gas bubble during reflow, expanding the radius according to equation (1). Without vacuum, the voids expand with the ideal gas law and increasing temperature in equation (2). However, they often do not expand and coalesce enough to escape from beneath the die, remaining trapped in the bondline. Both soldering processes with and without vacuum are shown in Figure 34.

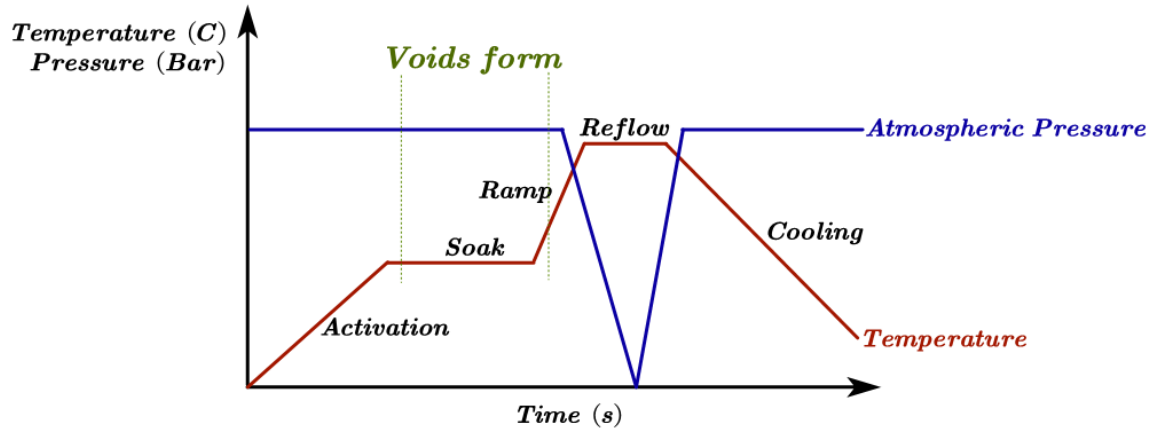


Figure 33: Typical vacuum reflow soldering profile.

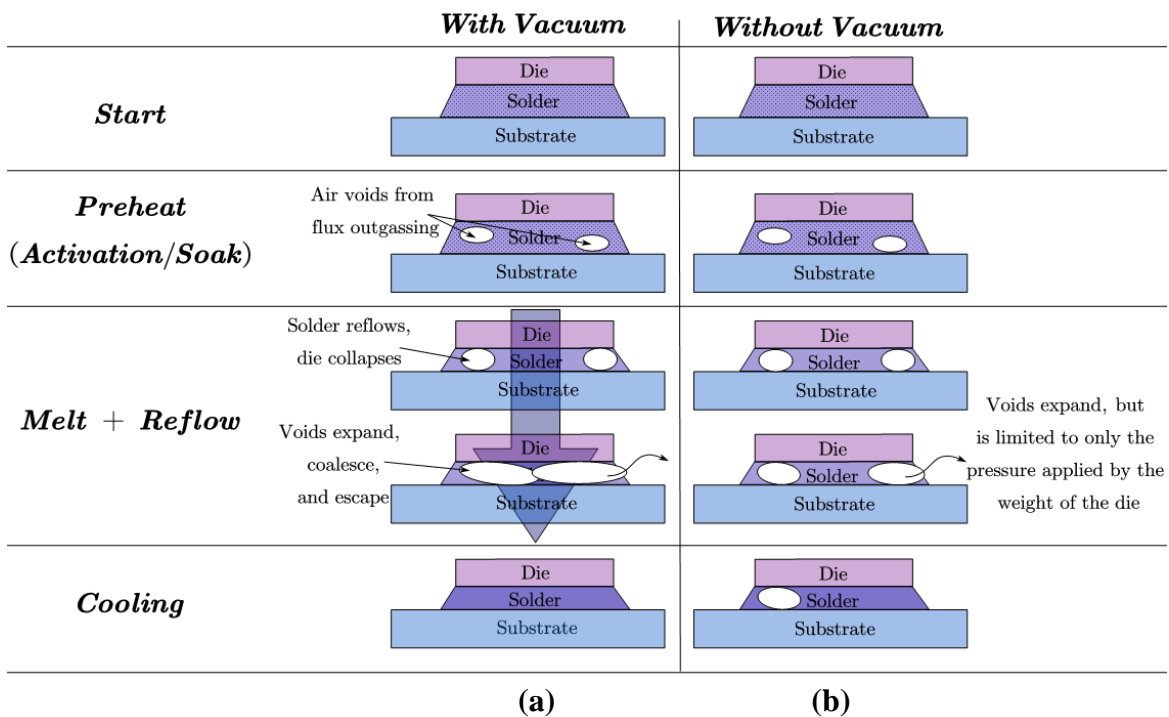


Figure 34: Solder reflow process when (a) a vacuum is applied and (b) without a vacuum, highlighting the behavior of the voids.

Utilizing the theory behind the chemistry and physics of void expansion and escape, void minimization can also be obtained by applying an external force while maintaining atmospheric pressure. The gas bubble continues to expand according to the ideal gas law. However, by applying pressure to the top of the post, the buoyancy force of the bubble can no longer displace the post (usually causing tilt). The bubble increases its volume while heating; however, it can no longer expand its radius uniformly and must elongate laterally.

This increases the probability of coalescence with other voids and becomes large enough to escape from the sides of the bond, reducing the concentration and size of the voids left after reflow.

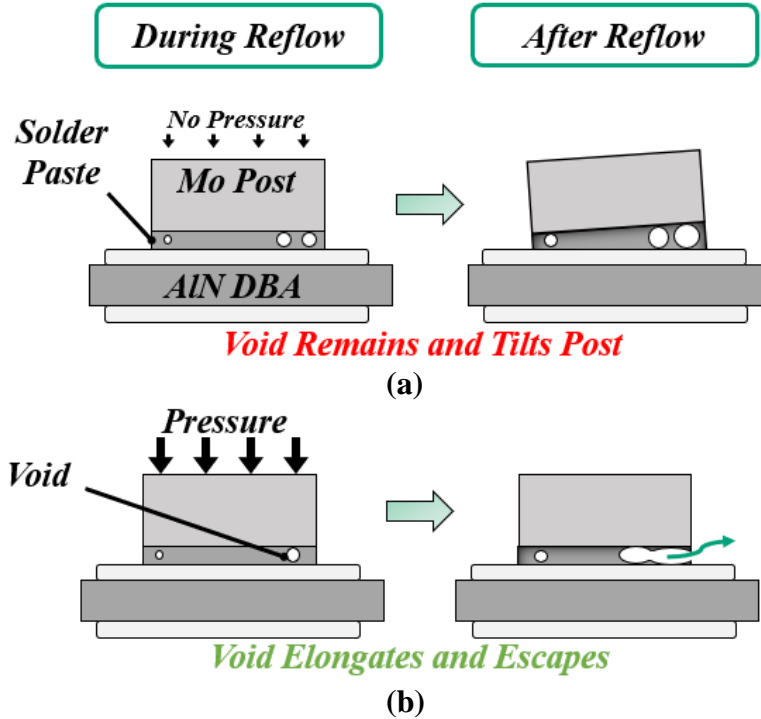


Figure 35: Impact of voids on post tilt during (a) pressure-less solder reflow that results in tilt versus (b) pressure-assisted solder reflow.

To determine the external pressure to apply, calculations are done using Equation 1 to understand the pressure required to overcome the surface tension of the gaseous flux void. Rearranging equation (1) results in equation (3), which describes the relationship between the pressure differential to overcome the surface tension of a bubble.

$$P_b - P_a \geq 2 \frac{\sigma}{r} \quad (3)$$

At equilibrium, the pressure applied from the atmospheric pressure and any pressure from an external force will equal the pressure inside the bubble; equation (4) can be written, visually represented in Figure 36.

$$P_b = P_a + P_{APP} \quad (4)$$

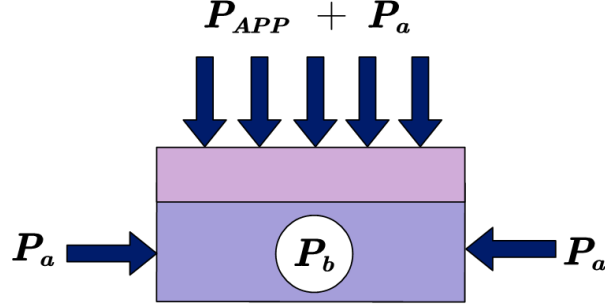


Figure 36: Visual representation of equation (4) during the external pressure-assisted soldering.

The substitution of equation (4) back into equation (3) yields the required applied pressure to overcome the surface tension of a certain-sized void.

$$P_a + P_{APP} - P_a \geq 2 \frac{\sigma}{r} \quad (5)$$

$$P_{APP} \geq 2 \frac{\sigma}{r} \quad (6)$$

By solving the equation for a certain pressure based on a minimum radius (based on the size of macro and microvoids that arise from flux during reflow), a radius of 20 μm is chosen. The surface tension of typical tin-silver alloys is around 600 N/m, resulting in a pressure of 0.06 MPa applied to the module during solder [90].

3.4.2 Pressure-Assisted Soldering Process

For these reasons, pressure-assisted soldering is investigated to reduce tilt and improve bond strength and connection reliability. An experiment evaluates the benefits of pressure-assisted soldering across two different groups of posts. Using a 200 μm stencil, the solder paste is screen-printed onto a DBA, and the posts are placed using a die bonder. The posts are reflowed in two groups: one without pressure and one with pressure applied.

In this experiment, three dependent variables determine the bond quality: post-height variation, shear strength, and void concentration. These variables demonstrate the execution of the experiment and how we measured the post-height variation. After

measuring the post-height variation, the posts are sheared to record the bond strength and observe the voiding content.

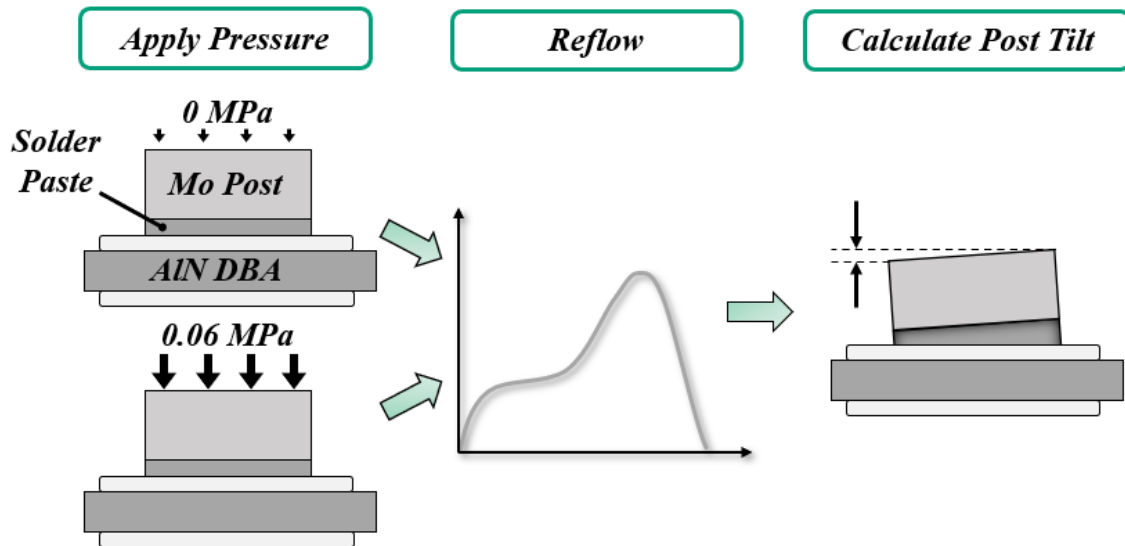


Figure 37: Steps to evaluate the benefit of pressure-assisted soldering for post-planarity, specifically, measuring the post-height variation.

Figure 38(a) presents the average tilt measured across a post without pressure and Figure 38(b) with pressure. The pressure-assisted soldered posts have 97.7% less height variation and 10.5% higher shear strength than posts soldered without pressure. Figure 39(a) presents the shear strengths of the bonds soldered without pressure and Figure 39(b) with pressure. The posts soldered with pressure have an 11% increase in bond strength.

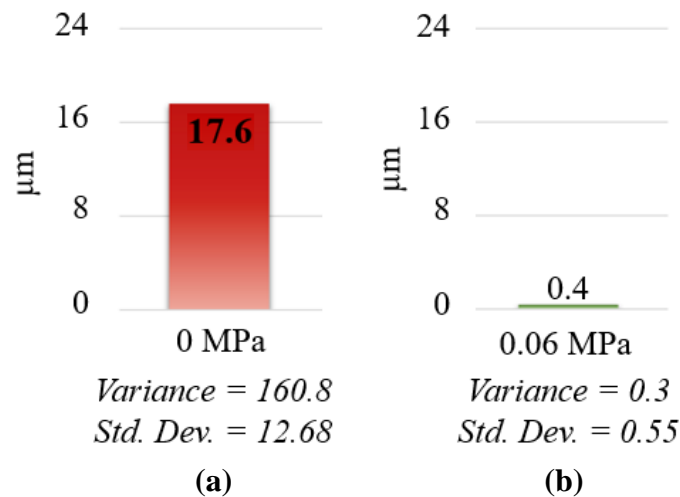


Figure 38: Average measured tilt across a singular post using the (a) pressure-less and (b) pressure-assisted soldering methods shown in Figure 37. Noted below each are the variance and standard deviation of the measurements.

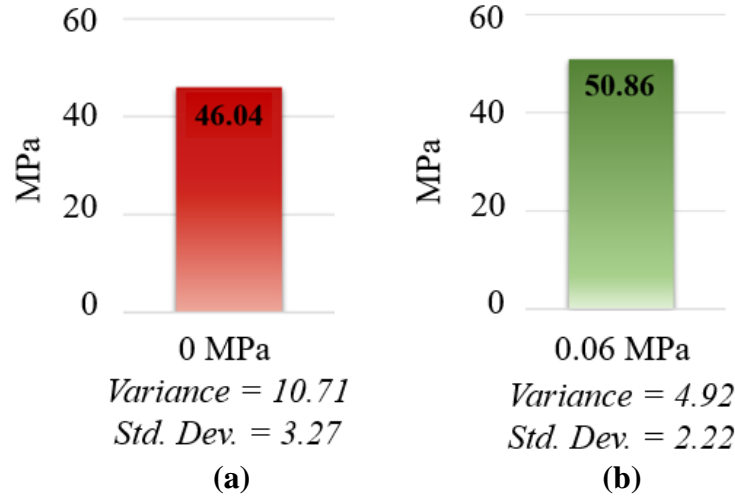


Figure 39: Average shear strength of posts using the (a) pressure-less and (b) pressure-assisted soldering methods shown in Figure 37. Noted below each are the variance and standard deviation of the measurements.

From analyzing the sheared bondlines in Figure 40(a), pressure-less soldered posts show large, concentrated voids in the bondline on both the substrate and the post and smaller voids dispersed in the pressure-assisted bondline. Studies have indicated that small, dispersed voids can provide some thermomechanical benefits, and voiding along the edges has minimal impact on bond reliability [57], [95]. Analyzing the voiding of the pressure-assisted bondlines proved challenging. Overall, the size of the voiding reduces, but it is important to note that not every void-like crater in Figure 40(b) is a void.

Figure 40(b) shows how one recessed area of the post has a raised complement area on the substrate, indicating it is not a void. Because the bondline was a cohesive failure, it is harder to piece the two images together, especially since this is a destructive test. CSAM images would be preferred as a non-destructive imaging method to better analyze these bonds in the future since fragments of the bond are lost during the destructive shear tests.

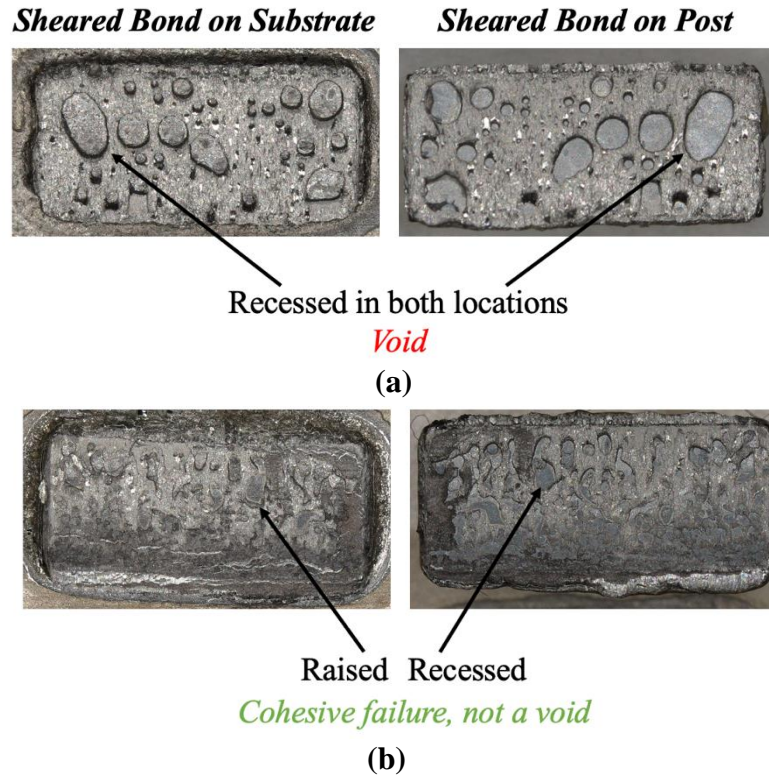


Figure 40: (a) Pressure-less soldered bond showing the cavernous voids on both the substrate and post. (b) Pressure-assisted soldered bond with raised and recessed edges that piece together due to a cohesive failure, not a void.

3.4.3 Pressure-Assisted Soldering Verification on a Mechanical Multi-Chip Power Module

Now that the post tilt is controlled with reduced voiding, a mechanical MCPM is soldered using the new pressure-soldering method. With solder dispensed on top of the posts, the entire bottom half of the module is placed in an alignment jig made of high-temperature resin. The top substrate is also placed in the jig, assuring alignment of all the pads to all the posts. Once on a hot plate, a pressure of 0.06 MPa is applied during the solder reflow using a weight. Figure 41(a) shows the probe locations to measure the resistance, and Figure 41(b) shows how this non-destructive test verifies the electrical connection and integrity of the solder bond by noting the resistance measurement path from kelvin to the power source. Table 8 lists the mean and standard deviation of the kelvin

source to power source resistances measured for each die in one module soldered with pressure and one soldered without. It is noted that the mechanical module soldered under pressure has one less DBA than usual, which may contribute an estimated 5 m Ω to the total resistance. Overall, the pressure-assisted soldered module has a 99% reduction in resistance.

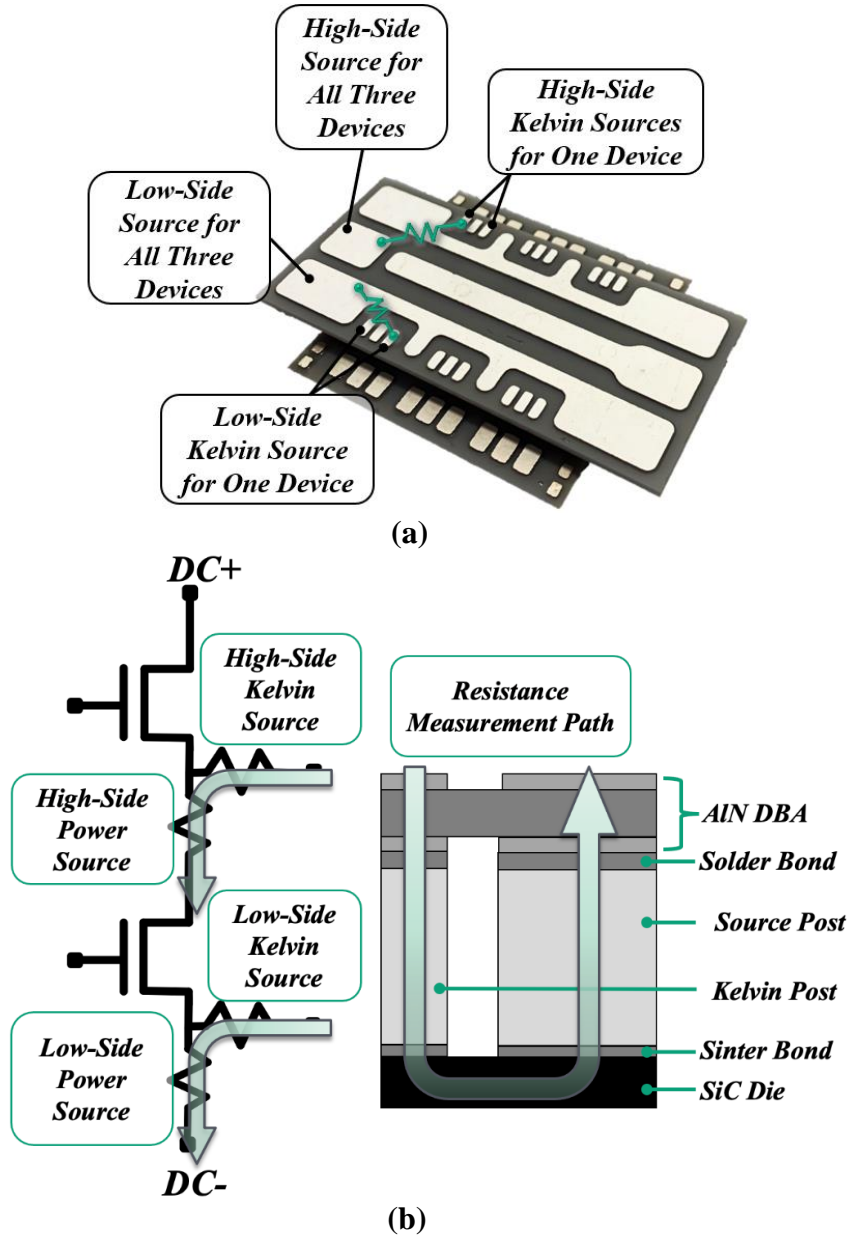


Figure 41: (a) Probe locations for resistance measurements from kelvin source to power source for two devices (one on the high-side and one on the low-side). (b) Resistance measurement path for soldered modules with and without pressure to verify the integrity of solder bonds.

Table 8: Kelvin Source to Power Source Resistances of Bonds Using Pressure-less and Pressure-assisted Soldering for the Mechanical MCPMs.

	Resistance Pressure-less Soldered Module <i>0 MPa</i>	Resistance Pressure-assisted Soldered Module <i>0.06 MPa</i>
Mean	44.7 Ω	72.6 $m\Omega$
Std. Dev.	146.9 Ω	9.0 $m\Omega$

3.5 Soldering Techniques for the Proper Alignment of Spring Pin Terminals for Multi-Chip Power Modules

The spring pins make up the terminals of the module to interface the die with the outside system. The pins completely compress to the field-graded busbar, sealing off the module from the air and reducing the in-air peak electric field, allowing for 6 mm spacing between pads [69]. The spring pins are attached in the last step before encapsulation and are soldered in a forced convectional reflow oven. The solder is an Sn63/Pb37 alloy, which has a lower reflow temperature (180 °C) than the Sn96.3/Ag3.7 alloy (240 °C) used in the previous step of attaching the Mo posts to the top substrate. A stencil of the spring-pin locations is laser etched into Kapton tape, then placed onto the substrate. The solder is dispensed into every pin location, and the pins are placed by hand. Once attached, the pins undergo the reflow profile in the convection oven.

Two issues arise with this method of soldering the pins. The pins have minimal mass, and the outgassing of flux can easily tilt and even knock the pins over. Additionally, since this process is done in a forced convection oven, the entire module is sealed off from users, so if a pin starts to move, it cannot be adjusted during the process and will remain crooked or misaligned. Misalignment of the spring pins can either short connections or bring conductors closer together and risk arcing and lowering the PDIV of the module. With previous two-die modules built, crooked spring pins, when interfaced with the busbar,

had a high likelihood of experiencing a shear force when compressed and broke off of the module.

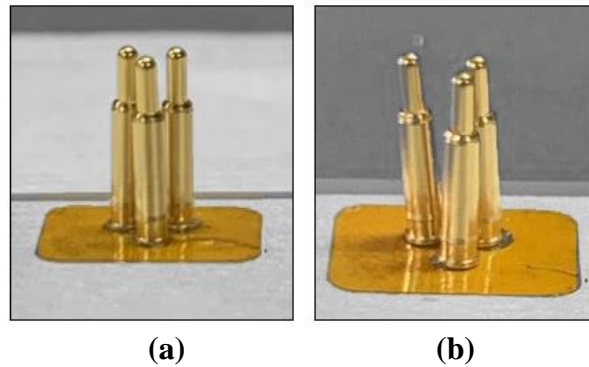


Figure 42: (a) Spring pins placed before soldering in the convectional reflow oven and (b) spring pins after soldering, ending crooked.

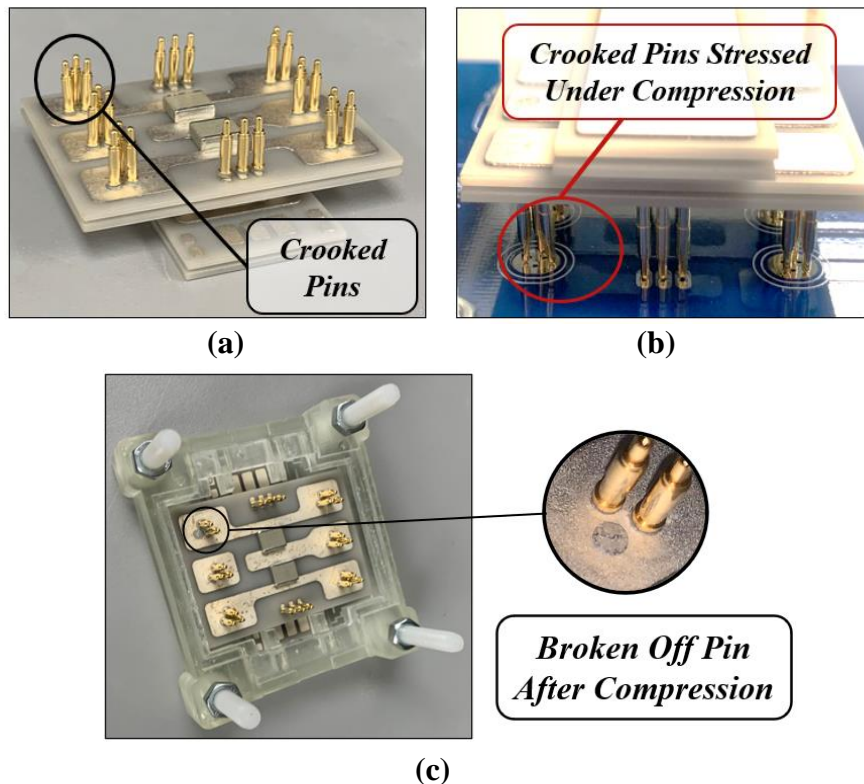


Figure 43: (a) Two-die module with crooked spring pins. (b) Two-die module interfaced with the characterization board, showing crooked pins stressed under compression. (c) Two-die module post characterization with the crooked pin broken off.

In order to prevent misalignment of the pins, an experiment was run to understand the potential benefit of tacky flux to help hold the pins in place. Tacky flux has a higher viscosity than solder paste and is used to help keep components from moving during

reflow. However, applying too much can harm the bond integrity, as it can remain in the solder bondline as voids [96]. Different pins were tested with different amounts of tacky flux, and their tilt was inspected before and after. It is shown in Figure 44 that the most effective way to keep the pins from becoming crooked during the reflow is by using a small amount in a small area. Shear tests also verify that this is the most effective method for creating a solid bond for the pins. Without using tacky flux, the fabrication of one two-die module resulted in the loss of two crooked pins breaking from the module. Five of the two-die modules were fabricated using this method, and only one pin was lost out of 120 pins.

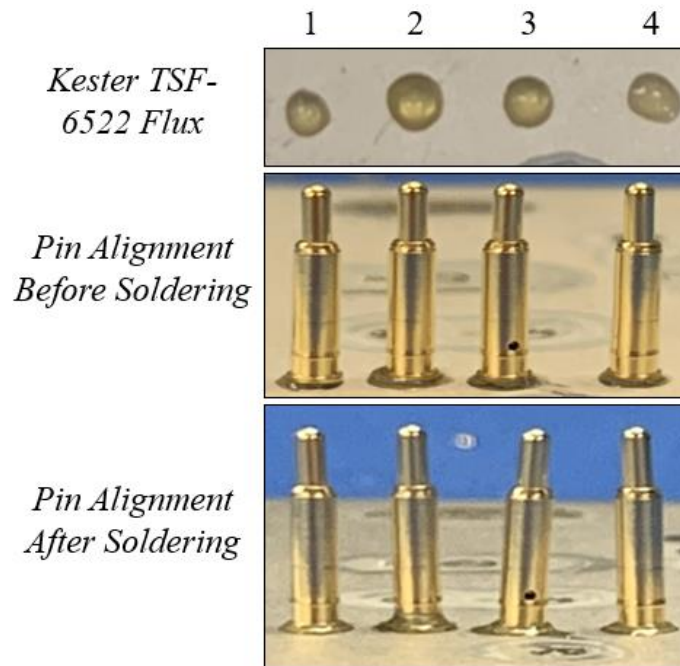


Figure 44: Testing the effect of tacky flux on keeping pins straight after solder reflow with (1) a small amount in a small area, (2) a large amount in a larger area, (3) a large amount in a small area, and (4) a small amount spread to a larger area.

Table 9: Shear Tests From the Pins in Figure 44 Attached with Different Amounts of Tacky Flux.

(1)	(2)	(3)	(4)
66.29 MPa	45.21 MPa	53.54 MPa	54.52 MPa

3.6 Summary

In summary, the alignment of the Mo posts was verified to ensure proper soldered connections are made without risking any gate-source shorts or open connections. With 36 posts, this check is crucial to the operation of the MCPM. Once aligned, the proper reflow profile for a large thermal mass is verified using a thermocouple attached to a mechanical module at the location of the solder joint to ensure adequate soaking time and time above liquids to minimize voiding and reflow all 36 bonds.

A pressure-assisted soldering process was developed to emulate the results of vacuum reflow without needing the equipment by applying an external force to the module. Applying this pressure increased the bond strength by 10.5% and reduced the post tilt to sub-micrometers. While visually, the reduction of voiding is noticeable, the quantification is challenging since they are sheared bonds. During destructive testing, bond fragments can disappear from the cohesive failure, making understanding the percentage of voiding content reduction challenging. Overall, there is still a reduction of voids and movement of large voids away from the center of the post, which is beneficial for thermal reliability.

Finally, the spring pins alignment is one of the last fabrication steps, which interfaces the devices with the busbar and system. During reflow, flux outgassing can tilt the spring pins, causing shear forces when the module is compressed to the busbar for characterization. Using tacky flux, the spring pins remain aligned during the reflow and are less susceptible to outgassing. Only one spring pin was broken across five modules utilizing this technique, and the rest adequately interfaced with their busbar pads without any failures.

Chapter 4 Statistical Tolerance Analysis of the Sandwich-Structure Module with Post Interconnects

4.1 Introduction

The previous refinements to advanced packaging techniques have manifested in improved mechanical and electrical functionality for MCPMs. Each layer of the module contributes to the overall success and yield. The new substrate bonding process allows for uniform bondlines with repeatable success in electrical connectivity between proper pads. The alignment of all 36 posts is verified, and pressure soldering of the substrate to these posts reduces post tilt and voiding and improves bond strength. All the refinements manifested in a successfully fabricated mechanical module. However, along the fabrication process, many steps still introduce variations that can cause planarity issues in the module, no matter how refined the packaging techniques are. Variation and tolerances are inherent to manufacturing, specifically manufacturing of vertical structures where the tolerance of each layer builds upon the previous.

The warpage analysis shed light on the fact that planarity issues within these sandwich structure modules are introduced during the first step of fabrication. Additionally, the machining tolerances on the Mo posts were addressed. While the tilt in silver-sintering of the posts to the die and the die to the substrate is reduced by utilizing a die bonder to pick and place the posts accurately, it is still not an ideal method of placing these posts since some need to be hand-dipped into the paste which can result in varying bondlines, while others have a screen-printed bondline. Nonidealities in the silver-sintered bondlines compound on each other while constructing the sandwich-structure module.

While the bondline for the solder reflow can be controlled using the pressure-assisted soldering methods detailed in the previous chapter to ensure no disconnections of the post, it begs the question of how this solder bondline thickness was chosen. It allows for compliance and can mask some of the planarity issues of these sandwich-structure modules. However, outside of the mechanical module built in this work, this solder bondline has not been enough to fill the gap for all posts to the top substrate, completing the module's electrical connection to its terminals.

After fabricating an entire module, the last bonding step seemed to be treated like a scapegoat, taking on the worst of the planarity issues to result in a functional module (Figure 45). These MCPMs' yield had yet to improve with this previous ideology. This motivated this work to understand the fabrication refinements required to improve electrical and mechanical functionality (Chapters 2-3) and to study the machining of the components themselves and how they contribute to variance throughout the assembly process.

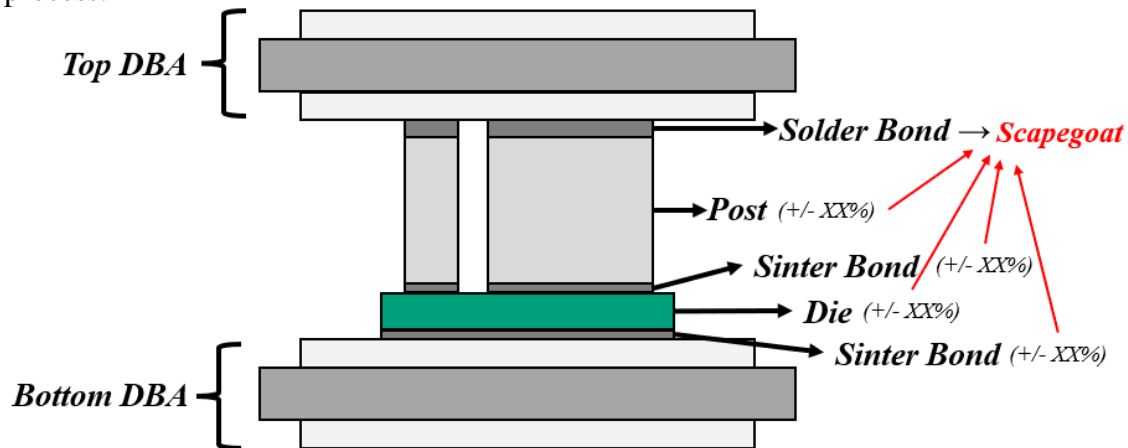


Figure 45: Side-view of a single die stack-up in the MCPM showing each layer and how their tolerances all accrue on top of each other to be filled by the final solder bond.

To improve the yield of sandwich-structure MCPMs with post interconnects, this section conducts a statistical tolerance analysis to predict better the maximum height

mismatch before soldering the posts to the top substrate and what sources of variation contribute the most to this mismatch. Different statistical analyses will be explained, along with the chosen analysis and result with their conclusions.

4.2 Motivation for a Statistical Tolerance Analysis Using a Monte Carlo Simulation

Tolerance analysis methods allow a visual depiction of understanding the variation in a part or assembly. These analyses can be done in one-dimension, two-dimension, or three-dimension and can also be considered a worse-case or statistical analysis. Not only can they be done across a population of a particular part, but they are also applied to assemblies, specifically stacked assemblies [97]. These analysis types apply to this MCPM because the sandwich-structure module exemplifies a stack. Work has been done to understand the vertical direction tolerancing on QFN packages and chip-to-substrate bonding with interposers [98]–[100]. However, no literature could be found on the size scale or topic of medium-voltage sandwich-structure power modules.

The method described in the introduction about sizing the solder bond for the worst possible gap in the MCPM uses an ideology called a one-dimensional tolerance. This method is commonly used in industry for stack-ups, where the tolerancing is done in one direction, starting at the lowest level of the stack. Two charts are generated, one assuming the minimum tolerance for each component of a part or each part of an assembly and the other considering the maximum tolerance. This process uses an appropriately named analysis: worst-case analysis. One-dimensional tolerancing is restricted to worst-case analysis, and since there is no algebraic representation of the tolerancing, no statistical analysis can be performed [97]. It is elementary and straightforward, so it is a popular

tolerancing method. It also covers a vast range of tolerances, resulting in robust, reliable component performance needing few design iterations for their applications since, with worst-case analysis, every part is designed to be fully interchangeable[101]–[103].

The caveat with applying worst-case analysis is that it formulates the design constraints on only two specific cases that are statistically very rare [98], [101], [104]. The worst-case analysis proposes one solution to the tolerance problem: design for the absolute minimum to maximum range, acquire high-precision machining instruments, and tighten the tolerances of every layer in the stack-up to reduce the mismatch and error. However, tighter tolerances result in an overdesigned part, complicated assembly requirements, an exponential increase in cost, and increased manufacturing time [105], [106].

If applied to the MCPM, as shown previously in Figure 45, the worst-case analysis would suggest designing the solder bond to fit all possible scenarios of height mismatch across all 36 posts. The result is either unattainable tolerancing standards resulting in high cost on pad thickness, post height, and bondline control, or an incredibly thick solder bondline that contributes to higher parasitic resistance in the signal and power loop paths and potentially the paste bridges gaps between pads that are spaced only 1 mm apart. Also, thicker solder bonds can increase device junction temperatures [42]. It can be analyzed quickly that worst-case analysis takes a conservative approach, often unrealistic or feasible in assembly manufacturing.

A worst-case analysis is often viewed as a more cynical, “preparing for Murphy’s Law” manufacturing part tolerance analysis that is not always necessary or the most representative of a part tolerance distribution [97], [101], [103]. A more attractive method of analysis for tolerancing stack-ups to incorporate statistical analysis is parametric

tolerance analysis. Parametric tolerance analysis develops analytical and algebraic expressions to represent the dimensioning and tolerancing as functions and can be employed in two-dimensional or three-dimensional tolerance analysis. It is a more reasonable assessment of the probability of manufactured parts within an acceptable tolerance [101]. Parametric tolerance analysis can be done linearly or nonlinearly [97].

Linear methods include the root sum squares (RSS) method. RSS does not focus on the extremes like a worst-case analysis but represents the distribution of the variation for each dimension in the tolerance stack-up. This method generates a probability density function (PDF) from a distribution of measured parts. A probability density function represents the likelihood of a particular dimension occurring within a range and is usually fit to a histogram distribution of part measurements [107]. It results in less restrictive tolerances that better represent the distribution of the part. This way, every layer of the stack-up assembly can be modeled as a distribution instead of a specific minimum and maximum tolerance, and their distributions make up a more comprehensive distribution much looser than the worst-case analysis, helping reduce tooling cost [104], [108].

One drawback to linear parametric tolerance analysis is that it assumes normal distributions. Many manufacturing processes part tolerances are often skewed distributions, meaning linear statistical analysis methods do not apply [97]. Nonlinear parametric statistical tolerance analysis is achieved by using the Monte Carlo simulation.

A Monte Carlo simulation models the probability of various outcomes from a process or experiment that typically does not follow a normal distribution by random sampling of distributions of existing data repeatedly [97], [105]. Monte Carlo simulations in statistical tolerance analyses are known better to represent the distribution of

manufacturing assemblies of parts [98], [109]. More informed tolerance design decisions can be made that better reflect the percentages of actual minimum and maximum tolerance parts, cutting down costs along the entire manufacturing, assembly, and inspection process [98], [101], [110]. The Monte Carlo simulation process can be broken down into four steps [97], [109]:

- (1) Define the dimension under analysis.
- (2) Generate a statistical distribution PDF for each component in the dimension under analysis. The PDF demonstrates the likelihood of an outcome based on the generated distribution.
- (3) Randomly sample each distribution until enough samples have been generated to plot a histogram (the essence of the Monte Carlo simulation).
- (4) Fit a distribution and PDF of the randomly sampled data set. Once created, a cumulative density function (CDF) can be generated. The CDF demonstrates how likely an outcome will be less than or equal to that value.

This analysis has been repeatedly done for manufacturing assembly tolerances for various applications, including gap predictions [111], [112]. A Monte Carlo shed light on what in the assembly process contributed to the gap created by lead pullback of QFN packages [98]. Another application predicted the distribution of different gap heights between flanges on wind turbines [111]. The probability that two gear teeth, after manufacturing and assembly, will adequately function is modeled by a Monte Carlo tolerance study [113]. This makes it very attractive to apply this type of analysis to the similar issue of the gap for the solder bond to fill in sandwich-structure MCPMs.

4.3 Monte Carlo Simulation for a Sandwich-Structure Multi-Chip Power Module

A Monte Carlo simulation will predict the maximum height mismatch between the posts before soldering the top substrate. The critical dimension to analyze is in the y-direction, as labeled in Figure 46. This results in the following layers to measure for the Monte Carlo simulation: substrates, sinter bonds, die, and posts. Each component labeled in Figure 47 has a distribution from the respective measurements. There are two types of sinter bonds: screen-printed and hand-dipped. These bonds each have separate distributions. Every post type in the module (kelvin, source, DBA, and midplane) also has its own distributions. The die distribution comprises 10 kV and 13 kV MOSFETs from AIST. The substrates could not be randomly sampled since there were only five samples of each top and bottom substrate. They do not have distributions created for them, but their warpages are known. They can be considered when constructing the modules and understanding their impact on the maximum height mismatch.

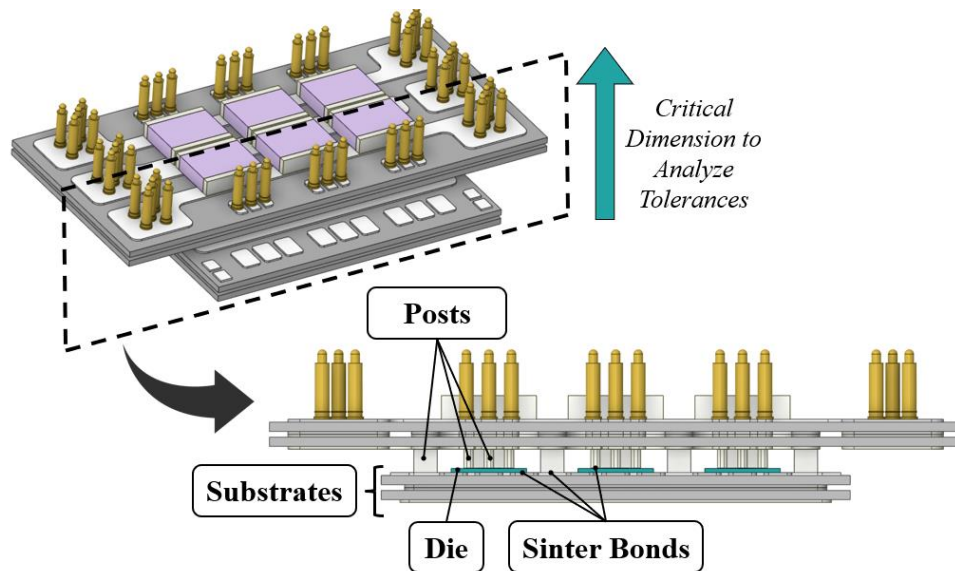


Figure 46: Side-view of MCPM consisting of four layers contributing to the tolerance stack-up: substrates, sinter bonds, die, and posts.

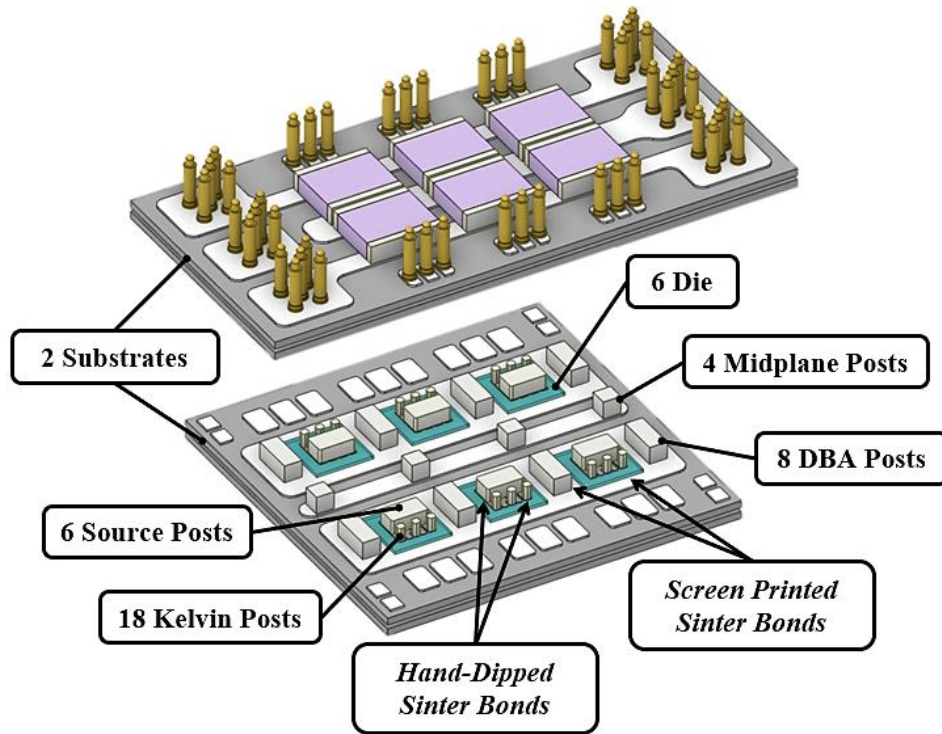


Figure 47: Each component in the statistical tolerance analysis that has a distribution generated for the Monte Carlo simulation.

4.3.1 Building the Monte Carlo Simulation

The entire process for the Monte Carlo simulation is shown below in Figure 48. To build distributions for each layer of the MCPM, many components need to be measured. Based on the central limit theorem, a rule of thumb for creating a distribution is a minimum of 30 data points [107, p.245]. In total, 308 kelvin posts, 134 source posts, 105 DBA posts, 63 midplane posts, 66 hand-dipped sinter bonds, 35 screen-printed sinter bonds, and 27 die were measured using either Mitutoyo Digimatic Micrometer or the Druker DekTak. The die are limited in measurement data compared to the other groups. However, since semiconductor fabrication is a very controlled process, the die's variation is less impactful than the other group's variation from the results.

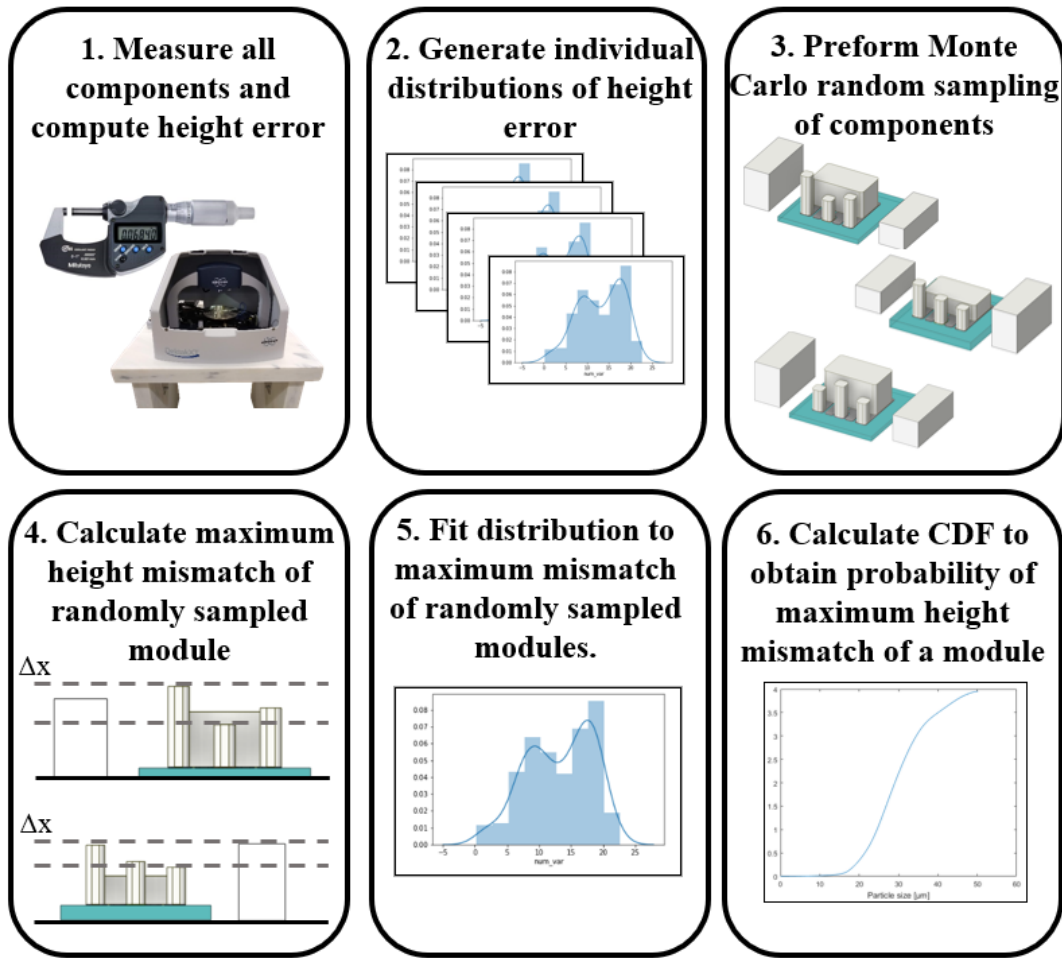


Figure 48: Monte Carlo statistical tolerance analysis simulation process.

Every post was measured with a Mitutoyo Digimatic Micrometer with a resolution of 1 mm to determine their distributions. To measure the hand-dipped sinter bonds and screen-printed sinter bonds, posts with known measurements were placed in the sinter paste on diced glass slides with known measurements. Glass was chosen to sinter the posts to due to its low CTE; thus, the measurement before and after sintering would have minimal deformation from the glass included [114]. The die were measured using the Bruker DekTak stylus profilometer previously used to measure the warpage of the substrates. After measuring all the layers for the stack-up, each measurement was subtracted from the nominal to quantify the error. It is important to note that every distribution consists of height errors. The reasoning for this is best explained in Figure 47. The goal is to achieve

the minimum mismatch across a module, and that does not only require that every component is in the specification since a net positive error of a post, when stacked onto a net negative of a sinter bond, can still result in a net mismatch of zero.

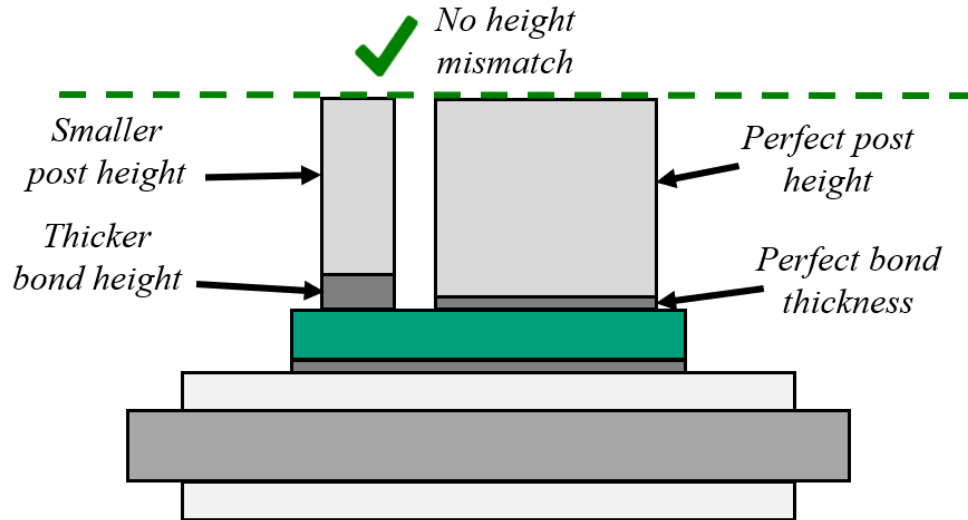


Figure 49: Visual representation of the motivation to perform the Monte Carlo simulation using component mismatch from nominal heights since the goal is not perfectly machined components but no mismatch when the tolerance of each component is stacked.

Once the height errors were determined for every point, different distribution types were fitted to the histograms to judge the best distribution for the data. Since data from manufacturing is often skewed, a Kernel distribution was chosen as the best fit for every layer. Kernel distributions are very smooth, meaning continuous, and do not experience sharp changes in the function, which indicates a good representation of the data. They are often used to represent the nonlinearity of many manufacturing and engineering part distributions [112], [115]. The distribution and PDF for the posts are in Figure 50, the sinter bonds in Figure 51, and the die in Figure 52.

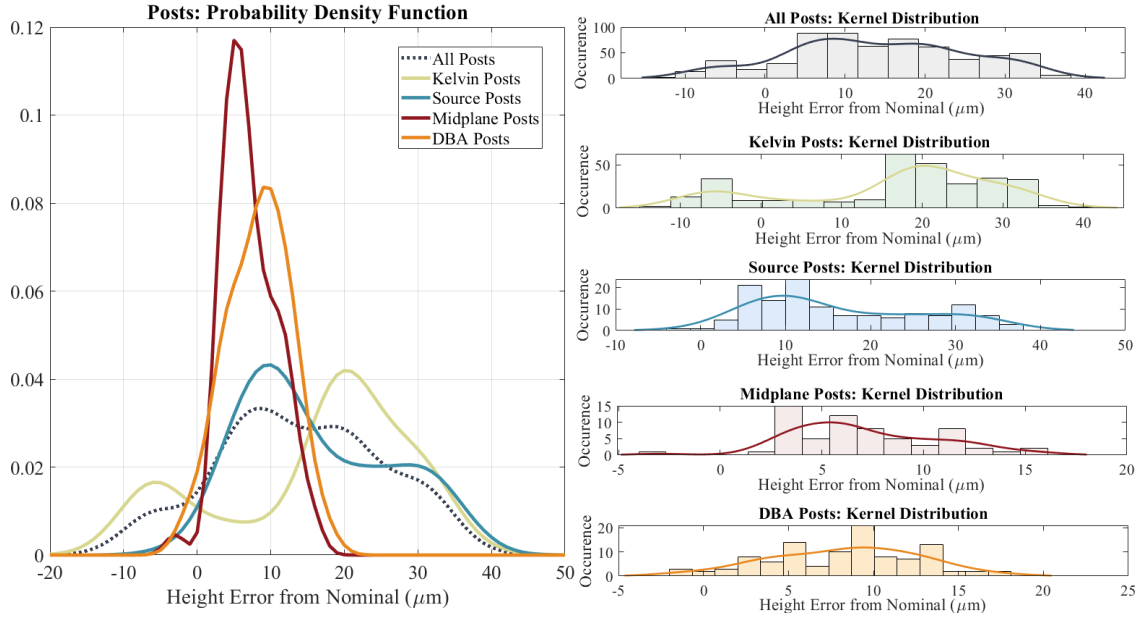


Figure 50: Post height error from nominal probability density function and each post's kernel distribution.

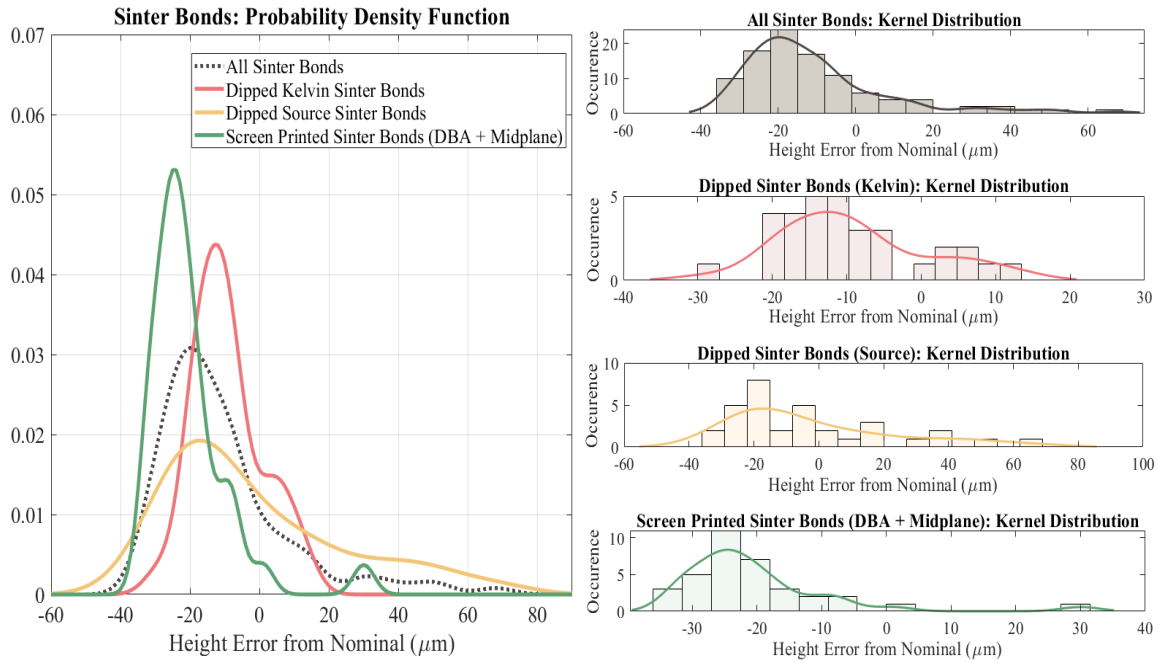


Figure 51: Sinter bond height error from nominal probability density function and each sinter bond's kernel distribution.

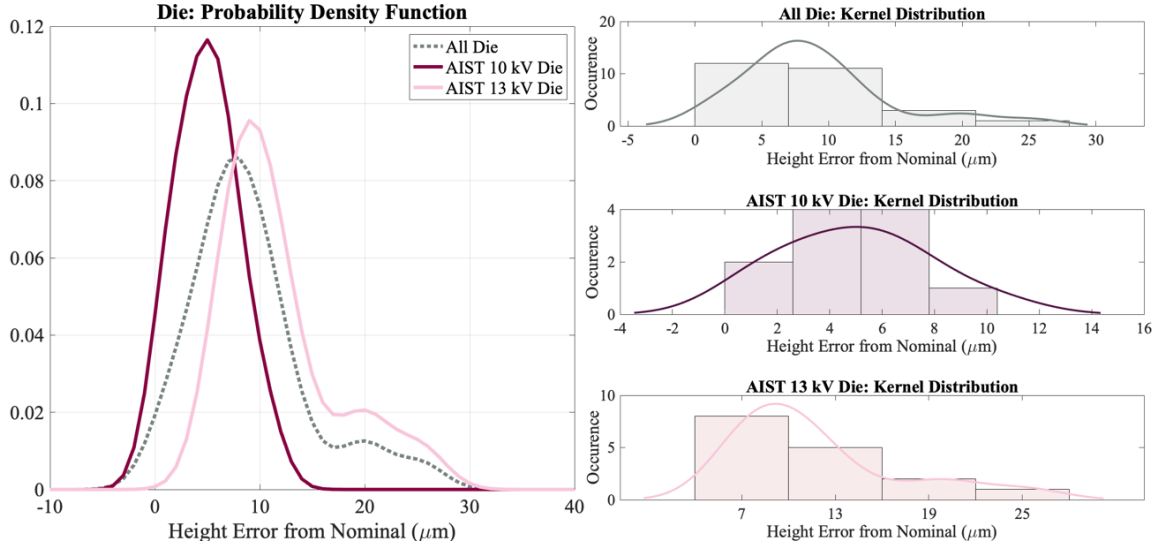


Figure 52: Die height error from nominal probability density function and each die's kernel distribution.

These distributions feed into the Monte Carlo simulation. First, each distribution is randomly sampled the number of times the component occurs in the MPCM. Thus, 18 kelvin posts, six source posts, eight DBA posts, four midplane posts, six die, 24 hand-dipped sinter bonds, and 18 screen-printed sinter bonds are randomly selected from their respective distributions. These values are stored in a 1x36 vector, and each location in the vector corresponds to a post designator and post location, shown in Figure 53.

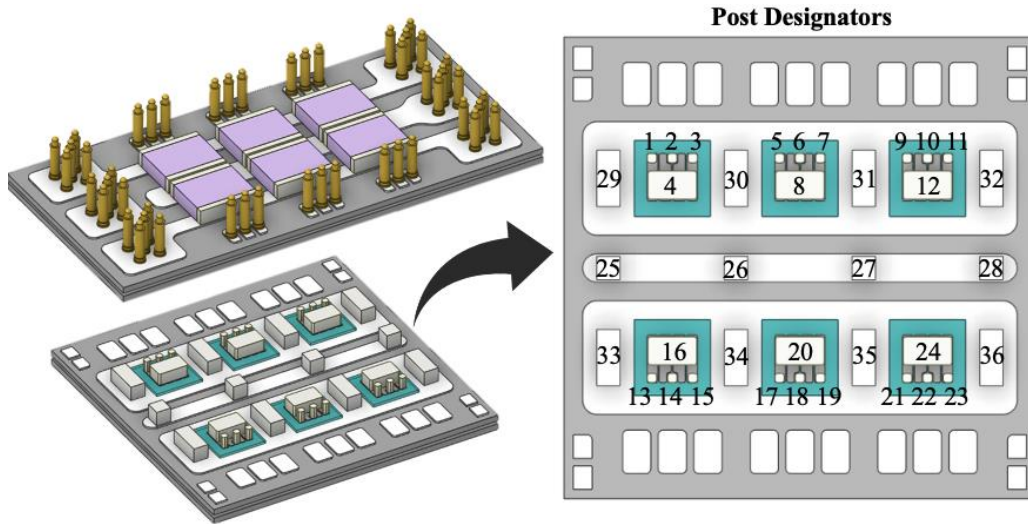


Figure 53: Post designators for the 1x36 matrix in the Monte Carlo simulation. Each post number corresponds to that column in the height mismatch matrix.

Each vector for every component is not complete, however. When looking at the tolerance stack-up in Figure 46, only some posts have the same bond type or a die beneath it. For example, the DBA posts consist of a mismatch from a screen-printed and their post, but they do not have a die or a hand-dipped bond. Thus, based on their designators, there is a zero populated in the die and hand-dipped bond mismatch array at the location of the DBA posts. This will be further explained in the following example.

Table 10 represents a matrix created from randomly sampling the screen-printed bond distribution for an MCPM shown in Figure 54. Based on Figure 53, the first four columns correspond to the location of 3 kelvin posts and one source post on top of a die. While the post bonds are hand-dipped, the die is placed in a screen-printed bond. Thus, the screen-printed sinter bond height mismatch matrix is populated with the same mismatch in columns 1-4 to represent the screen-printed bond for that die. Later in the matrix, locations 27, 28, 29, and 30 correspond to two midplane posts and two DBA posts. Those posts all have their screen-printed bonds; thus, they all have their own sampled bond.

Monte Carlo: Randomly Sampled Screen-Printed Sinter Bonds

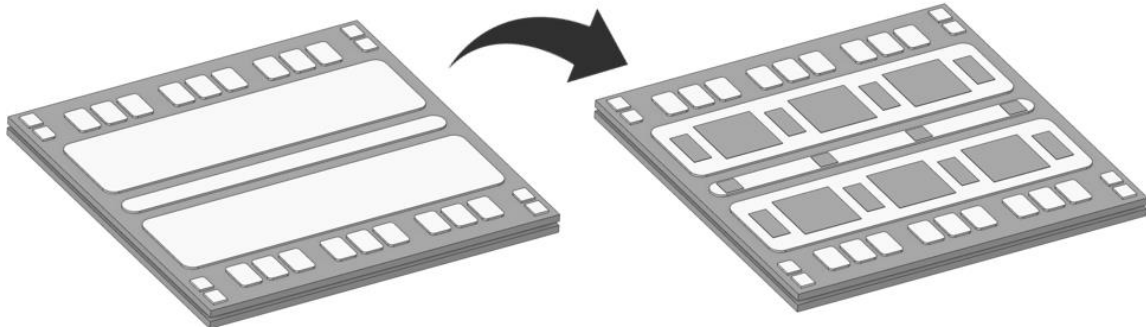


Figure 54: Monte Carlo simulation: Random sampling of 18 screen-printed sinter bonds for an MCPM. Their height mismatches correspond to Table 10.

Table 10: Screen-Printed Sinter Bond Height Mismatch Matrix Based on Locations in Figure 53.

1	2	3	4	...	27	28	29	30	...
12 μm	12 μm	12 μm	12 μm	...	9 μm	27 μm	14 μm	-6 μm	...

Table 11 represents a matrix created by randomly sampling the die distribution for an MCPM, shown in Figure 55. As mentioned, the first four columns are all posts on a die (Figure 53). Since it is the same die under those four posts, columns 1-4 are populated with only one die sampled, thus one mismatch measurement. Once reaching the columns corresponding to the two midplane posts and two DBA posts, it is shown in Figure 55 do not have a die beneath them. Thus, the die matrix has 0 mm of mismatch at that location.

Monte Carlo: Randomly Sampled Die

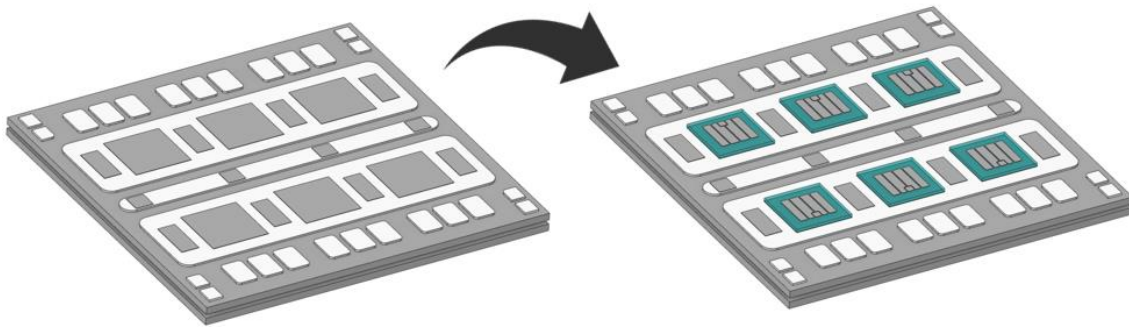


Figure 55: Monte Carlo simulation: Random sampling of 6 die for an MCPM. Their height mismatches correspond to Table 11.

Table 11: Die Height Mismatch Matrix Based on Locations in Figure 53.

1	2	3	4	...	27	28	29	30	...
1 μm	1 μm	1 μm	1 μm	...	0 μm	0 μm	0 μm	0 μm	...

The concept continues to Table 12, representing the matrix of hand-dipped sinter bonds on top of the die shown in Figure 56. Every location with a kelvin post and a source post will have a mismatch populated from sampling the hand-dipped sinter bond distribution, but since the midplane and DBA posts only have a screen-printed bond, those locations have 0 μm of mismatch.

Monte Carlo: Randomly Sampled Hand-Dipped Sinter Bonds

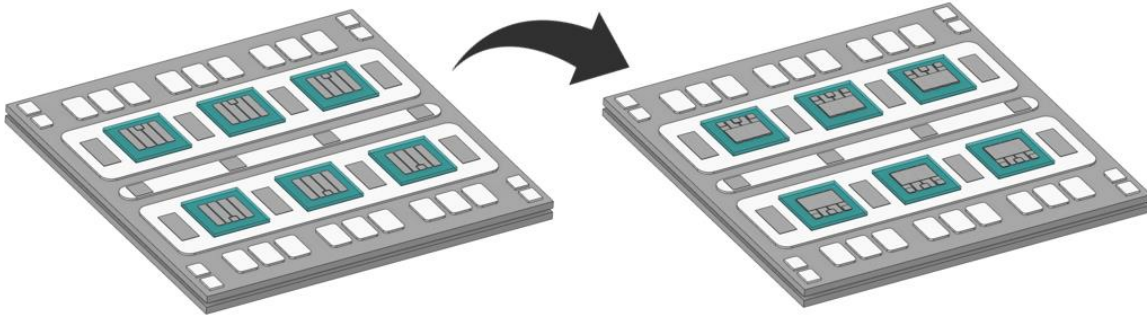


Figure 56: Monte Carlo simulation: Random sampling of 24 hand-dipped sinter bonds for an MCPM. Their height mismatches correspond to Table 12.

Table 12: Hand-Dipped Sinter Bond Height Mismatch Matrix Based on Locations in Figure 53.

1	2	3	4	...	27	28	29	30	...
24 μm	16 μm	-3 μm	21 μm	...	0 μm	0 μm	0 μm	0 μm	...

Finally, all the posts are sampled (36 total) in Figure 57 to populate the post height mismatch matrix. One row of each matrix represents the components for one MCPM. This random-sampling, matrix-populating process repeats 10,000 times, resulting in a 10,000x36 matrix where each row is a different potential MCPM.

Monte Carlo: Randomly Sampled Posts (Kelvin, Source, DBA, Midplane)

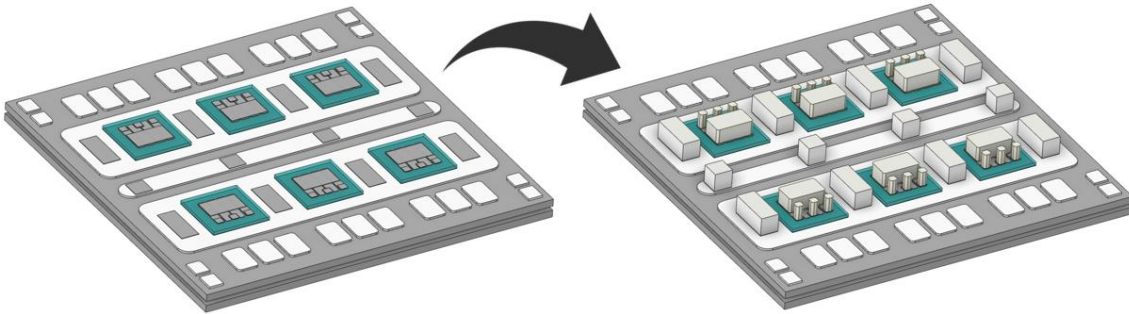


Figure 57: Monte Carlo simulation: Random sampling of 36 posts for an MCPM. Their height mismatches correspond to Table 13.

Table 13: Post Height Mismatch Matrix Based on Locations in Figure 53.

1	2	3	4	...	27	28	29	30	...
22 μm	5 μm	17 μm	31 μm	...	6 μm	12 μm	14 μm	-22 μm	...

Once the 10,000x36 matrix for each layer in the tolerance stack-up is populated, every matrix is summed into one matrix to create the entire MCPM mismatch. That is why

the respective component matrices must have zeros populated in their appropriate locations, so they do not sum to create more mismatch at a post location that does not have that specific component. This summed matrix is shown as an example for one module (one row) in Table 14, which shows the sum of Table 10 to Table 13.

Table 14: Total Height Mismatch Matrix Across One MCPM Based on Locations in Figure 53 (Summation from Table 10 to Table 13).

1	2	3	4	...	27	28	29	30	...
59 μm	34 μm	30 μm	65 μm	...	15 μm	39 μm	28 μm	-28 μm	...

The range is taken from the total mismatch table of the module to obtain the maximum mismatch across one module, and that number is stored. For this example, the maximum height mismatch for an MCPM from the Monte Carlo simulation is 93 mm. This process generates 10,000 MCPMs maximum height mismatch, resulting in a 10,000x1 vector of maximum height mismatch that can occur across an MCPM. With 10,000 samples, a robust distribution can be fit, and the expected probability of the maximum height mismatch for an MCPM can be attained from integrating that PDF. This was done for a single die (3 kelvin posts, one source post, and four hand-dipped sinter bonds), a two-die module (6 kelvin posts, two source posts, 4 DBA posts, two midplane posts, eight hand-dipped sinter bonds), and the full MCPM.

4.3.2 Results from the Monte Carlo Simulation

The distributions from the Monte Carlo simulation for a single die (one die, four Mo posts), two-die module (two die, 14 Mo posts), and MCPM (six die, 36 Mo posts) are shown in Figure 58, Figure 59, and Figure 60, respectively. The CDF created from the distributions of the Monte Carlo simulation is shown in Figure 61. It is evident that as the number of die in parallel increases, so does the maximum height mismatch possible. With an MCPM, it is impossible to achieve no mismatch and only about a 55% chance of

achieving a mismatch of less than 100 μm . This is very insightful to understanding why the yield of the MCPMs is much lower than the 1/3 modules that typically do not experience issues with yield noting the drastic difference in the minimum height mismatch that can be achieved. While 200 μm of solder paste is screen-printed to fill this gap, it is known that solder loses about half its volume during reflow when the flux burns off [86], [116].

However, it is essential to note that this CDF does not indicate yield; it only indicates maximum height mismatch. Using engineering knowledge, inferences and hypotheses can be made about why this CDF can identify the yield issues, such as correlating maximum height mismatch and yield. A better understanding of these relations will be explored in the next section. To the best of the author's knowledge, this is the first statistical tolerance analysis of these sandwich-structure MCPMs and can pave the path to understanding what processes need control to reduce the maximum mismatch and target the improvement in yield of these modules.

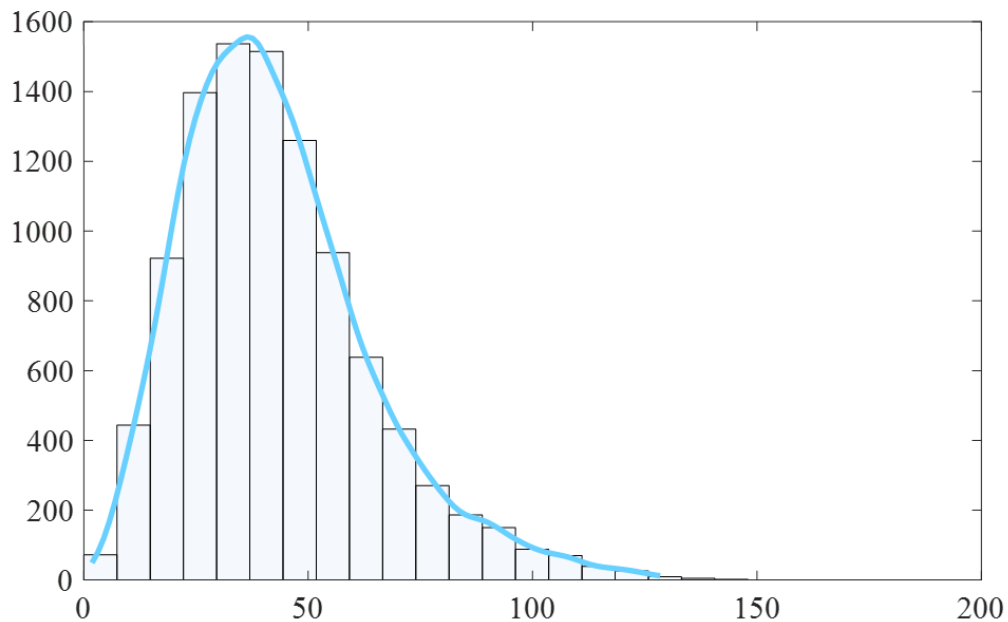


Figure 58: Single die Monte Carlo simulation: kernel distribution of the maximum height mismatch for 10,000 modules.

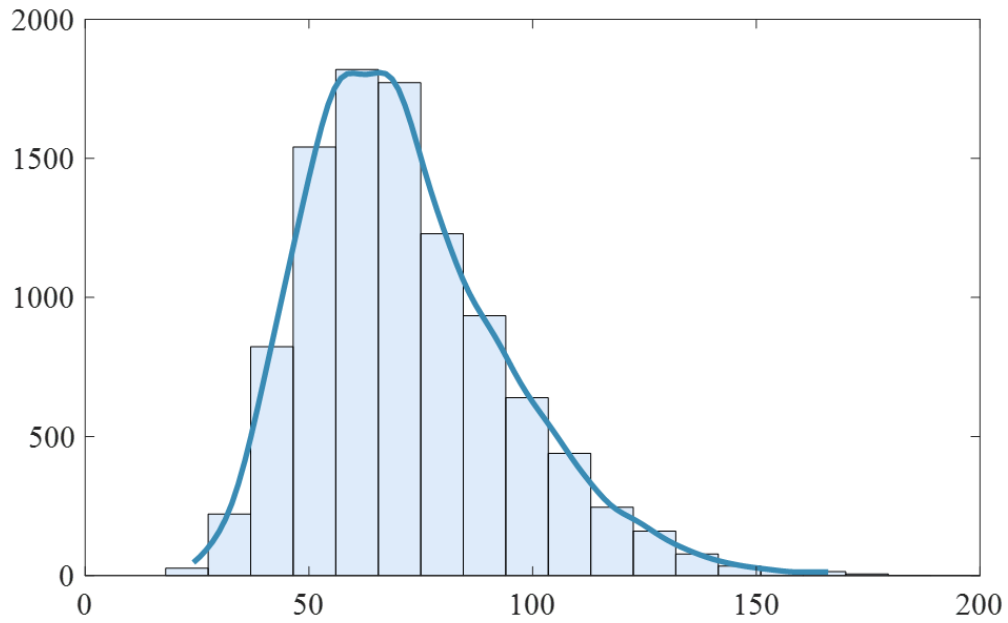


Figure 59: Two-die module Monte Carlo: kernel distribution of the maximum height mismatch for 10,000 modules

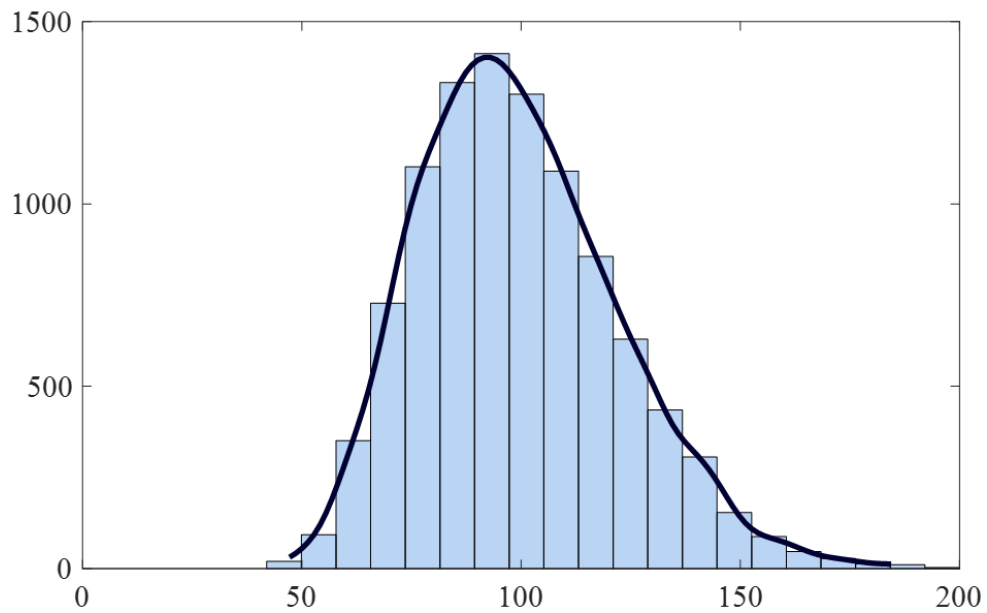


Figure 60: MCPM Monte Carlo simulation: kernel distribution of the maximum height mismatch for 10,000 modules

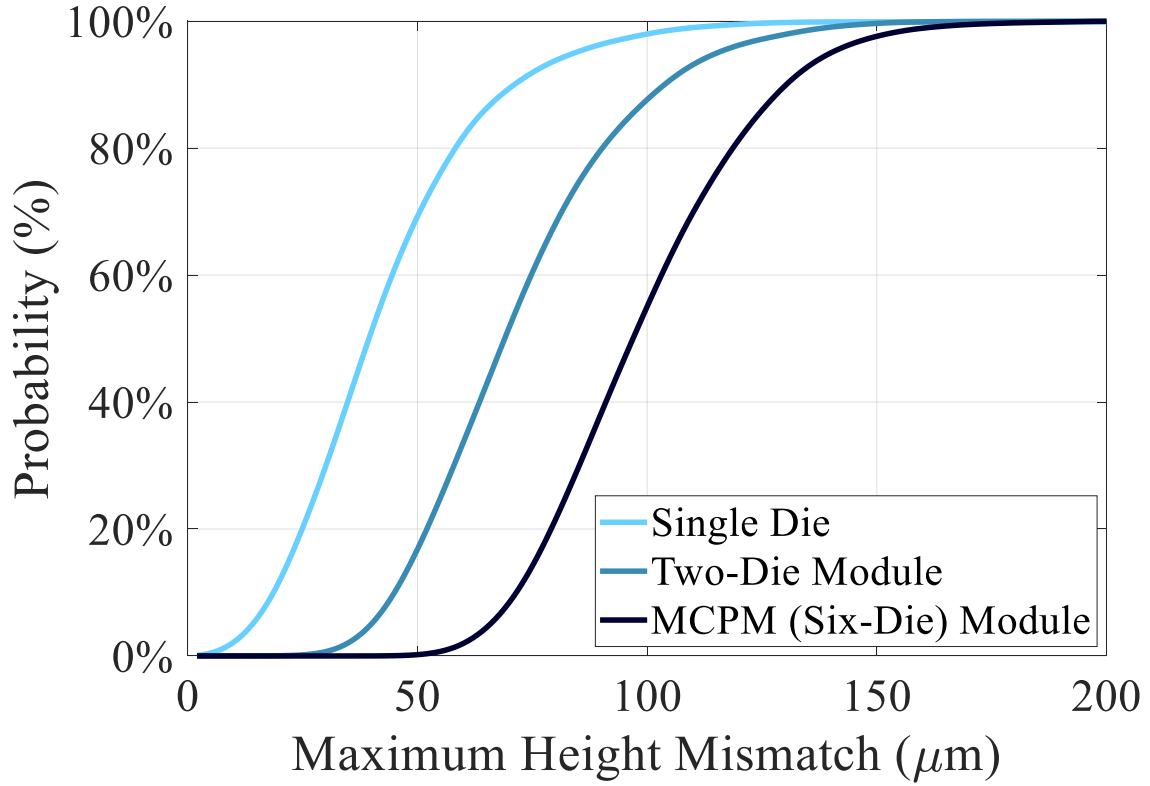


Figure 61: CDF for the maximum relative height mismatch comprised of a distribution of 10,000 randomly sampled modules from a Monte Carlo simulation.

4.4 ANOVA Analysis Using the Monte Carlo Simulation

Using the Monte Carlo simulation results, it is desirable to understand which layer in the Monte Carlo is considered a controllable variable. Controllable variables have the most impact on a procedure, and by identifying them and quantifying their impact, these statistical experiments can improve yield and reduce variability in the process [107, p. 540]. That way, a targeted approach can be taken to improve the yield of these sandwich-structure MCPMs.

This is typically done with an analysis of variance (ANOVA). An ANOVA determines if data from several groups have a common mean. The different groups are called treatments. The ANOVA tests the following for a group of treatments, $\tau_1, \tau_1, \dots \tau_n$:

$$H_0: \tau_1 = \tau_2 = \dots = \tau_n = 0 \quad (7)$$

$$H_1: \tau_i \neq 0 \text{ for at least one } i \quad (8)$$

This null hypothesis (7) returns true if all treatment means are equal with little random error contribution, meaning no specific treatment affects the controlled group. If the null hypothesis is rejected, the alternative hypothesis (8) is accepted, meaning at least one mean is statistically different from the control. However, it does not indicate which mean is statistically different. To find which mean is statistically different, a Tukey's honestly significant difference (HSD) can identify which treatments are statistically different from the control group. Tukey's HSD takes the ANOVA results as input and identifies which specific treatments are statistically different from the control and other treatments [107, p.540-545,549].

In the case of the MCPM, each treatment is a different layer of the tolerance stack-up (screen-printed sinter bonds, die, hand-dipped bonds, and posts), and the response to these treatments is the maximum height mismatch across an MCPM. The following distributions are created to test if each treatment's means are statistically equal to the control variable (a randomly sampled module). The previously detailed Monte Carlo simulation is completed as expected. Next, the screen-printed sinter bonds are fixed to have no mismatch and 10,000 modules are sampled, and the distribution is built. This continues, where another distribution fixes the post heights to have no mismatch, the hand-dipped bonds, and the die. Once these distributions are each separately generated, the ANOVA is performed to determine which groups statistically impact the mean, meaning that one of these treatment levels is a controllable variable.

Each distribution is generated, and their CDFs are shown in Figure 62. While the CDF indicates that there are variables that exhibit control authority based on the shifted

curves, the visual inspection of the CDF is not a statistically mathematical method to evaluate the impact of the fixed components means. Thus, the ANOVA can statistically analyze if treatments impact the response by comparing the means. The ANOVA is robust to non-normal data, but for accuracy, the log of each dataset is imported into the ANOVA to transform the data to normal. This method is standard for ANOVA analysis on skewed or non-normal data [107, p.463-465]. As shown from the ANOVA results in Table 15, using a 95% confidence interval, the p-value returned is 0, less than the associated significance level at 95% (0.05), meaning there is a statistical difference between different treatments. The large F-statistic also indicates a rejection of the null hypothesis. Thus, Tukey's analysis can be performed to determine which treatments are statistically different from the control group.

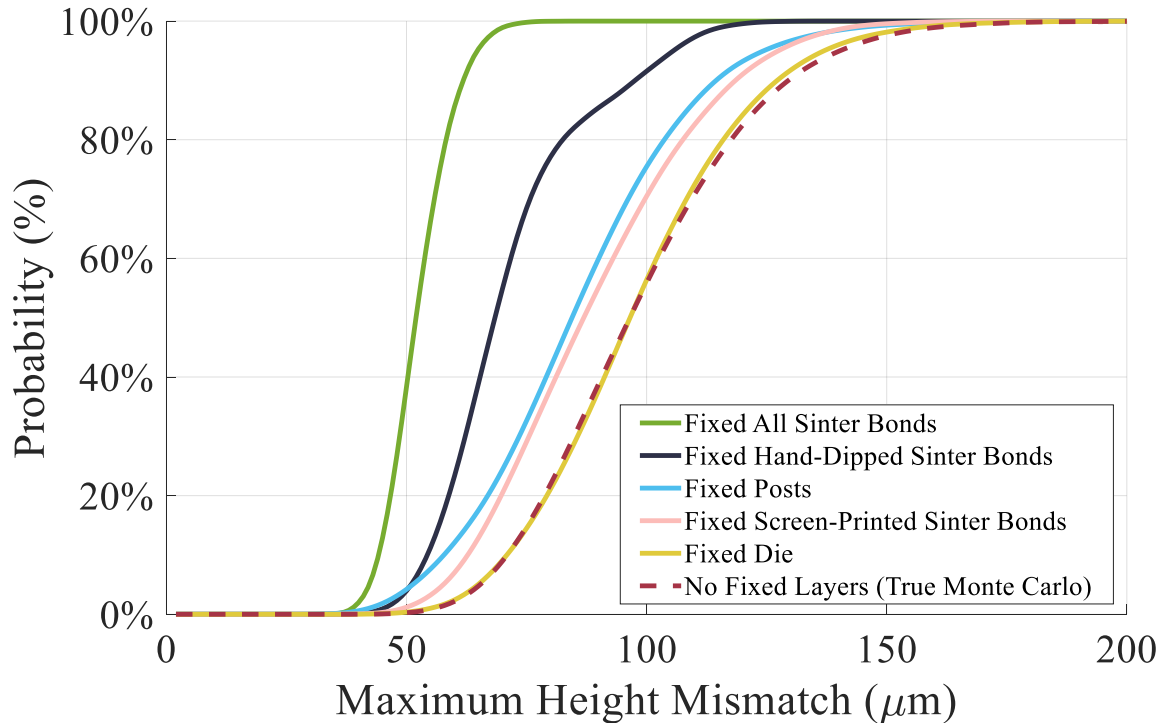


Figure 62: MCPM cumulative density function (CDF) for relative height mismatch with different layers fixed at zero height mismatch (i.e., perfectly planar).

Table 15: Full-Module ANOVA Results from Different Fixed Components.

Source	Degrees of Freedom	Sum of Squares	Mean Square	F Ratio	Prob > F
Treatments	5	2844.98	568.995	11888.5	0
Error	59994	2871.37	0.048		
C. Total	59999	5719.35			

From Tukey's analysis in Table 16 and represented in Figure 63, every group except for the die impacts the maximum mismatch based on the comparison of the means of each treatment. An ordered letters report in this table groups the rows based on which are statistically significant to each other. From this lettering, only the fixed die has the same letter as the control, the true Monte Carlo random sampling of an MCPM. This means the mean of the fixed die distribution is not statistically different enough from the mean of the randomly sampled module (98.08 and 98.27, respectively), and the fixed die distribution is the only p-value greater than 0.05 (set by the 95% confidence interval). Thus, the die has little impact on the maximum height mismatch compared to the other groups with distinct letters.

Table 16: Tukey's HSD Ordered Letters Report for the MCPM Fixed Layer Treatments Compared to the Control Group (No Fixed Layers, True Monte Carlo).

Treatment					Mean	P-Value
CONTROL: No Fixed Layers (True Monte Carlo)	A				4.5675	NA
Fixed Die	A				4.4207	0.55
Fixed Posts		B			4.5623	$2.07 \cdot 10^{-8}$
Fixed Hand-Dipped Sinter Bonds			C		4.2393	$2.07 \cdot 10^{-8}$
Fixed Screen-Printed Sinter Bonds				D	4.4597	$2.07 \cdot 10^{-8}$
Fixed All Sinter Bonds				E	3.9447	$2.07 \cdot 10^{-8}$

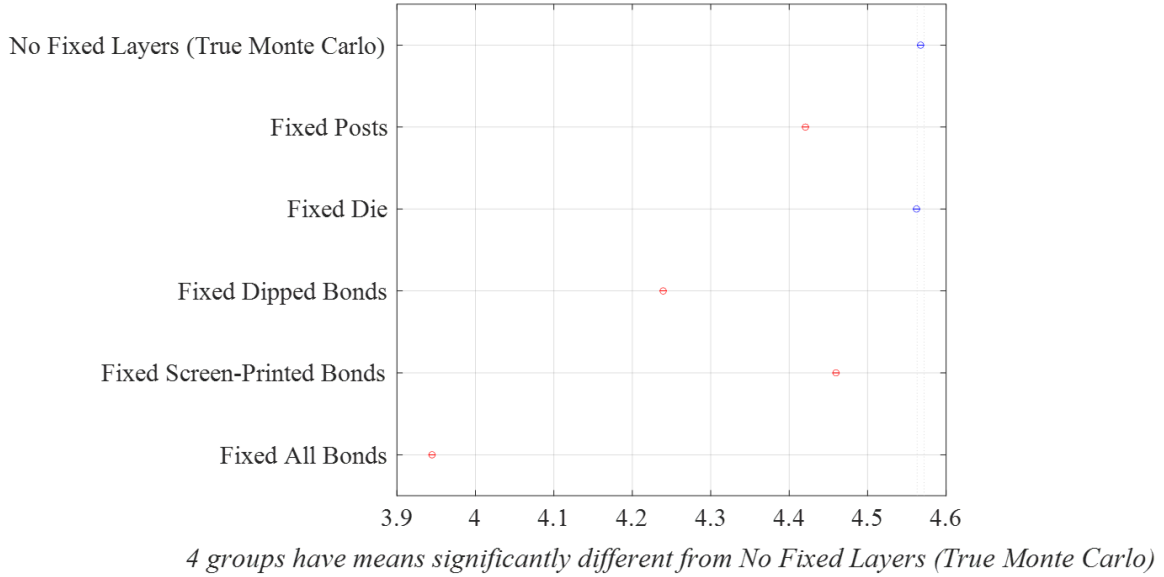


Figure 63: Visual interpretation of Tukey's HSD demonstrating that every layer of the module is statistically different from the randomly sampled module, meaning there is control authority over which each of those layers except the die.

4.5 Scalability of the Monte Carlo Analysis

Using the results from the single-die, two-die, and six-die MCPM, it is evident that the maximum height mismatch will increase as more devices are added in parallel. The Monte Carlo Analysis was run from a single die to twelve die in parallel. As shown by Figure 64, the maximum mismatch increases as the number of die in parallel, but it increases in smaller increments. This is most likely because the distribution is limited to a specific maximum mismatch range, so additional die after a certain point will start to have less effect on the maximum height mismatch.

By analyzing the maximum height mismatch at different probabilities, it is clear that there is a logarithmic increase with the increased number of die in a module. At some point, no matter how many die are added in parallel, the maximum mismatch will start to plateau at around 150 μm with a 90% probability of occurring. This provides insight into

the feasibility of the maximum height mismatch that there needs to be a concern about when the module is scaled to more and more die.

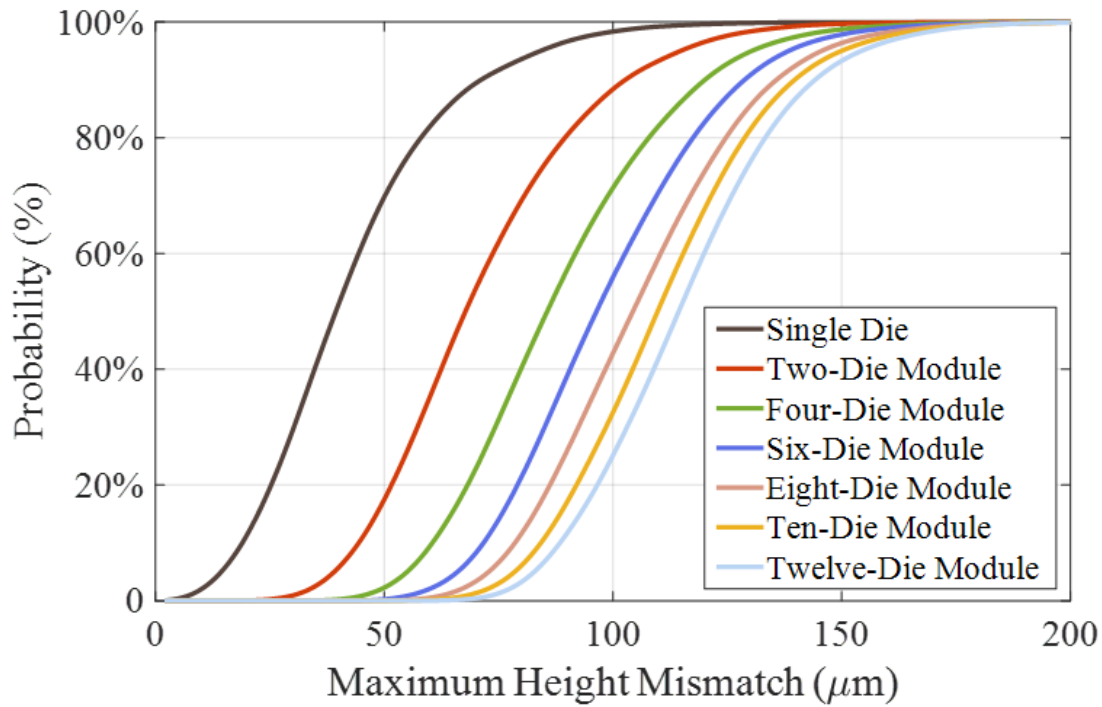


Figure 64: CDF of the maximum height mismatch of different die counts ranging from a single die to a twelve-die module from left to right.

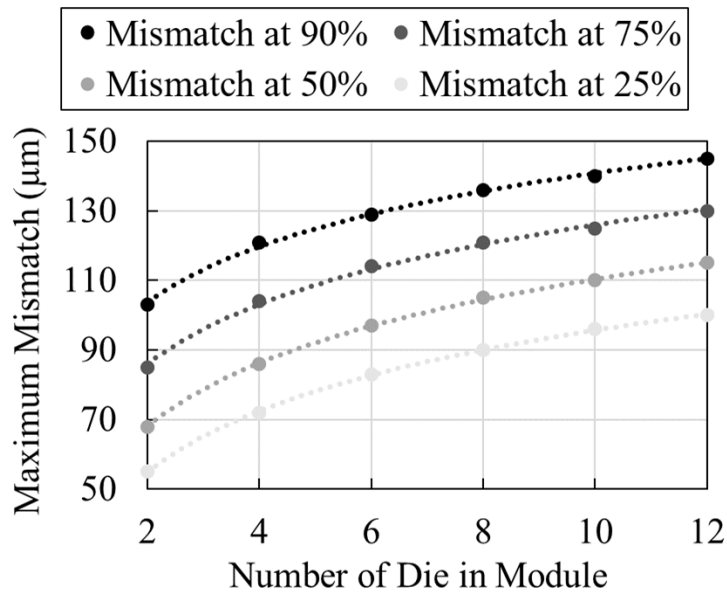


Figure 65: Relationship between the maximum height mismatch across a module with a certain number of die at varying percentages from top to bottom: 90%, 75%, 50%, and 25%.

Another valuable way to further scale the ANOVA analysis with more die in parallel is to understand the impact of reducing the mismatch of the hand-dipped sinter bonds. From the six-die MCPM, a significant improvement in the mismatch was noted. It is beneficial to analyze if that notion will still hold with the additional die in parallel. The way to fix the dipped sinter bonds in the assembly of this module would be to use silver preform, like for the sintering of the substrates, which has a controlled thickness. Figure 64 was reassessed, instead of with dipped sinter bonds but with perfectly matched preform bonds. The results are shown in Figure 66. There is a significant reduction in the maximum height mismatch using this method. For example, a 12-die module fabricated with hand-dipped sinter bonds has a 25.1% chance of achieving 100 μm of mismatch. However, when the dipped bonds are preplaced with silver preform, the 12-die module now has an 85.1% chance of achieving 100 μm of mismatch. This dramatically improves the likelihood of fabricating successful, wirebond-less multichip power modules.

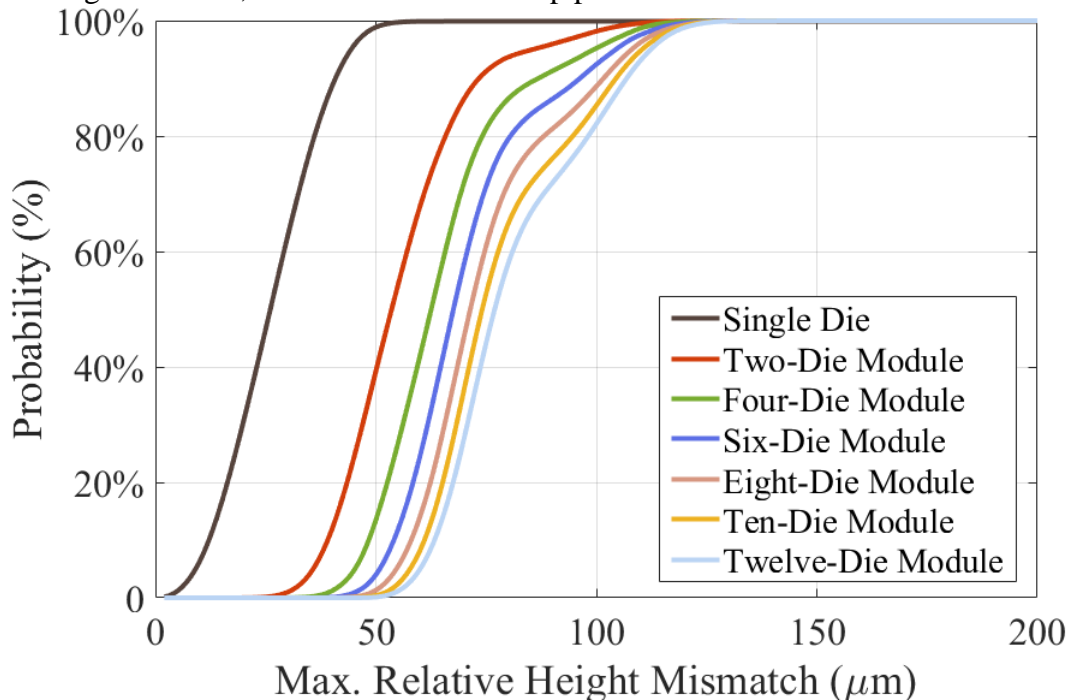


Figure 66: CDF of the maximum height mismatch of different die counts ranging from a single die to a twelve die module from left to right using silver preform instead of hand-dipped sinter bonds.

The final scalability analysis using the Monte Carlo is to include the substrates. As mentioned, these substrates were not included in the original analysis because there were only five samples, and their warpages could not represent the actual substrate population since a sample would require at least 30 substrates. However, to analyze the importance of the warpage impact, as noted in Chapter 2, an average substrate model was created from the five samples for each substrate type, then added to the final CDF. It is noted that there are more accurate representations of the substrate's warpage impact and that this is not a statistical analysis, but it is beneficial to visualize the potential effects. The measured substrates for DBA1-2 and DBA3-4 are shown in Figure 67 and Figure 68, respectively, with the average warpage noted in a dashed grey.

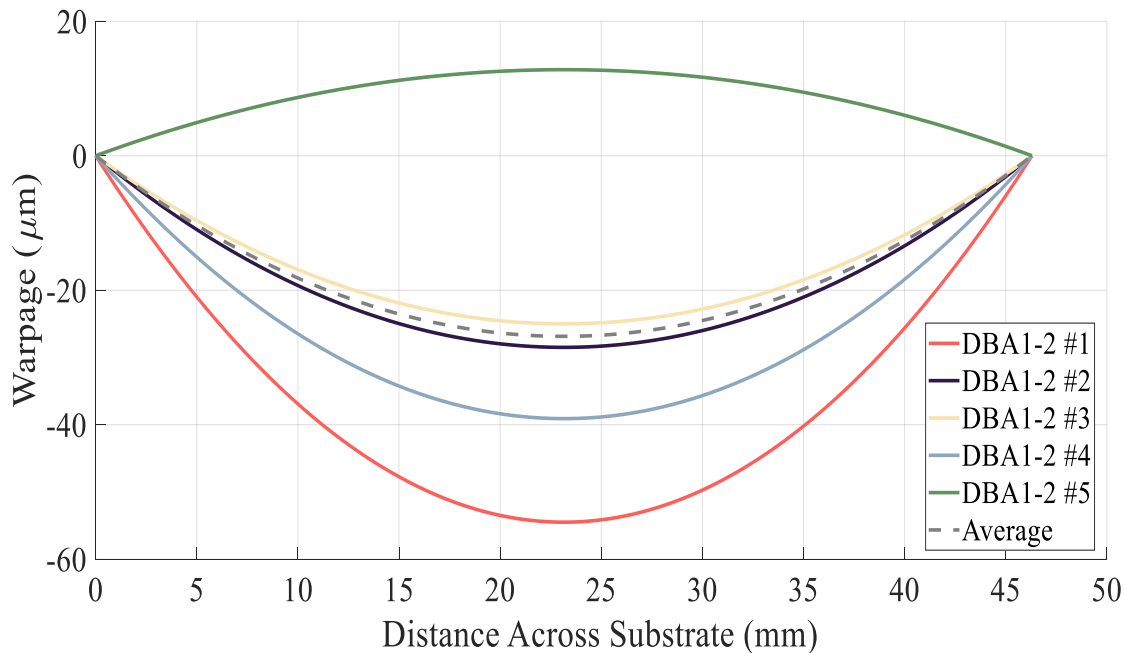


Figure 67: Maximum warpage trends of each DBA1-DBA2 substrate pair after sintering, with their average model used for the Monte Carlo represented by the dashed grey line.

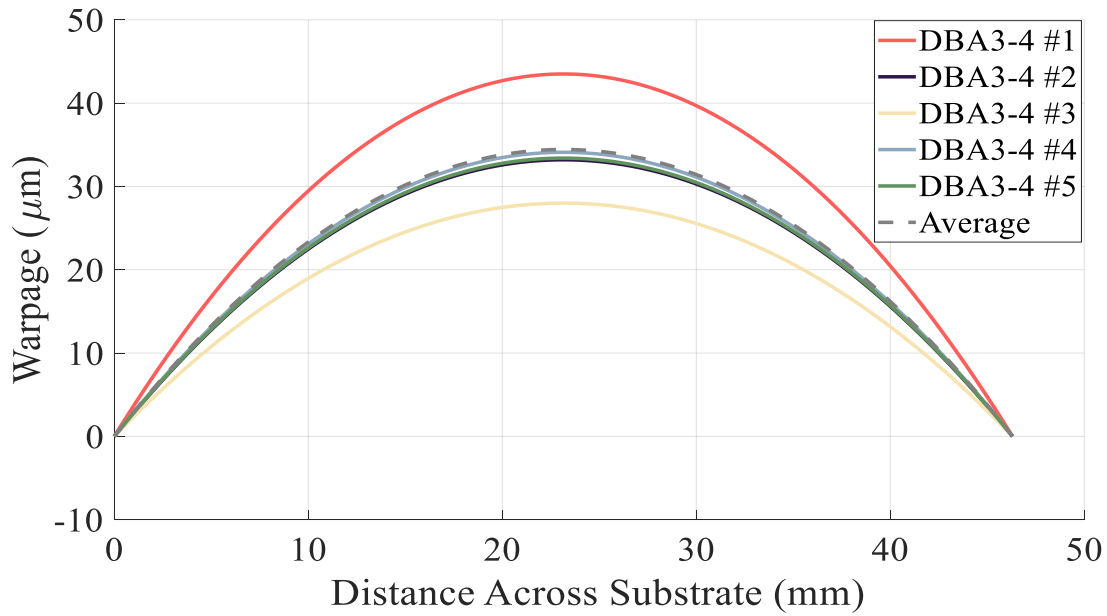


Figure 68: Maximum warpage trends of each DBA3-DBA4 substrate pair after sintering, with their average model used for the Monte Carlo represented by the dashed grey line.

The analysis was conducted by comparing the completely randomly sampled module without substrates, the randomly sampled module with DBA1-2 warpage, the randomly sampled module with DBA3-4 warpage, and finally, the randomly sampled module with both substrates. In this way, the impact of each substrate can be analyzed. Figure 69 depicts the impact of the maximum height mismatch for each of these cases. It is shown that DBA1-2 introduces less warpage than DBA3-4. This is most likely because its metal pads are much larger and more symmetrical compared to the patterning variations on DBA3-4. Overall, from the Monte Carlo without substrates to the Monte Carlo with substrates, the probability of achieving 100 μm of mismatch decreases from 55% to 36%. There is less of a decline as the maximum mismatch increases, which follows the same ideology as the logarithmic trend from an increasing die in parallel. To achieve 150 μm of mismatch, there is only a decrease from 97% to 96%. Therefore, future work is essential

to create a more representative distribution of the substrate warpage since there is quite a significant impact on the CDF.

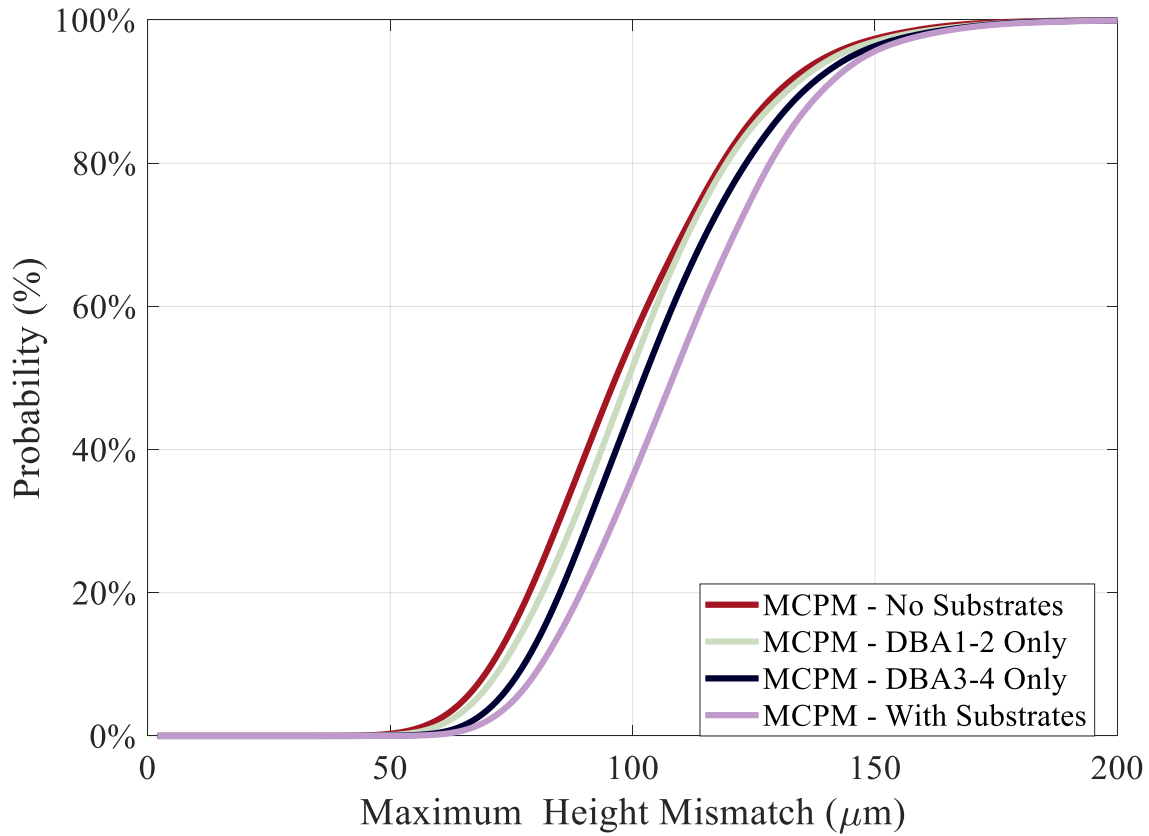


Figure 69: CDF of the MCPM without substrates (red), with DBA1-2 (light green), with DBA3-4 (dark blue), and with both substrates (light purple), in that order from left to right.

4.6 Summary

In summary, the statistical tolerance performed addresses the crux of the fabrication challenges for MCPMs by understanding which components contribute the most height mismatch to the overall module. A Monte Carlo simulation randomly samples different components within an MCPM to understand the maximum height mismatch across these components. These distributions were built by measuring the posts, different types of sinter bonds, and die thicknesses. While future work will explore possible methods to replace the hand-dipped bonds, for this work, the MCPMs in the following chapter will be fabricated

by fixing posts as the first solution in an effort to lower the maximum height mismatch across the module.

From the statistical tolerance analysis, the following questions with the fabrication of the MCPM were addressed: why are the MCPMs more challenging to fabricate successfully, and what components have the most control in reducing the maximum height mismatch. From Figure 61, it is clearly shown that the reason MCPMs are more challenging to fabricate is due to the significant increase in the lowest mismatch achievable. The more devices in parallel, the more variation that is introduced across the module. This can be a root cause for missed connections and disconnected devices, compared to the two-die modules, which have four fewer devices and historically have a higher yield. Additionally, from the ANOVA results and CDF in Figure 62, it is noted that the bondlines have the most significant control authority in reducing the maximum mismatch across an MCPM, specifically the hand-dipped bonds. While those are the most difficult to control, fixing the post heights also reduces the maximum height mismatch. This knowledge will be used to fabricate a mechanical and functional MCPM in the following chapter.

Chapter 5 Experimental Validation of the Fabrication Refinements and Statistical Tolerance Analysis for the Multichip Power Module

5.1 *Introduction*

This chapter focuses on validating the electrical performance of modules with refined fabrication techniques. Each chapter verifies each technique individually, and this chapter will employ the refinements and conduct static and dynamic characterization of the modules. Results from the fabrication refinements described in Chapter 2 and 3 show promise for the successful fabrication of MCPMs; however, due to the limited availability of 13 kV die, scaled-down versions of the module with one die per switch position was first fabricated and characterized to de-risk the final functional module fabrication. The sandwich-structure module has two die and 14 Mo posts of varying sizes, making it an excellent candidate for analyzing the impact of fabrication refinements on characterization behavior.

First, a semi-functional two-die module with off-the-shelf devices from Wolfspeed is fabricated and statically characterized to verify that the fabrication process does not damage the characteristics of the MOSFET. Next, six functional two-die modules are built out of six attempts, and statically characterized using research-level die from AIST, and one 13 kV module is double-pulse tested. Finally, a mechanical MCPM is fabricated to understand the impact of the statistical tolerance analysis and a functional MCPM. The functional MCPM is statically characterized. The materials used for fabricating the modules are listed below in Table 17.

**Table 17: Packaging Process Details for the Multi-Chip Power Module
Corresponding to Figure 7.**

Component	Material Specifications	Assembly Process
<i>Substrate</i>	AlN ceramic, Al pads with Ag plating, 1-mm vias	Fabricated by DOWA METALTECH
<i>Substrate-Substrate Attachment</i>	NBE Tech nano-silver preform	Pressure-assisted silver sintering
<i>Post Interconnect</i>	Mo with 100-200 nm Ti and 200-500 nm of Ag	Fabricated by Saneway Electronic Materials
<i>Die</i>	13 kV, 5 A SiC	Fabricated by AIST
	10 kV, 5 A SiC	Fabricated by AIST
	10 kV, 20 A SiC	Fabricated by Wolfspeed
<i>Post-Die Attachment</i>	NBE Tech nano-silver paste	Pressure-less silver sintering
<i>Die-Bottom Substrate and Post-Bottom Substrate Attachment</i>	Kyocera Nano-silver Paste	Pressure-less silver sintering
<i>Post-Top Substrate Attachment</i>	Sn96.3/Ag3.7	Solder reflow (conduction)
<i>Spring-Pin and Capacitor Attachment</i>	Gold plated spring pins, 820 pF C0G capacitors, Sn63/Pb37	Solder reflow (forced convection)
<i>Housing</i>	Formlabs high-temp photopolymer resin	Formlabs Form3+ 3D Printer
<i>Encapsulate</i>	Wacker SilGel 612	Outgas mixture and pour, cure 24 hours in air

5.2 Two-Die Module Fabrication and Characterization

5.2.1 Mechanical Two-Die Module Fabrication and Characterization

A scaled-down version of the MCPM (named a two-die module) is first constructed with semi-functional devices from Wolfspeed, shown in Figure 70. The two-die module was presented in the statistical tolerance analysis in Figure 61 and had a much lower maximum mismatch than the MCPM. This module fabrication aims to characterize the devices after each step of fabrication to ensure the sintering and soldering processes do not

cause any damage to the devices. However, due to limited substrate materials, the module is fabricated with single substrates instead of the pressure-sintered stacked substrates. Since the devices are not involved in the sintering of the substrates, it does not impact their functionality and is not necessary for this section.

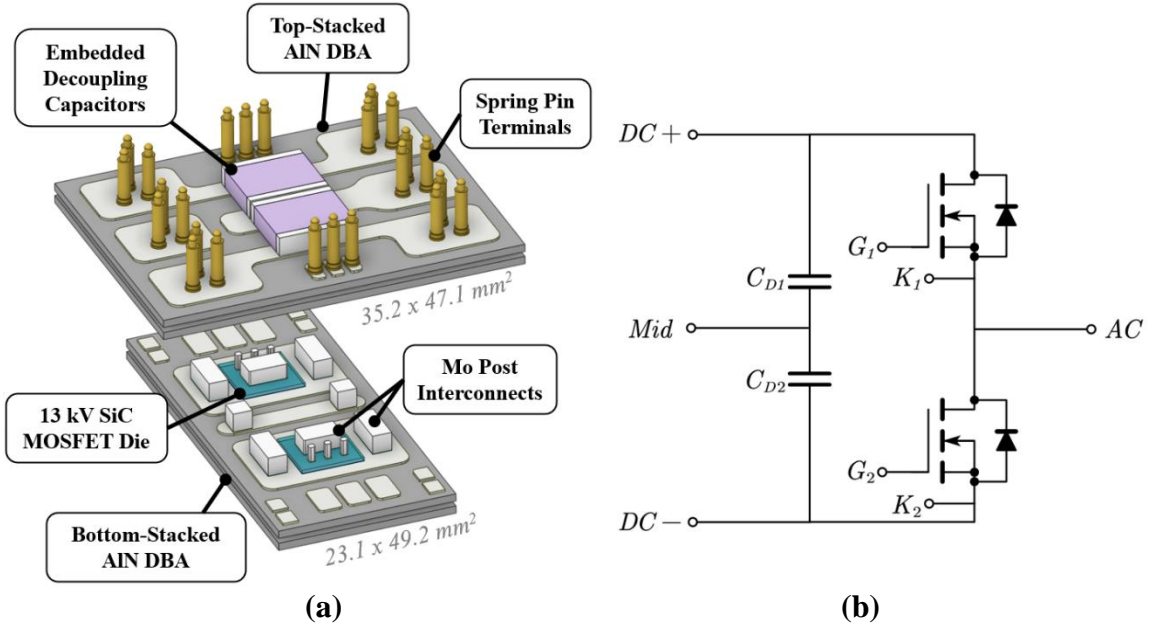


Figure 70: (a) Two-die SiC half-bridge power module with callouts of components. (b) Two-die module circuit diagram with one die per switch position.

The fabrication follows the same process presented in Figure 7 for the MCPM and is shown below in Figure 71, and each colored step corresponds to the characterization color in Figure 72. After every step of the fabrication, the devices are statically characterized. After every step of the fabrication, the devices are statically characterized. The Wolfspeed devices were used for the semi-functional module since they are commercial devices and have reliable performance to understand the fabrication process, compared to the research-level devices from AIST, which are the first of their kind.

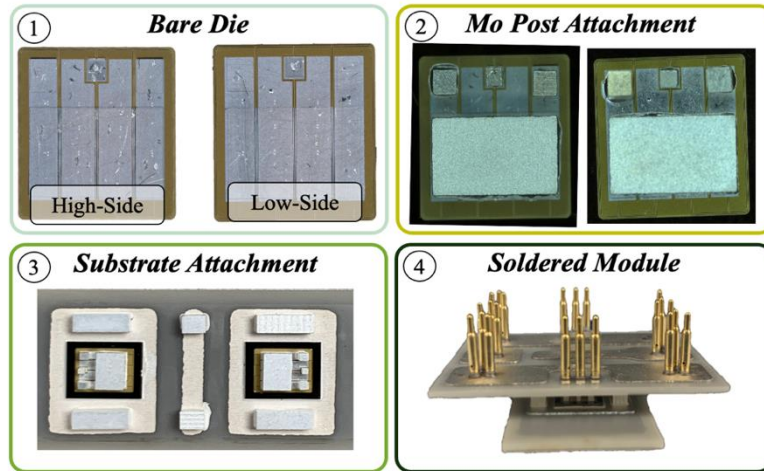


Figure 71: Fabrication steps of the semi-functional two-die module, with the colored boxes corresponding to the characterization curves in Figure 72.

The on-resistance characterization results of each device are shown in Figure 72. It is noted that the bare die measurement is much higher than the packaged devices. This is most likely due to an oxide build-up on the aluminum over time, which can cause the probes to have insufficient contact with the pads and read a higher measurement. While the image in Figure 71 shows the metalized die, the characterization was done before. When the die are metalized, an argon etch removes the oxide barrier before placing the posts, resulting in a lower resistance measurement. This effect can be seen in the significant decrease in resistance after metallization and Mo post attachment.

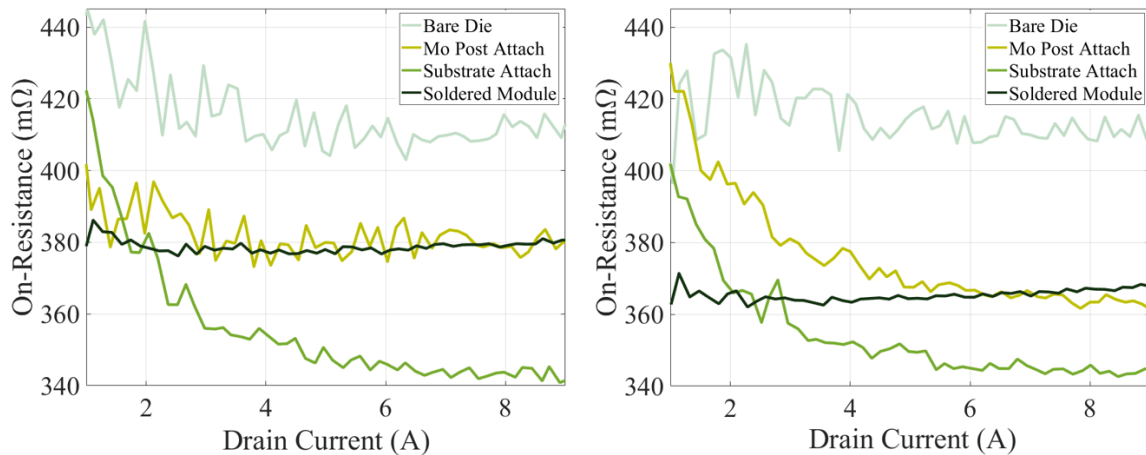


Figure 72: Characterization curves of the bare device, the device with Mo posts attached, the devices + posts attached to the substrate, and the soldered module with spring-pin terminals.

Additionally, the probe station connected to the Keysight B1505A curve tracer has a $30\text{ m}\Omega$ variation across measurements due to the probe sensitivity to the vibrations and setup, which can contribute to some discrepancies in the measurement. The bare device, Mo post attachment, and substrate attachment measurements are taken on the probe station, and the final measurement of the soldered module is connected directly to the Keysight B1505A curve tracer. While the $30\text{ m}\Omega$ variation is present from measurement to measurement, the post-argon-etched device with posts matches the final soldered module measurement. As shown, both devices experienced no degradation in their on-resistance from the packaging process, allowing the process to continue with the research devices from AIST.

5.2.2 Functional Two-Die Module Fabrication and Characterization

Once the fabrication process is verified with the semi-functional module, the process is then conducted on six functional two-die modules. Out of the six attempts, all six were functional. One module utilizes 13 kV SiC MOSFETs from AIST, while the other five utilize 10 kV SiC MOSFETs from AIST. For both devices, the kelvin connections arise from extended source metallization. Additionally, due to limited substrates, two modules have a single, combined top substrate instead of the stacked substrates. Since there was a limited number of 13 kV devices, the rest were reserved for the fabrication of an MCPM instead of more two-die modules. AIST took all initial device measurements on an unknown setup. The final packaged device measurements were taken on the Keysight B1505A curve tracer at the Center for Power Electronics Systems (CPES). The hardware packaging process for the two-die module with AIST devices is shown in Figure 73.

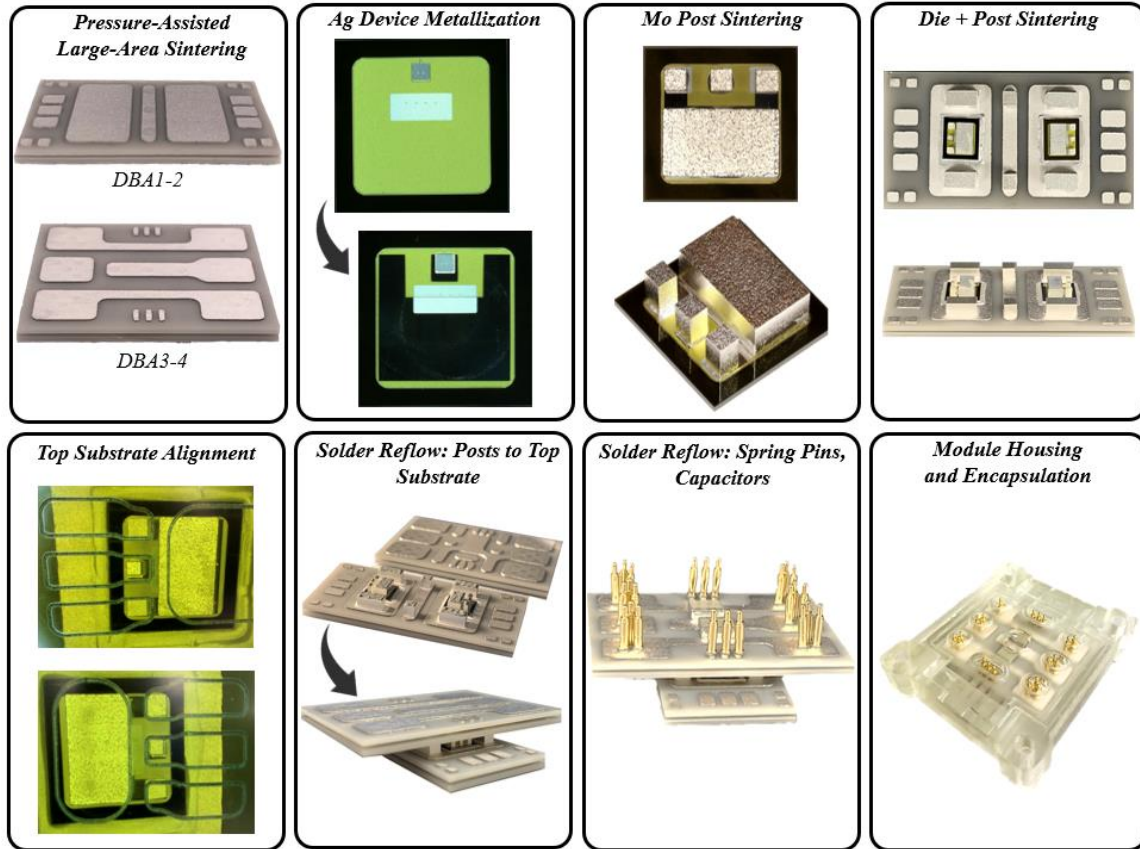


Figure 73: Two-die module fabrication process.

The first two-die module was fabricated (Figure 74) with 13 kV devices and had no refinements utilized. As a result, the kelvin post was not connected, and the overall on-resistance of each device experienced a significant increase, demonstrating the need for refinements. This is concluded from the poor voiding noticed with posts soldered without pressure from Chapter 3. The functional module was still successfully characterized. Figure 75(a) shows the forward characteristics of the packaged low-side device. Figure 75(b) shows the blocking voltage versus leakage current, exhibiting less than 350 nA of drain leakage current up to 10 kV, limited by the curve tracer maximum voltage.

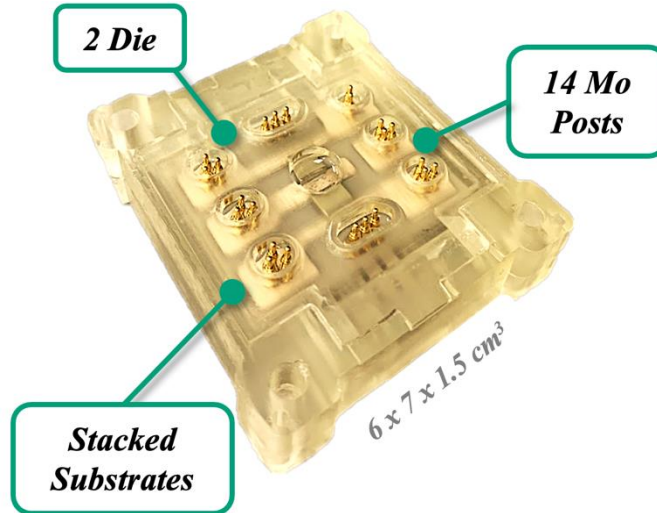


Figure 74: Encapsulated, two-die, 13 kV SiC MOSFET, half-bridge power module with one die per switch position, stacked substrates, and 14 Mo posts.

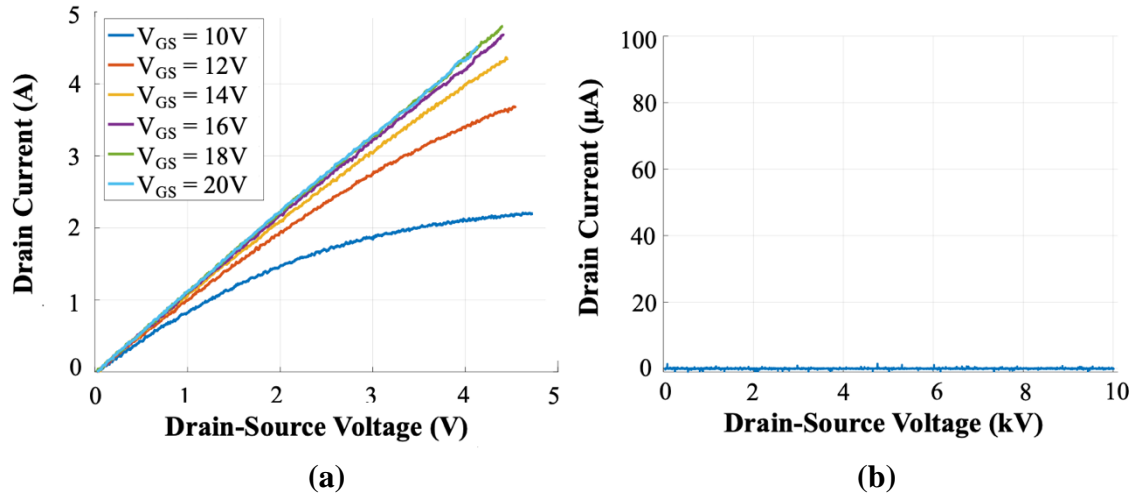


Figure 75: Static characterization results, including (a) the forward characteristics of the packaged low-side device and (b) the breakdown voltage of the packaged low-side device up to 10 kV (limited by the curve tracer).

The following five modules were fabricated using the AIST 10 kV MOSFETs. The same fabrication process is used, except now the refinements are employed. Across all the modules, every post was successfully connected, every substrate sintered with a uniform bondline, only one spring pin was broken, and every device was characterized successfully as fully functional. The de-capsulated modules are pictured in Figure 76, and the

encapsulated module static characterization test conditions are listed in Table 18, with the results detailed in Table 19.

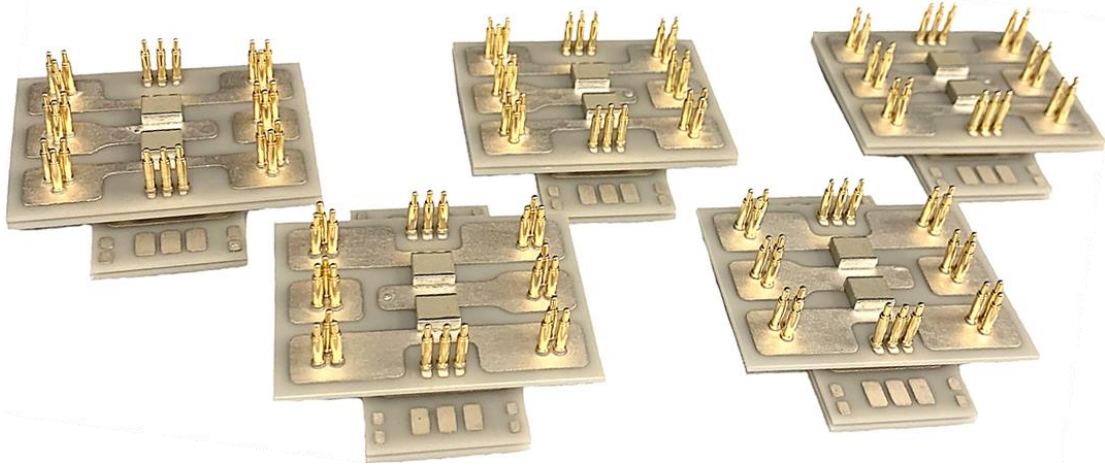


Figure 76: Fabricated 10 kV, AIST SiC half-bridge two-die power modules, decapsulated.

Table 18: Test Conditions for the Static Characterization of the Two-Die Modules.

Measurement	Conditions
$R_{DS,on}$ (m Ω)	$V_{GS} = 20$ V, $I_D = 3$ A
V_{TH} (V)	$V_{DS} = V_{GS}$ V, $I_D = 1$ mA
I_{GSS} (nA)	$V_{DS} = 0$ V, $V_{GS} = 20$ V
I_{DSS} (nA)	$V_{GS} = 0$ V, $V_{DS} = 10$ kV

Table 19: Static Characterization from the Six Two-Die Modules, Detailing the Bare Die and Packaged Die Results.

	SN001							
	High-Side Device				Low-Side Device			
	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} (nA)	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)
AIST Bare Die	685.5	3.38	6.25	9.28	684.8	3.37	5.5	4.7
CPES Packaged Die	1004	3.56	45	< 300	767	3.54	25	< 300
	SN002							
	High-Side Device				Low-Side Device			
	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)
AIST Bare Die	613.8	3.75	7.4	5.6	612.5	3.81	8.7	3.5
CPES Packaged Die	759	3.67	24.2	< 300	766	3.67	28.5	< 300
	SN003							
	High-Side Device				Low-Side Device			
	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)

AIST Bare Die	621.7	3.84	8.1	8	623	3.84	7.8	4.7
CPES Packaged Die	793	3.77	25.9	< 300	761	3.77	21.2	< 300
	SN004							
	High-Side Device				Low-Side Device			
	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)
AIST Bare Die	617.8	3.74	8.1	25.2	618.4	3.91	8.1	11.2
CPES Packaged Die	801	3.66	21.1	< 300	772	3.84	29.8	< 300
	SN005							
	High-Side Device				Low-Side Device			
	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)
AIST Bare Die	611.2	3.9	7.4	5.5	610.6	3.75	8.4	4.8
CPES Packaged Die	748	3.89	22.9	2000*	699	3.69	22.5	1500*
	SN006							
	High-Side Device				Low-Side Device			
	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ (nA)
AIST Bare Die	626.3	3.9	8.4	9.5	627.7	3.78	8.4	4.5
CPES Packaged Die	886	3.8	69.1	2000*	903	3.68	47.5	1000*

**Module built with a single-layer top substrate, limiting
breakdown voltage performance*

It is noted that these research-level devices exhibited basal-plane dislocation, which is known to affect the forward characteristics after repeated use of the body diode, thus impacting the threshold voltage and on-resistance, as shown in Table 19 [117], [118]. This is why the first two-die module was fabricated with an off-the-shelf device from Wolfspeed to rule out the packaging process as detrimental to the device's performance. Also, the measurement setup for the bare devices was unknown and may contribute to the discrepancies between the bare device and packaged device results. Due to the resolution of the Keysight B1505A curve tracer, the leakage drain current under blocking voltage measurement is noisy and not representative of the actual leakage drain current. Thus, only

the range can be noted. A test was run with simply the probes not connected to the module, and the noise was the same, concluding that the drain leakage was much smaller than the measured amount.

Even so, the demonstration of these research-level medium-voltage SiC MOSFETs is accomplished, indicating that the fabrication refinements positively impact the module yield and functionality. The five modules were sent to AIST without further testing at CPES. Thus, the two-die module with 13 kV devices is utilized in the next section for dynamic characterization.

5.2.3 Functional Two-Die Module Dynamic Characterization

Double pulse tests (DPTs) were performed on the low-side device using the DPT setup and driver for a high-voltage power module designed in prior work [69]. The circuit schematic is pictured in Figure 77, and the physical setup is in Figure 78. Isolated power supplies at the input of the gate driver with twisted wires and CM chokes aid in reducing EMI and CM current noise. The 6 kV capacitor bank maintains the applied voltage across the devices and has a multimeter attached to safely monitor the energy storage before approaching the setup. The gate signal transmits through fiber optic cables for signal integrity. It is programmed into the function generator based on the desired current (5 A for the AIST devices) and the voltage applied across the device. Two power supplies connect to the input of the isolated power supplies to power the gate driver and the fiber optic transmitter board. After these tests, the setup has been scaled to 9 kV by improving the voltage rating of the decoupling capacitors, and future DPTs will be done with the higher-rated setup.

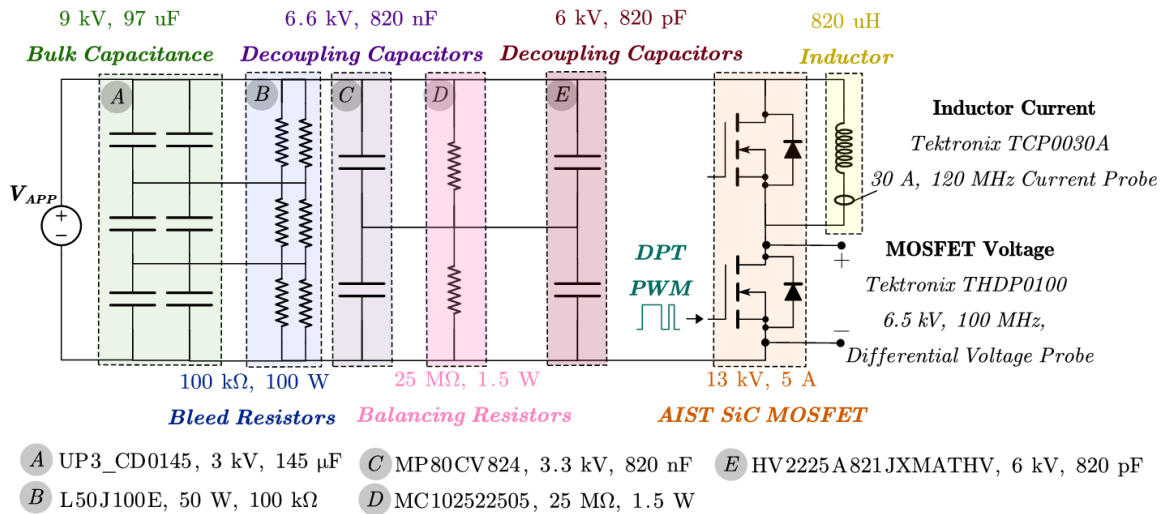


Figure 77: Double-pulse test setup circuit diagram and part information.

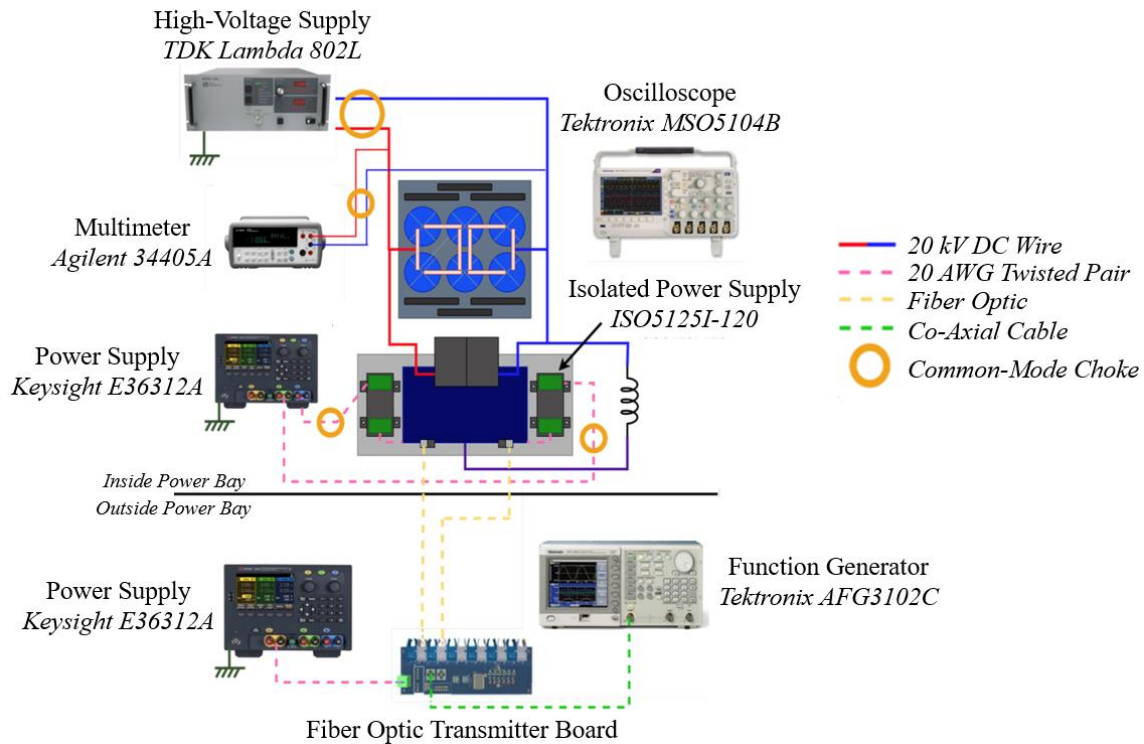


Figure 78: Double-pulse test equipment setup and interface to the gate driver.

Figure 79 shows waveforms during a 2.2 kV, 5 A DPT for one 13 kV module with a single die per switch position. The test was only run to 2.2 kV due to a gating error that turned the device on for an extended time and resulted in an overcurrent failure. Initial testing indicates the successful fabrication of the module. The drain-source voltage overshoot was limited to 3% due to the low parasitic inductance offered by the post-

interconnect module structure. The drain-source voltage rise and fall times are 130 ns and 30 ns, respectively, with a maximum dv/dt of 62 V/ns at 2.2 kV, 5 A, enabled by the low parasitic capacitance and low-resistance bonds in the gate loops. Additionally, the DPT evaluates the devices switching at their maximum current without any bond failures, indicating solid bonds from the fabrication refinements. After successfully fabricating the six two-die modules and dynamic characterization at the devices rated current, there is confidence to move forward and build the full MCPM.

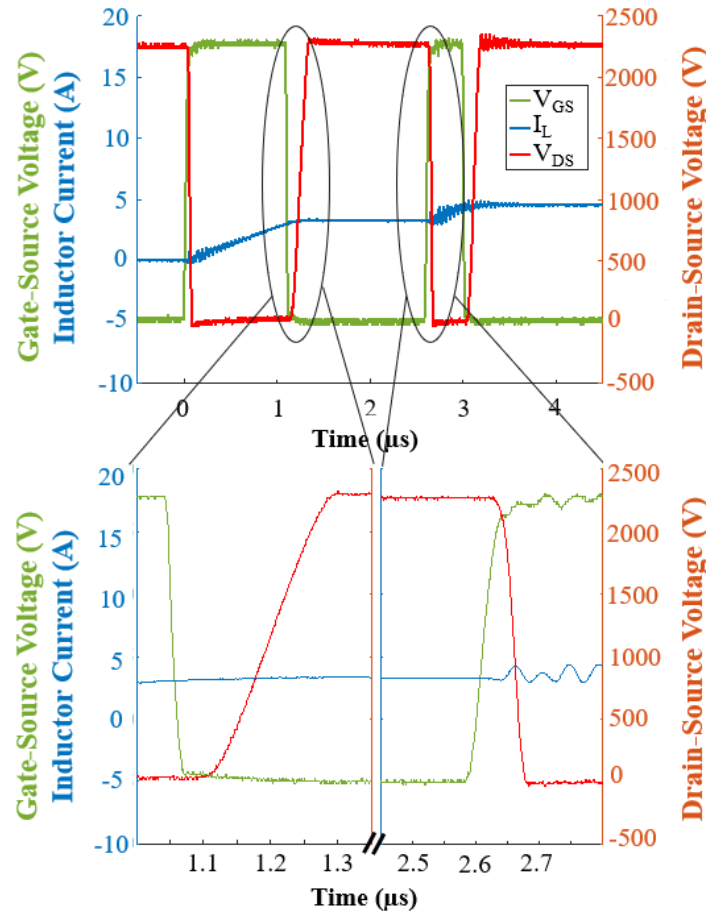


Figure 79: Double pulse test waveform for the 13 kV SiC module at 2.2 kV, 5 A, 100 mΩ gate resistance, including a zoomed-in image of the drain-source voltage rise and fall.

5.3 Multi-Chip Power Module Fabrication and Static Characterization

From the statistical tolerance analysis, it is clear that the fabrication of the MCPM is not trivial. As the number of die in parallel and the number of bondlines increase, more variation is introduced during the fabrication. Using the fabrication refinements and the knowledge of the statistical tolerance analysis, a mechanical MCPM is first fabricated. For the fabrication of the mechanical MCPM, the posts are fixed to the lowest possible mismatch to reduce the maximum possible mismatch, as shown in Figure 62. While the sinter bonds would be the best layer to control, the fabrication process makes that challenging. It would require a complete change in the process, such as stamp-transferring preform instead of dipping the wet bonds. Thus, the posts are a much simpler option to implement to shift the CDF to the left and reduce the maximum mismatch since they have fixed measurements that can be controlled.

It is known that the two-die modules have been successfully fabricated without any missing bond connections using the fabrication refinements, based on the previous section. Thus, the CDF of an MCPM with fixed post heights is compared to the true Monte Carlo, randomly sampled two-die module CDF to compare the correlation between modules that have been functionally fabricated with a particular height mismatch and understand if fixing the post heights is close to this CDF.

Using the available posts, the smallest maximum mismatch that can be achieved is 15 μm . This is added to the Monte Carlo, and the CDF for this case of fixed posts is generated. From Figure 80, it is shown that this does not quite match the two-die module Monte Carlo as well as fixing the dipped bonds for an MCPM does, but it comes much closer than the true Monte Carlo of the MCPM and could indicate that this is still an

effective method of reducing the mismatch. However, it is important to note that these CDFs do not indicate yield, and engineering knowledge is being used to determine if the maximum height mismatch may only be small enough to ensure all posts are connected. Both the mechanical and functional MCPMs utilize this fixed-post method during fabrication to analyze the impact of the statistical tolerance analysis on the module.

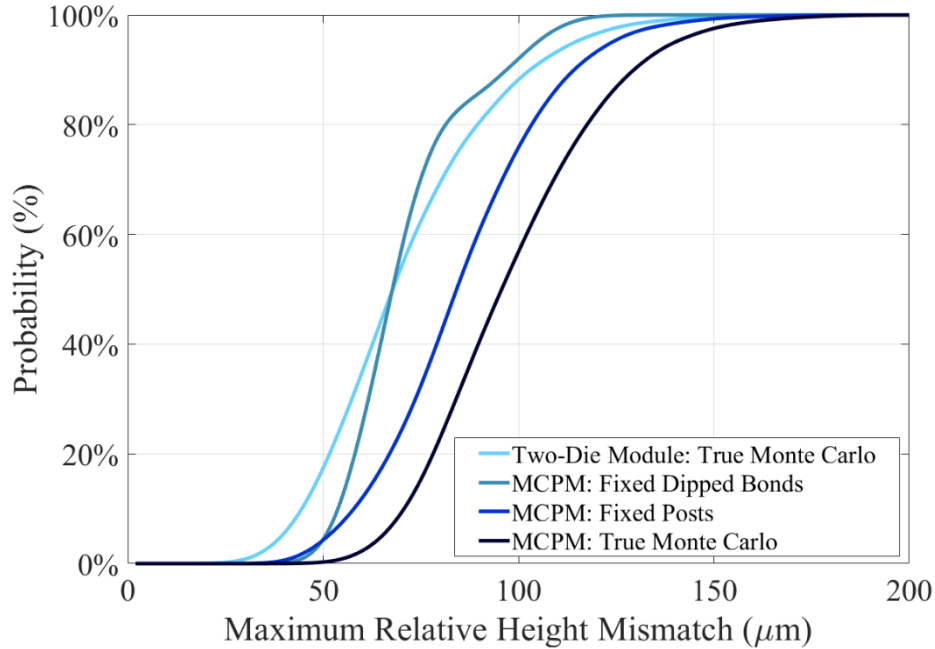


Figure 80: CDFs of the Monte Carlo two-die module, fixed dipped posts for the MCPM, fixed posts for the MCPM, and Monte Carlo full module.

5.3.1 Mechanical Multi-Chip Power Module Fabrication

The mechanical MCPM (Figure 81) is fabricated by fixing post heights to a maximum mismatch of 15 μm . The module fabrication process utilizes all fabrication refinements: large-area, pressure-assisted sintering for the uniform transfer of silver preform to substrates, Mo post interconnect attachment utilizing a die bonder to reduce tilt and control bondlines, screen-printed sinter-paste for die attach, Mo post interconnect alignment checks to prevent module failure and missed connections, and pressure-assisted soldering to reduce voiding content and prevent any tilt from causing open connections.

The substrates are chosen from the warpage analysis section in Chapter 2, with DBA 1-DBA 2 having a warpage of 12.8 μm and DBA 3-DBA 4 having a warpage of 43.5 μm . The rest of the process is left random to best emulate the Monte Carlo simulation results.

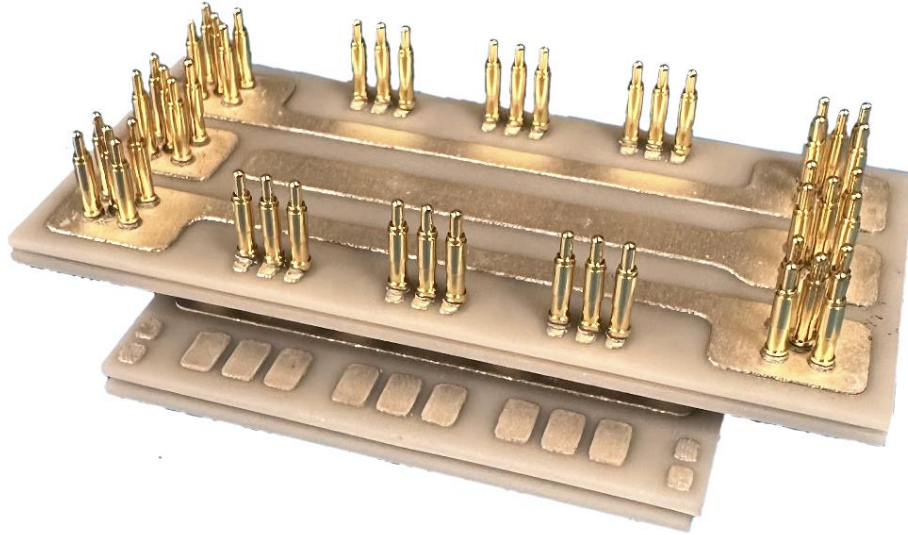


Figure 81: Mechanical MCPM successfully fabricated using the refinements from Chapter 2 and Chapter 3, as well as fixed posts from the Chapter 4 statistical tolerance analysis.

To check for a successful connection, a multimeter is used to probe from the post connected to the die to the metal pad with the solder bond in between since there is no via in these mechanical substrates to connect the metal pads through the ceramic. Additionally, it was not possible to fit all four probes for a 4-wire measurement of the resistance of the bond, so just a shorted connection was verified. Every post measured a short to its respective pad. From this result, fixing the posts was enough to minimize the maximum height mismatch to achieve all bonded connections. This one case is not enough to represent the population that always fixing the posts will improve the yield. Fixing the posts still helps reduce the maximum gap height mismatch, which may be enough to have a successful fabrication process for this module. This gives enough validation to proceed

with the fabrication of the functional module and again test if fixing the posts is enough to reduce the maximum warpage and connect the posts to the top substrate.

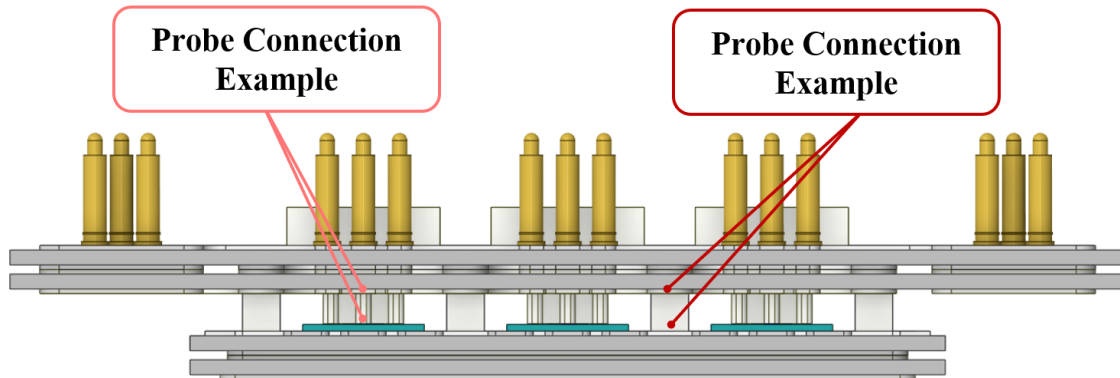


Figure 82: Probe-tip locations to measure the shorted connection from the post to the stop pad through the solder bond after reflow.

5.3.2 Functional Multi-Chip Module Fabrication

The functional MCPM is fabricated using 13 kV, 5 A, SiC MOSFETs from AIST. From this one attempt, the module was fully functional. Their parameters are referenced in Table 20. Per switch position, the on-resistances of the devices are within 6.16% and 0.72% for the high-side and low-side, respectively. The threshold voltages are within 2.31% and 0.59% for the high-side and low-side, respectively. The hardware fabrication of the functional MCPM is shown step by step in Figure 83. While these measurements were taken on an unknown setup at AIST, two die were measured at CPES in order to compare the bare die measurements. From the results, there was a 70-80 m Ω measurement difference between the AIST results and the CPES curve tracer, and this will be noted when comparing the final CPES measurements of the completed package to the expected AIST measurements of the devices.

Table 20: AIST 13 kV Functional Bare Die Characterization Data

Die Number	Switch Position	$R_{DS,on}$ (m Ω)	V_{TH} (V)	I_{GSS} (nA)	I_{DSS} @ 10 kV (nA)
5	High-Side	672.3	3.40	6.50	5.31
6	High-Side	667.1	3.45	5.15	14.40
12	High-Side	713.7	3.37	6.78	4.21
8	Low-Side	719.7	3.38	13.03	4.21
9	Low-Side	727.5	3.37	11.09	3.93
11	Low-Side	724.9	3.39	6.84	4.43

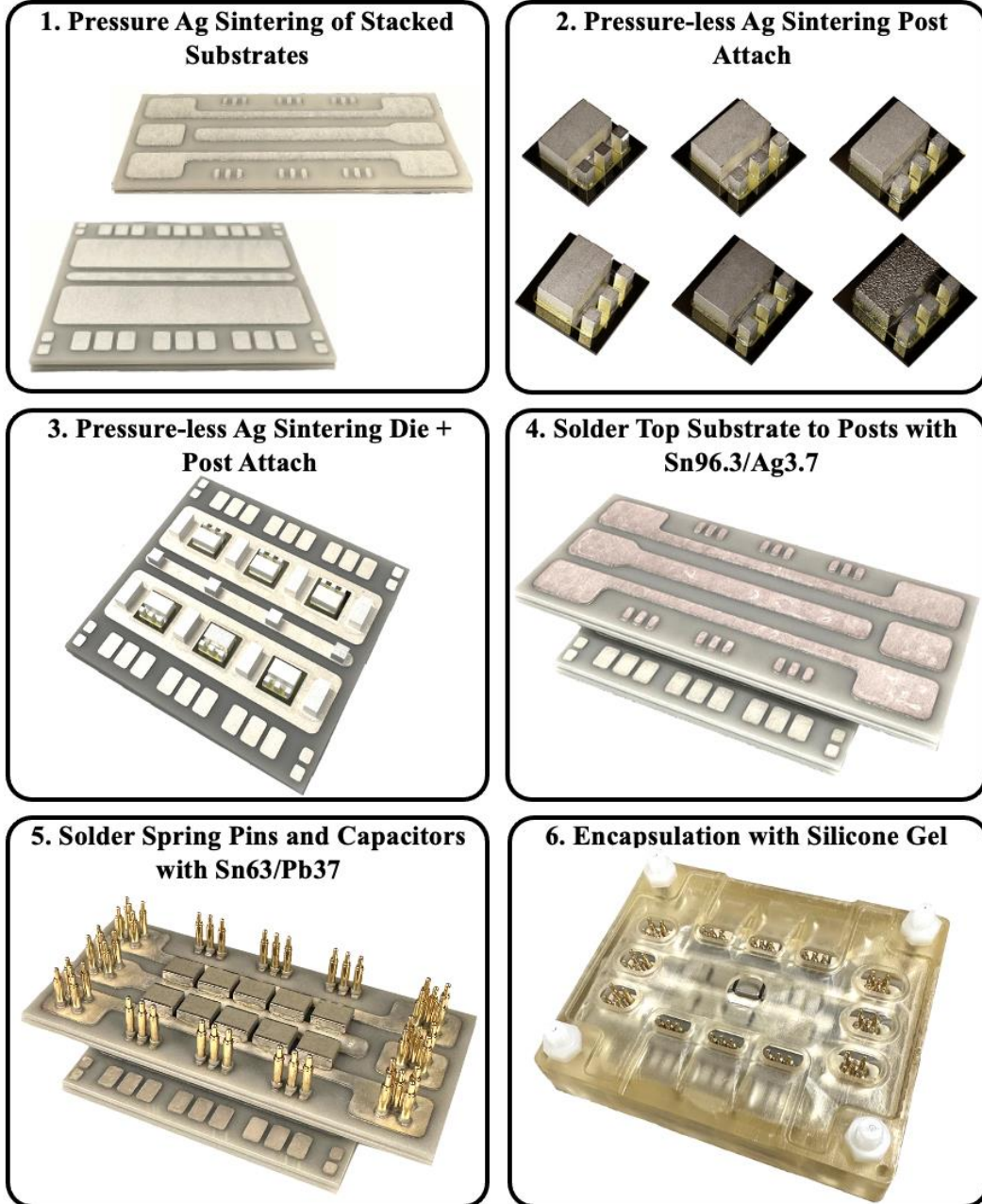


Figure 83: Hardware fabrication steps for the functional, 13 kV SiC MOSFET MCPM.

The electrical connectivity of each post is verified by measuring the resistance from each kelvin source to the power source and probing the connection of the gate post to the top gate pad on DBA 4 before the spring pins are attached. The gate cannot be verified with a resistance measurement since it is not feasible to do a four-wire measurement in the 2 mm opening between the substrates, and there are no additional pads to measure a complete resistance loop through the gate. The resistance measurements are representative of the same path in Figure 41 and are noted in Table 21. While this resistance seems high, the majority of it arises from the metallization. Once subtracting the metallization, the resistance contributed from the solder bonds can be found in Table 22. The maximum height mismatch is reduced enough to ensure every post is electrically connected by fixing the height. Once verified, the spring pins and capacitors are soldered to the top DBA, and the module is ready for the first static characterization.

Table 21: Kelvin-Source to Power-Source Resistance Measurements to Verify all Connected Bonds.

	Average Kelvin to Power Source Resistance (mΩ)	Resistance Standard Deviation (mΩ)
High-Side	59.25	6.18
Low-Side	66.93	6.19

Table 22: Kelvin-Source to Power Source Resistance Measurements of Only Solder Bonds.

	Average Kelvin to Power Source Resistance (mΩ)	Resistance Standard Deviation (mΩ)
High-Side	4.16	2.92
Low-Side	4.13	2.82

5.3.3 Static Characterization of the Multi-Chip Power Module

The module is connected to the same Keysight B1505A curve tracer used to characterize the two-die modules. The forward characteristics for both the high-side and low-side switch positions are shown in Figure 84(a) and Figure 84(b), respectively, up to

the rated current of 15 A. The blocking voltage versus leakage current for the high-side and low-side switch positions are shown in Figure 85(a) and Figure 85(b), respectively, exhibiting no leakage up to 10 kV, limited by the curve tracer maximum voltage. The on-state resistances for the equivalent high-side and low-side devices are shown in Figure 86, respectively. The on-resistance measured at CPES is 66 m Ω higher for the high-side and 71 m Ω higher for the low-side than the AIST measurements, which falls in the measurement tolerance range of the bare devices as previously noted, indicating no actual degradation in the on-resistance.

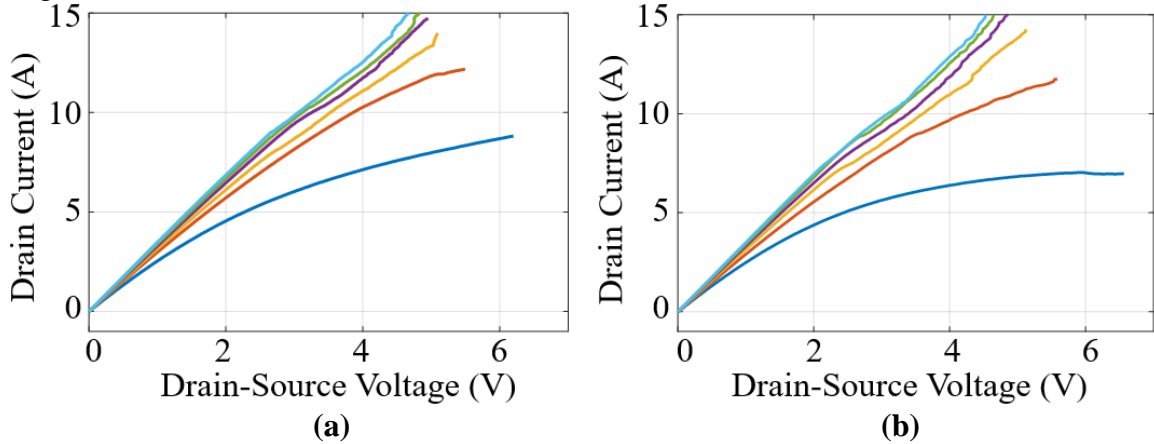


Figure 84: MCPM (a) high-side and (b) low-side forward characteristics up to rated current (15 A).

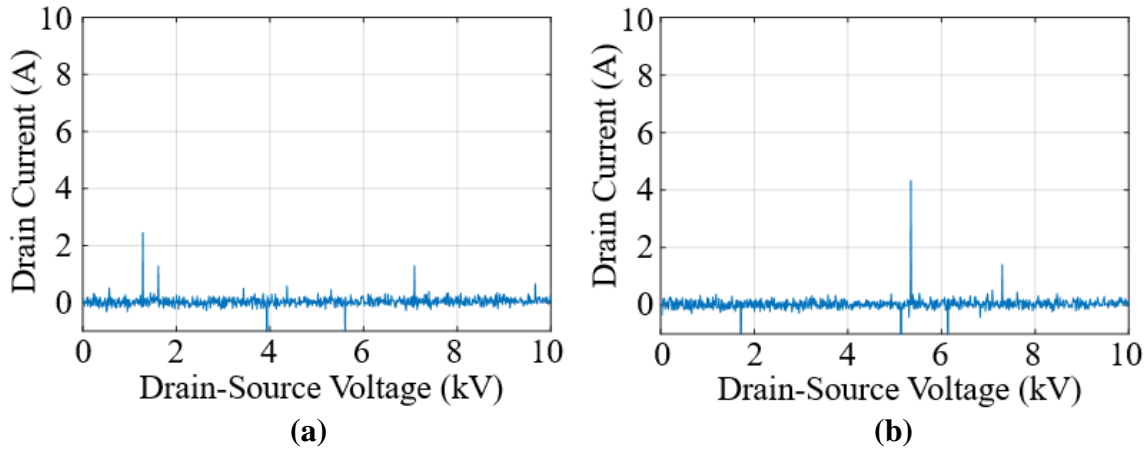


Figure 85: MCPM (a) high-side and (b) low-side breakdown voltage versus leakage current, up to 10 kV (limited by curve tracer).

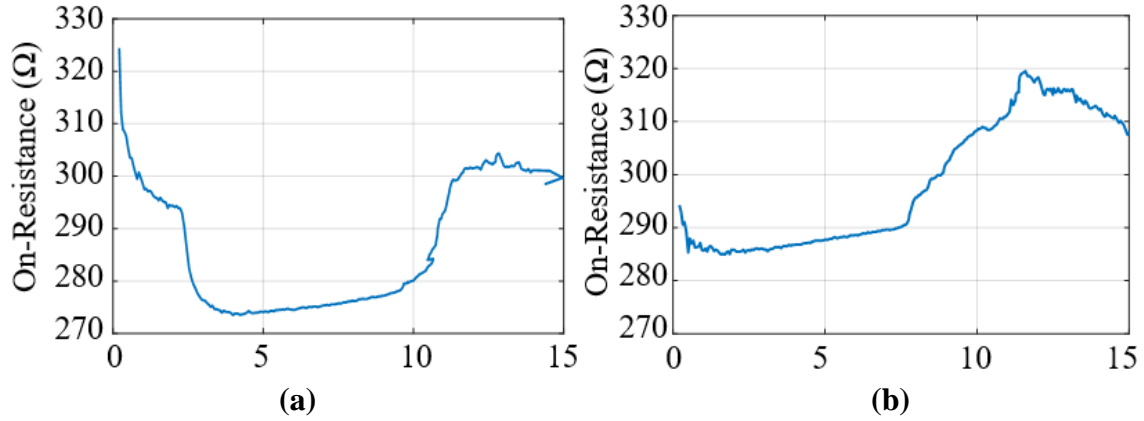


Figure 86: MCPM (a) high-side and (b) low-side on-resistance up to rated current (15 A).

This is the first successfully fabricated and characterized MCPM using this packaging scheme, and to the best of the author’s knowledge, the only 13 kV wirebond-less MCPM successfully fabricated. The characterization of the module allows for verification that the devices are functional after the packaging process. This functional MCPM demonstrates that the fabrication refinements are effective for electrical functionality and that the statistical tolerance analysis effectively reduces the maximum-height mismatch.

5.4 Summary

In summary, the module fabrication and characterization are used to understand the electrical impacts of the fabrication refinements. A semi-functional, two-die module is fabricated to demonstrate that the packaging process does not impact the bare device measurement using off-the-shelf MOSFETs from Wolfspeed. Six out of six two-die modules are then fabricated and successfully statically characterized using the refinements detailed in Chapters 2 and 3 for research-level devices from AIST. One module is dynamically characterized at its maximum current with no bond failures and switching speeds of 63 V/ns.

Once the two-die modules are fabricated, it gives the motivation to demonstrate the fabrication refinements on the MCPM. The statistical tolerance analysis is also employed to analyze the impact of fixing the post heights to reduce the maximum height mismatch. Using the statistics and the fabrication refinements, both a mechanical module and a functional module are successfully fabricated for their first attempts, indicating that the statistical tolerance analysis identified a potential method to reduce the maximum height mismatch enough to fabricate functional modules. This is the first successfully fabricated MCPM and the first 13 kV power module fabricated of its kind. It can be concluded that the refinements developed in this work are effective, and the statistical tolerance analysis was insightful to successful fabrication.

Chapter 6 Summary, Conclusions, and Future Work

6.1 Summary and Conclusions

This work refined and improved advanced packaging techniques required for sandwich-structure MCPMs. These techniques are essential to improve the electrical functionality of MCPMs and increase yield. A statistical tolerance analysis also helped to understand the inherent impact of stacked, machined components on the maximum mismatch across this sandwich-structure module. The team demonstrated the refinements on mechanical and functional two-die modules (two die per module, one die per switch position) and the MCPM (six die per module, three die per switch position). Figure 87 addresses the concerns with the packaging of these MCPMs.

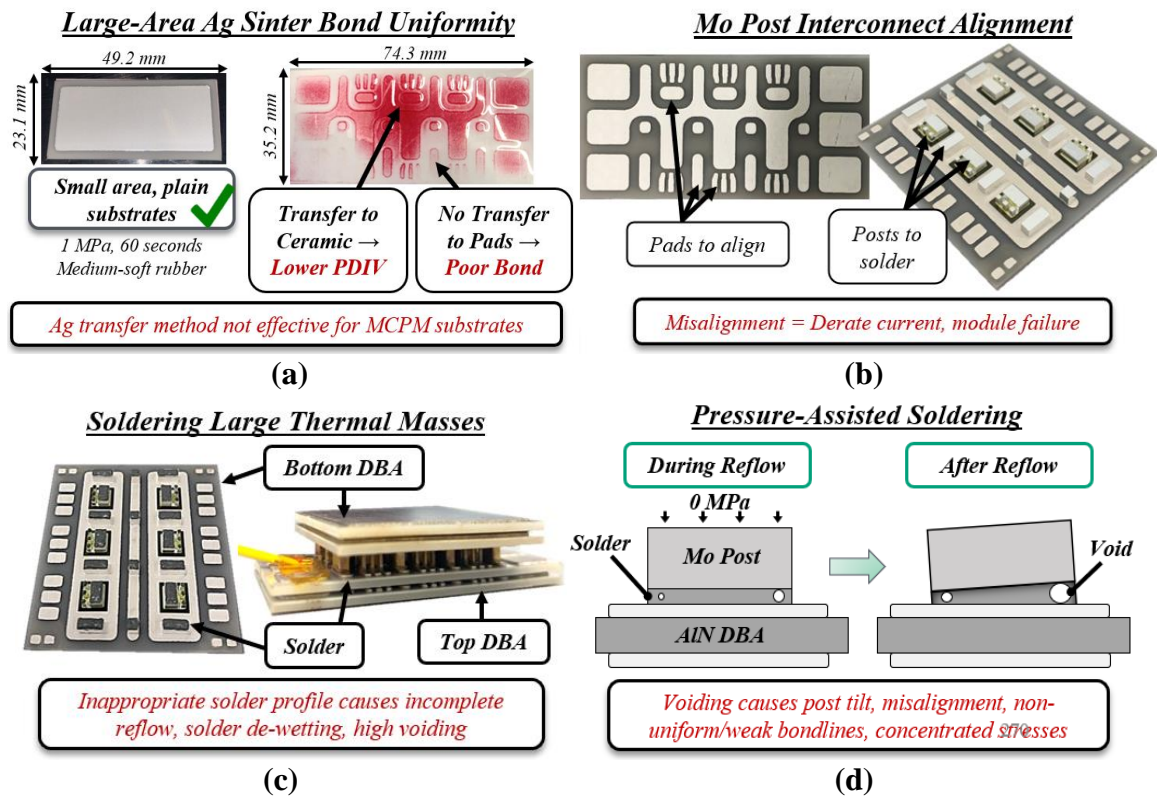
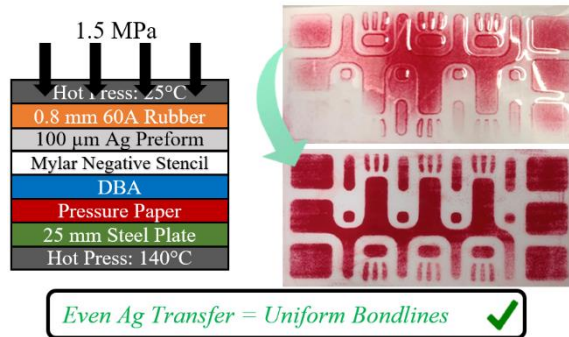


Figure 87: Fabrication concerns for advanced packaging techniques in MCPMs, including (a) large-area silver sintering bond uniformity, (b) Mo post interconnect alignment, (c) soldering large thermal masses, and (d) pressure-assisted soldering.

Among the refinements, the first involved nano-silver sintering. Large-area patterned substrates have been successfully sintered with uniform bond lines by refining the stamp transfer process. This was crucial to the functionality of the medium-voltage module to not only ensure electrical connections between pads but the stacking of substrates improves the PDIV of the module, meeting the insulation requirements of the devices. The accurate placement of Mo posts to the die and substrate was refined by reducing the variation in the rigid sinter bond. Since any defects during the application of sinter paste remain, it is vital to ensure accurate, repeatable bonds. By repurposing a die bonder, the tilt of the post can be reduced, as well as controlling the bondline to avoid any shorts or paste oozing onto the field grading of the device.

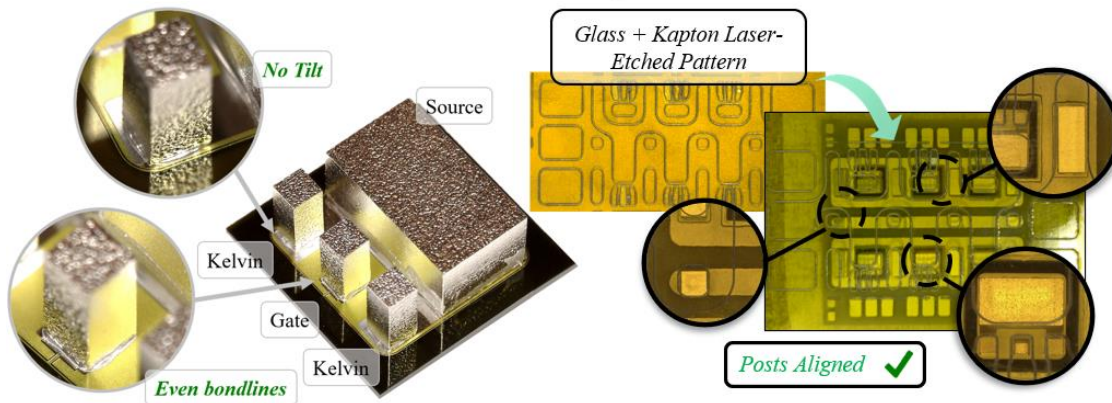
The subsequent refinements involved the soldering of the module. Once attached, the post interconnect alignment was verified before proceeding with the sintering and soldering of the module by overlaying a glass slide with the module and examining the connections under a microscope. This way, shorts can be avoided. Next, a proper reflow profile for the large thermal mass of an MCPM is verified. A mechanical module and thermocouple at the location of the solder bond ensure proper soaking time and time above liquids to avoid de-wetting of the solder and high voiding contents. The module is then soldered under pressure to reduce post tilt, control bondline uniformity, and reduce voiding content. The proposed solution of soldering under pressure successfully improves the bonds in the signal and power loops, increasing the bond strength by 10.5%, reducing post-height variation by 97.7%, and reducing the bond line resistance by 99.8% compared to a module soldered without pressure. A summary of the fabrication refinements is shown in Figure 88.

Large-Area Ag Sinter Bond Uniformity



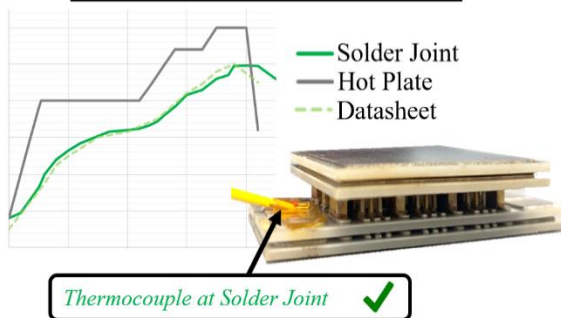
(a)

Mo Post Interconnect Alignment



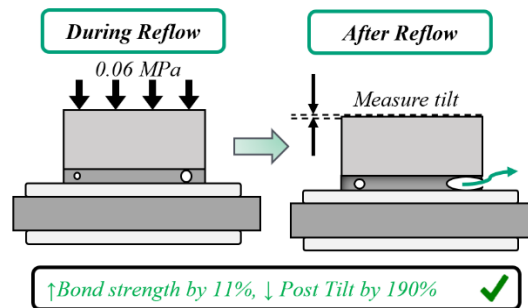
(b)

Soldering Large Thermal Masses



(c)

Pressure-Assisted Soldering



(d)

Figure 88: Fabrication refinements for the fabrication concerns in Figure 87 regarding the (a) large-area silver sintering bond uniformity, (b) Mo post interconnect alignment, (c) soldering large thermal masses, and (d) pressure-assisted soldering to improve the yield for MCPMs.

A two-die semi-functional module is fabricated to verify the impact of the packaging process on the bare device, demonstrating no degradation. Next, the research-level MOSFETs from AIST are populated in 6 two-die modules. The static characterization

of all modules shows successful operation, with healthy forward voltages and every module blocking up to 10 kV with a maximum drain-leakage current of only 1 mA. A 2.2 kV, 5 A double-pulse test verifies the bond quality with only 3% voltage overshoot while switching at the device's maximum current, achieving switching speeds of 63 V/ns with no bond failures at maximum current while also indicating low parasitic capacitance and resistance in the signal loops.

Next, a mechanical MCPM is fabricated to better understand the statistical tolerance analysis impacts on the fabrication. While it would be best to control the bondlines and reduce the dipped bond variation, it is chosen to reduce the maximum height mismatch of the post. This is easier to control since it is not dependent on measurements that can only be acquired after sintering. The posts have only the manufacturing tolerances which can be measured. From the mechanical fabrication, every post is connected during the final soldering step, giving the motivation to apply the fixed-post method for the functional module. The functional MCPM was fabricated using the statistical tolerance analysis and fabrication refinements, all detailed above. From the successful static characterization, the entire process has been validated as beneficial to improving the functionality and yield of these MCPMs. This is the first of this module to be successfully fabricated and characterized. The updated fabrication process with the refined steps from this work is detailed in Figure 89.

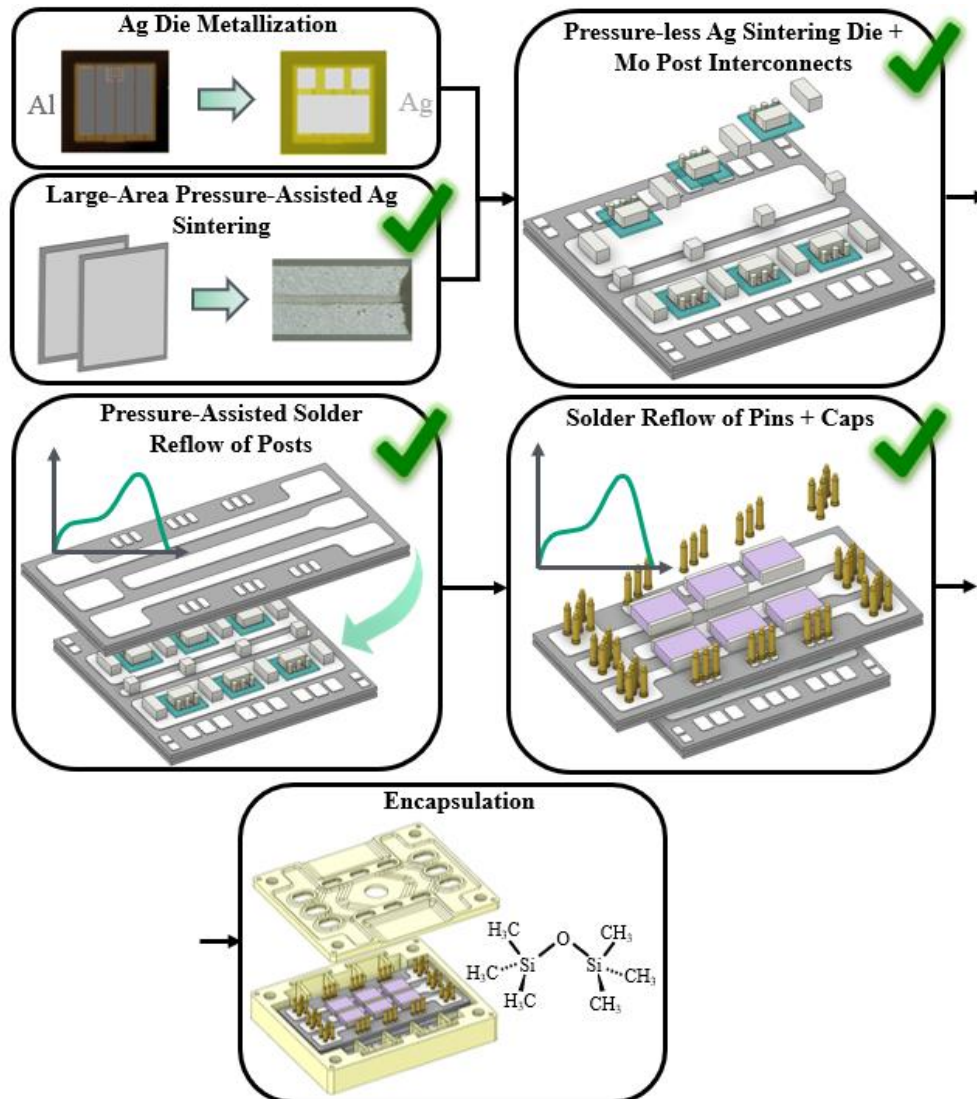


Figure 89: Fabrication process with refined steps from this work noted with a green checkmark.

6.2 Future Work

To verify the impact of the new fabrication processes on the module's reliability, thermal cycling and power cycling tests should be done to identify which processes are the least reliable in the module fabrication. This will help identify which refinements need to be re-evaluated for future modules.

To better understand the substrate warpage in Chapter 2, the simulations should be re-run with the obtained stress-strain curve of the Aluminum from DOWA METALTECH

based on the manufacturing process the substrates undergo, changing the zero-stress state. Once obtained, the substrates should also be simulated with different concavity pairings to verify what is seen in the experiments. While the substrates have additional pads for the gate and kelvin connections to be potentially wirebonded, those pads can be removed, and the reduction of substrate size can then be simulated to understand the impact on the warpage while also improving the power density. Additionally, more substrates should be fabricated to understand the population warping better. That way, the one planar substrate from DBA 1-DBA 2 can be deemed a percentage of the population or simply an outlier.

For the pressure-assisted soldering experiment, more posts should be soldered with and without pressure and compared using CSAM imaging instead of shear testing. Shear testing is a destructive test, which can lose bond fragments and make it difficult to understand the bond failure mechanism (cohesive or adhesive) or the size of the voids. Additionally, thermal cycling tests of the two groups can help verify the experiment's validity and provide insight into the improvement of reliability due to the void reduction. Different experiments can also be done with smaller pressure to better understand the impact on the void reduction, post-tilt, and shear strengths.

The statistical tolerance analysis in itself can suggest a plethora of future work. While the fabrication of the modules utilized fixing of the post heights, it is noted that the dipped bonds provide the most variation and should be the target component to try and re-evaluate. This can be done by instead using silver preform for the bondline. The preform has a controlled thickness, and a stamp-transfer methodology can be developed to transfer the preform to the posts, then sinter the posts to the die. It can be similar to the large-area sintering process of the substrates, but the transfer time can be significantly reduced since

the post sizes are much smaller. This will also reduce the sintering time of a single die with posts from 2 hours to 90 seconds while providing the benefits of silver preform over silver paste for bond reliability. The challenges of this process involve the small pads of the SiC devices. If there is misalignment during the pressure sintering, it cannot be undone, whereas a dipped post with sinter paste can be adjusted after placement. By fixing these bonds, the CDF can shift to the left and reduce the maximum height mismatch, which makes it very close to the two-die module, which historically has been successfully fabricated.

Additionally, to further understand the statistical tolerance analysis of the maximum height mismatch, a distribution of modules can be created to understand the impact of what mismatch contributes to what yield (i.e., all the posts connected). This would require 32 modules to be fabricated, which can be challenging and time-consuming given the limited materials. However, this analysis would provide a great understanding of which components contribute the most to the maximum mismatch and, by controlling them, understand the yield of the module. From this analysis, the near-perfect fabrication of functional MCPMs could be statistically and realistically possible.

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