

Chapter Four

Optimization of Multiphase VRMs

Multiphase technology has been successfully used for today's VRM designs. However, the remaining tradeoff involves selecting the appropriate number of channels, which is still an empirical trial-and-error process. This chapter proposes a methodology for determining the right number of channels for the optimal design of multiphase VRMs.

There are two constraints corresponding to the transient and efficiency requirements. Four design variables need to be traded off, including the channel number, switching frequency, control bandwidth and output inductance. However, the control bandwidth is eliminated as an independent variable. The selection of the objective function is the preference of individual manufacturers or designers. Minimized weighted volume and cost could be the objective function for most of today's multiphase VRMs.

The optimization problem is illustrated by a series of surfaces in a three-dimensional space, with the objective function as the vertical axis, the switching frequency and the output inductance as the two horizontal axes, and the channel number as the parameter. The proposed optimization method first looks for the lowest points of these surfaces, which represent the optimal designs for given channel numbers. For most of today's multiphase designs, these lowest points correspond to the design of the minimum

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efficiency and the critical inductance. Connecting these lowest points together forms a curve, and the optimization solution is located at the valley point of that curve.

Two optimization examples are given using typical VRM 9.0 designs for the latest Pentium 4® processors in order to demonstrate the optimization procedure. The first example is simple; its objective function is to minimize the number of output capacitors. The second example is more complex and realistic; its objective function is to minimize the cost of multiphase VRMs.

Finally, the more generalized formulation of the optimization is discussed. Its objective function is to minimize the weighted volume and cost of multiphase VRMs.

4.1. INTRODUCTION

The topology of a multiphase VRM is shown in Figure 4.1, using a buck converter as an example. It consists of N_C identical converters with interconnected input and output. The duty cycles of adjacent channels have a phase shift of $360/N_C$ degree, where N_C is the total number of channels.

Significant efforts of past years have attempted to analyze and design VRMs. The main focus was to optimize the output filter, power stage and controller characteristics in order to keep the output voltage within the tight dynamical tolerance requirements.

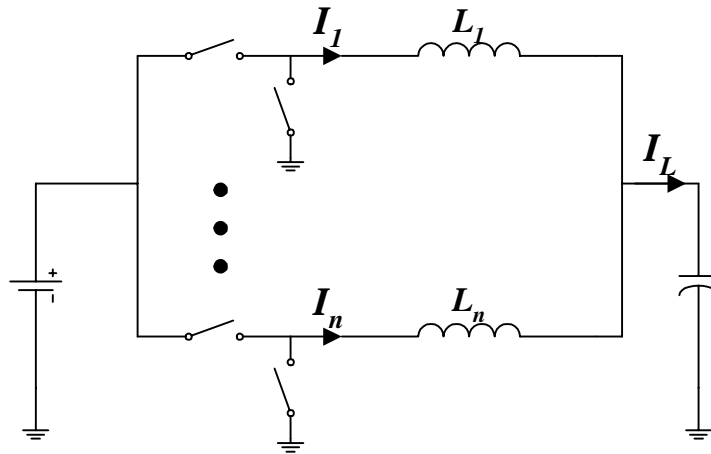


Figure 4.1. Topology of the multiphase VRM.

Currently, selecting the number of channels is still an empirical tradeoff, based on trial and error. Table 4.1 lists some industrial designs based on the same VRM 9.0 specifications. The selection of channel number is quite different. The minimum phase is two, and the maximum is ten. Most use three or four phases. Obviously, all are able to meet the design requirements, but their volumes and costs vary widely. With all the hardware available, it is easy to judge which design is the best, based on certain criteria. However, building hardware for every possible selection of the channel number is very time-consuming and expensive. It is important to determine how many channels are really necessary as early as possible in the design process. So far, no effort has been made to address this issue and the answer is unclear.

The purpose of this work is to develop a methodology for determining the right number of channels for specific design targets.

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Table 4.1. Industrial designs choose quite different numbers of channels for the same VRM 9.0 specification.

	Channel Number	Switching Freq. (kHz)	Inductance Per Channel (nH)	Output Bulk Capacitor
ADI	2	200	600	8x1200uF (OSCON)
Intersil	3	200	850	6x1000uF (OSCON)
On-Semi	3	250	500	14x1200uF (Aluminum)
Semtech	4	250	600	6x820uF (OSCON)
Voltera	10	1000(?)	200	20~40x22uF(Ceramic)

4.2. OPTIMIZATION PROBLEM FORMULATION

This study considers general multiphase VRMs with the following design parameters: channel number (N_C), switching frequency (F_S), control bandwidth (F_C), and output inductance (L_O). Their typical design specifications are listed as follows: input voltage (V_{IN}), output voltage (V_O), maximum load current (I_O), maximum load step change (ΔI_O), load slew rate (SR_O), minimum efficiency (η_{MIN}), and maximum transient voltage deviation (ΔV_{OMAX}).

Two fundamental constraints exist for VRM optimizations: the transient constraint and the efficiency constraint.

In order to meet transient requirements, the voltage deviation during load transients must be less than the specified values (ΔV_{OMAX}). With available output capacitors (ESR,

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ESL, C_o), the transient voltage is mainly determined by the channel number (N_C), switching frequency (F_S), control bandwidth (F_C), and output inductance (L_O). Therefore, the transient constraint for multiphase VRM optimization can be formulated as follows:

$$\Delta V_o(N_C, F_S, F_C, L_O) \leq \Delta V_{O_{MAX}}. \quad (4.1)$$

Because of the limited space available for VRMs around microprocessors, the efficiency of multiphase VRMs must be higher than the specified value, η_{MIN} , in order to keep the temperature increase within thermal limits. The major power losses in multiphase VRMs come from semiconductor devices and magnetic components. With available components, the efficiency of multiphase VRMs is mainly determined by the channel number (N_C), switching frequency (F_S), and output inductance (L_O). Consequently, the efficiency constraint can be formulated as follows:

$$\eta(N_C, F_S, L_O) \geq \eta_{MIN}. \quad (4.2)$$

As shown in Equations 4.1 and 4.2, the constraints are the functions of the channel number (N_C), switching frequency (F_S), control bandwidth (F_C), and output inductance (L_O). With the satisfaction of the preceding constraints, the tradeoff among these design variables can offer the optimal design.

The selection of the objective function is the preference of individual manufacturers or designers. The objective function is the function of the channel number (N_C), switching frequency (F_S), control bandwidth (F_C), and output inductance (L_O), and can be represented as follows:

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$$F_o = F_o(N_c, F_s, F_c, L_o). \quad (4.3)$$

Generally, small volume and low cost are the two major considerations for VRM designs. The importance of volume and cost is dependent on the preferences of individual manufacturers or designers, and can be modeled by weighting factors. A good example of the objective function for the optimization is to minimize the weighted volume and cost of VRMs.

In summary, the optimization problem in this study can be described as follows. For given specifications and available components, with the satisfactions of the transient and efficiency constraints formulated in Equations 4.1 and 4.2, the optimal solution can be found as a result of an appropriate tradeoff among the following design variables: the channel number (N_c), switching frequency (F_s), control bandwidth (F_c), and output inductance (L_o). An example of this type of optimization is minimizing the weighted volume and cost of multiphase VRMs, as formulated in Equation 4.3.

4.3. OPTIMIZATION METHOD AND GENERAL PROCEDURE

As formulated in Equation 4.3, four design variables need to be traded off in order to minimize the weighted volume and cost of multiphase VRMs; they are the channel number (N_c), switching frequency (F_s), control bandwidth (F_c), and output inductance (L_o).

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However, the control bandwidth (F_C) can be treated as a dependent variable because it is relevant to the switching frequency (F_S). Keeping other design variables constant, the increase in the control bandwidth (F_C) improves the transient responses, which can reduce the size and cost of output capacitors. The control bandwidth needs to be pushed as high as possible in order to reduce the size and cost of multiphase VRMs. Generally, the highest control bandwidth is limited by the switching frequency. In order to attain sufficient phase margins to ensure system stability, the control bandwidth cannot be pushed beyond half of the switching frequency. Typical control bandwidths are designed at a fraction of the switching frequency, and can be expressed as follows:

$$F_C = k \cdot F_S, \quad (4.4)$$

where k is a constant that is less than $\frac{1}{2}$ and is determined by manufacturers or designers.

Based on the preceding discussion, only three independent variables exist: channel number (N_C), switching frequency (F_S), and output inductance (L_O).

The method and general procedure used for the optimization of multiphase VRMs are explained in the following discussions. Because there are three independent design variables involved in the optimization, it is necessary to simplify the optimization process by assuming that one variable is actually a constant. The two remaining design variables are then traded off and the optimization solution is found for the constant variable. Repeating this procedure for a range of values for the constant variable, the optimization solutions can be found for each “constant” variable. Next, the objective functions that

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correspond to the optimization solutions for the range of constant variables can be compared; the minimum objective function is found, and the final optimization solution is obtained.

Figure 4.2 illustrates the optimization method. The two horizontal axes represent the output inductance (L_O) and the switching frequency (F_S). Here, the output inductance (L_O) is normalized to the channel number, which equals the output inductance in the individual channels divided by the channel number. The vertical axis represents the objective function (F_O). For a given channel number (N_{C1}), a surface that represents the objective function is formed in this three-dimensional space. Every selection of the channel number has such a three-dimensional surface. For a given channel number (N_{C1}), the optimization area is limited by several factors, and can be illustrated by the blue and pink curves, as shown in Figure 4.2.

The blue curve, as illustrated in Figure 4.2(a), represents the critical inductance, which is a function of the switching frequency. As discussed in Chapter 1, the critical inductance is the largest inductance that gives the fastest transient responses. Any design that chooses an output inductance (L_O) that is less than the critical inductance value increases transient responses but decreases efficiency. Therefore, for optimal designs the output inductance should be no less than the critical inductance.

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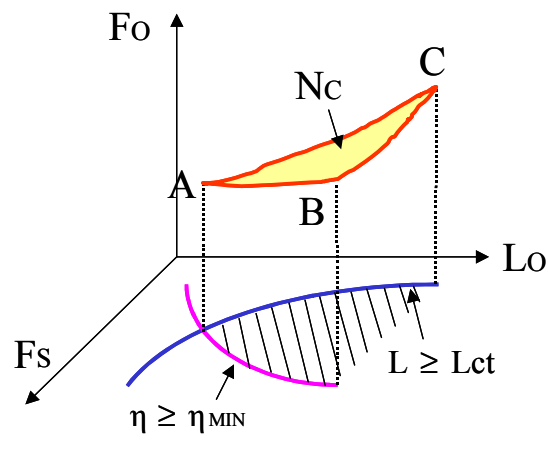
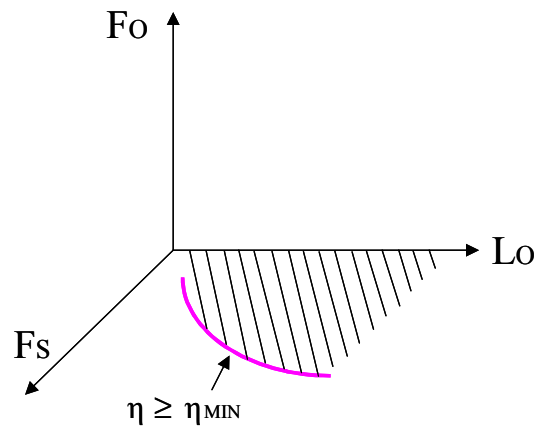
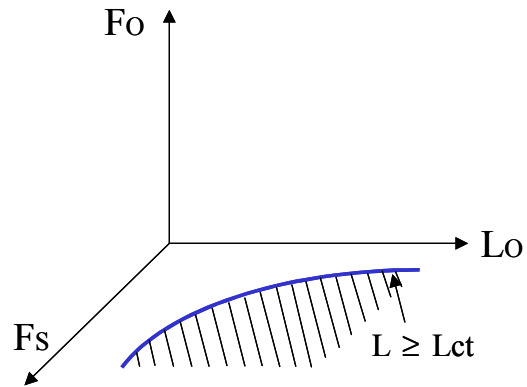


Figure 4.2. Optimization method for a given channel number (N_C): (a) critical inductance, (b) minimum efficiency requirement, and (c) objective function.

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For buck converter, the critical inductance can be derived as follows:

$$L_{ct} = \frac{V_{IN} \cdot \Delta D_{MAX}}{4 \cdot \Delta I_O \cdot F_C} = \frac{V_{IN} \cdot \Delta D_{MAX}}{4 \cdot \Delta I_O \cdot k \cdot F_S}, \quad (4.5)$$

where ΔD_{MAX} is the maximum duty cycle increase during the transient response. When the increase of the duty cycle reaches ΔD_{MAX} , the duty cycle is considered saturated.

As mentioned, for optimal designs, the output inductance is no less than the critical inductance, which is a function of the switching frequency, and can be expressed as follows:

$$L_O \geq L_{ct}(F_S). \quad (4.6)$$

Correspondingly, the optimization solution exists in the area above and including the blue curve, as illustrated in Figure 4.2(b).

The pink curve, as illustrated in Figure 4.2(a), corresponds to the efficiency constraint, as formulated in Equation 4.2. The efficiency is a function of the switching frequency (F_S) and output inductance (L_O). The higher the switching frequency, the lower the efficiency. In order to meet the efficiency constraint, the switching frequency should be lower than a certain level, which is a function of the output inductance (L_O). Correspondingly, the optimization solution exists in the area below and including the pink curve. Along the pink curve, the efficiency is the same. This is the minimum efficiency required by the given specifications.

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For a given channel number (N_{C1}), the optimal design exists in the shaded area formed by the blue and pink curves, as illustrated in Figure 4.2(b). For the given channel number (N_C), the optimization solution is located at the lowest point of the surface area ABC. The location of this lowest point is depends on the shape of the surface area ABC, which is strongly dependent on the objective function of the optimization.

If the objective function is related to the size and cost of the multiphase VRM, some general features for ABC can be illustrated in Figure 4.2(c). For any point not located in the curve AB, both the efficiency and the output inductance increase. Because the output inductance is either greater than or equal to the critical inductance, the duty cycle is saturated during transients. The transient response is limited by the output inductance, and is unrelated to the switching frequency. The increase in the output inductance impairs the transient responses and increases the size and cost of the output inductors and capacitors, while the increase in the efficiency potentially reduces the size for heat spreads. Whether or not the improvement in efficiency can reduce the volume or cost depends on the methods used for thermal management.

Most of today's multiphase VRMs use surface-mounted MOSFETs. Their packaging areas are used for heat spreads. As long as the minimum efficiency requirement is satisfied, the volume and cost of VRMs are limited only by the packaging sizes and costs of individual components. Therefore, to further increase efficiency can only reduce the temperature increase, which would improve the reliability of VRMs, but which cannot

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reduce the volume and cost. In this sense, the optimization solution is located at the minimum required efficiency points, which correspond to the curve AB in Figure 4.2.

In Figure 4.2, along the curve A->B, the efficiency is the same while both the switching frequency and the output inductance increase. Because the output inductance is larger than the critical inductance, the duty cycle is saturated during transients. Therefore, the transient response is not related to the switching frequency, but is limited by the output inductance. With the increase in the output inductance, the transient responses become worse, and larger output capacitors are needed. Both the size and cost of output inductors and capacitors increase along the curve A->B. Therefore, if the optimization solution is located in the curve AB, it must be at the point A.

Based on the preceding discussion, for most of today's multiphase VRMs, the surface area ABC that represents the weighted volume and cost is monotonous, and the optimization solution is located at the point A, which corresponds to the minimum required efficiency and the critical inductance value. With this conclusion, the optimization process for multiphase VRMs is greatly simplified.

The next step of the optimization is to repeat the step illustrated in Figure 4.2 for a range of given channel numbers (N_C) to determine the optimal solution as well as the corresponding switching frequencies (F_S) and output inductances (L_O) for those given channel numbers (N_C).

Finally, the points that correspond to the optimal solutions for those given channel numbers (N_C) can be connected to form a curve. The lowest point along that curve represents the final optimization solution. The resulting curve can also be plotted in a simpler way, as shown in Figure 4.3. The horizontal axis is the channel number (N_C), and the vertical axis is the objective function. The curve in Figure 4.3 represents the optimal solutions for a range of given channel numbers (N_C). The optimal channel number can be easily found in Figure 4.2. Usually a U-shaped curve is obtained, and the optimization solution is simply located at the lowest point of that curve.

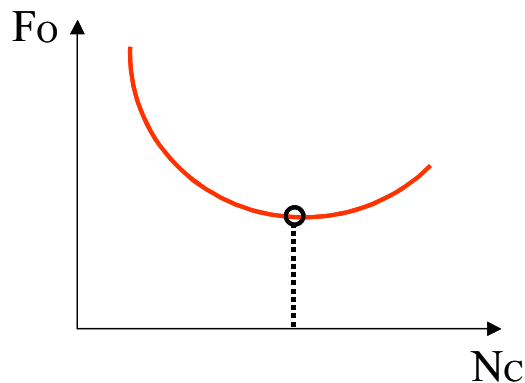


Figure 4.3. Method for finding the optimal channel number.

4.4. DEMONSTRATION OF PROPOSED OPTIMIZATION METHODOLOGY

In the following, the typical VRM 9.0 design for the latest Pentium 4 ® processors is used as an example to demonstrate the proposed optimization method. The multiphase VRM is based on the buck converter.

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According to VRM 9.0 specifications, the optimization problem formulated in Section 4.2 is rewritten, given the following specifications: $V_{IN}=12$ V, $V_O=1.5$ V, $I_O=50$ A, $\Delta I_O=50$ A, $SR_O=50$ A/ μ S, $\Delta V_{OMAX}=100$ mV, and $\eta_{MIN}=80\%$ or 85% (in order to see the impact of the minimum efficiency requirement).

Most of today's multiphase VRMs use surface-mounted MOSFETs and OSCON-type capacitors for input and output capacitors. This study assumes that the most popular MOSFETs and capacitors are used so that the results can represent the current practice. The same process is applicable to other components.

The available MOSFETs are listed as follows: The top switches are Siliconix's Si4884DY ($R_{DS(ON)}=10.5$ m Ω , $Q_G=15.3$ nC, and $Q_{GD}=4.8$ nC), and the bottom switches are Siliconix's Si4874DY ($R_{DS(ON)}=7.5$ m Ω , and $Q_G=35$ nC).

The available types of capacitors are listed as follows: The output capacitors are Sanyo's 4SP820M, (OSCON, ESR=12 m Ω , ESL=4 nH, and $C_o=820$ μ F), and the input capacitors are Sanyo's 16SP270M, (OSCON, ESR=12 m Ω , ESL=4 nH, $C_o=270$ μ F, and $I_{RMS}=4.4$ A).

The transient and efficiency constraints are formulated respectively, as follows:

$$\begin{aligned} \Delta V_o(N_c, F_s, F_c, L_o) &\leq \Delta V_{OMAX}, \text{ and} \\ \eta(N_c, F_s, L_o) &\geq \eta_{MIN}. \end{aligned} \tag{4.7}$$

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The optimization results are strongly dependent on the objective function of the optimization. In this demonstration, a simple objective function is used first to go through the optimization process. After understanding the whole process, a more realistic objective function and its optimization are demonstrated. Finally, a more generalized formulation is given for the optimization of multiphase VRMs.

4.4.1. Example I: Minimizing the Number of Output Capacitors

The output capacitors are the most expensive components of multiphase VRMs in terms of both cost and size. Therefore, the simple objective function used here is to minimize the volume and cost of the output capacitors. Since the volume and cost of output capacitors are proportional to the number of output capacitors, the objective function is modified to minimize the number of output capacitors. This simple objective function can be expressed as follows:

$$F_o(N_c, F_s, F_c, L_o) = \min(N_B). \quad (4.8)$$

Because the objective of the optimization is to minimize the number of output capacitors, the transient response must be designed to be as fast as possible. This requires the use of both the highest possible switching frequency and the critical inductance value for the output inductance. The optimization solution corresponds to the minimum required efficiency and the critical inductance value, located at point A, as illustrated in Figure 4.2.

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Following the optimization method proposed in Section 4.2, the optimal output inductance value is determined first for a range of switching frequencies, as shown in Figure 4.4. The optimal output inductance is designed according to the critical inductance value. The relationship between the optimal output inductance and the switching frequency can be derived as follows:

$$L_o = L_{ct} = \frac{V_{IN} \cdot \Delta D_{MAX}}{4 \cdot \Delta I_o \cdot k \cdot F_s}, \tag{4.9}$$

where k is the ratio of the control bandwidth to the switching frequency. In Figure 4.4, the control bandwidth is designed at one sixth of the switching frequency, which is the typical value in practice. The same process is applicable to other bandwidth designs.

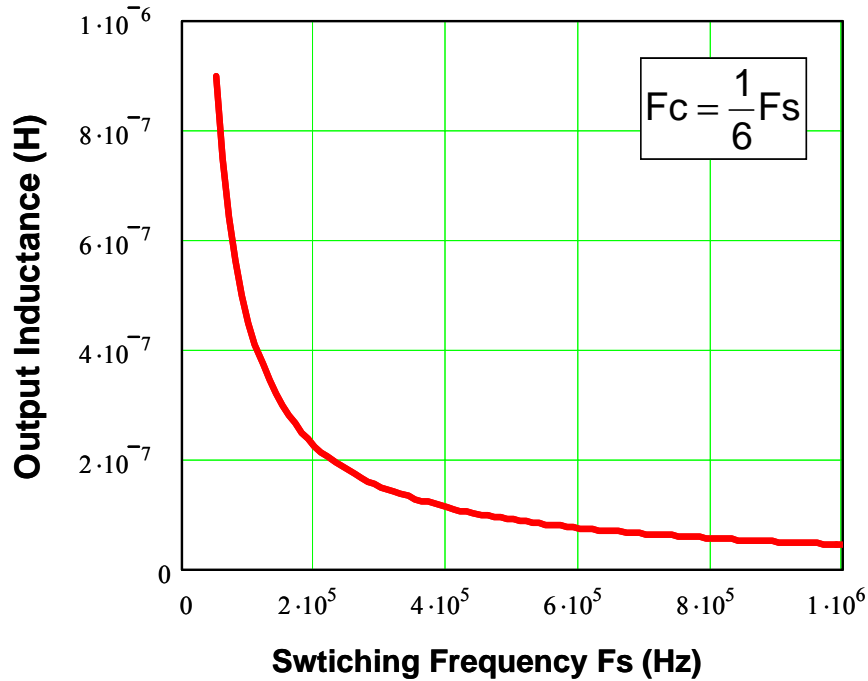


Figure 4.4. Selecting the critical inductance value as the output inductance.

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The second step of the optimization is to develop a family of efficiency curves, $\eta(N_C, F_S)$, and then to determine the maximum allowable switching frequency for each selected channel number, in accordance with the constraints on the developed family of efficiency curves.

Since the optimal output inductance is related to the switching frequency, the efficiency of the multiphase VRM is a function of the channel number (N_C) and switching frequency (F_S), and can be derived as follows:

$$\eta(N_C, F_S) = \frac{V_O \cdot I_O}{P_{tot} + V_O \cdot I_O}, \quad (4.10)$$

where P_{tot} is the total power losses, as derived in Chapter 2.

With the loss model developed in Chapter 2, a family of efficiency curves can be generated for a range of selected channel numbers. Figure 4.5 shows the efficiency of multiphase VRMs under a range of switching frequencies and channel numbers. The horizontal axis is the switching frequency. The channel number is the parameter. Different design criteria could generate different curves. In Figure 4.5, the design criteria are that there are no paralleled devices in the individual channels. The benefit is that the power level of each channel drops as the number of channels increases, so that the switching frequency can be raised to improve the transient response while still allowing the system to meet the efficiency requirements. The limitation is that more semiconductor devices must be used with the increased number of channels. The optimization procedure is the same for other design criteria. Following the same process, the results of using the

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same active area of semiconductors for MOSFETs are also given at the end of this section in order to see the impact of this design criterion.

According to the efficiency constraint, the maximum allowable switching frequency can then be determined for a range of channel numbers. In Figure 4.5, two straight lines corresponding to 80% and 85% represent the efficiency constraint. For a selected channel number, the intersection of the corresponding efficiency curve with the constraint line gives the maximum allowable switching frequency. Table 4.2 shows the maximum allowable switching frequencies for different numbers of channels.

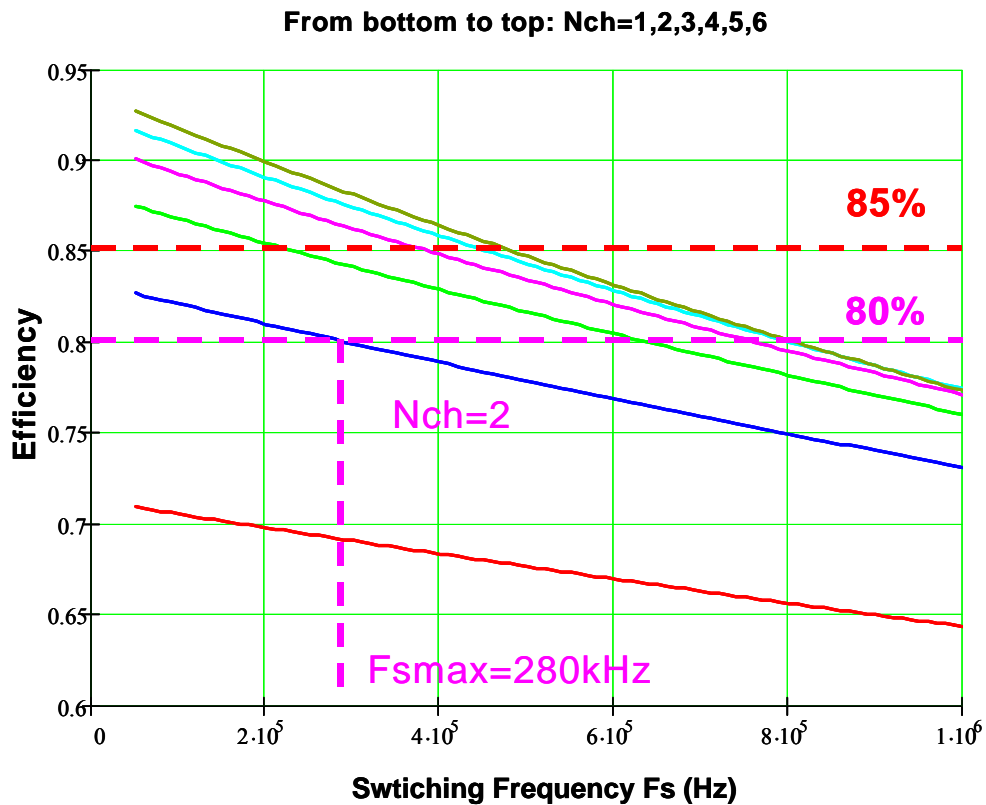


Figure 4.5. Determining the maximum switching frequency for a selected channel number in accordance with the efficiency constraint.

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Table 4.2. Maximum allowable switching frequency for selected channel number.

	80% (1)	85% (2)
Nch	Fs1 max kHz	Fs2 max kHz
2	280	-
3	630	220
4	750	390
5	800	430
6	800	440

The third step of the optimization is to develop a family of curves for the required output capacitor number versus the switching frequency and channel number, $N_B(N_C, F_S)$, and then mapping the maximum switching frequency and corresponding channel number obtained from the second step into the developed family of curves $N_B(N_C, F_S)$ to determine the minimum required number for the output capacitors, which is the objective function of the optimization.

In order to establish a detailed mathematical form for the transient constraint as formulated in Equation 4.1, the transient for a multiphase VRM is studied and the transient voltage deviation is quantified. The main results are given as follows.

Two voltage spikes exist on typical transient waveforms for the VRM output voltage. The first spike is mainly determined by the ESL and ESR of the output capacitors. The magnitude of the first spike can be derived as follows:

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$$\Delta V_{p1} \approx R_{ESR} \cdot (\Delta I_O + \Delta I_L) + L_{ESL} \cdot SR_O, \quad (4.11)$$

where ΔI_L is the peak-to-peak value of the steady-state inductor current.

The second spike is mainly determined by the capacitance and ESR of the output capacitors. The magnitude of the second spike can be obtained as follows:

$$\Delta V_{p2} = \frac{\Delta I_O}{2C_O \cdot SR_L} \cdot \left(\Delta I_O + \Delta I_L + \frac{\Delta I_L^2}{4\Delta I_O} \right) - \frac{\Delta I_O^2}{2C_O \cdot SR_O} + R_{ESR} \cdot \frac{R_{ESR} \cdot C_O \cdot SR_L + \Delta I_L}{2}. \quad (4.12)$$

The transient voltage deviation is the larger of these two spikes. As can be seen from Equations 4.11 and 4.12, the transient voltage deviation is a function of the channel number (N_C), output inductance (L_O) and switching frequency (F_S). Figure 4.6 shows the influence of the channel number (N_C) and output inductance (L_O) on the transient voltage deviation. It is assumed that the VRM output uses eight pieces of 820 μ F OSCON capacitors.

As can be seen from Equations 4.11 and 4.12, the transient voltage deviation is proportional to the number of output capacitors. In order to meet the transient constraint, the transient voltage deviation must be less than the specified values, ΔV_{OMAX} . Since the optimal output inductance is related to the switching frequency, the number of required output capacitors is a function of the channel number (N_C) and switching frequency (F_S), and can be derived as follows:

$$N_B \geq \frac{\max(\Delta a_{P1}, \Delta V_{P2})}{\Delta V_{OMAX}}. \quad (4.13)$$

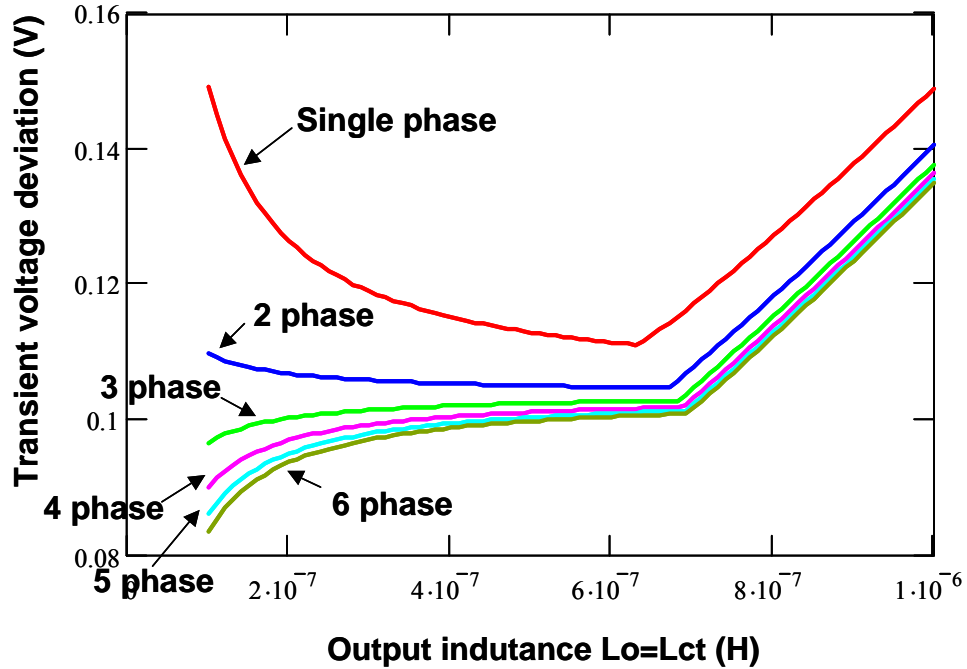


Figure 4.6. Transient voltage deviation for selected channel numbers.

Based on Equation 4.13, a family of curves for the required output capacitor number versus the switching frequency and channel number, $N_B(N_C, F_S)$, can be plotted as shown in Figure 4.7. The horizontal axis is the switching frequency. The channel number is the parameter. The results from the second step, the maximum switching frequency and corresponding channel number, are mapped into the developed family of curves $N_B(N_C, F_S)$, and then the minimum required number for the output capacitors can be determined. The detailed manipulation is explained in Figure 4.7. For a selected channel number, for example $N_C=2$, as shown in the Figure 4.7, the maximum allowable switching frequency for the satisfaction of the efficiency constraints is 280 kHz. Consequently, the minimum required number of output capacitors is obtained from the vertical axis. The required

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number should be chosen such that the minimum integer that exceeds the value corresponds to the maximum switching frequency. Correspondingly, a smaller switching frequency exists for the minimum number, which allows a higher efficiency while still satisfying the transient response. For the minimum required capacitor number, there is a range from which the switching frequency must be selected. Within the range, the transient requirement is stratified.

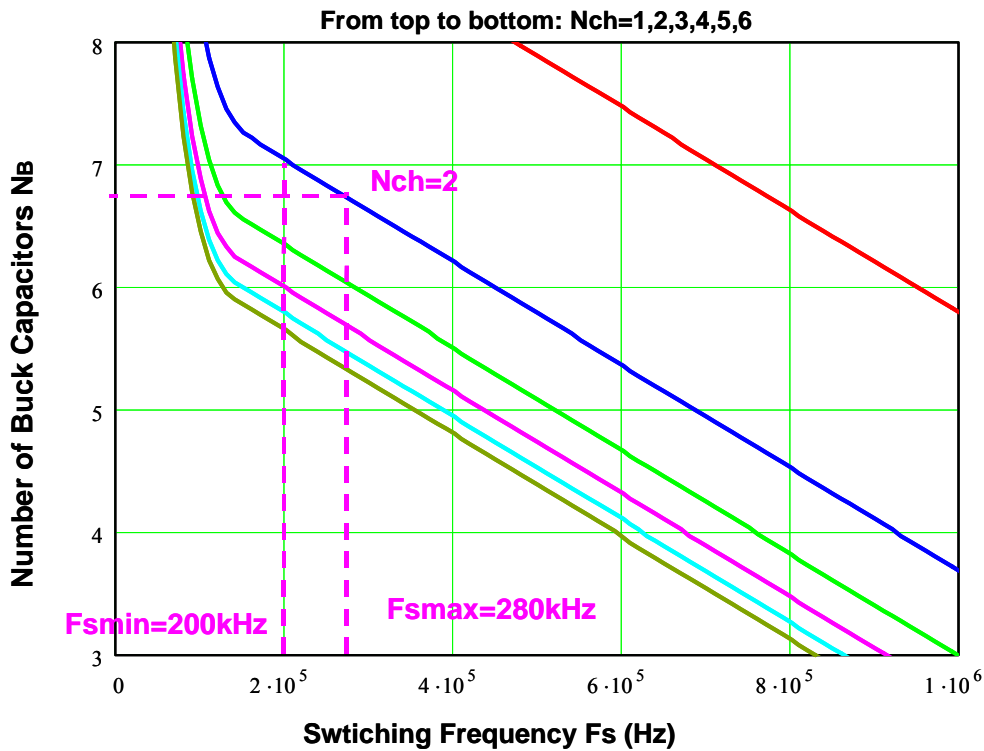


Figure 4.7. Determining the minimum required numbers of output capacitors for selected channel numbers in accordance with the transient constraint.

For a range of channel numbers, the minimum required capacitor numbers and the corresponding switching frequency ranges are determined, as listed in Table 4.3.

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Table 4.3. Minimum required number of capacitors and corresponding switching frequency ranges for selected channel numbers.

Nch	80%(1)			85%(2)		
	Fs max KHz	NB	Fs min KHz	Fs max KHz	NB	Fs min KHz
2	280	7	200	-	-	-
3	630	5	510	220	7	120
4	750	4	680	390	6	200
5	800	4	620	430	5	390
6	800	4	600	440	5	370

Since the objective function in this example is to minimize the number of output capacitors, the final step of the optimization is to compare the results in Table 4.3, and thus obtain the optimization solution.

As can be seen from Table 4.3, the greater the channel number, the fewer the required output capacitors. This result agrees with the common sense that more channels are always preferred in order to minimize the number of output capacitors. Because of such a simple objective function, the optimization cannot determine the right number of channels for real designs. Table 4.4 shows the comparison of the optimization results with some typical designs in industrial practice. A more realistic objective function

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should be considered in order to determine the right number of channels for an optimal design.

Table 4.4. Comparison of optimization results with industry practice.

Vin=12V, Vo=1.5V, Io=50A, SRo=50A/uS, ΔIo=50A, ΔVo=100mV

	Channel Number	Switching Freq. (kHz)	Full Load Eff. (%)	Inductance Per Channel (nH)	Output Bulk Capacitors
	2	200~280	80	400	7x820uF (OSCON)
	3	120--220	85	630	7x820uF (OSCON)
	4	200~390	85	480	6x820uF (OSCON)
ADI	2	200	79	600	8x1200uF (OSCON)
Intersil	3	200	83	850	6x1000uF (OSCON)
On-Semi	3	250	83	500	14x1200uF (Aluminum)
Semtech	4	250	83	600	6x820uF (OSCON)

In the preceding optimization, the design criteria used in the second step assumes that there are no paralleled devices in the individual channels. Other design criteria could generate different results. Another possible design criterion involves the use of the same active area of semiconductors for the MOSFETs in the selection of different channel numbers. Table 4.5 shows the optimization results using this criterion.

As can be seen from Tables 4.4 and 4.5, due to the simple objective function, the optimization cannot determine the right number of channels for real designs. Again, a more realistic objective function should be considered.

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Table 4.5. Optimization results using the same active area of semiconductors for MOSFETs and their comparison with industry practice.

V_{in}=12V, V_o=1.5V, I_o=50A, S_{Ro}=50A/uS, ΔI_o=50A, ΔV_o=100mV

	Channel Number	Switching Freq. (kHz)	Full Load Eff. (%)	Inductance Per Channel (nH)	Output Bulk Capacitors
	1	250~390	85	120	9x820uF (OSCON)
	2	200~390	85	240	7x820uF (OSCON)
	3	280~390	85	360	6x820uF (OSCON)
	4	200~390	85	480	6x820uF (OSCON)
ADI	2	200	79	600	8x1200uF (OSCON)
Intersil	3	200	83	850	6x1000uF (OSCON)
On-Semi	3	250	83	500	14x1200uF (Aluminum)
Semtech	4	250	83	600	6x820uF (OSCON)

4.4.2. Example II: Minimizing the Cost of the VRM

A more realistic objective function should consider not only the output capacitors but also other components. Most of today’s VRM designs are cost-driven. As long as they can meet the specifications, cutting cost is the first priority. In this sense, the more realistic objective function is to minimize the cost of entire VRMs, and it can be expressed as follows:

$$F_o'(N_c, F_s, F_c, L_o) = \min(C). \tag{4.14}$$

The total cost of multiphase VRMs consists of the costs of output capacitors, input capacitors, output inductors, MOSFETs, gate drive ICs and the multiphase control IC. Figure 4.8 shows the cost breakdown for typical multiphase VRMs. Capacitors,

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semiconductors and inductors occupy 44%, 48% and 9% of the total cost, respectively.

The major costs come from capacitors and semiconductors.

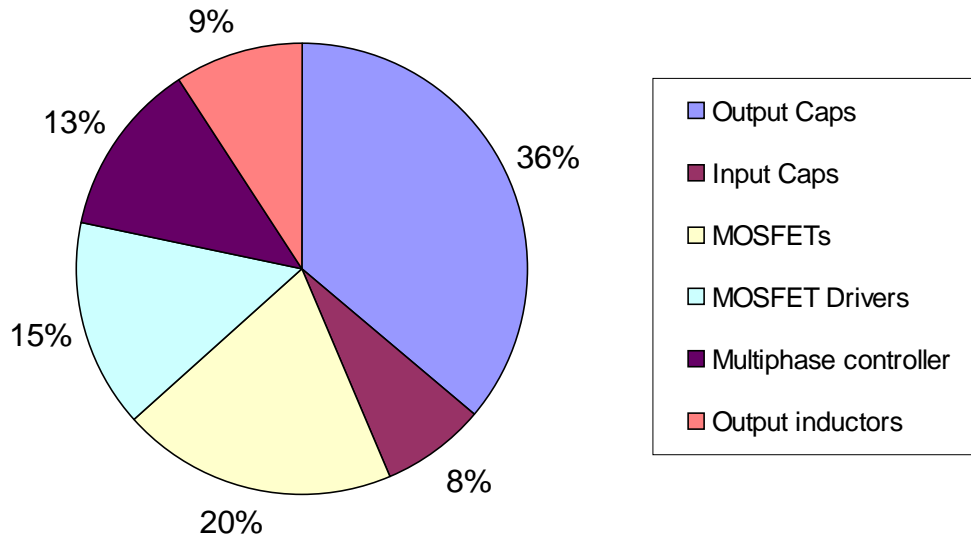


Figure 4.8. Cost breakdown for typical multiphase VRMs.

Following the optimization method proposed in Section 4.2, the optimization solution to minimize the total cost of VRMs corresponds to the minimum required efficiency and the critical inductance value, located at point A, as illustrated in Figure 4.2. This conclusion assumes that increasing the efficiency beyond the minimum requirement cannot reduce the cost of VRMs. Most of today's multiphase designs follow this kind of criterion. Therefore, it is reasonable to make such an assumption for the following optimization.

The first three steps for this optimization example are the same as those for the previous example in Section 4.3.1. They can be briefly described as follows.

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First, the optimal output inductances are chosen as the critical inductance values within a range of switching frequencies, as shown in Figure 4.4.

Second, in accordance with the efficiency constraints on the family of efficiency curves, $\eta(N_C, F_S)$, the maximum allowable switching frequencies are determined for selected channel numbers. In this example, the area of semiconductors for the MOSFETs are assumed to be the same for the selected channel numbers, and the minimum required efficiency is assumed to be 80%.

Third, in accordance with the transient constraints, by mapping the maximum switching frequencies from the second step into the family of curves, $N_B(N_C, F_S)$, the minimum required numbers of the output capacitors are determined for selected channel numbers.

Based on these three steps, for the selected channel numbers, the optimal designs for output inductors and capacitors are determined. The next step of this optimization is to find out the minimum required numbers of input capacitors for the selected channel numbers. Generally, OSCON capacitors have a large energy capacity, so the number of input capacitors is designed to ensure that the RMS current through the input capacitors will be less than the RMS current rating of the input capacitors. With available OSCON capacitors, the minimum number of input capacitors can be derived as follows:

$$N_{CIN} \geq \frac{I_{CIN}}{I_{RMS}}, \quad (4.15)$$

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where I_{RMS} is the RMS current rating of one input capacitor, and I_{CIN} is the RMS current through all of the input capacitors. The RMS current through the input capacitors can be derived as follows:

$$I_{CIN} = I_O \sqrt{\left(D - \frac{m}{N}\right)\left(\frac{m+1}{N} - D\right) + \frac{N}{12} \left(\frac{\Delta I_{LCH}}{D \cdot I_O}\right)^2 \left[(m+1)^2 \left(D - \frac{m}{N}\right)^3 + m^2 \left(\frac{m+1}{N} - D\right)^3 \right]}, \quad (4.16)$$

where I_O and ΔI_{LCH} are the load current and the channel peak-to-peak inductor current, respectively. The $m = \text{floor}(N \cdot D)$ is the maximum integer that does not exceed the $N \cdot D$.

Based on the preceding steps, the optimal designs for selected channel numbers can be determined. They are summarized in Table 4.6.

Table 4.6. Optimal designs for selected channel numbers.

Channel Number	Output Capacitors	Input Capacitors	Output Inductors
2	7x4SP820M	5x16SP100M	2x240μH/25A
3	5x4SP820M	4x16SP100M	3x360μH/17A
4	4x4SP820M	3x16SP100M	4x480μH/12.5A
5	4x4SP820M	3x16SP100M	5x600μH/10A

The final step of this optimization is to find out the number of channels that achieves the lowest total cost for the VRMs. Based on the optimal designs for selected channel numbers, the cost data for individual components are collected first, including those for

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the output capacitors, the input capacitors, the output inductors, the MOSFETs, the drive ICs and the multiphase control IC. Generally these cost data can be obtained from manufacturers, and may vary from designer to designer. By totaling the costs of individual components, the overall cost of multiphase VRMs can be obtained for selected channel numbers. Generally, the costs of input and output capacitors decrease with the increase of the channel number, while the cost of semiconductors increases with the increase of the channel number. Normally, the relationship between the total cost of VRMs and the channel number can be illustrated in a U-shaped curve; the optimization solution is located at the valley point.

As an example, Figure 4.9 shows the cost breakdown for multiphase VRMs within a range of channel numbers. The cost data are normalized against the total cost of the three-phase VRM. Since the active area of semiconductors used for the MOSFETs is assumed to be the same for different numbers of channels in this example, the cost of the MOSFETs is also the same. The costs of drive ICs and the multiphase control IC are assumed to increase by 25% each time the channel number increases by one. The cost of output inductors is simply assumed to be the same for different channel numbers.

As can be seen from Figure 4.9, with the increase of the channel number, the costs of input and output capacitors are reduced. However, the increased channel number requires more gate drive ICs, as well as a more complicated multiphase control IC, both of which increase their costs. Therefore, the relationship between the total cost of VRMs and the channel number is a U-shaped curve, and the optimal channel number corresponding to

the lowest cost is located at the valley point. As can be seen from Figure 4.9, the selection of four channels gives the lowest total cost, and the optimal channel number is four in this example.

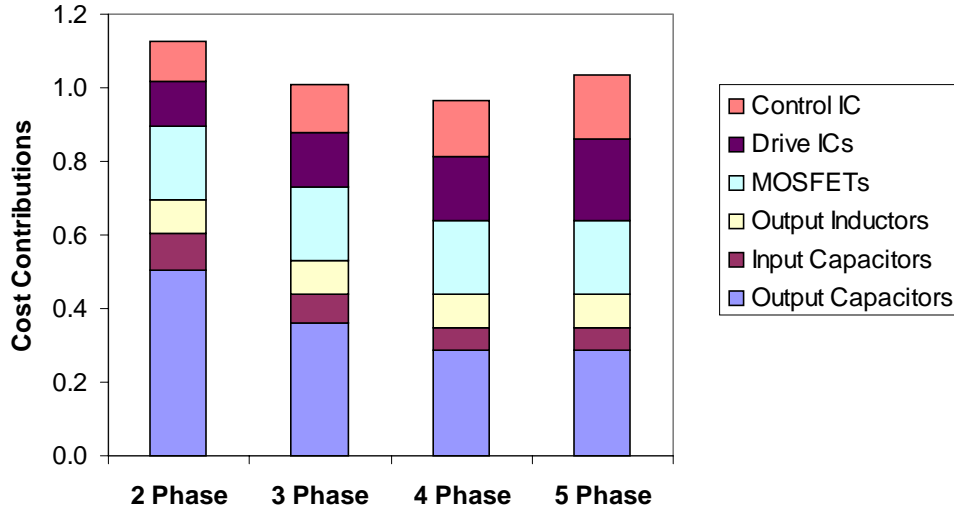


Figure 4.9. Influence of the channel number on the cost of multiphase VRMs.

4.4.3. More Generalized Formulation

Generally, small volume and low cost are the two major considerations for VRM designs. The importance of volume and cost is dependent on the preferences of individual manufacturers or designers, and it can be modeled by individual weighting factors.

The more generalized objective of the optimization is to minimize the weighted volume and cost of VRMs, and its objective function can be formulated as follows:

$$F_o(N_c, F_s, F_c, L_o) = \min(V \cdot W_v + C \cdot W_c), \quad (4.17)$$

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where V and C are the normalized volume and cost of multiphase VRMs, respectively. W_V and W_C are their corresponding weighting factors.

With the satisfaction of the efficiency and transient constraints, as formulated in Equations 4.7 and 4.8, the tradeoff among the channel number (N_C), switching frequency (F_S), control bandwidth (F_C), and output inductance (L_O) gives the optimal solution. The optimization process is similar to that of Example II. However, additional data on the volume of individual components, as well as the weighting factors of volume and cost, need to be determined by individual manufacturers or designers and put into the optimization objective function.

4.5. SUMMARY

In this chapter, an optimization methodology has been proposed for multiphase VRMs, in order to determine the appropriate number of channels for an optimal design.

The formulation of the optimization problem has been discussed. Two constraints exist, corresponding to the requirements of the transient responses and the minimum efficiency. Four design variables need to be traded off; they are the channel number, switching frequency, control bandwidth and output inductance. The selection of the objective function is the preference of individual manufactures or designers. Minimized weighted volume and cost could be the objective function for most of today's multiphase VRMs.

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The general method of optimization has been proposed. As a dependent variable, the control bandwidth is eliminated from the four design variables. The optimization problem can be illustrated by a series of surfaces in a three-dimensional space, with the objective function as the vertical axis, the switching frequency and the output inductance as the two horizontal axes, and the channel number as the parameter. The proposed optimization method first looks for the lowest points of these surfaces, which represent the optimal designs for the given channel numbers. For most of today's multiphase designs, these lowest points correspond to the design of the minimum efficiency and the critical inductance. Connecting these lowest points together forms a curve, and the optimization solution is located at the lowest point of this curve.

Two optimization examples have been provided in order to demonstrate the optimization procedure. Both are performed on typical VRM 9.0 designs for the latest Pentium 4® processors. The first example has a simple objective function, to minimize the number of output capacitors. A more realistic objective function is used for the second example, to minimize the cost of multiphase VRMs. The optimization results are compared with the industry practice. The optimization results provide not only the appropriate channel number, but also the complete design, including the output inductance value, the switching frequency and total number of input and output capacitors required. The more generalized formulation has been discussed. Its objective function could be to minimize the weighted volume and cost of multiphase VRMs.