Third Quadrant Operation of 1.2-10 kV SiC Power MOSFETs

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(ABSTRACT)

The third quadrant (3^{rd}-quad) conduction (or reverse conduction) of power transistors is critical for synchronous power converters. For power metal-oxide-semiconductor field-effect-transistors (MOSFETs), there are two current paths in the 3^{rd}-quad conduction, namely the MOS channel path and the body diode path. It is well known that, for 1.2 kV silicon carbide (SiC) planar MOSFETs, the conduction loss in the 3^{rd}-quad is reduced by turning on the MOS channel with a positive gate bias (V_{GS}) and keeping the dead time as small as possible. Under this scenario, the current is conducted through both paths, allowing the device to take advantage of the zero 3^{rd}-quad forward voltage drop (V_F^{3rd}) of the MOS channel path and the small differential resistance of the body diode path.

However, in this thesis work, this popular belief is found to be invalid for power MOSFETs with higher voltage ratings (e.g., 3.3 kV and 10 kV), particularly at high temperatures and current levels. The aforementioned MOS channel and body diode paths compete in the device's 3^{rd}-quad conduction, and their competition is affected by V_{GS} and device structure.

This thesis work presents a comparative study on the 3^{rd}-quad behavior of 1.2 kV to 10 kV SiC planar MOSFET through a combination of device characterization, TCAD simulation and analytical modeling. It is revealed that, once the MOS channel turns on, it changes the potential distribution within the device, which further makes the body diode turn on at a source-to-drain voltage (V_{SD}) much higher than the built-in potential of the pn junction. In 10 kV SiC MOSFETs, with the MOS channel on, the body diode does not turn on over the entire practical V_{SD} range. As a result, the positive V_{GS} leads to a completely unipolar conduction via the MOS channel, which could induce a higher V_F^{3rd} than the bipolar body diode at high temperatures. Circuit test is performed, which validates that a

negative V_{GS} control provides the smallest 3rd-quad voltage drop and conduction loss at high temperatures in 10 kV SiC planar MOSFET. The study is also extended to the trench MOSFET, another major structure of commercial SiC MOSFETs. Based on the revealed physics for planar MOSFETs, the optimal V_{GS} control for the 3rd-quad conduction in different types of commercial trench MOSFETs is discussed, which provides insights for the design of high-voltage trench MOSFETs. These results provide key guidelines for the circuit applications of medium-voltage SiC power MOSFETs.

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(GENERAL AUDIENCE ABSTRACT)

Recent years, the prosperity of power electronics applications such as electric vehicle and smart grid has led to a rapid increase in the adoption of wide bandgap (WBG) power devices. Silicon Carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) is one of the most attractive candidates in WBG devices, owing to its good tradeoff between breakdown voltage and on resistance, capability of operation at high temperatures, and superior device robustness over other WBG power devices.

In most power converters, power device is required to conduct current in its third quadrant (3rd-quad) (i.e., conduct reverse current) either for handling current during the dead time or acting as a commutation switch. In a SiC MOSFET, there are two current paths in the 3rd-quad conduction, namely the MOS channel path and the body diode path. It is widely accepted that by turning on the MOS channel with a positive gate-to-source bias (V_{GS}), both paths are turned on in parallel such that the 3rd-quad conduction loss can be reduced.

In this thesis work, it is shown that this long-held opinion does not hold for SiC MOSFETs with high voltage ratings (e.g., 3.3 kV and 10 kV). Through a combination of device characterization, TCAD simulation, and analytical modeling, this thesis work unveils the competing current sharing between the MOS channel and the body diode. Once the MOS channel turns on, it delays the turn-on of the body diode and suppresses the diode current. This effect is more pronounced in MOSFETs with higher voltage ratings. In 10 kV SiC MOSFETs, with the MOS channel on, the body diode does not turn on in the practical operation conditions. At high temperatures, as the bipolar diode path possesses the conductivity modulation, which can significantly lower the voltage drop and is absent in the MOS channel, it would be optimal to turn off the MOS channel. Circuit test is also

performed to validate these device findings and evaluate their impact on device applications. Finally, the study is also extended to the commercial SiC trench MOSFET, the other mainstream type of SiC power MOSFETs. These results provide key guidelines for the circuit applications of medium-voltage SiC power MOSFETs.

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Chapter 1: Introduction of SiC MOSFETs

1.1 Wide Bandgap Power Devices

Power switch is one of the key components in almost any power electronics circuit. From the first successful demonstration of the metal-oxide-semiconductor field-effect transistor (MOSFET) in 1959 [1], MOSFET has been widely adopted in power electronics systems as the power switch. The MOSFET properties perfectly fit the requirements of power electronics applications: it blocks high voltage in the off-state but has small on resistance (R_{ON}) when being turned-on. It switches fast as controlled by the gate with small gate charge (Q_G) and is equipped with bi-directional current conduction capability.

Most of power MOSFETs are fabricated with Silicon (Si), the most well-known semiconductor material. With the invention of superjunction MOSFET in 1980s [2], the R_{ON} of Si-based MOSFETs drastically reduced, and Si CoolMOS^{TM} hit the market with over 600 V voltage rating. Meanwhile, the potential of Si was almost fully exploited.

However, the quest never stops on the development of new power devices. With the potential of enabling smaller size, faster switching speed and lower R_{ON}, wide bandgap (WBG) power semiconductor devices are drawing more and more attention for next-generation power electronics applications. The two most popular candidates in the WBG material family are Silicon Carbide (to be more specific, 4H-SiC, with a bandgap of ~3.2 eV) [3] and Gallium Nitride (GaN, with a bandgap of ~ 3.4 eV) [3] [4]. Compared to Si, whose bandgap is ~ 1.1 eV, SiC and GaN are equipped with an around 10 times higher critical electric field (E_C). When judging the potential of a material for unipolar power devices, a figure of merit (FOM) proposed by Baliga is usually used, which is defined in formula (1) [5]:

$$\frac{V_B^2}{R_{on,sp}} = \frac{\epsilon \mu_n E_C^3}{4} \tag{1}$$

where V_B is the device breakdown voltage, $R_{on,sp}$ is the specific on-resistance (resistance per unit area), ϵ is material permittivity, μ_n is the carrier mobility, and E_C is the critical electric field of the material. Fig. 1 plots the limits of Si, SiC and GaN for unipolar power

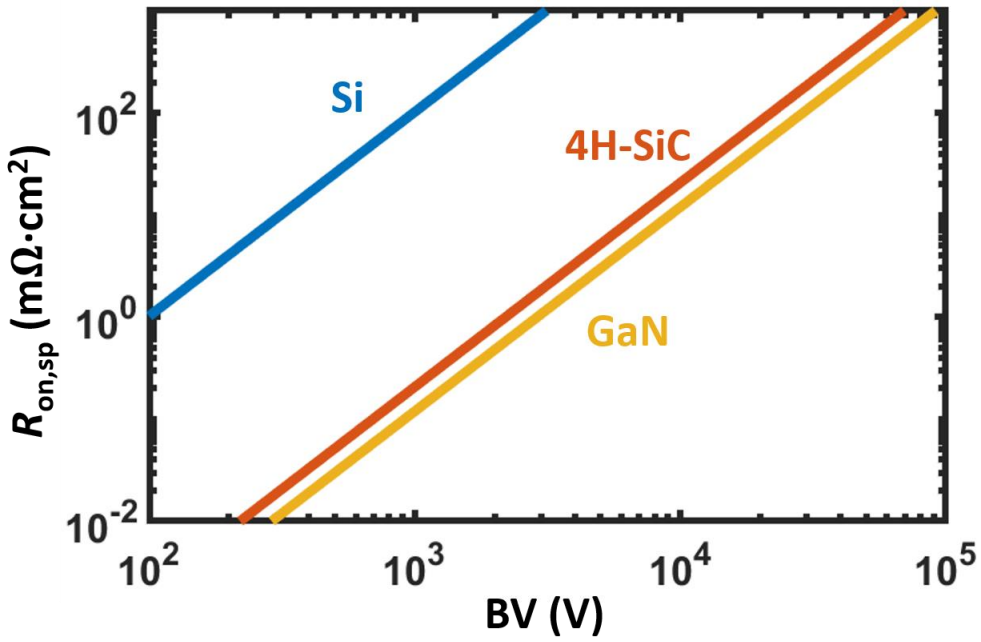

Figure 1. Unipolar limits of Si, 4H-SiC and GaN power devices.

devices. From the FOM, it can be clearly seen that a 10 times higher E_C gives a drastic decrease in $R_{on,sp}$ while maintaining the same V_B: by increasing the doping concentration and reducing the thickness of the drift layer. Therefore, WBG devices come with smaller die size and device capacitance as compared to Si devices, enable fast switching operation up to megahertz, and reduce the size of the passive components, which allow for the system miniaturization in many applications such as electric vehicle (EV) and portable adapter [6] [7] [8].

Another advantage of WBG device is the high temperature operation capability. Since semiconductor material bandgap usually shrinks with increasing temperature, leading to an increase in intrinsic carrier density and off-state leakage current [9]. Wider bandgap gives higher temperature tolerance in operation. SiC-based power junction-gate field-effect transistor (JFET) has been reported to safely operate at 400 ^{o}C [10], which is an unmatched capability by Si-based power devices.

1.2 SiC Power MOSFETs

SiC power MOSFETs have been commercialized from 650 V to 1.7 kV by multiple vendors [11] and pre-commercialized up to 10 kV as well [12]. The structure of commercial SiC MOSFETs can be divided into two categories: the planar MOSFET and the trench MOSFET.

As illustrated in Fig. 2, in a planar MOSFET, the channel is formed underneath the planar gate. When device is turned-on, electron current goes through the channel of an inversion layer to the heavier doped JFET region, then spreads in the n-type drift region. The composition of R_{ON} is listed in formula (2) (ignoring the substrate and contact resistance):

$$R_{ON} = R_{Channel} + R_{JFET} + R_{Drift} \tag{2}$$

Where $R_{Channel}$ is the resistance of the MOS channel, R_{JFET} is the resistance of the heavier-doped JFET region, R_{Drift} is the resistance of the thick, lightly-doped drift region in a power MOSFET.

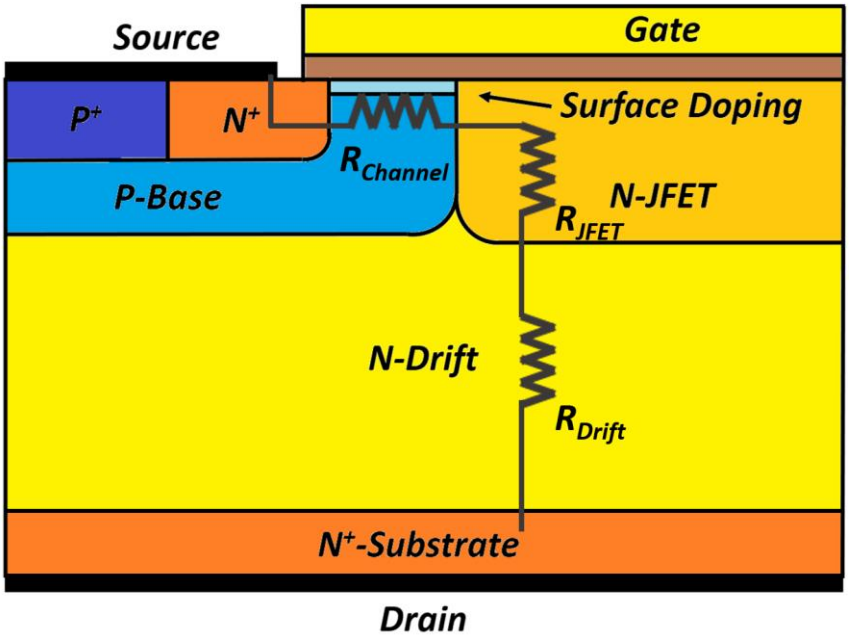

Figure 2. Typical structure of a power planar MOSFET half-cell.

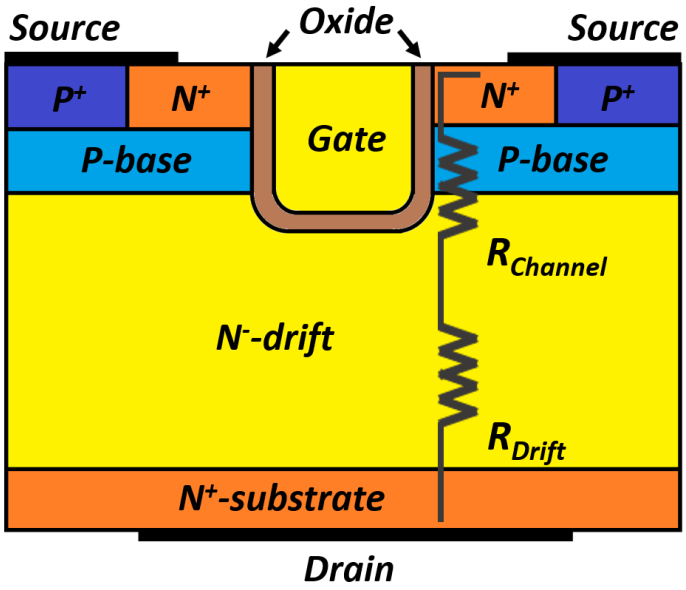

Figure 3. Illustration of a trench MOSFET unit-cell.

In a standard trench MOSFET, gate electrode is embedded into a carved trench, forming a vertical channel (Fig. 3). Compared to a planar MOSFET, a trench MOSFET eliminates the current spreading in the JFET region, resulting in a smaller cell pitch, higher channel density and smaller $R_{on.sp}$. The composition of R_{ON} can be written as:

$$R_{ON} = R_{Channel} + R_{Drift} \tag{3}$$

Despite the advantages in device characteristics, trench MOSFET faces additional challenges in device reliability: electric field can congregate at the edge of the gate trench in device off-state and damage the gate oxide layer, causing catastrophic device failure.

To alleviate this issue, different designs are implemented in commercial SiC trench MOSFETs. The basic design rule is to shield the gate edge from the peak electric field. Fig. 4(a) shows the cross-section schematic of Rohm's double-trench MOSFET [13], where two source trenches are fabricated along with the gate trench and act as the gate shield. Fig. 4(b) shows the schematic of the Infineon CoolSiC^{TM} transistor [14], where a p^+ emitter on the other side of the gate trench shields both gate edges from high electric field. Note that a narrow JFET region is formed in both designs. Therefore, for commercial trench MOSFETs, the R_{ON} composition is similar to that in planar MOSFETs as described in formula (2).

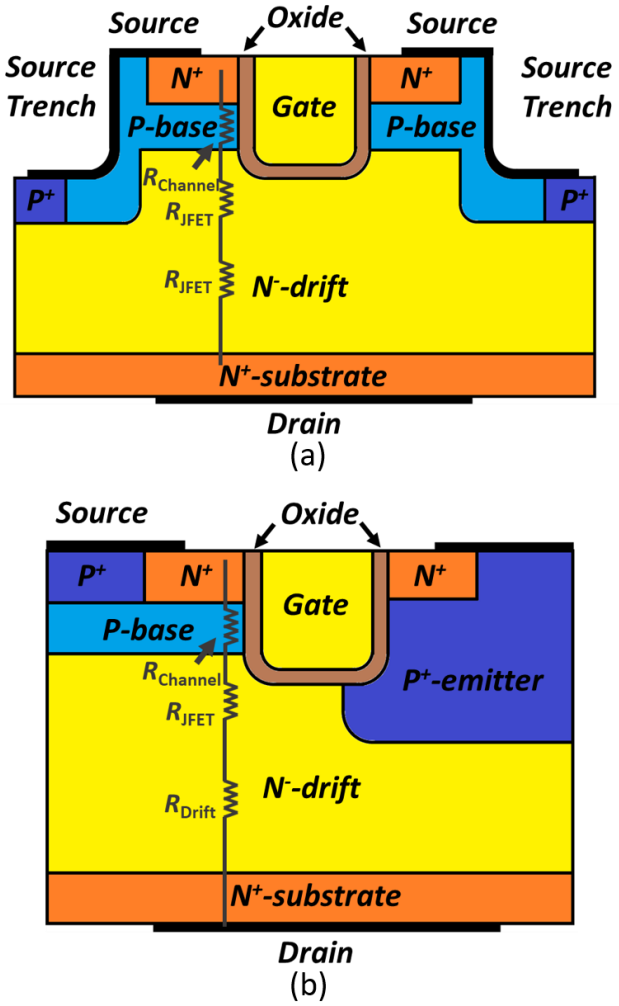

Figure 4. Illustration of (a) commercial double-trench MOSFET and (b) CoolSiC trench MOSFET.

1.3 Comparison between SiC MOSFETs and GaN HEMTs

GaN power devices have been commercialized up to 900 V with a device structure known as the high electron mobility transistor (HEMT). As shown in Fig. 5, GaN HEMTs are usually fabricated on Si substrates to reduce cost and compromise a thick transition layer to compensate the lattice mismatch between GaN and Si and reduce defect density in the GaN buffer layer [15], [16]. An AlGaN layer is grown on the GaN buffer, forming a high mobility two-dimensional electron gas (2DEG) channel at the AlGaN/GaN interface due to the spontaneous and piezoelectric polarizations [17]. Emerging lateral GaN diodes and HEMTs have also been demonstrated at medium-voltage up to 10 kV [18]–[21].

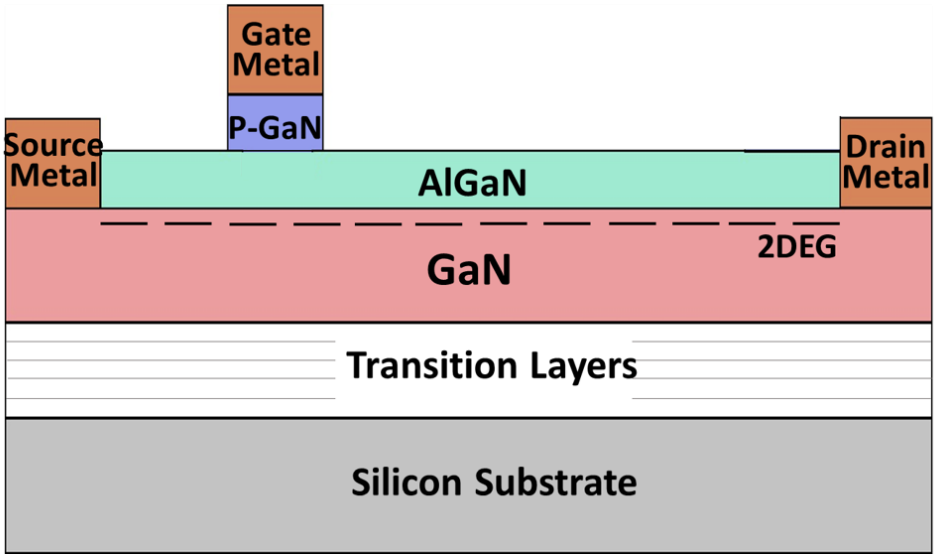

Figure 5. Typical structure of a GaN HEMT.

Vertical GaN FETs have recently achieved superior performance over SiC MOSFETs and lateral GaN HEMTs at a voltage class over 1 kV [22]–[27]. Due to the relatively early stage of development and a relatively high cost of the high quality GaN substrate [28], [29], vertical GaN FETs have not been commercialized, and GaN HEMT is the only type of available commercial GaN power device in the market at present.

Though GaN HEMTs have the advantages in material properties such as higher bandgap and higher E_C, as well as higher electron mobility, SiC MOSFETs are more robust in harsh conditions such as the unclamped inductive switching (UIS), avalanche, and short circuit (SC).

The pn junction in SiC MOSFETs allow them to dissipate the inductive energy safely through avalanching. The critical avalanche energy (E_{AVA}) of 1.2 kV SiC MOSFET was reported as high as 14.9 J/cm^2 [30]. However, there is no pn junction in GaN HEMTs, and they can only transfer the inductive energy via capacitive charging without dissipating it [31]–[33] . The equivalent E_{AVA} is less than 1% of the E_{AVA} of SiC MOSFET with similar rating [31].

Under the SC condition, GaN HEMTs are known to be vulnerable: at 400 V bus voltage (V_{BUS}), the reported short circuit withstanding time (SCWT) is less than 1 µs in all types of 600-V class commercial GaN HEMTs [34] [35] [36]. While the SCWT can be ~ 5 µs in

1.2 kV SiC MOSFETs at 800 V V_{BUS} [37]. Therefore, SiC MOSFETs are more favorable in motor drive and power grids applications.

It should be noted that the inferior robustness in GaN HEMTs is mainly due to the HEMT structure. Vertical GaN JFETs have recently demonstrated excellent avalanche and short-circuit capabilities with an E_{AVA} comparable to SiC MOSFETs [38], [39] and a SCWT of over 30 μs at 400 V bus voltage [40]. Nevertheless, these vertical GaN transistors have not reached commercialization and massive applications.

Besides the advantages in device robustness, SiC MOSFETs are particularly attractive for kilovolt applications thanks to its vertical structure: for a higher device breakdown voltage, the drift region thickness of vertical devices increases without increasing device area. But in lateral GaN HEMTs, to increase device breakdown voltage, drain to gate distance needs to be expanded, which increases chip size and the cost. The vertical structure can also allow for a superior thermal management due to more spreading current and electric field distributions [41]. In general, SiC MOSFETs are more used in power electronics applications with a voltage class over 600 V [42] [43], which forms the power device matrix today. In this work, we are going to see the unique physics in the 3rd-quad conduction of 1.2-10 kV rated SiC MOSFETs.

Chapter 2: Introduction of Third Quadrant Operation

2.1 Power Circuit Requirement

The third quadrant (3rd-quad) conduction or the reverse conduction capability of power device is required in various applications, e.g., almost all the DC-DC converters and voltage source inverters. Here we use a basic buck converter (Fig. 6) and a half-bridge voltage source inverter (Fig. 7) as examples. In buck converter, when the top switch is turned off, the bottom switch should work in the 3rd-quad conduction mode as a freewheeling device (Fig. 6(b), (c)). If zero voltage switching (ZVS) is applied, the top switch shall also work in 3rd-quad conduction in the inductor current (I_L) commutation (Fig. 6(e), (f)). Similarly, in a half-bridge voltage source inverter, both switches work in the 3rd-quad conduction mode for I_L commutation (Fig. 7(b), (c), (e), (f)). To minimize the conduction loss and optimize system efficiency, it is important to understand the basic physical process in power device 3rd-quad conduction.

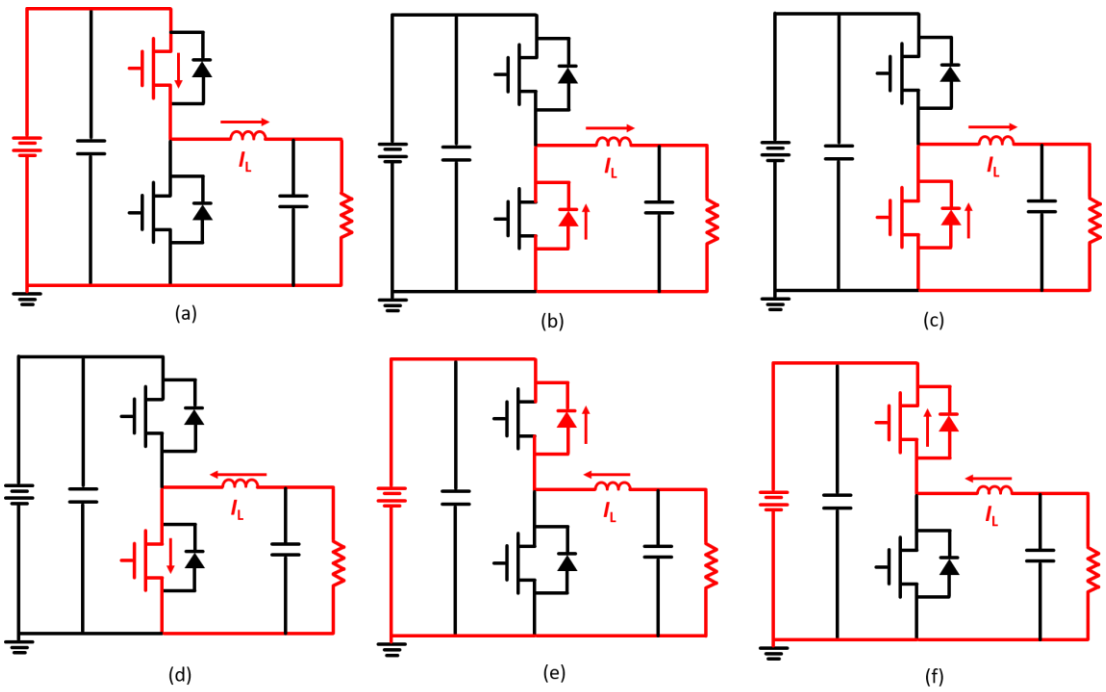

Figure 6. Illustration of different current stage of buck converter with ZVS operation with current direction marked.

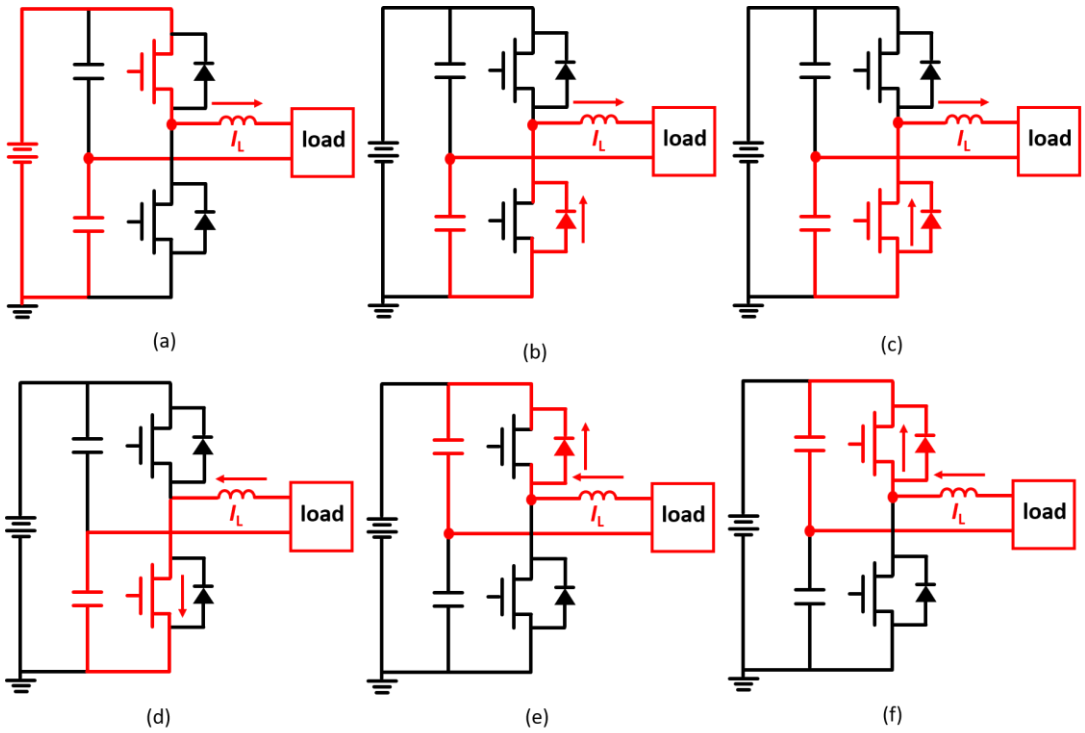

Figure 7. Illustration of different current stages in a half-bridge voltage source inverter with the current direction marked.

2.2 Current Paths in Power MOSFETs

Shown in Fig. 8, in power MOSFETs, there are two current paths during the 3rd-quad conduction, namely the MOS channel path and the body diode path:

The MOS channel path, which is a unipolar path with only electron acts as the carrier, turns on when the gate-to-source bias (V_{GS}) exceeds the device threshold voltage (V_{th}). As shown in Fig. 9(a), it has a zero source-to-drain turn-on voltage, but an increase of differential R_{ON} with the rise of temperature due to enhanced scattering and reduced carrier mobility at high temperatures [44] [45]. The percentage of the carrier mobility drop could be more severe in lighter doped semiconductor material, i.e., more severe in higher voltage rated SiC MOSFETs. The reason behind it is, with different doping concentrations, as the temperature rises, carrier mobility starts to show less dependency on the doping concentration and converges to the same value [44]. As lighter doped SiC shows a higher electron mobility at room temperature compared to heavier doped ones. 10 kV SiC MOSFETs suffer from more R_{ON} increase at higher temperature (around 4-folds increase

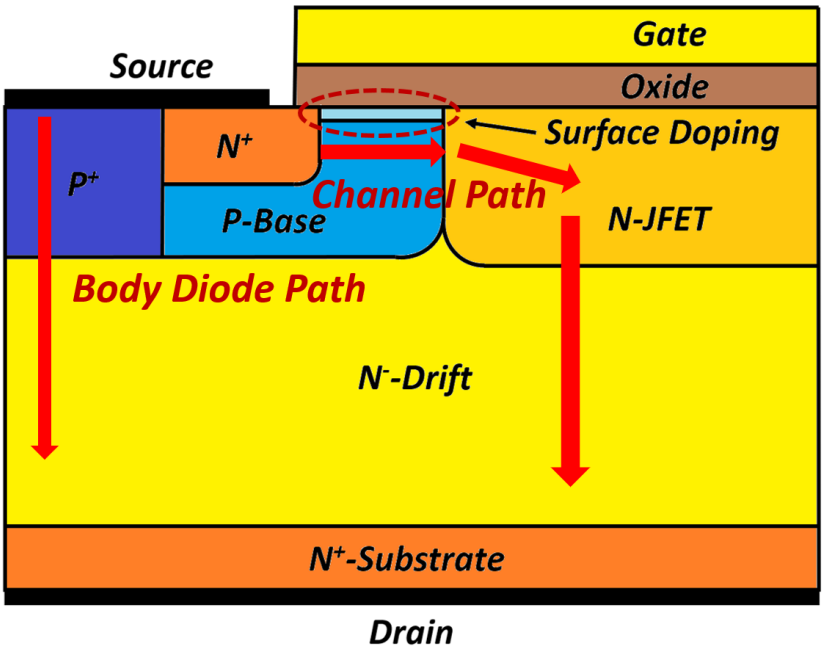

Figure 8. Illustration of the two current paths in SiC power MOSFET.

at 175 °C compared to 25 °C) than 1.2 kV SiC MOSFET (around 1.8-folds increase under same conditions).

The body diode path is a bipolar current path with both electrons and holes conducting current. It turns on when source-to-drain voltage (V_{SD}) is high enough that the voltage drop at the pn junction reaches the built-in potential, the value of which is ~ 3 V in SiC. Despite the decrease of carrier mobility at higher temperatures, the number of generated electron-hole pairs increases with temperature [46]. As the result, the differential R_{ON} of the body diode path increases slowly, or even decreases with increasing temperature, as shown in Fig. 9(b).

The body diode conduction capability is necessary in power applications due to the need of dead time in circuits when both devices in a half bridge are turned-off and the inductive current needs a path to flow. For power devices without a body diode, such as the insulated gate bipolar transistor (IGBT), a Schottky barrier diode (SBD) or pn diode can be put in parallel with the device to provide the 3rd-quad conduction capability with the gate being turned off [47] [48].

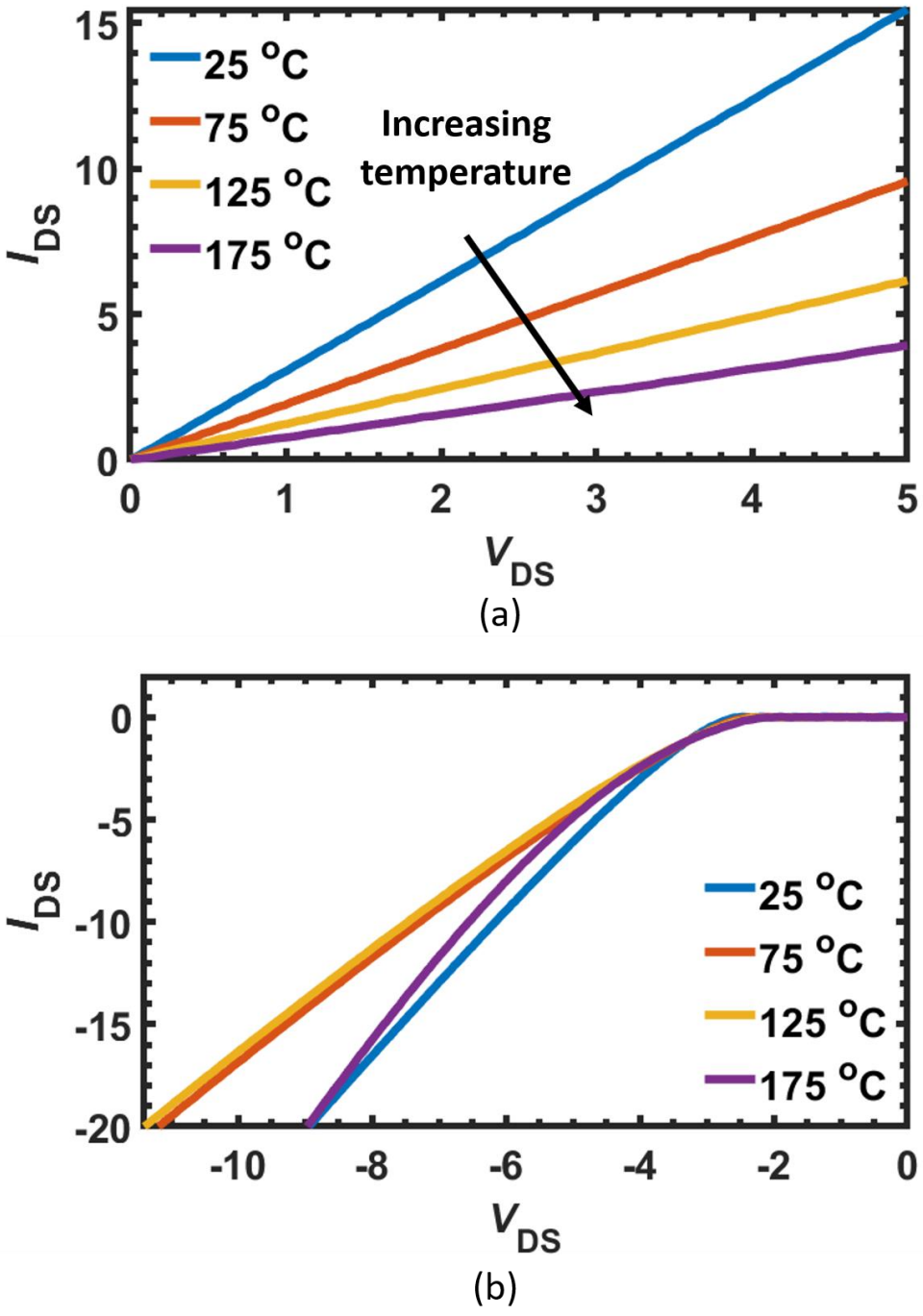

Figure 9. Characterization of 10 kV SiC MOSFET (a) body diode conduction (b) MOS channel conduction at various temperature.

In some applications, SBDs are also put in parallel with SiC MOSFETs to reduce the voltage drop and reverse recovery loss of the body diode [49], as the SBD is a unipolar device with a turn-on voltage of only ~ 1 V. However, this may not be a good design for 10 kV SiC MOSFETs. For 10 kV rated SBDs, the R_{ON} increases drastically with the rising

temperature, showing no superiority in efficiency as compared to using the parasitic body diode [50], while it increases the system volume and cost due to the implementation of an additional device [51]. In this thesis, to make fair comparison and catch the generic physics in the 3rd-quad conduction of different types of SiC MOSFETs, only the standalone SiC MOSFETs are studied, i.e., without an additional SBD in parallel.

2.3 Traditional Gate Bias Control

The MOS channel path has zero turn-on voltage but a high differential R_{ON} at high temperatures, while the body diode path has a relatively high turn-on voltage but smaller differential R_{ON} at high temperatures. To leverage the advantages of both paths, in traditional gate bias control, during the 3rd-quad conduction, the MOS channel is turned-on as long as possible with a small dead time to prevent the arm shoot-through.

This gate control concept was proved to be effective in 1.2 kV SiC MOSFETs. Fig. 10 shows the 3rd-quad characteristics of 1.2 kV commercial SiC MOSFETs (C2MO280120D), at 25 °C and 175 °C, with various V_{GS}. Device characterization was performed on the Keysight B1505A Power Device Analyzer, and the device under test (DUT) was attached

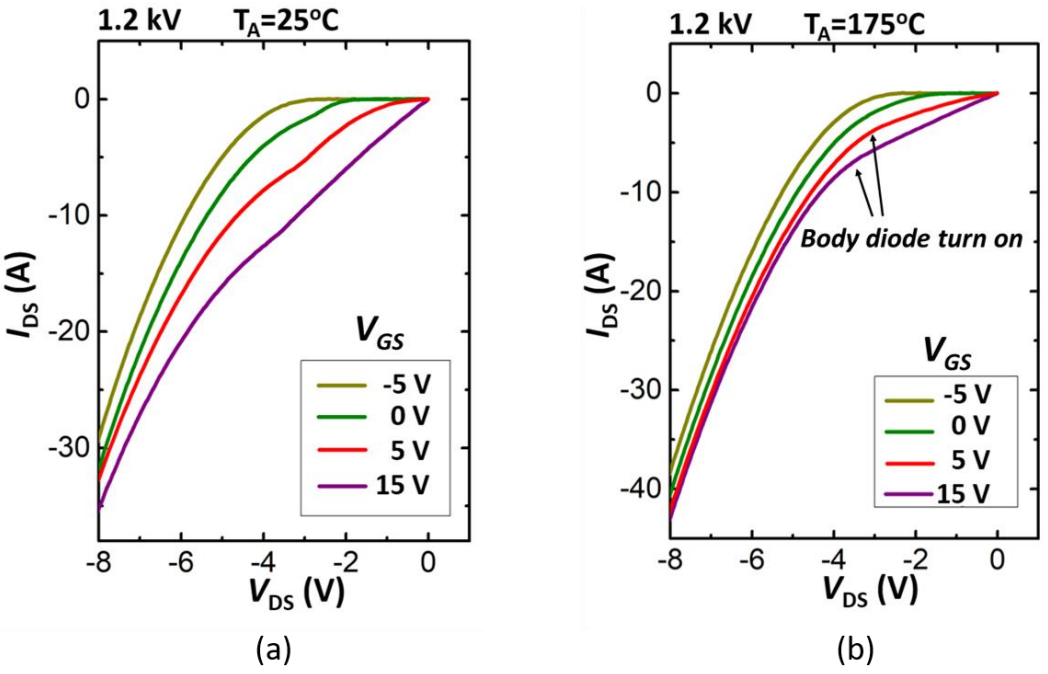

Figure 10. 3rd-quad I-V characterization of 1.2 kV SiC MOSFET at 25 °C and 175 °C.

to a hot plate for temperature control. The temperature was checked by thermocouple and thermal camera. At steady state, the ambient temperature (T_A) could be considered the same as device junction temperature (T_J). From the characteristics, it can be clearly seen at both temperatures, $V_{GS} > V_{th}$ gives a lower 3rd quadrant forward voltage drop (V_F^{3rd}) over the entire V_{SD} range. The key reason is that the body diode also turns on at a positive V_{GS}, and the parallel conduction of both paths results in a lower V_F^{3rd}. The kink in Fig. 10 under V_{GS} of 5 V and 15 V marks the turn-on of the body diode, which occurs at V_{SD} of ~3.5 V. These results are consistent with previous literature reports about the 1.2 kV SiC MOSFET 3rd-quad conduction [52]. However, this straightforward result does not hold for higher rated (e.g. 3.3 kV & 10 kV) SiC MOSFET, which will be discussed in Chapter 3 in this thesis.

Chapter 3: Third quadrant operation of SiC MOSFETs

3.1 Static Characterization

Fig. 11 and Fig. 12 show the 3rd-quad I-V characterization of the industrial 3.3 kV SiC planar MOSFET from GeneSiC and 10 kV SiC planar MOSFET from Wolfspeed, respectively. The characterizations were performed at 25 °C and 175 °C, with V_{GS} from -5 V to 15 V. At 25 °C, their characteristics are consistent with 1.2 kV SiC MOSFETs, where a 15 V V_{GS} gives the smallest V_F^{3rd} in both devices. However, at 175 °C, the I-V curves under -5 V and 15 V V_{GS} show intersections. The intersection occurs ~ 15 V V_{SD} in 3.3 kV MOSFET while ~ 5 V V_{SD} in 10 kV MOSFET. This suggests, especially in 10 kV SiC MOSFET, at high current levels, the lowest V_F^{3rd} is produced by the -5 V V_{GS}.

The turn on of body diode at positive V_{GS} is once again marked with the kink in the I-V curve. The body diode turns on ~ 8 V V_{SD} in 3.3 kV MOSFET while no body diode turn-on is shown in 10 kV SiC MOSFET in both 25 °C and 175 °C. Fig. 13 shows the extracted differential conductance as a function of V_{SD} from 10 kV SiC MOSFET 3rd-quad I-V curve at V_{GS} of -5 V and 15 V at 175 °C. The differential conductance at 15 V V_{GS} keeps constant with V_{SD} and while it is much smaller than the conductance of body diode at V_{SD} over 6 V.

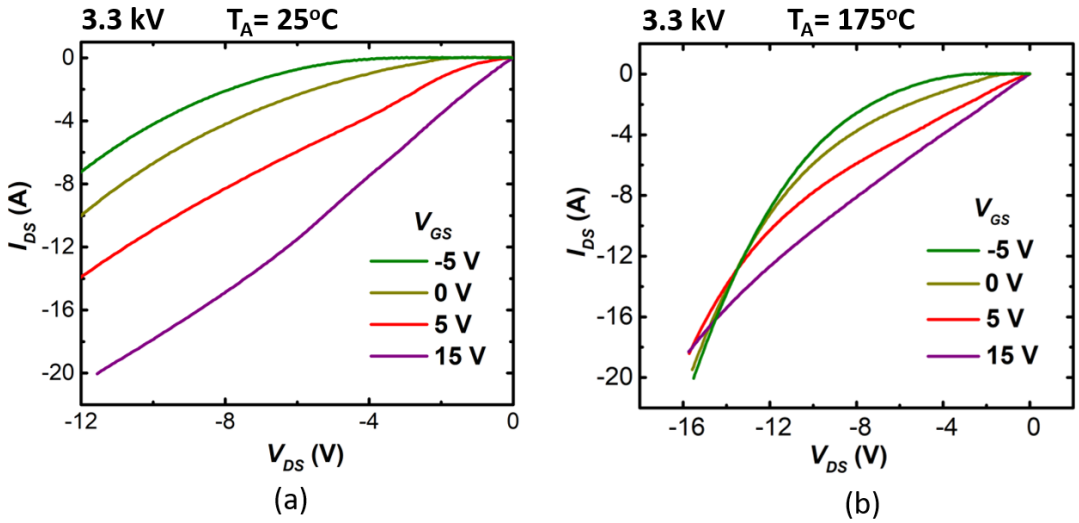

Figure 11. 3rd-quad I-V characteristics of 3.3 kV SiC planar MOSFET.

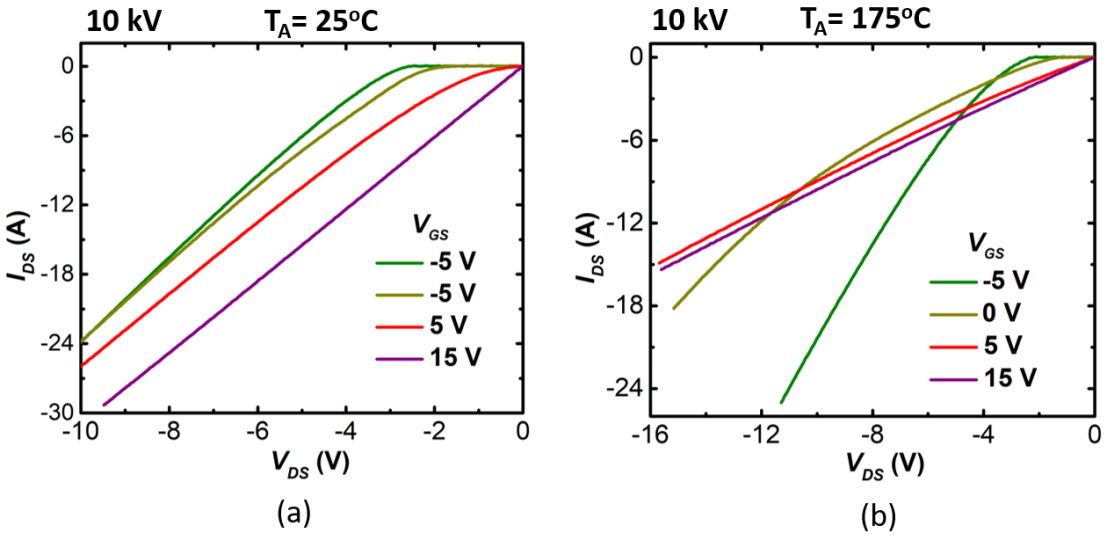

Figure 12. 3rd-quad I-V characteristics of 10 kV SiC planar MOSFET.

This further verifies that the body diode does not turn on in 10 kV SiC MOSFET with $V_{GS} > V_{th}$.

Another notable curve is at V_{GS} of 0 V. Intuitively, at this V_{GS}, the MOS channel is considered turned-off with the body diode conduction only, in other words, the same as the

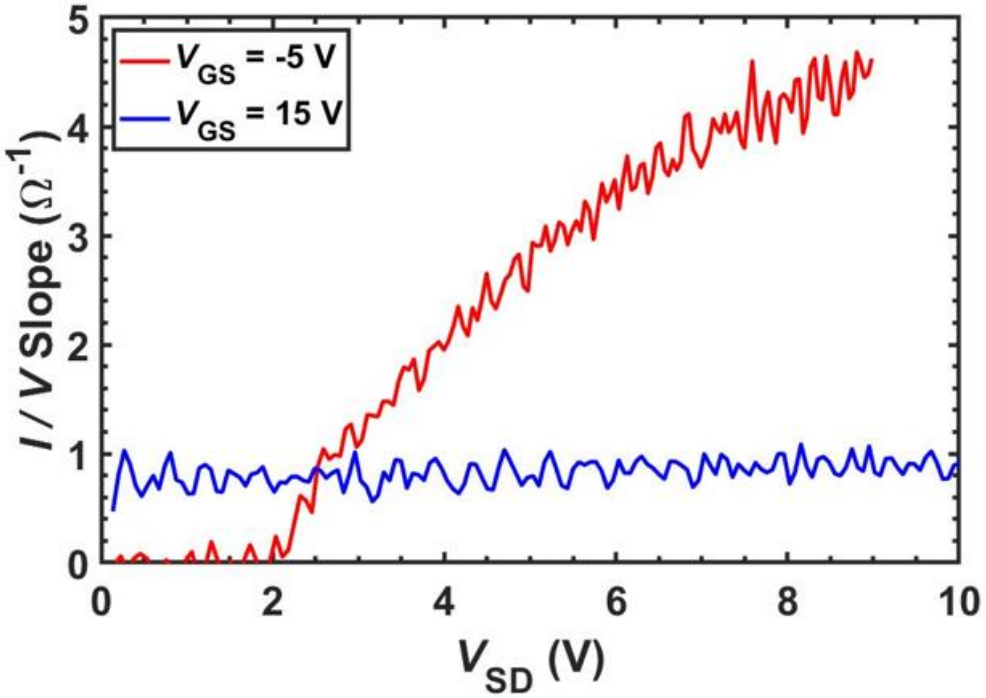

Figure 13. Extracted differential conductance in 10 kV SiC MOSFET 3rd conduction at 175 °C.

case at -5 V V_{GS}. But in Fig. 11(b) and Fig. 12(b), the 0 V V_{GS} curve shows intersections with both -5 V V_{GS} curve and positive V_{GS} curves. All the aforementioned phenomena will be explained in detail in *Section 3.2*.

3.2 Physical Explanation and Simulation

In this section, the 3rd-quad behaviors of SiC planar MOSFETs, regardless of the voltage rating, will be discussed under different V_{GS} conditions, as different device physics are involved.

3.2.1 V_{GS} = -5 V

Fig. 14 illustrates the 3rd-quad operation at a sufficiently negative V_{GS}, where the MOS channel path is completely off with only body diode conducting current. In this case, all V_{SD} falls onto the pn junction, therefore, the body diode turns on when V_{SD} exceeds the knee voltage (V_{knee}), at which the current flow in the pn diode starts to increase rapidly. V_{knee} value almost equals to the built-in potential of SiC pn junction and is mainly

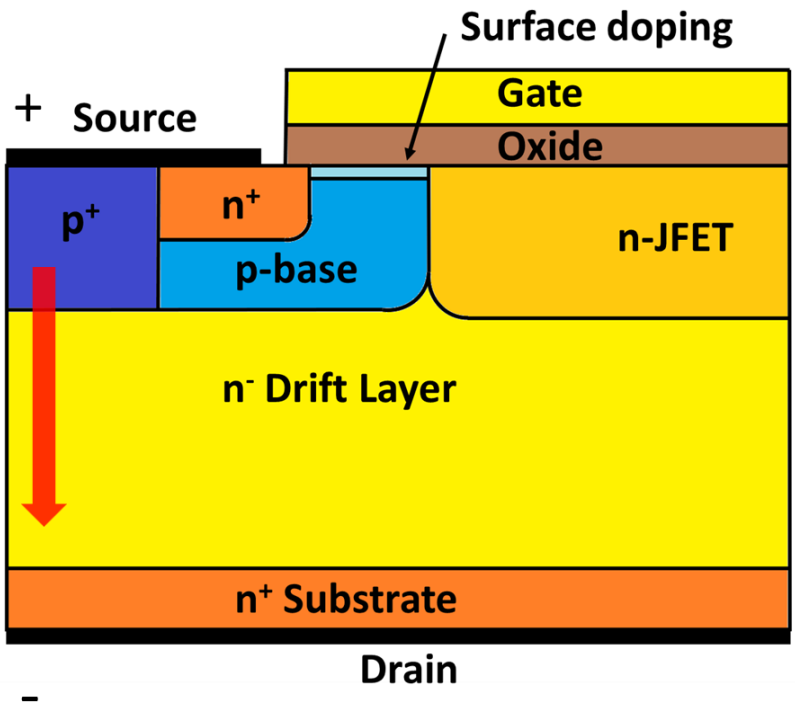

Figure 14. Illustration of the body diode conduction at V_{GS} = -5 V.

determined by the ionized donor concentration (N_D) in the drift region and acceptor concentration (N_A) in the p-base region:

$$V_{knee} \approx (kT/q)\ln(N_D N_A / n_i^2) \quad (3)$$

where n_i is the intrinsic carrier density of SiC.

For a SiC pn junction with not too low N_D and N_A, V_{knee} is close to the bandgap of SiC, i.e., V_{knee}~3 V.

3.2.2 V_{GS} = 15 V

At $V_{GS} > V_{th}$, the MOS channel turns on, and a unipolar electron current flows in the device. This electron current establishes a potential distribution in device following the Ohm's law. As illustrated in Fig. 15, the potential distribution is determined by V_{SD} and the resistance components in the planar MOSFET. The voltage falls onto the body diode pn junction (V_{PN}) is no longer the entire V_{SD}: as the p-base forms an Ohmic contact to the source electrode, V_{PN} is approximately the voltage drop across the MOS channel ($R_{Channel}$)

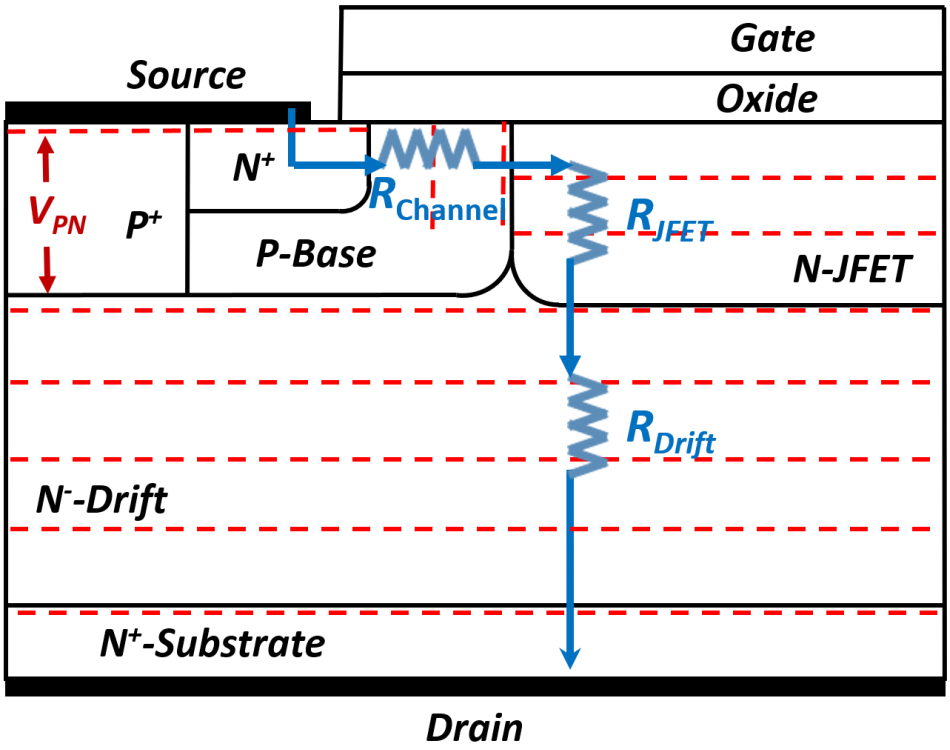

Figure 15. Illustration of the approximate potential distribution established by the MOS channel current.

and the JFET (R_{JFET}) region. If ignoring the contact and substrate resistance, as well as the resistance from the metal and wire bond in package, V_{PN} can be calculated as:

$$V_{PN} \approx V_{SD}(R_{Channel} + R_{JFET})/R_{ON} \tag{4}$$

where

$$R_{ON} \approx R_{Channel} + R_{JFET} + R_{Drift} \tag{5}$$

Defining the body diode turn-on voltage as $V_{BD\text{-}on}$, with channel turned-on, V_{BD-on} can be estimated by the condition that V_{PN} exceeds the V_{knee} of the pn junction ($V_{PN} \geq V_{knee}$):

$$\begin{aligned} V_{BD-on} &\approx V_{knee}R_{ON}/(R_{Channel} + R_{JFET}) \\ &\approx V_{knee}[1 + R_{Drift}/(R_{Channel} + R_{JFET})] \end{aligned} \tag{6}$$

From equation (6), it can be concluded that, due to the potential distribution established by the unipolar current, a voltage higher than V_{knee} is required to turn on the body diode with the MOS channel conduction.

Now the experimental results in Fig. 11 and Fig. 12 can be well explained. In SiC MOSFETs, the blocking voltage is mainly sustained by the thick and lightly doped drift region. With the increase of breakdown voltage, the resistance of an optimal drift region also scales up, usually following a power law as described by equation (1). On the other hand, $R_{Channel}$ and R_{JFET} do not change much with device voltage rating. Therefore, the proportion of R_{Drift} in R_{ON} increases with the increasing voltage rating, resulting in a higher $V_{BD\text{-}on}$ (or delayed body diode turn-on) as predicted by equation (6). This explains why 3.3 kV MOSFET has a $V_{BD\text{-}on}$ of ~ 9 V. In 10 kV SiC MOSFET, since $R_{Drift} >> R_{Channel} + R_{JFET}$, $V_{BD\text{-}on}$ is so large that the body diode will not turn on over the entire V_{SD} safe-operating range up to 16 V.

It should be noted that equation (6) only gives a rough approximation of $V_{BD\text{-}on}$. Taking the uneven potential distribution inside the device cell in consideration, a more accurate $V_{BD\text{-}on}$ model is discussed in ***Section 3.3***.

In the aforementioned comparison between the MOS channel path and body diode path in ***Section 2.2***. The body diode path has high turn-on voltage but smaller differential R_{ON} at high temperatures, while the MOS channel path has a zero turn-on voltage but higher

differential R_{ON} at high temperature. At $V_{GS} > V_{th}$, in 1.2 kV devices, since $V_{BD\text{-}on}$ is small (~3.5 V), the body diode turns on before the I-V curve intersects the curve with negative V_{GS}, at both 25 °C and 175 °C, enabling the current conduction in both paths. Therefore, the V_F^{3rd} at V_G = 15 V is always lower than the V_F^{3rd} at V_G = -5 V. In 3.3 kV and 10 kV MOSFETs, the delayed body-diode turn-on leads to a larger differential resistance at 175 °C, which offsets the benefits of the zero turn-on voltage at high current levels. As a result, the I-V curves at V_{GS} = 15 V and V_{GS} = -5 V intersects. At high current levels and high temperatures, a lower V_F^{3rd} is provided by a -5 V V_{GS}.

3.2.3 V_{GS} = 0 V

At V_{GS} = 0 V, there is no n-type inversion layer in the p-base, in other words, the MOS channel is turned off. However, an additional "surface path" is formed in 3rd-quad conduction due to the depletion in the p-base underneath the gate oxide. Fig. 16 shows the illustration of the energy band diagram along the cutline of the metal-oxide-semiconductor (MOS) structure: the valance band (E_V) and conduction band (E_C) in the p-type SiC bend down at the interface due to the work function difference between poly silicon gate and p-type SiC. This band bending leads to a smaller built-in barrier in the pn junction near the

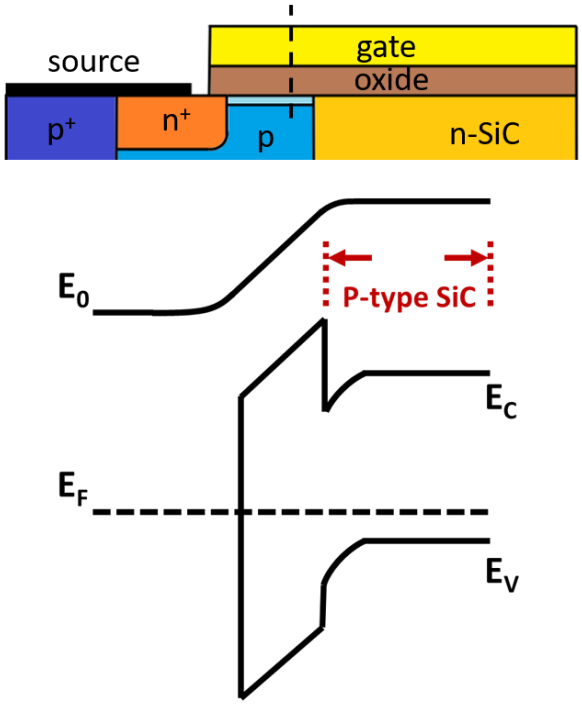

Figure 16. Energy band diagram of the MOS structure.

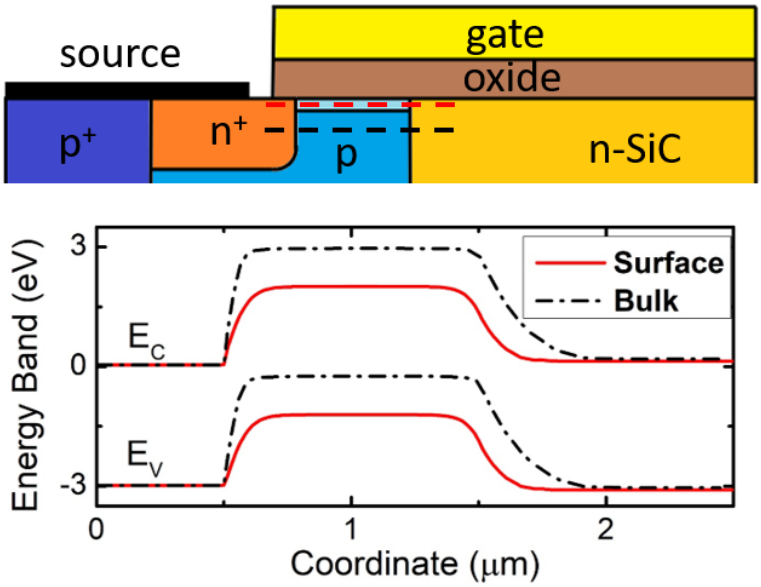

Figure 17. Simulated energy band diagram near the surface and in the bulk SiC.

surface compared to the pn junction in bulk SiC. Fig. 17 shows the simulated band diagram along two cutlines: the npn structure near the surface, and that in the bulk p-base, revealing a ~ 1 V lower barrier in the surface npn junction.

The lower barrier at the surface junction leads to a ~ 1 V smaller turn-on voltage in V_{GS} = 0 V as compared to V_{GS} = 5 V, as shown in Fig. 10, 11 and 12. The conduction of the surface channel is quite similar to a npn BJT: with V_{PN} exceeding the barrier between p-base and n-JFET at the surface, the pn junction turns on with hole current injecting into the n-JFET region and electron current injecting into the p-base. The electrons then drift through the p-base and are collected by the n-source.

The formation of this "surface channel" has also been discussed in [53] [54] [55]. When V_{GS} decreases below zero, the V_{knee} of the surface channel gradually increases due to the weakened MOS depletion. At $V_{GS} \leq$ -5 V, as the surface p-SiC region changes from the depletion mode into accumulation mode, the V_{knee} of the surface channel is no longer smaller than the body diode. The body diode then dominates the 3rd-quad conduction.

Once this npn surface channel turns on at V_{GS} = 0 V, the current establishes the potential distribution following the Ohm's law within the device, in the same way as the MOS channel does at $V_{GS} > V_{th}$. As a result, V_{BD-on} is determined by (6) and becomes much larger than the built-in potential in high-voltage SiC MOSFETs. Once again, the

intersection is shown between the I-V curves at V_G = 0 V and V_G = -5 V in Fig. 11 and 12. Note that the differential R_{ON} at V_{GS} = 0 V are smaller than the one at V_{GS} = 15 V at high temperatures. This is because the npn channel has a bipolar nature, and its resistance is lower than the unipolar MOS channel at high temperatures. The I-V curves of 3.3 kV and 10 kV MOSFETs at V_{GS} = 0 V and V_{GS} = 15 V also show intersections at 175 ^{o}C.

3.2.4 TCAD Simulation Verification

To validate our theories on the 3rd-quad conduction of SiC MOSFETs including the delayed body-diode turn-on and the formation of the surface channel, physics-based TCAD simulations were performed in Silvaco Atlas. 3.3 kV SiC MOSFET was chosen as it showed a prominent higher V_{BD-on} (~8 V) as compared to the V_{knee} of pn junction (~3 V) but still within the normal V_{SD} operating range.

The physical models were based on the ones described in [56] [41] [57]. The conductivity modulation, velocity saturation, temperature-dependent carrier mobility, and incomplete dopant ionization were accounted for in the simulation models. The simulated device model was calibrated to the experimental *I-V* curves in the first and third quadrants.

Fig. 18-20 show the simulated current density distribution in the 3rd-quad conduction of 3.3 kV SiC MOSFETs at V_{GS} of -5 V, 5 V and 0 V, respectively. As shown in Fig. 18, at V_{GS} of -5 V and V_{SD} of 4 V, the current flows entirely through the body diode. Fig. 19 shows the simulated current density at V_{GS} of 5 V (> V_{th}). At V_{SD} of 4 V (higher than the

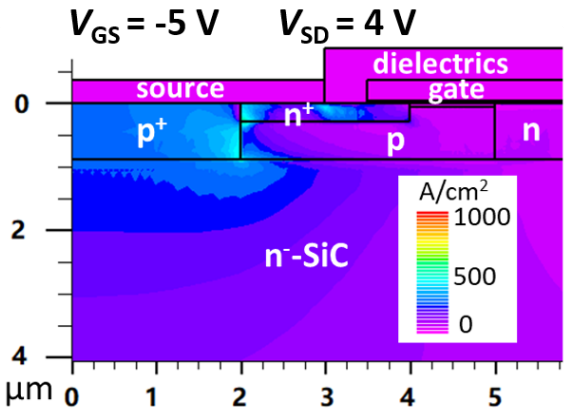

Figure 18. Simulated current density distribution at -5 V V_{GS}.

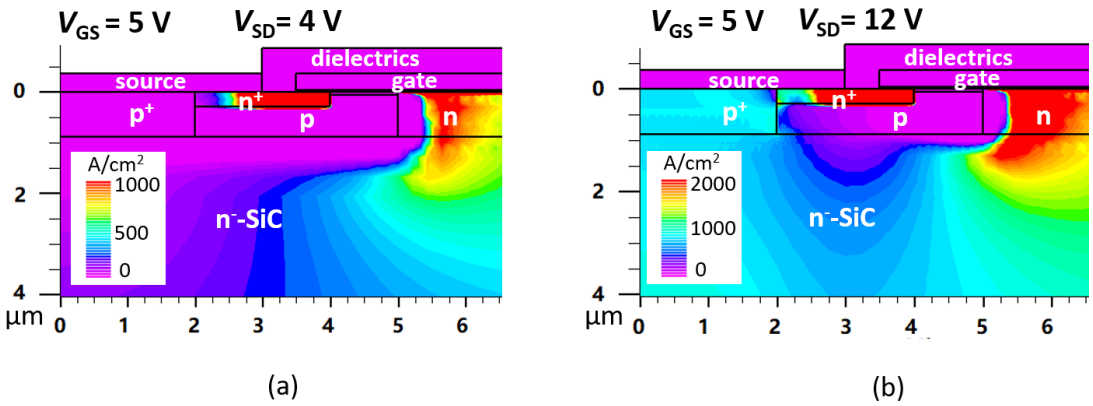

Figure 19. Simulated current density distribution at 5 V V_{GS}.

built-in potential), the body diode does not turn on, validating the delayed body diode turn-on. At V_{SD} of 12 V, the body diode finally turns on, and shows parallel conduction through the MOS channel and the body diode. Fig. 20 shows the simulated current density at V_{GS} of 0 V. As shown in Fig. 20(a), the npn surface channel turns on at V_{SD} of 2.5 V and the body diode is still off. After this surface channel turns on, at V_{SD} of 4 V, the body diode keeps off (Fig. 20(b)), validating the delayed body diode turn-on due to the potential distribution set by the conducting surface channel. At V_{SD} of 12 V, the body diode is on, and the current shows parallel conduction in both channels (Fig. 20(c)). These simulation results are consistent with experimental results shown in Fig. 11 and validat our theoretical explanations.

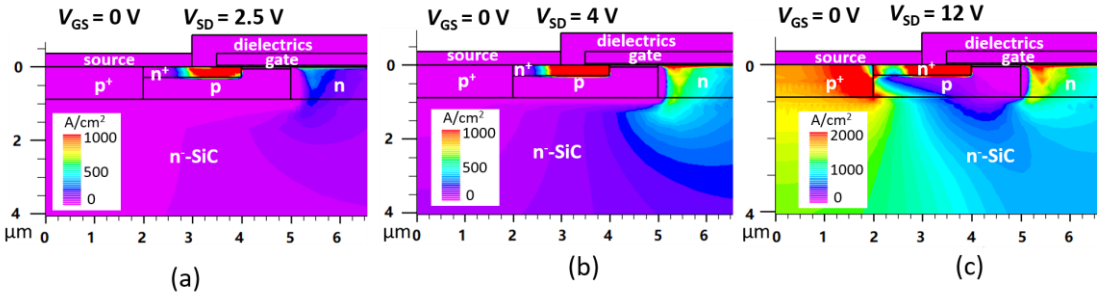

Figure 20. Simulated current density distribution at 0 V V_{GS}.

3.3 $V_{BD\text{-}on}$ Modeling

The objective of this section is to develop easy-to-use analytical models to describe and predict the V_F^{3rd} of SiC planar MOSFETs with different rated voltages, with the focus on a sufficiently negative V_{GS} (e.g., -5 V) and a $V_{GS} > V_{th}$, the two most common gate-bias controls in power converters. While the V_F^{3rd} at a negative V_{GS} is merely the forward voltage drop of the body diode, the V_F^{3rd} at $V_{GS} > V_{th}$ is much more complicated. The key to modeling V_F^{3rd} at $V_{GS} > V_{th}$ is obtaining V_{BD-on} with given parameters, either from the static characterization or from the datasheet. To this end, the V_{BD-on} model based on (6) is first extended to establish a correlation between V_{BD-on} and the device voltage rating (or breakdown voltage).

3.3.1 $V_{BD\text{-}on}$ Estimation

According to the theories developed in ***Section 3.2***, an equivalent circuit model for the 3rd-quad current conduction in planar MOSFETs was developed, as shown in Fig. 21. All the resistance components listed are the specific values ($\Omega \cdot cm^2$) normalized with respect to the device die size or active region. Fig. 22 shows the simulated potential distribution within the device at $V_{GS} > V_{th}$. When compared to the approximate model shown in Fig. 15, the equipotential lines originated from the pn junction penetrating into the drift region

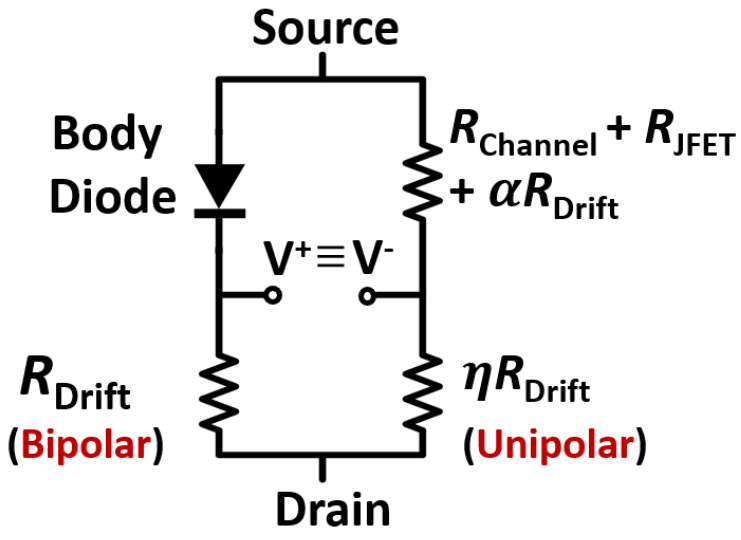

Figure 21. Equivalent circuit model describing 3rd-quad conduction.

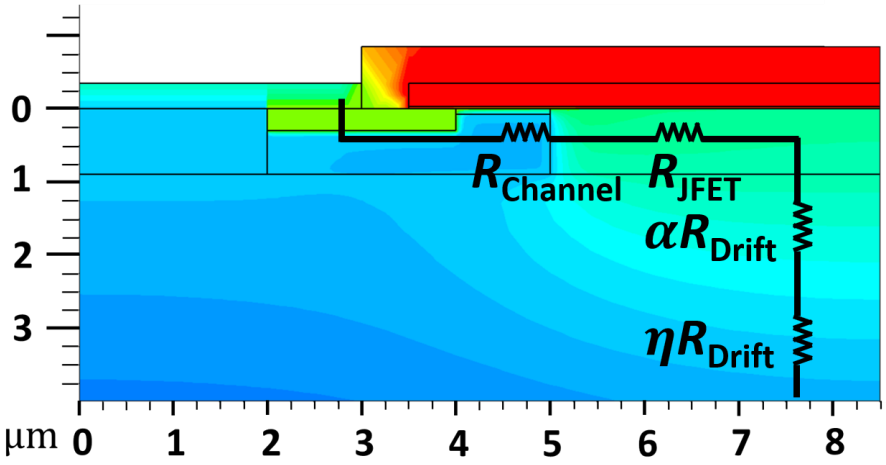

Figure 22. Simulated potential distribution in MOSFET 3rd-quad conduction with positive V_{GS}.

rather than extending laterally along the lower boundary of the JFET region. This is due to the current spreading effect and suggests that a portion of R_{Drift} (defining the portion as α) needs to be accounted for when calculating the voltage drop across the pn junction (i.e., V^+ and V^- in Fig. 21). Equation (6) can be rewritten as

$$V_{BD-on} = V_{knee} R_{ON} / (R_{Channel} + R_{JFET} + \alpha R_{Drift}) \quad (\alpha < 1) \tag{7}$$

Defining $\eta = 1 - \alpha$, (7) is transformed into

$$\begin{aligned} V_{BD-on} &= V_{knee} / [(R_{Channel} + R_{JFET} + \alpha R_{Drift}) / R_{ON}] \\ &= V_{knee} / [(R_{ON} - \eta R_{Drift}) / R_{ON}] \\ &= V_{knee} / (1 - \eta R_{Drift} / R_{ON}) \qquad (\eta < 1) \end{aligned} \tag{8}$$

In (8), V_{knee} and R_{ON} can be extracted from the datasheet or the static I-V characteristics. To separate R_{Drift} from R_{ON}, all the three major components of R_{ON} were modeled as follows:

Assuming the MOSFET operates in the linear region, $R_{Channel}$ is proportional to the reciprocal of the gate overdrive

$$R_{Channel} \propto 1/(V_{GS} - V_{th}) \tag{9}$$

where V_{th} is the threshold voltage extracted from the device datasheets or static transfer characteristics.

R_{JFET} depends on the geometry and doping concentration of the JFET region [58] and usually is not disclosed in the datasheets. As R_{JFET} is not dependent on the device voltage rating and is usually a very small component in the R_{ON} of high-voltage devices, we approximate R_{JFET} as a constant value:

$$R_{JFET} = cons. \tag{10}$$

Note (10) is neither the most accurate assumption but nor a bad one, particularly for devices from the same manufacturer. Even for the devices from different manufactures, the reported specific R_{JFET} in the literature shows variations in a quite limited range. The reported JFET region designs in 1.2 kV [59] [60], 3.3 kV [61] [62], 10 kV [63] [64], and 13 kV [65] SiC planar MOSFETs have a similar JFET depth of 0.7~1 μm, a JFET width to cell pitch ratio of 0.2~0.3, and a doping concentration of 1~2×10^{16} cm^{-3}. Based on the range of these parameters, the resulted variations in the specific R_{JFET} of devices with different voltage ratings are usually negligible as compared to the R_{Drift} which increases significantly with the increased voltage rating.

The specific resistance of the ideal unipolar drift region increases with the square of V_B [5]. The drift region resistance in the state-of-the-art high-voltage SiC MOSFETs is very close to this theoretical limit [12]. Therefore, R_{Drift} can be approximated as

$$R_{Drift} \propto V_B^2 \tag{11}$$

where the V_B for 1.2-10 kV-rated SiC MOSFETs can be extracted from [12] or simply approximated with a 20% margin over the device voltage rating.

Finally, the correction factor η was tuned to match the experimental $V_{BD\text{-}on}$ extracted at different V_G for each device. For example, as shown in Fig. 23, with a η of 0.80, the modeled $V_{BD\text{-}on}$ of 3.3 kV SiC MOSFETs agrees well with experiment over a wide range of V_{GS}, whereas no correction (η = 1) leads to overestimation in $V_{BD\text{-}on}$. The η values fitted from experimental data for 1.2 kV and 3.3 kV SiC MOSFETs were also validated with the simulated potential distribution in each device.

Table 1 summarizes the estimated $V_{BD\text{-}on}$ from the above analytical models for 1.2 kV, 3.3 kV, and 10 kV devices. The modeled $V_{BD\text{-}on}$ agrees with the experimental data for 1.2

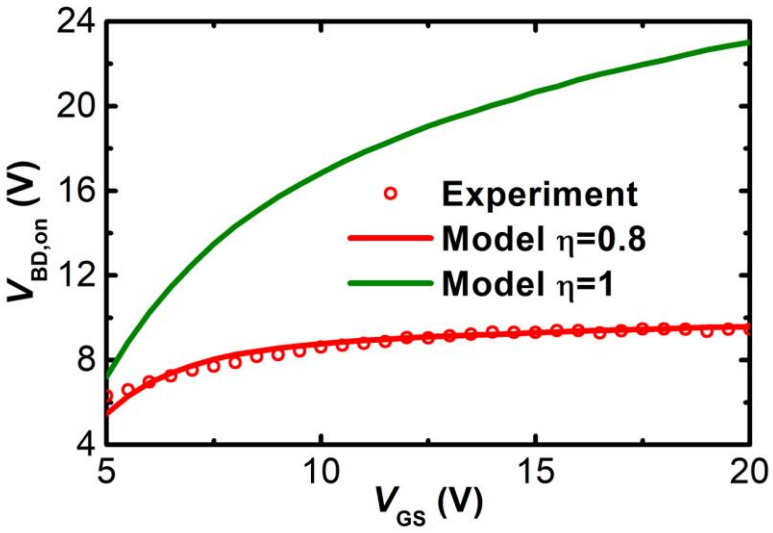

Figure 23. Estimated $V_{BD\text{-}on}$ with different correction factor values.

kV and 3.3 kV MOSFETs. In addition, the model predicts a $V_{BD\text{-}on}$ of 28 to 66 V in 10 kV MOSFETs at V_{GS} of 5-15 V, by using a $\eta \approx 0.97$ which is extracted from the simulated potential distribution in 10 kV MOSFETs. This is consistent with the experimental results shown in Fig. 12 that the body diode does not turn on up to V_{SD} of 16 V. The modeled $V_{BD\text{-}on}$ suggests that, once the MOS channel is on, the body diode of 10 kV MOSFETs will never turn on under practical 3rd-quad conditions. Hence, only one current path can be selected in the model shown in Fig. 21. Note this high $V_{BD\text{-}on}$ is expected for the 10 kV planar MOSFETs with different designs of the channel and JFET regions (e.g., doping concentration and geometries). The fundamental root cause of the high $V_{BD\text{-}on}$ is the much larger R_{Drift} as compared to the channel/JFET resistances. As a very thick and lightly doped

Table 1. $V_{BD\text{-}on}$ FROM EXPERIMENT AND MODELS.

Voltage Rating (kV)	η	V_{GS} (V)	$V_{BD\text{-}on}$ (exp) (V)	$V_{BD\text{-}on}$ (model) (V)
1.2	0.6	5	3.17	3.30
		10	3.20	3.32
		15	3.30	3.36
3.3	0.8	5	6.32	5.47
		10	8.62	8.77
		15	9.31	9.31
10	0.97	5	N/A	28.14
		10	N/A	52.12
		15	N/A	65.86

drift region is always required for high voltage MOSFET, a very high $V_{BD\text{-}on}$ is expected to be universal in all 10 kV SiC planar MOSFETs instead of being manufacturer specific.

It can be seen in Table 1 that the fitted η value increases with the device voltage rating, which shows its physical significance. The equipotential lines penetrating from the pn junction into the drift region varies very little in the devices with different voltage ratings, while the R_{DRIFT} increases with the device voltage rating. This leads to a smaller α and a closer-to-unit η for higher-voltage devices.

It is important to note that existing SPICE circuit models for SiC planar MOSFETs simply put MOSFET in parallel with the body diode, which do not capture the impact of the MOS channel conduction on the body-diode turn-on. The model proposed in the thesis provides a more accurate description of the 3rd-quad behavior of SiC MOSFETs and can be easily implemented in circuit-based simulations.

3.3.2 Temperature-Dependent *I-V* Characteristics

The discussions in ***Section 3.2*** suggest the importance to develop a datasheet-driven V_F^{3rd} model for high-voltage SiC MOSFETs, which can be used to determine the optimal V_{GS} control to minimize the 3rd-quad conduction loss at a given I_{SD} and temperature (T). In this section, we develop the V_F^{3rd} model for Wolfspeed's third-generation 10 kV SiC MOSFETs as a case study, which also lays a foundation for the converter test in ***Chapter 4*** of this thesis.

For the model calibration, static 3rd-quad characterizations were first carried out from 25 ℃ up to 175 ℃ with a 25 ℃ step at V_{GS} of 15 V and -5 V. At V_{GS} of 15 V, as illustrated in *Section 3.3.1*, the current completely went through the MOS channel and the device R_{ON} is dominated by R_{Drift}. Given the unipolar nature, the temperature dependence of R_{Drift} is mainly induced by electron mobility degradation at high temperatures, and R_{Drift} can be modeled as:

$$R_{Drift}(V_{GS} > V_{th}) = R_{Drift,25}[(T + 273)/298]^K \quad (12)$$

where $R_{Drift,25}$ is the R_{Drift} at 25 ℃, and K is a temperature coefficient. The value of K appears to vary with devices according to [66] [67]. As shown in Fig. 24, K of Wolfspeed 10 kV SiC MOSFET tested in this work is fitted to be around 3.2 in the V_{GS}=15 V curve.

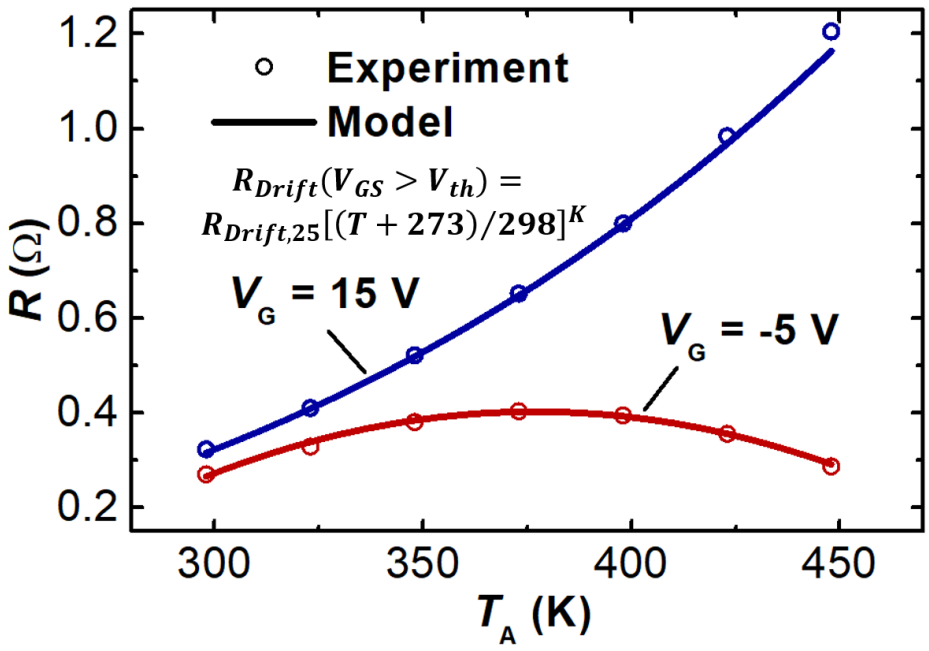

Figure 24. Fitting of resistance of the conduction of MOS channel and body diode.

At V_{GS} of -5 V, the current goes through the body diode. The forward voltage drop of the body diode can be described as

$$V_{3rd}^{F}(V_{GS} = -5\,V) = V_{knee} + R_{DIODE} I_{SD} \tag{13}$$

where R_{DIODE} represents the total differential resistance of the bipolar current path through the body diode and drift region. Significant conductivity modulation has been reported in the body diode of 10 kV SiC MOSFETs [68]. Due to the bipolar nature, R_{DIODE} does not increase monotonically with temperature. At high temperatures, on the one hand, conductivity modulation is enhanced due to the increased lifetime of the injected holes, the decreased V_{knee} of the pn junction, and the increased acceptor ionization in p-base [69]; on the other hand, the carrier mobility decreases due to the increased phonon scattering. As shown in Fig. 24, a quadratic polynomial equation can well fit the temperature dependence of R_{DIODE} with a peak R_{DIODE} at ~100 °C.

The temperature-dependent 3rd-quad I-V characteristics of 10 kV SiC planar MOSFET can be well reproduced based on (12) and (13), as shown in Fig. 25. Below 75 °C, within the safe-operating range of V_{SD} and I_{SD}, no intersection shows up between V_{GS} of -5 V and 15 V. The crossing point (at ~15 A) first appears at 100 °C and continues to drop at higher

temperatures. At 175 °C, the early intersection at 4 A indicates that a negative V_{GS} control is preferred for most of I_{SD} operation.

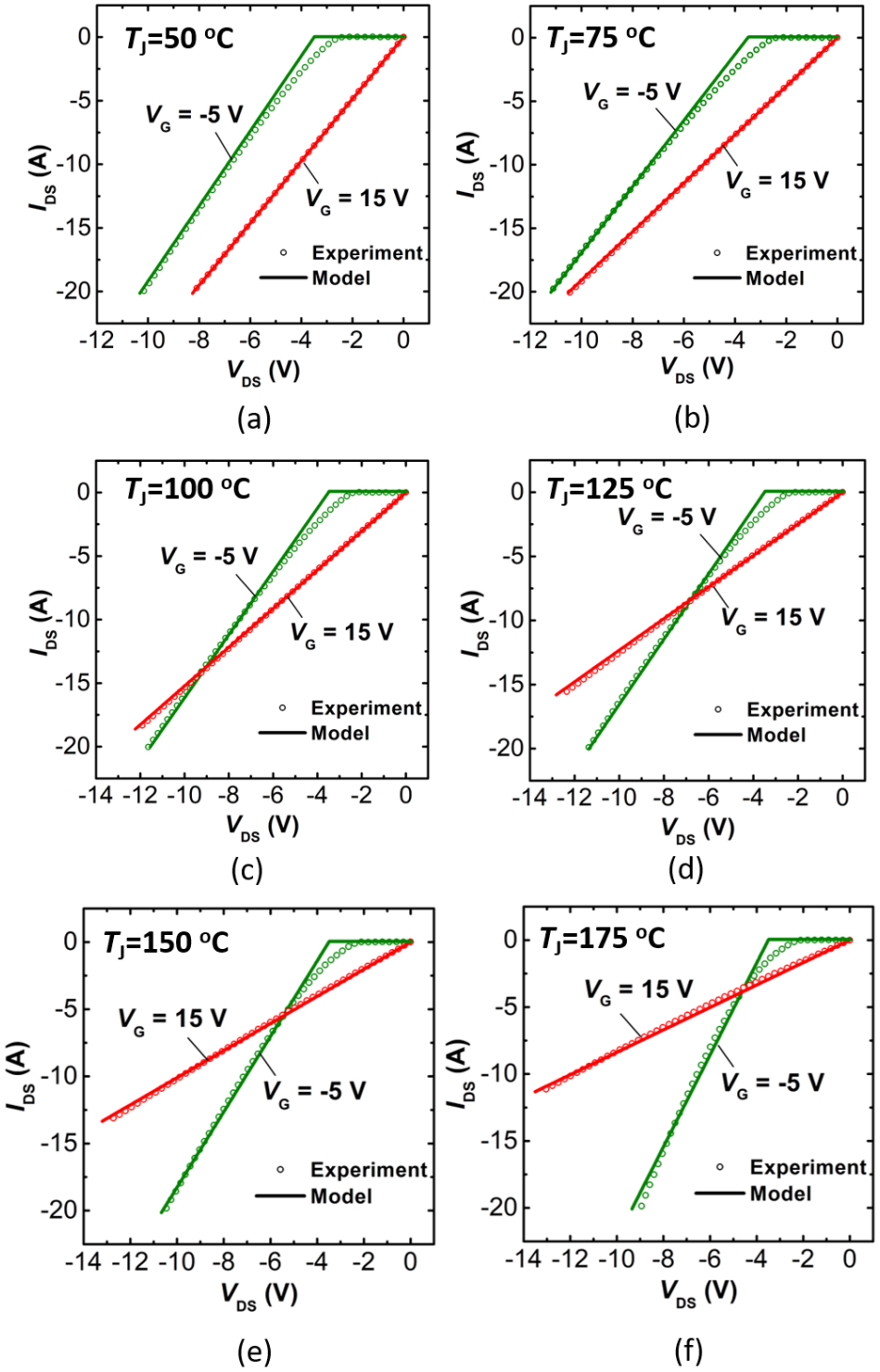

Figure 25. Experimental and modeled 3rd-quad I-V characteristics of 10 kV SiC MOSFETs under various temperatures.

3.4 Further Discussion on Trench MOSFETs

Compared to the planar MOSFET, trench MOSFETs allow for a higher gate density and smaller $R_{on,sp}$ with similar voltage ratings. Up to now, SiC trench MOSFETs have been commercialized at the voltage class of 1.2 kV. Based on the device physics unveiled for planar MOSFETs, in this section. the competing current sharing between body diode and MOS channel in the 3rd-quad conduction of trench MOSFETs will be discussed. The standard trench MOSFET structure and two commercial 1.2 kV trench MOSFETs were investigated. The discussions in this section would also be useful for the design and application of future SiC trench MOSFETs with higher voltage ratings.

3.4.1 Standard Trench MOSFETs

Fig. 3 shows the standard structure of a SiC trench MOSFET. As discussed before, there is no JFET region in this structure, at $V_{GS} > V_{th}$, the body diode turn-on voltage can be written based on (6)

$$V_{BD-on} = V_{knee}(R_{Channel} + R_{Drift})/R_{Channel}$$
$$= V_{knee}[1 + R_{Drift}/R_{Channel}] \quad (14)$$

From the comparison between (6) and (14), V_{BD-on} of trench MOSFETs is expected to be much higher than that of planar MOSFETs with similar voltage rating, due to the lack of R_{JFET} and a smaller $R_{Channel}$ (as a consequence of the higher channel density). This implies that the body diode may not turn on over the entire V_{SD} safe-operating range, and the $V_{GS} > V_{th}$ control would lead to a completely unipolar 3rd-quad conduction.

3.4.2 Commercial Trench MOSFETs

The device structures of commercial SiC trench MOSFETs deviate from the standard one. As discussed in ***Chapter 1.2***, Rohm's third-generation trench MOSFETs feature a double trench (DT) structure [13] [70] [71] (Fig. 4(a)) Infineon's CoolSiC™ features an asymmetric structure with a deep P^+ emitter [72] [73] (Fig. 4(b)) The common feature in these two structures that differs from the standard one is a source-connected P^+ region penetrated deeply into the drift region, beyond the bottom of the trench gate. This structure is designed mainly to shield the trench gate from the high electric field in the reverse biases.

As the pn junction between the P^+ emitter and the drift region are deeper than the end of the MOS channel, this deep P^+ design would induce an effective JFET region. As a result, when calculating the V_{BD-on}, an effective R_{JFET} needs to be added in (14), making V_{BD-on} equation the same as (6).

Fig. 26 and Fig. 27 shows the 3rd-quad I-V characteristics of commercial 1.2 kV SiC trench MOSFETs from Rohm (SCT3080KL, 31 A rated) and Infineon (IMZ120R045M1, 52 A rated), respectively, at 25 ºC and 175 ºC. At V_{GS} of -5 V and 15 V. At V_{GS} of -5 V, the 3rd-quad conduction is through the body diode in both devices. As shown in Fig. 26, at V_{GS} of 15 V, no body-diode turn-on is observed at V_{SD} up to 10 V in Rohm's DT MOSFET, and therefore, the 3rd-quad characteristics are symmetric to the 1st-quad characteristics (including the current saturation at high V_{SD}). This implies a $V_{BD\text{-}on}$ higher than 10 V in Rohm's devices. As shown in Fig. 27, at V_{GS} of 15 V, the body diode turns on at V_{SD} of ~7 V in Infineon's devices. The larger $V_{BD\text{-}on}$ of Rohm's devices compared to the one of Infineon's is believed to be due to the wider effective JFET region in the device unit-cell (~3 µm in Rohm's device versus ~1 µm in Infineon's device [74]) and therefore a smaller effective R_{JFET}. It should be noted that $V_{BD\text{-}on}$ of Infineon's 1.2 kV trench MOSFETs (~7

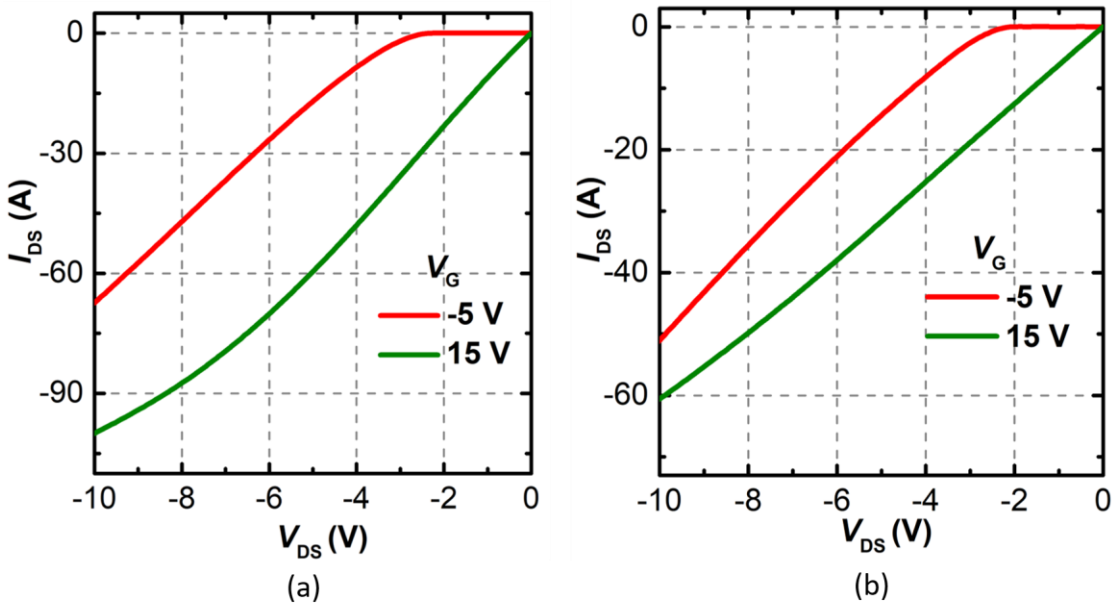

Figure 26. 3rd-quad I-V characteristics of the Rohm's double-trench SiC MOSFET.

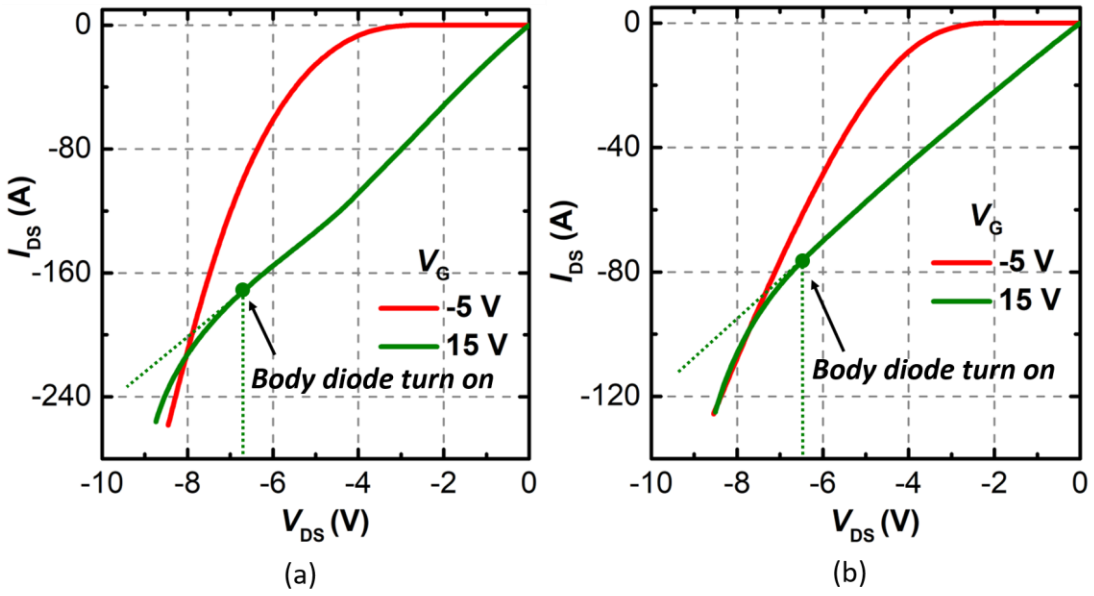

Figure 27. 3rd-quad I-V characteristics of Infineon/s asymmetric CoolSiC™ SiC MOSFET.

V) is larger than the 1.2 kV planar MOSFETs (~3.5 V, as shown in Fig. 10), due to the inherently smaller $R_{Channel}$ and effective R_{JFET} in trench MOSFETs.

In summary, although the 3rd-quad characteristics of SiC trench MOSFETs show a dependence on specific device structures, their $V_{BD\text{-}on}$ is generally expected to be larger than the one of the planar MOSFETs with the same voltage rating. While V_{GS} of 15 V generally gives smaller V_F^{3rd} for 1.2 kV SiC trench MOSFETs in the normal current operation range, the 3rd-quad conduction of future higher-voltage (e.g., 2.5 kV, 3.3 kV, etc.) SiC trench MOSFETs could be similar to that of 10 kV planar MOSFETs. A negative V_{GS} is probably optimal to control the 3rd-quad conduction of higher-voltage SiC trench MOSFETs at high junction temperatures and high load currents.

Meanwhile, if $V_{GS} > V_{th}$ is preferred in some applications, a larger effective R_{JFET} would facilitate to reduce $V_{BD\text{-}on}$ and V_F^{3rd}, which, however, increases the total R_{ON}. For $V_{GS} > V_{th}$, there will be a trade-off between the device R_{ON} and the 3rd-quad conduction loss. This trade-off needs to be carefully considered in the design of future high-voltage trench MOSFETs.

Chapter 4: Power Circuit Test

4.1 Dynamic Discharging Test

The purpose of this test is to capture the dynamic 3rd-quad R_{ON} of 10 kV SiC MOSFET in a power circuit. Fig. 28 shows the inductor discharging test circuit schematic and test setup. A 10 kV SiC MOSFET half-bridge module from Wolfspeed was used. During the test, the top switch was turned-on first to charge a 500 µH inductor until the inductor current (I_L) reached the set value. Then the top switch is turned off and the inductor was discharged through the low-side MOSFET by the 3rd-quad conduction. The temperature of the power module was controlled by a hot plate and calibrated by thermal imaging. At each temperature, V_{GS} of -5 V and 15 V were used to control the low-side MOSFET in the discharging process.

The current of the low-side MOSFET was measured, the voltage across the MOSFET was calculated by the inductor discharging slope

$$V_F^{3RD} = -L\frac{dI_L}{dt} \tag{14}$$

Then the "dynamic" 3rd-quad I-V characteristics was constructed, as shown in Fig. 29, which were found to be almost the same as the static one at 50 °C and 150 °C.

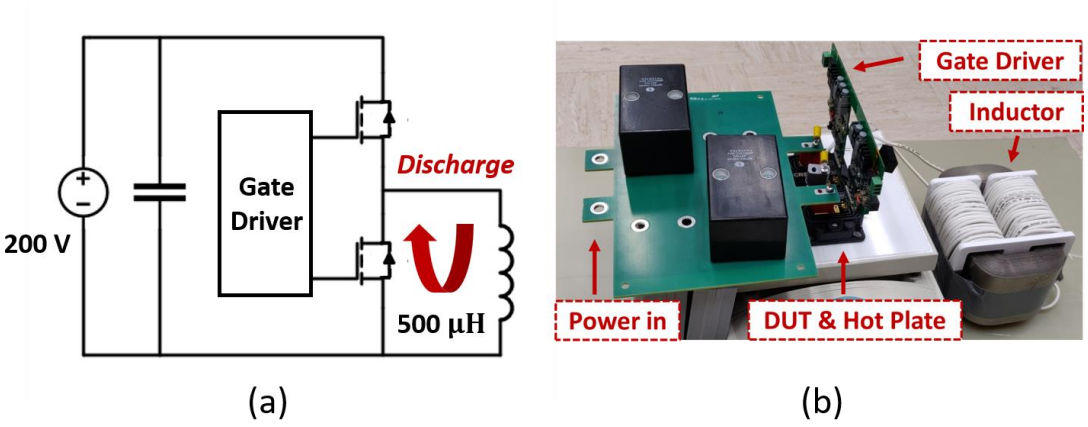

Figure 28. Circuit schematic and setup of the inductor discharging test.

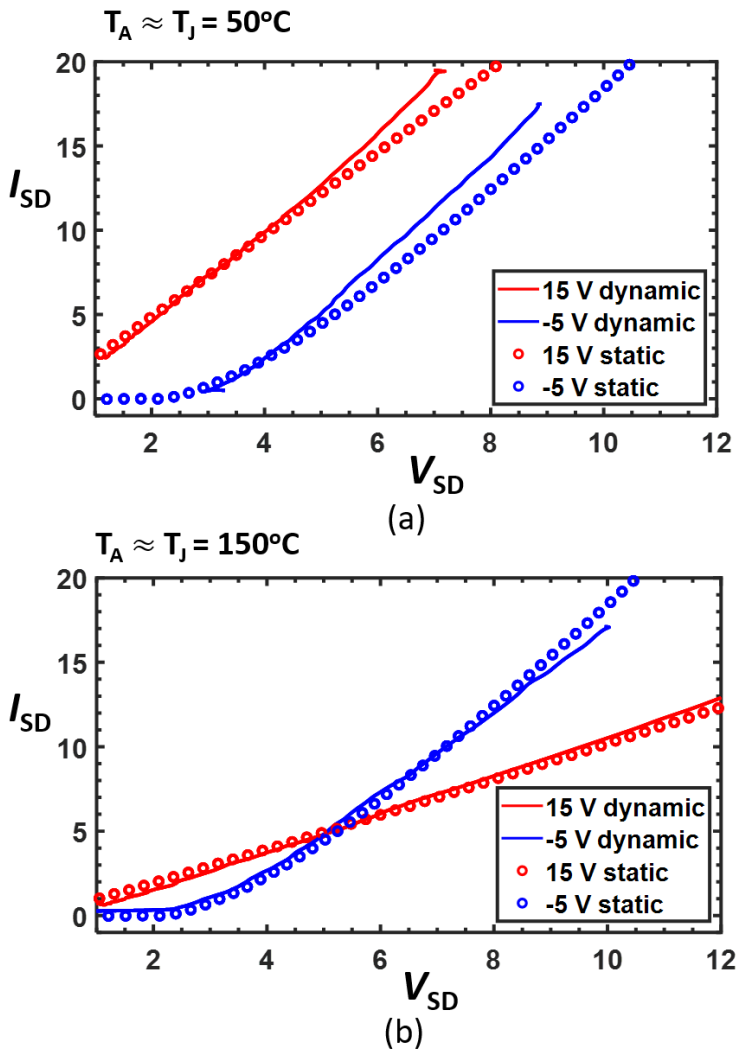

Figure 29. Comparison between extracted dynamic and static 3rd-quad I-V characteristics under (a) 50 °C and (b) 150 °C

4.2 Buck Converter Test

To further validate if a negative V_{GS} control can lead to a smaller V_F^{3rd} in 10 kV SiC MOSFETs in switching conditions, a synchronous dc-dc buck converter was built up using a 10 kV SiC MOSFET half-bridge power module.

4.2.1 Test Setup

The circuit schematic and the test setup are shown in Fig. 30. The input voltage (V_{in}) is 280 V, and the load resistor is 2 Ω, the customized gate driver design for 10 kV SiC

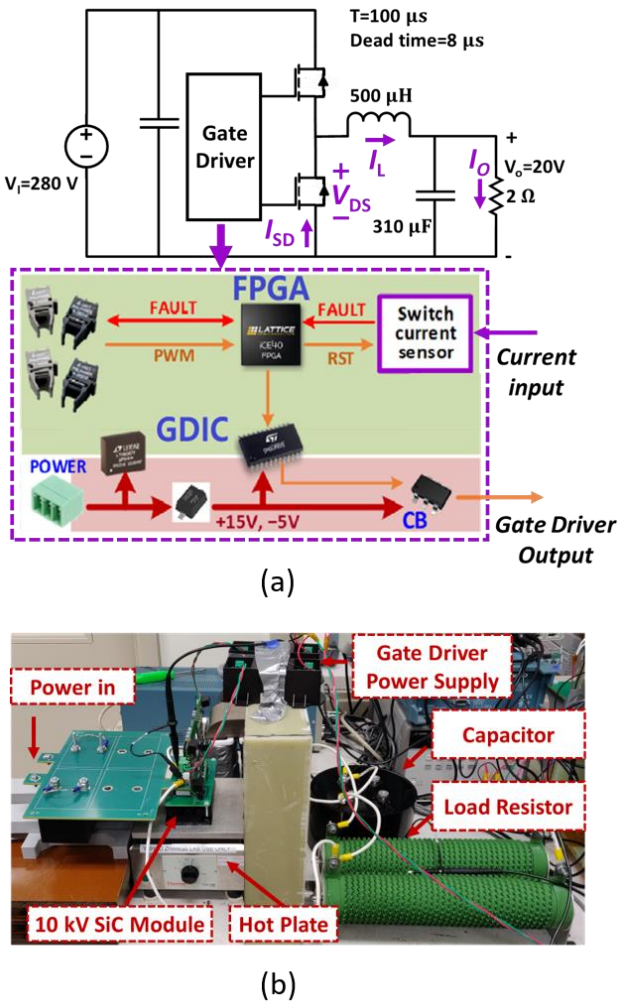

Figure 30. (a) Circuit diagram with the illustration of the customized gate driver and (b) setup of the buck converter test.

MOSFET is based on the one described in [75]. The switching frequency is 10 kHz, which is usually implemented in the hard-switching of 10 kV SiC MOSFET power modules [53] [76] [77]. The test was performed under different temperatures, and the module case temperature (T_C) was controlled by a hot plate and calibrated by a thermal camera as well. Device junction temperature (T_J) was estimated by:

$$T_J \approx T_C + R_{\theta JC} P \tag{15}$$

where $R_{\theta JC}$ is the module junction-to-case thermal resistance (0.4 °C/W), P is the power loss on the module that can be estimated by:

$$P = V_{in} I_L D - V_{out} I_L \tag{16}$$

where I_L is the inductor current, V_{in} and V_{in} are input voltage and output voltage, D is the duty cycle of the buck converter.

At each temperature, two V_{GS}, -5 V and 15 V, were used to control the low-side MOSFET in the 3rd-quad conduction. Due to the concern of false turn-on [78], V_{GS} of 0 V is rarely used in real converter applications and therefore not studied in the converter tests. For V_{GS} of 15 V, the dead time was set to 8 µs with V_{GS} of -5 V in the dead time. Under different test conditions, the input voltage and output current were maintained at 280 V and 10 A, respectively, by modulating the buck converter duty cycle. The relatively small input voltage, 280 V, was chosen to minimize the switching loss in the converter test, which facilitates the measurement of the 3rd-quad voltage drop and the comparison of 3rd-quad conduction loss under different test conditions. The duty cycle (D) was chosen to be small (around 10%) to make the low-side device mainly work in the 3rd-quad conduction. During the test, the output voltage, output current, and the voltage drop on the low-side MOSFET were measured.

4.2.2 Test Results and Analysis

Fig. 31 shows two switching periods in the test waveforms of the low-side MOSFET, with V_{GS} of -5 V and 15 V for 3rd-quad control, and at a T_J of 50 °C and 150 °C, respectively. At T_J of 50 °C, V_G of 15 V leads to lower V_F^{3rd}. However, at T_J of 150 °C, V_{GS} of -5 V provides a lower V_F^{3rd}. This trend is consistent with our static test results and device

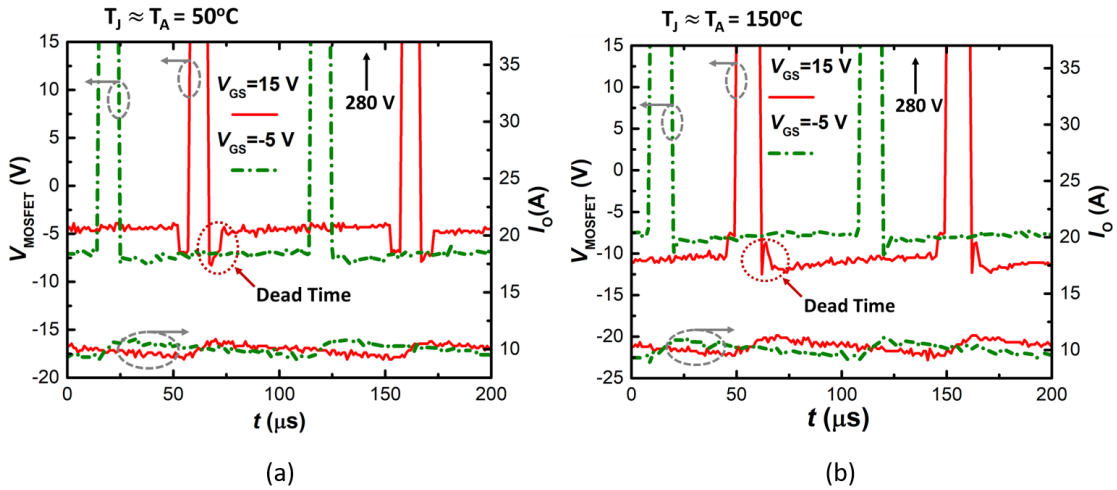

Figure 31. Testing waveforms at 50 °C and 150 °C.

models. Note that the same reverse recovery loss is expected for two V_{GS} controls, due to the need for dead time for the 15 V V_{GS} control, the conduction loss determines the total loss of the low-side device. It can be therefore inferred that a negative V_{GS} leads to the minimal loss for 3rd-quad operation of 10 kV SiC MOSFETs at high temperatures.

Table 2 shows the extracted D and V_F^{3rd} under different testing conditions. As the output current (and power) at the load resistor was kept constant, a larger duty cycle suggests more energy provided by the input power supply and a higher power loss in the converter system. For example, at T_J of 150 ºC, the duty cycle for V_{GS} of 15 V was higher than that for V_{GS}

Table 2. COMPARISON OF CONDITIONS AND THE MEASURED DUTY CYCLE AND THIRD-QUAD VOLTAGE DROP IN DIFFERENT TESTS.

T_J (ºC)	V_G (V)	D	V_{3rd} (V)
50	-5	10.4%	~7
	15	9.5%	~4.5
100	-5	10.9%	~7.4
	15	10.7%	~7.2
150	-5	10.8%	~7.5
	15	11.9%	~10.5

of -5 V, indicating a higher loss for V_G of 15 V. These converter test results verify that a negative V_{GS} is optimal to control the 3rd-quad conduction of 10 kV SiC MOSFETs at high T_J and I_{SD}.

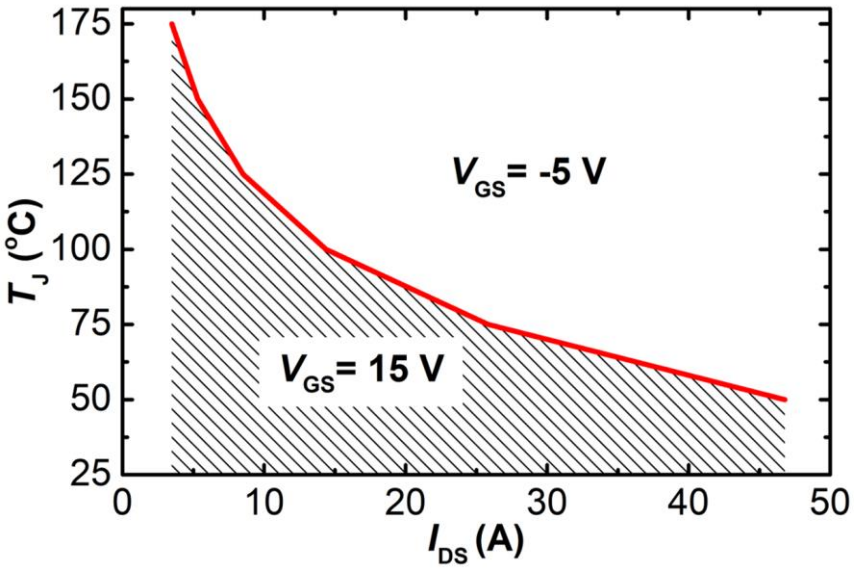

Figure 32. T_J-I_{SD} boundary of 16 A, 10 kV SiC MOSFET.

With a good agreement between static tests, converter tests, and device models, the optimal V_{GS} to control the 3rd-quad conduction of 10 kV SiC planar MOSFETs can be confidently determined under different load current levels and device junction temperatures. Fig. 32 shows the extracted T_J-I_{DS} boundary curve for the tested Wolfspeed 3rd-generation 16 A, 10 kV MOSFET. The conditions above this curve call for a negative V_{GS} control, while the ones below this curve would prefer a $V_{GS} > V_{th}$ control for the device 3rd-quad conduction.

Chapter 5: Conclusions

This work presents a comprehensive study on the 3rd-quad conduction of SiC power MOSFETs. By comparing the 3rd-quad I-V characteristics of industrial 1.2 kV, 3.3 kV, and 10 kV SiC MOSFETs, the competing current sharing between the MOS channel and the body diode at different V_{GS} is identified. At $V_{GS} > V_{th}$, the body diode is found to turn on at a V_{SD} much higher than the built-in potential of the pn junction in higher-voltage rated SiC planar MOSFETs. Comprehensive device physics accounting for this phenomenon has been revealed and validated by TCAD simulation. The potential distribution formed by the channel current reduces the voltage drop across the body diode pn junction. At the case where V_{GS} is not sufficiently low (e.g. 0 V), a surface current path turns on before the body diode conducts, leading to the competing current sharing as well. Analytical models have been developed to correlate $V_{BD\text{-}on}$ with the device voltage rating, which reveals that, in 10 kV SiC planar MOSFETs, the body diode would not turn on in the practical V_{SD} range once the MOS channel is already on. The selection of optimal gate control for 10 kV SiC planar MOSFETs hinges on a direct comparison between the MOS channel path and the body diode path; no V_{GS} allows the simultaneous turn-on of both paths.

The study is then extended to the 3rd-quad characteristics of commercial trench MOSFETs. By comparing the Rohm's double-trench MOSFET and Infineon's CoolSiC™ MOSFET, the 3rd-quad current competition between the MOS channel and body diode is found to be a universal phenomenon in vertical MOSFET s. A new trade-off between the JFET region resistance and V_F^{3rd} for high-voltage trench MOSFET design is proposed.

Finally, the 3rd-quad conduction and voltage drop of 10 kV SiC planar MOSFETs are studied by different power circuit tests. It is found that, in contrary to the optimal V_{GS} control for 1.2 kV MOSFETs, a negative V_{GS} would lead to smaller V_F^{3rd} and conduction loss for 10 kV MOSFETs at high junction temperatures and under high load currents. This work provides new insights for the power MOSFET design, optimization of control strategy, and converter applications of medium-voltage SiC MOSFETs.

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