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James Spencer Lundh,[1,a)] Cory Cress,[1] Alan G. Jacobs,[1] Zhe Cheng,[2] Hannah N. Masten,[1] Joseph A. Spencer,[1,3] Kohei Sasaki,[4] James Gallagher,[1] Andrew D. Koehler,[1] Keita Konishi,[4] Samuel Graham,[5] Akito Kuramata,[4] Travis J. Anderson,[1] Marko J. Tadjer,[1] Karl D. Hobart,[1] and Michael A. Mastro[1]

AFFILIATIONS

[1]U.S. Naval Research Laboratory, 4555 Overlook Ave. SW, Washington, DC 20375, USA
[2]Department of Materials Science and Engineering, University of Illinois, Urbana, Illinois 61801, USA
[3]Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, Virginia 24060, USA
[4]Novel Crystal Technology, Inc., 2-3-1, Hirosedai, Sayama, Saitama 350-1328, Japan
[5]Department of Mechanical Engineering, University of Maryland, College Park, Maryland 20742, USA

[a)]**Author to whom correspondence should be addressed:** james.s.lundh.civ@us.navy.mil

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ABSTRACT

The electrothermal device performance of β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ heterostructure field-effect transistors (HFETs) was enhanced by incorporating a 400 nm thick AlN capping layer via back-end-of-line room-temperature reactive sputter deposition. The AlN-capped HFETs demonstrated DC power densities >5 W/mm, higher than any previous report on lateral β-Ga_2O_3 transistors on native substrates. The breakdown voltage (V_B) of the uncapped HFETs was 569 ± 250 V with a maximum V_B of 947 V. For the AlN-capped HFETs, V_B increased to 1210 ± 351 V with a maximum V_B of 1868 V. The AlN-capped HFETs demonstrated a 27% reduction in device-level thermal resistance (R_{TH}) as measured from the gate electrode. The combined use of electrical and thermal simulation helped elucidate the coupled electrothermal contributions to the measured reduction in the temperature rise for the AlN-capped HFETs. Although the measured AlN film thermal conductivity (13.3 ± 1.3 W/mK) was comparable to that of bulk β-Ga_2O_3, the capping layer still reduced the simulated peak channel temperature rise by ~4% due to heat spreading only. Electrical simulation revealed that electric field spreading was an additional mechanism that contributed to the majority of the simulated 18% reduction in the peak channel temperature rise through delocalization and redistribution of the heat generation in the channel. Thermal modeling was used to evaluate further improvements in thermal performance that can be realized by optimizing the sputter deposition process to achieve thicker and higher thermal conductivity AlN.

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INTRODUCTION

Over the past few decades, wide bandgap (WBG) semiconductors have been heavily researched, and both SiC and GaN device technologies have been commercialized. To further increase performance capabilities, ultrawide bandgap (UWBG) semiconductors, such as gallium oxide (Ga_2O_3), have become a focal point for the power electronics community.[1] Specifically, the monoclinic (β) phase of Ga_2O_3 has garnered much attention due to its ultrawide bandgap (UWBG) of ~4.8 eV, low-cost production of large diameter, high quality, single crystal wafers, and a wide range of n-type doping.[2,3] Since the first demonstration of a β-Ga_2O_3 metal–semiconductor field-effect transistor (MESFET),[4] numerous device technologies have been reported, including Schottky barrier diodes (SBDs), p–n heterojunction diodes, metal–oxide–semiconductor FETs (MOSFETs), heterostructure FETs (HFETs), current aperture vertical electron transistors (CAVETs), and finFETs.[5–16]

While the electrical performance of these devices has progressed significantly, the target high power densities and low thermal conductivity [11–27 W/m K (Ref. 17)] of this UWBG semiconductor have presented a formidable bottleneck to fully harness the potential of β-Ga_2O_3-based power electronics.[18] With device-level thermal resistances (R_{TH}) many times larger than any other relevant semiconductor,[19] thermal management of β-Ga_2O_3 devices is an urgent design consideration, especially considering that thermal management of devices based on gallium nitride (GaN)—with thermal conductivity an order of magnitude greater than that of β-Ga_2O_3—was researched for a decade and was the focal point of multiple Defense Advanced Research Programs Agency (DARPA) programs.[20–35] To address this need, there have been several reports on the potential benefits of bottom-side, top-side, and double-side cooling of β-Ga_2O_3-based devices.[18,21,36–38,40–47] While β-Ga_2O_3 device development is in its early stages, electrothermal co-design must become a priority to ensure that both electrical and thermal obstacles are addressed concurrently. In this work, we demonstrate a device design approach for β-Ga_2O_3 lateral transistors that simultaneously benefits both electrical and thermal performance by incorporating a back-end-of-line (BEOL) room-temperature reactive-sputtered aluminum nitride (AlN) capping layer. The AlN capping layer significantly increased the breakdown voltage (V_B) of β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ HFETs while also reducing the device-level R_{TH}. Thermal modeling suggested that significant improvements in the device thermal performance can be achieved by optimizing the sputter deposition process to realize thicker, higher thermal conductivity sputtered AlN films.

RESULTS AND DISCUSSION

Figure 1(a) shows a cross-sectional schematic of the β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ HFETs with an AlN capping layer. Ozone-assisted molecular beam epitaxy (O_3-MBE) was used to homoepitaxially grow 125 nm of unintentionally doped (UID) β-Ga_2O_3 on an Fe-doped (010) β-Ga_2O_3 substrate.[47,48] Subsequently, a 21 nm thick β-$(Al_{0.21}Ga_{0.79})_2O_3$ barrier layer was grown with Si delta-doping ∼3 nm above the β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ interface. To form the Ohmic contacts, Si was ion implanted (dose: 3×10^{19} cm^{-3}) and activated (10 min, 900 °C anneal in N_2) followed by deposition of Ti/Au (20/200 nm^2) and rapid thermal annealing (1 min, 470 °C in N_2). After Ohmic contact formation, (uncapped) test structures were evaluated, and the specific contact resistivity, Hall mobility, sheet carrier concentration, and sheet resistance at room temperature were measured to be 4.6×10^{-4} Ω cm^2, 61 cm^2/V s, 9.55×10^{12} cm^{-2}, and 10.76 kΩ/□, respectively. Next, atomic layer deposition (ALD) was used to deposit a 20 nm thick aluminum oxide (Al_2O_3) layer for the gate dielectric. Finally, Pt/Au (20 nm/200 nm) was deposited as the gate electrode. The devices were designed to have a gate length (L_G) of 3 μm, a gate width (W_G) of 75 μm, a gate-drain (L_{GD}) spacing of 10 μm, and a gate-source (L_{GS}) spacing of 2.5 μm. After device fabrication, BEOL room-temperature reactive sputter deposition was used to lift off a 400 nm thick AlN film, exposing the contact pads for probing and selectively keeping some devices without an AlN cap for comparison. Si witness samples were included during the sputter deposition of AlN for characterization. Using atomic force microscopy (AFM), the surface roughness of the AlN film in the gate-drain channel region of one of the HFETs was measured to be 3.12 nm and the lateral grain size was ∼50 nm [Fig. 1(b)].

DC output and transfer characteristics of the AlN-capped HFETs were then measured and are shown in Figs. 2(a) and 2(b) from a representative device. The maximum drain-source (I_{DS}) current density measured was 130 mA/mm at a gate voltage (V_{GS})

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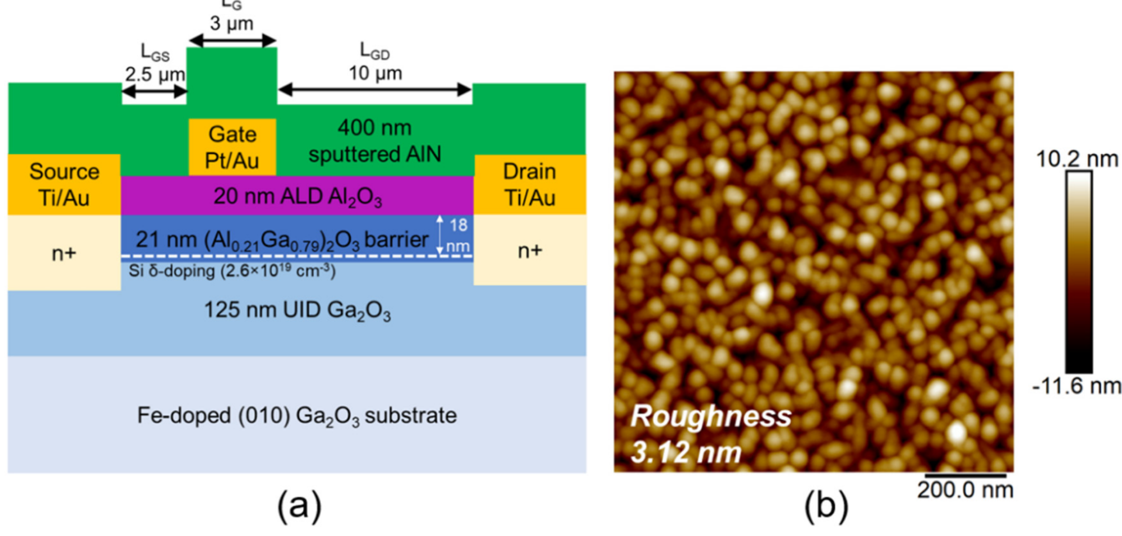

FIG. 1. (a) Cross-sectional device schematic of the β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ HFET with the 400 nm sputtered AlN capping layer. (b) AFM image of the 400 nm AlN capping layer in the gate-drain channel region of an HFET. The root mean square (rms) roughness was measured to be 3.12 nm.

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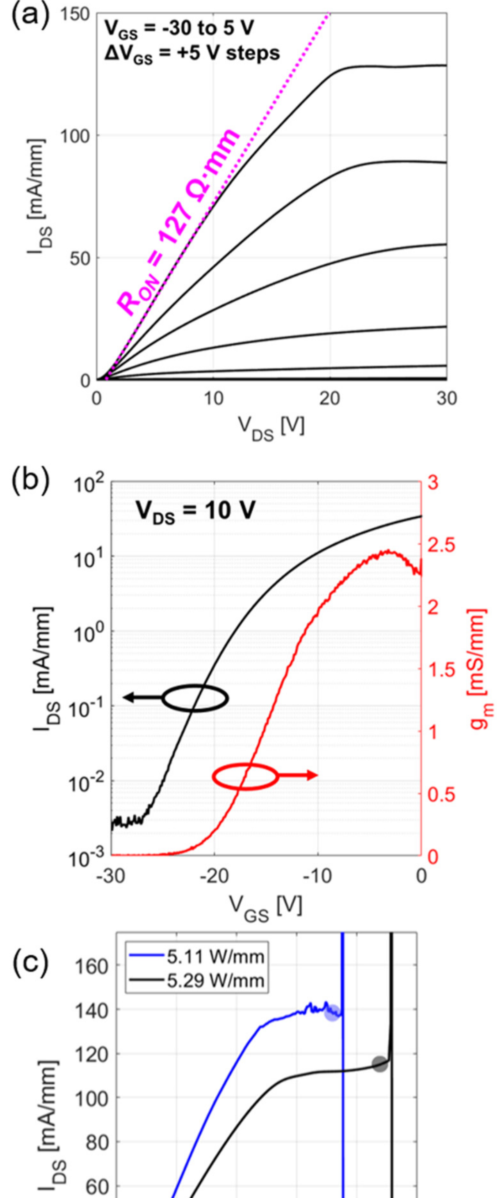

FIG. 2. (a) DC output and (b) DC transfer characteristics of an AlN-capped β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ HFET ($L_G = 3\,\mu m$, $W_G = 75\,\mu m$, $L_{GD} = L_{GS} = 2.5\,\mu m$). (c) I_{DS}–V_{DS} measured at $V_{GS} = 0$ V for the AlN-capped HFETs showing maximum power density reached (see the legend). The circles indicate the datum from which the power density was extracted. Reproduced with permission from 2022 Device Research Conference. Copyright 2022 IEEE.[39]

of 5 V and a drain-source voltage (V_{DS}) of 30 V. At similar bias conditions, the maximum I_{DS} measured from the uncapped devices was ∼75 mA/mm. It should be noted that the isolation current was measured to be on the order of 10^{-11} A from both AlN-capped and uncapped isolation test structures. Additionally, the AlN-capped devices were able to reach much higher power densities than the reference uncapped devices. While the uncapped devices reached a maximum power density of ∼3 W/mm at $V_{GS} = 0$ V before catastrophic failure, the AlN-capped devices were able to exceed 5 W/mm [Fig. 2(c)]. To the authors' best knowledge, this is the highest DC power density reported from a lateral β-Ga_2O_3 transistor on a native bulk β-Ga_2O_3 substrate. Possible explanations for the increase in the maximum DC power density include improved top-side heat dissipation with the AlN cap, changes in the electric field distribution due to the additional top-side dielectric, and the combination of these two effects.

Having observed an increase in the maximum power density in the ON-state, OFF-state breakdown characteristics of several uncapped [Fig. 3(a)] and AlN-capped [Fig. 3(b)] HFETs were measured. The maximum V_B of the uncapped and AlN-capped devices tested were 947 and 1868 V, respectively. While there was an appreciable range in the measured V_B, it is clear from Figs. 3(a) and 3(b) that there was a systematic shift in the V_B by introducing the AlN cap. The average V_B of the uncapped devices was 569 ± 250 V, and the average for the AlN-capped devices was 1210 ± 351 V. Error analysis was performed using a 95% confidence interval based on $t_{0.975}$ times the standard error of the mean. The increase in the OFF-state breakdown voltage suggests that there was a change in the electric field profile due to the AlN cap, similar to previous reports for addition of a top-side dielectric.[49] Electrical models developed in Silvaco™ TCAD further confirmed the redistribution of the electric field and reduction in the electric field at the drain-side edge of the gate electrode (see Fig. S1 in the supplementary material).

To quantify the effectiveness of the AlN cap as a heat-spreading layer, steady state thermoreflectance thermal imaging[50] (TMX Scientific T°Imager®, 100× objective, 530 nm LED) was used to measure and compare the temperature rise of an uncapped and AlN-capped HFET at several power densities with $V_{GS} = 0$ V. Thermoreflectance thermal imaging relies on the temperature dependence of the reflectivity of a material to measure the temperature rise[51] and is very effective at probing the temperature of metallization structures. Therefore, the temperature rises of the Au-coated gate, drain, and source electrodes were measured. Since the peak temperature rise in these lateral device structures is typically in the channel at the drain-side of the gate,[52] the measured temperature rise of the Au in the gate electrode is useful for assessing device R_{TH}.

Figure 4 compares the average temperature rise from the center of the gate electrode (see the inset of Fig. 4) for the uncapped reference and AlN-capped HFETs at various power densities. The slope of the temperature rise as a function of power density represents R_{TH} at the center of the gate of the device. As shown in Fig. 4, R_{TH} at the gate decreased from 49.5 mm K/W for the uncapped reference device to 36 mm K/W for the AlN-capped device, which is a 27% reduction. This can most likely be attributed to a combination of heat spreading by the AlN-capping layer and

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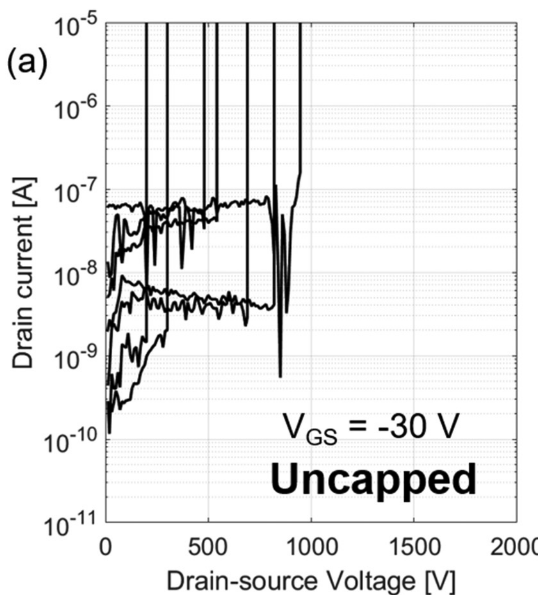

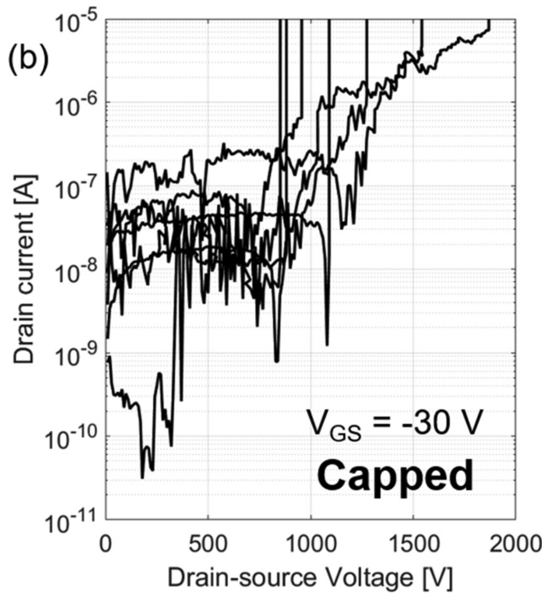

FIG. 3. OFF-state breakdown measurements of the (a) uncapped and (b) AlN-capped HFETs performed with $V_{GS} = -30$ V.

the electric field redistribution and thus alteration of the Joule heating profile.

The thermal conductivity of the AlN capping layer was subsequently measured using time domain thermoreflectance (TDTR). Time domain thermoreflectance is an optical pump-probe technique, which can measure the thermal diffusivity of a film or substrate, and then thermal conductivity can be calculated given the density and specific heat.[53] Since sample preparation for TDTR requires the deposition of a blanket thin metal transducer (e.g., 80 nm of Al), TDTR measurements were performed on the Si witness samples that were sputter deposited during the same run as the AlN-capped HFETs. Prior to blanket metal deposition for TDTR, the surface morphology of the sputtered AlN/Si witness was measured using AFM and had similar surface roughness and grain size to that shown in Fig. 1(b) from the sputtered AlN in the channel of the HFET. As such, the witness sample should be representative of the sputtered AlN on the HFET. The thermal conductivity of this sputtered AlN layer was measured to be 13.3 ± 1.3 W/m K. This result is noteworthy because capping the devices even with such a low thermal conductivity film, indeed one comparable to that of the β-Ga_2O_3 device, resulted in significant improvement in device R_{TH} and electrical performance. However, it should be noted that any electric field redistribution would also alter the heat generation profile in the device, which would help alleviate device self-heating and lower peak temperature rise.[44,54–57]

There have been reports of thicker (>1 μm) sputtered AlN films with thermal conductivities exceeding 100 W/m K.[58] This raises the question of how much improvement in thermal performance can be expected with a possible 10× improvement in the thermal conductivity of our sputtered AlN capping layers. It is also plausible that increasing the thickness of the AlN cap can further spread the electric field and reduce the peak electric field in the device,[49] leading to additional increases in breakdown voltage and reductions in peak temperature rise.

To evaluate the effect of the thermal conductivity and thickness of the AlN capping layer on the peak temperature rise of the HFET, a 3D finite element method (FEM) thermal model was developed using COMSOL Multiphysics. The device surface geometry is generated by importing the lithographic mask layout of the electrical contacts and the channel region. The device mesa incorporated the Al_2O_3 gate dielectric (20 nm), the β-$(Al_{0.21}Ga_{0.79})_2O_3$ barrier (21 nm), and the β-Ga_2O_3 epilayer (125 nm). The Ti/Au Ohmic contacts and the Pt/Au gate contact were modeled as Au. The β-Ga_2O_3 substrate had dimensions of 2.5 mm (length), 2.5 mm (width), and 0.5 mm (thickness). Through a series of substrate parametric sweeps, these dimensions were the smallest that yielded no change in the peak temperature at the gate within the temperature range studied. To model the AlN capping layer, a conformal layer over the surface of the device was defined.

When available, we used the COMSOL material database thermal properties of the materials simulated. The β-Ga_2O_3 thermal (and temperature dependence) in the [010] direction reported by Slomski *et al.* was used.[59] The thermal conductivities of β-$(Al_{0.21}Ga_{0.79})_2O_3$ and Al_2O_3 were assumed to be 3[60] and 1.5 W/m K,[61,62] respectively, and were not modeled to be temperature dependent. Between dielectric materials of different chemical composition, we included a thermal boundary conductance (TBC) of 200 MW/m^2 K,[62,63] and for metal–dielectric interfaces, the TBC was reduced to 15 MW/m^2 K.[64] Within the heat transfer module of COMSOL Multiphysics, we defined four fixed temperature regions (T = 293.15 K), including the bottom of the substrate, and circles on each of the three electrical contacts signifying heat dissipation

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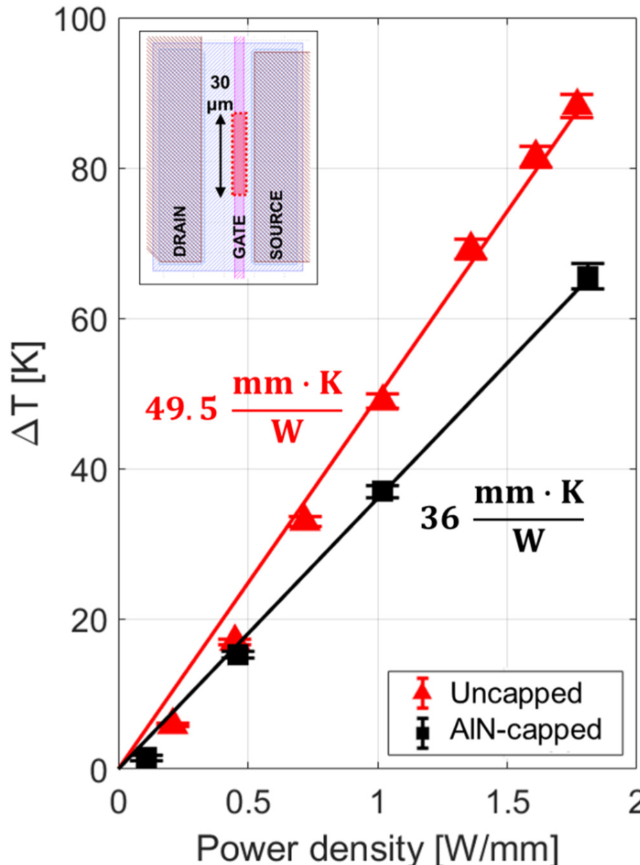

FIG. 4. Average gate temperature rise of the uncapped reference HFET (triangles) and AlN-capped HFET (squares) as a function of power density. The device-level R_{TH} in units of mm K/W are also provided for each device. Error bars for the temperature rise (ΔT) were calculated using a 95% confidence interval based on $t_{0.975}$ times the standard error of the mean. The inset shows a plan-view image of the mask design for the HFET with the red dashed box, indicating from where the average gate temperature rise was extracted.

by the electrical probes. We included a hot-plate convective heat-flux term to all top-side surfaces and the built-in thermal insulation boundary condition applied to the four sides of the substrate.

To approximate the device Joule heating, we used a volumetric heat source [Fig. 5(a)] consisting of (i) a thin layer below the β-$(Al_{0.21}Ga_{0.79})_2O_3$/$Ga_2O_3$ interface that spanned the full device channel region with thickness, t, and (ii) an inverted triangular region centered at the drain edge of the gate finger with height, h, and base, b.[37,44,65] For simulations without the AlN cap, t = 2.5 nm, and the inverted triangular region had b = 1000 nm and h = 30 nm.

A comparison of the simulated and measured temperature distributions across the length of the uncapped reference HFET is shown in Fig. 5(b). Since thermoreflectance imaging was used to measure the temperature rise of the metallization, these data are comparable to the simulated temperature rise across the top of the metal electrodes [Sim. Metals in Fig. 5(b)] and shows good agreement. The temperature rise at the surface of the β-Ga_2O_3 epilayer is also shown in Fig. 5(b) (Sim. β-Ga_2O_3) since this will provide insights regarding the magnitude of the peak temperature rise in the device structure. Raw temperature distributions across the device length are provided, and as such, there are outliers in the data near edges/features in the device topography (e.g., edge of mesa, edge of Ohmic contacts, etc.). This results from image misregistration, thermal expansion effects, or the fact that the incident light used in the measurement is no longer at normal incidence, and thus, the assumptions of the experimental method are no longer valid, all of which can lead to errant data.[66–68]

Having calibrated the device thermal model using the experimentally measured temperature rise of the uncapped reference HFET, the AlN cap was introduced in the thermal model and the simulated temperature distribution across the AlN-capped HFET was extracted. However, as shown in Fig. 6(a), simulation of the temperature rise, including the AlN cap with heat spreading only, does not fully account for the reduction in the temperature rise measured experimentally. Since the OFF-state breakdown voltage of the AlN-capped HFETs significantly increased compared to the uncapped reference HFETs (Fig. 3), we hypothesize that electric field spreading due to the AlN cap must have a significant coupled electrothermal effect on altering the heat generation in the device and lowering the temperature rise. To further investigate, electrical models of the uncapped and AlN-capped HFETs were developed using the Silvaco TCAD package. As shown in Fig. 7, under ON-state conditions (VGS = 0 V), the addition of the AlN capping layer redistributes the electric field, spreading the electric field across the gate to drain region. This redistribution of the electric field has been reported previously in a passivation thickness study on GaN HEMTs[49] and spreading of the electric field would indeed change the heat generation profile as they are inextricably linked.[44,54–57] The redistribution of the electric field in the AlN-capped HFETs would also help explain the high voltage operation realized when achieving the high DC power densities measured in Fig. 2(c). This could be a complementary explanation along with the reduced self-heating suggesting an improvement in the coupled electrothermal performance, which contributed to the very high DC power densities.

To account for the electric field redistribution in the AlN-capped HFET simulated using Silvaco [Fig. 7(b)], the assumed heat generation volume in the thermal model was adjusted such that the inverted triangular region (b, h) was eliminated, leaving only the thin rectangular volume below the β-$(Al_{0.21}Ga_{0.79})_2O_3$/$Ga_2O_3$ interface (t = 3.6 nm). Despite the different heat source geometries, the total heat source volume remained constant to realize identical simulated power densities. As shown in Figs. 6(b) and 6(c), adjustment of the heat generation volume in the thermal model to account for both heat and electric field spreading led to excellent agreement between the experimentally measured and simulated temperature distribution across the length of the AlN-capped HFET.

Having calibrated the thermal model, a parametric study (Fig. 8) was performed to assess the dependence of the peak device temperature rise at the β-Ga_2O_3 surface on both thermal conductivity and thickness of the AlN capping layer. Thermal conductivities of 5, 10, 13, 20, 30, 55, 80, 105, and 130 W/m K and

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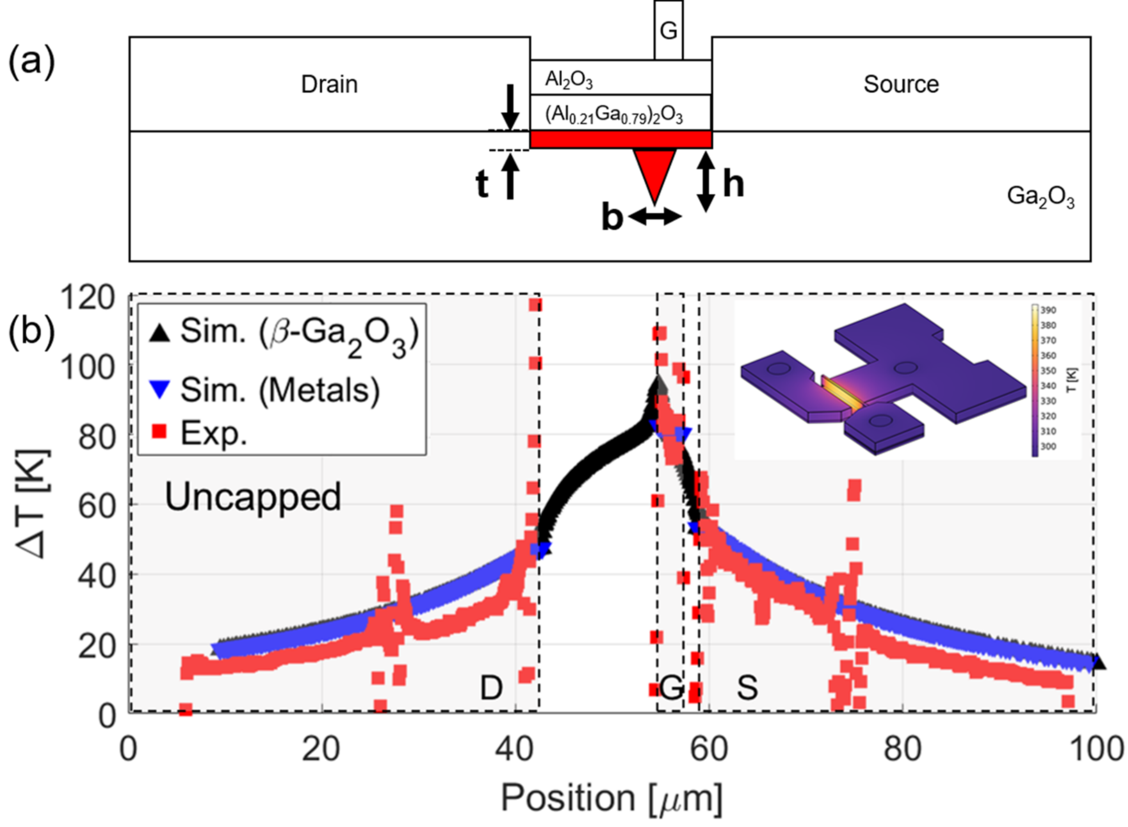

FIG. 5. (a) Cross-sectional schematic detailing the heat generation volume incorporated in the device thermal modeling. The heat generation volume and dimensions (thickness, t; base, b; height, h) are not drawn to scale. (b) Comparison of the simulated (sim.) and measured (exp.) temperature rise across the length of an uncapped reference HFET at a power density of 1.8 W/mm (V_{GS} = 0 V). Simulated temperature rises are shown for a cutline at the surface of the β-Ga_2O_3 epilayer (Sim. β-Ga_2O_3) and at the surface of the gate electrode (Sim. Metals). D, G, and S represent the drain, gate, and source electrodes. The inset shows the thermal model geometry and the temperature rise at P = 1.8 W/mm.

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thicknesses of 400 nm and 1 μm were simulated for an HFET operating with a power density of 1.8 W/mm. To highlight the contributions of heat spreading and electric field spreading, the simulated peak temperature rises for the (i) 400 nm AlN cap with heat spreading only and (ii) 400 nm AlN cap with heat and electric field spreading are shown for comparison. Additionally, the peak temperature rise of the uncapped reference HFET (94.4 K) is shown (dashed line) for benchmarking.

First, as expected, a significant reduction in the device peak temperature is realized by increasing the thermal conductivity of the AlN capping layer. As thermal conductivity increases from 5 to 130 W/m K, the peak temperature rises of the 400 nm thick (squares, Fig. 8) and 1 μm thick (stars, Fig. 8) AlN cap with heat and electric field spreading decrease by 8.9% and 21.8%, respectively. Second, for low AlN thermal conductivities, the reduction in the peak temperature rise is primarily due to electric field spreading. For example, for 400 nm thick AlN with a thermal conductivity of 5 W/m K, the peak temperature rise reduces by only 2.9% with heat spreading only (compared to the uncapped baseline); this increases to 16.8% when both heat and electric field spreading are considered. As the AlN thermal conductivity is increased to 130 W/m K, the contributions of heat spreading and electric field spreading to the reduction in the temperature rise become comparable. When only heat spreading is considered, a 12.9% reduction in the peak temperature rise can be expected for a 400 nm AlN cap with a thermal conductivity of 130 W/m K. This reduction becomes 24.3% when both heat and electric field spreading are taken into consideration. Moreover, by increasing the thickness of the AlN capping layer to 1 μm (thermal conductivity of 130 W/m K), the peak temperature rise is shown to decrease by 35.3% (compared to the uncapped baseline) since the heat spreading capabilities are enhanced due to the greater cross-sectional area for heat flow.

It should also be noted that the thermal simulation assumes that the electric field distribution and heat generation are constant for both AlN thicknesses. In a previous study, it was shown that increasing the thickness of the passivation from 10 to 200 nm significantly increased the breakdown strength and spread/redistributed the electric field across the gate to drain region.[49] Accordingly,

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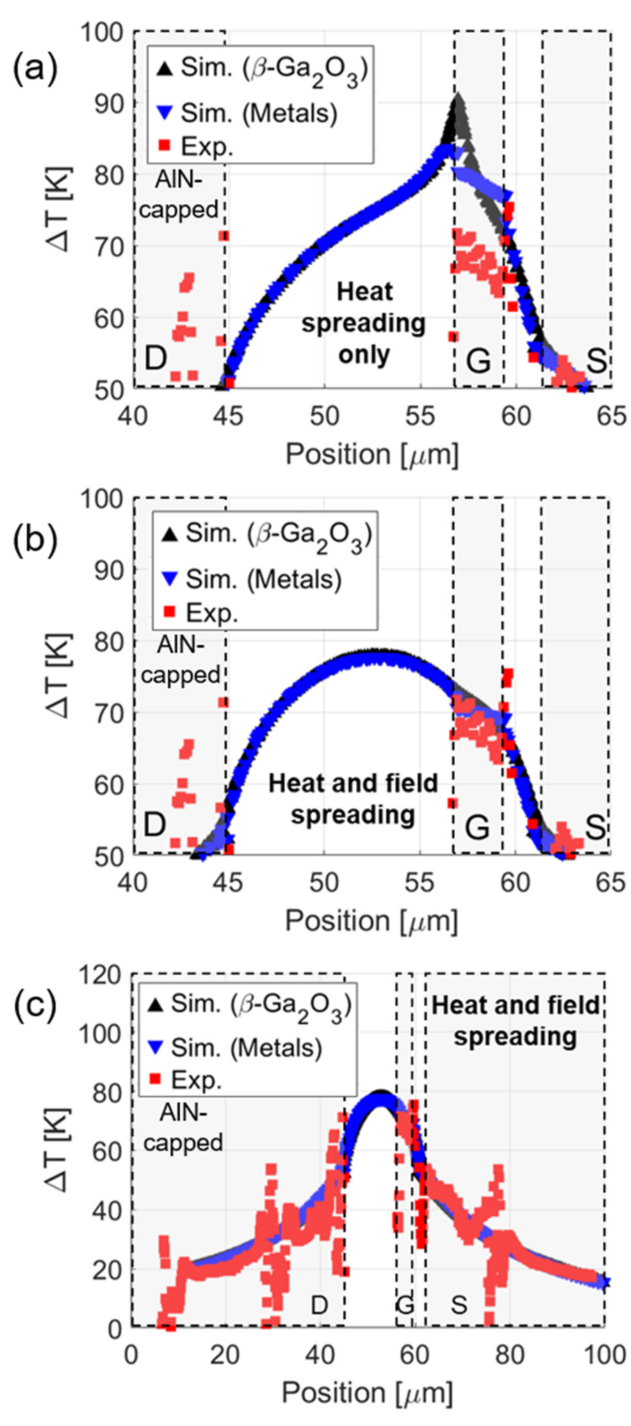

FIG. 6. Comparison of the simulated (sim.) and measured (exp.) temperature rise across the length of an AlN-capped HFET (a) with heat spreading only and (b) with heat and electric field spreading at a power density of 1.8 W/mm (V_{GS} = 0 V). (c) Temperature distribution across the entire length of the AlN-capped device with heat and electric field spreading at a power density of 1.8 W/mm (V_{GS} = 0 V).

further peak electric field mitigation and electric field redistribution with the thicker 1 μm AlN could contribute to an additional increase in the breakdown voltage and an additional reduction in the temperature rise, which is not captured by this simulation; therefore, the temperature rise for the 1 μm thick AlN is a conservative estimate. Moreover, the reduction in the temperature rise due to heat and electric field spreading would also have a second-order effect on the electrical performance of the device. For example, reduced self-heating would minimize detrimental self-heating effects, such as a reduction in electron mobility. This would also allow the device to operate at the same power density but with a lower V_{DS}, which would then change the peak electric field and its distribution and accordingly alter the heat generation. Consequently, the totality and complexity of the semiconductor device physics are unfortunately impossible to capture with a

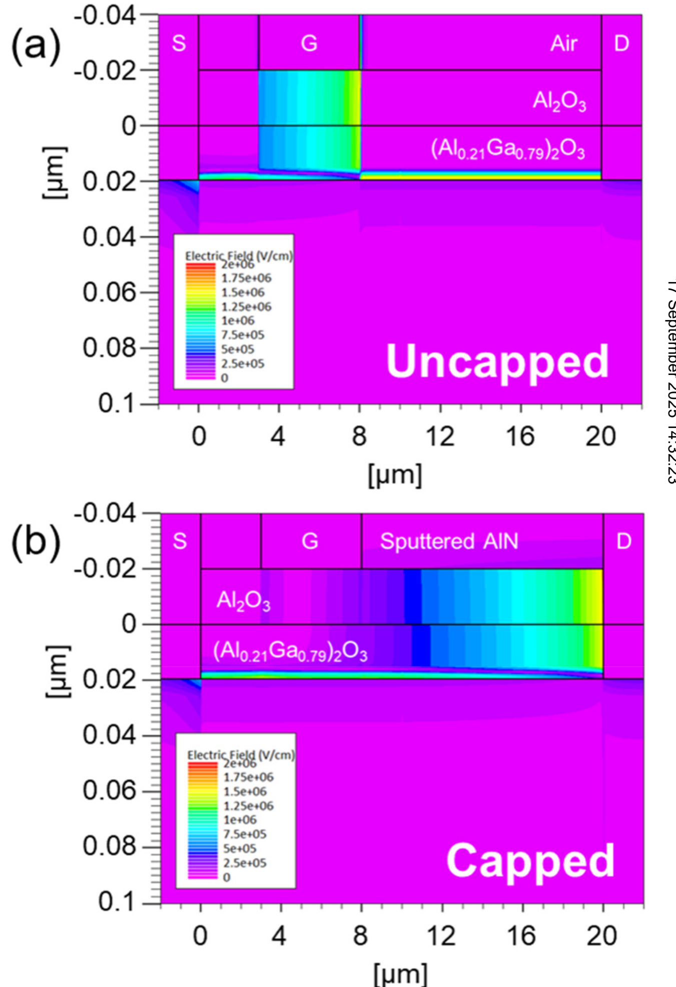

FIG. 7. Silvaco simulation of the electric field distribution (sum of lateral E_x and vertical E_y components) of the (a) uncapped and (b) AlN-capped HFETs. Simulations were performed with V_{GS} = 0 V and V_{DS} = 8 V.

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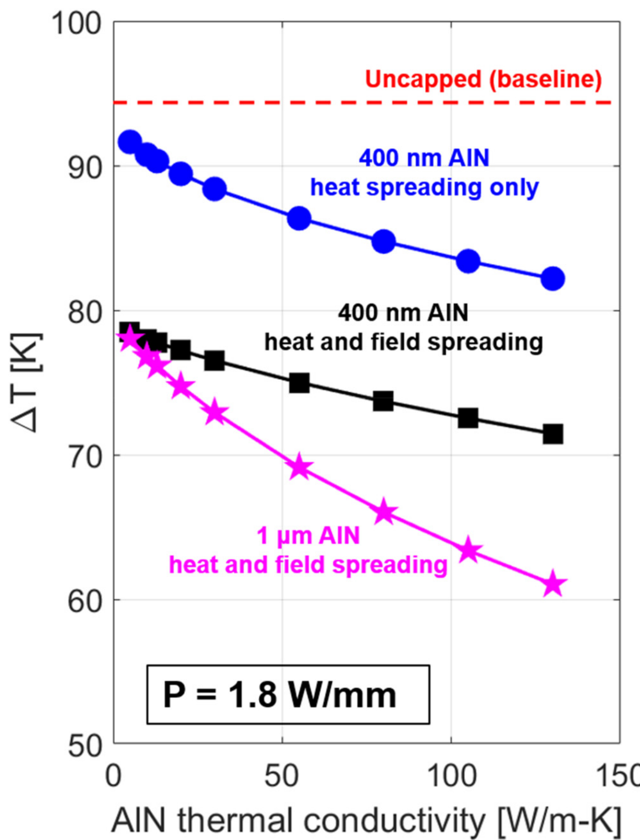

FIG. 8. Effect of AlN thermal conductivity on the device peak temperature rise (peak) for a 400 nm thick AlN cap with heat spreading only (circles), 400 nm thick AlN cap with heat and electric field spreading (squares), and a 1 μm thick AlN cap with heat and electric field spreading (stars). The peak temperature rise of the uncapped reference HFET (dashed line) is also included for benchmarking. The simulated power density was 1.8 W/mm.

purely thermal model. The preceding discussion of the interdependence of electrical and thermal device performance highlights the necessity for fully coupled electrothermal modeling[69] to truly capture the device physics and is the subject of future work.

CONCLUSION

In this report, we demonstrated β-$(Al_{0.21}Ga_{0.79})_2O_3/Ga_2O_3$ HFETs with AlN capping layers, which offered both electrical and thermal performance improvements. The AlN cap was deposited via BEOL reactive sputter deposition at room temperature and was measured to have a thermal conductivity of 13.3 W/m K. Compared to the uncapped HFET, the AlN-capped device demonstrated a 27% reduction in the average gate temperature rise. Additionally, the AlN cap helped to significantly increase the average breakdown voltage of the HFETs by ∼110%. The coupled electrothermal device improvement enabled the demonstration of record high DC power densities >5 W/mm in the AlN-capped HFETs. A 3D thermal model was also developed in COMSOL to assess additional thermal benefits that can be realized by obtaining thicker and higher thermal conductivity AlN films. The thermal model revealed that simulation of heat spreading only could not fully account for the measured reduction in the device temperature rise. Further electrical simulation in Silvaco showed that the AlN cap redistributed the electric field profile, which would help delocalize the heat generation in the channel and contribute to the measured reduction in the average gate temperature rise. By accounting for both heat and electric field spreading, excellent agreement was demonstrated between the measured and simulated peak temperature rises. Moreover, by increasing the thickness (1 μm) and thermal conductivity (130 W/m K) of the AlN cap, a 35% reduction in the peak temperature rise can be achieved. In accordance with the thermal model, we intend to optimize the AlN sputtering conditions in future work to increase the thickness and thermal conductivity of the AlN cap to further improve the device-level thermal performance and increase the breakdown strength. This work also demonstrates an alternative BEOL CMOS-compatible top-side thermal management approach for β-Ga_2O_3 devices that does not require any protective barrier dielectric (e.g., SiN interlayer for nanocrystalline diamond-capped β-Ga_2O_3 devices[47]).

SUPPLEMENTARY MATERIAL

See the supplementary material for electrical simulation (Silvaco) of the uncapped and AlN-capped HFETs under OFF-state bias conditions.

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17 September 2025 14:32:23

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

James Spencer Lundh: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Cory Cress:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (supporting); Writing – review & editing (equal). **Alan G. Jacobs:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal);

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Writing – review & editing (equal). **Zhe Cheng:** Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Hannah N. Masten:** Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Joseph A. Spencer:** Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Kohei Sasaki:** Formal analysis (equal); Resources (equal); Writing – review & editing (equal). **James Gallagher:** Formal analysis (equal); Software (equal); Writing – review & editing (equal). **Andrew D. Koehler:** Formal analysis (equal); Investigation (equal); Supervision (equal); Writing – review & editing (equal). **Keita Konishi:** Formal analysis (equal); Resources (equal); Writing – review & editing (equal). **Samuel Graham:** Formal analysis (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Writing – review & editing (equal). **Akito Kuramata:** Funding acquisition (equal); Resources (equal); Writing – review & editing (equal). **Travis J. Anderson:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Marko J. Tadjer:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal). **Karl D. Hobart:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Michael A. Mastro:** Formal analysis (equal); Funding acquisition (equal); Methodology (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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17 September 2025 14:32:23

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