Design and Fabrication of Emitter Controlled Thyristors

by

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(ABSTRACT)

The Emitter Controlled Thyristor (ECT) is a new MOS-Gated Thyristor (MGT) that combines the ease of a MOS gate control with the superior current carrying capability of a thyristor structure for high-power applications. An ECT is composed of an emitter switch in series with the thyristor, an emitter-short switch in parallel with the emitter junction of the thyristor, a turn-on FET and the main thyristor structure. The ECT also offers superior high voltage current saturation capability even for high breakdown voltage devices. Two different ECT structures are investigated in this research through numerical simulations and experimental fabrications.

A novel ECT structure that utilizes IGBT compatible fabrication process was proposed. The emitter short FET, emitter switch FET and turn-on FET are all integrated with a high voltage thyristor. Numerical simulation results show that the ECT has a better conductivity modulation than that of the IGBT and at the same time exhibits superior high voltage current saturation capability, superior FBSOA and RBSOA. The technology trade-off between turn-off energy loss and forward voltage drop of the ECT is also better than that of the IGBT because of the stronger conductivity modulation. A novel self-aligned process is developed to fabricate the device. Experimental characteristics of the fabricated ECT devices show that the ECT achieves lower forward voltage drop and superior high voltage current saturation capability.

A Hybrid ECT (HECT) structure was also developed in this research work. The HECT uses an external FET to realize the emitter switching function; hence a complicated fabrication

issue was separated into two simple one. The cost of the fabrication decreases and the yield increases due to the hybrid integration. Numerical simulations demonstrate the superior on-state voltage drop and high voltage current saturation capability. A novel seven-mask process was developed to fabricate the HECT. Experimental results show that the HECT could achieve the lower forward voltage drop and superior current saturation capability. The resistive switching test was carried out to demonstrate the switching characteristics of the HECT.

To my parents and wife

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Chapter 1 Introduction

1.1 Power Semiconductor Switches

Power semiconductor switches are essential components for load power regulation in all power electronics systems. The continuous development of power electronics technology has opened up wide applications for power semiconductor devices. The performance and the controlling of the power semiconductor device determine the efficiency, size and weight of the entire power electronics system. It is recognized that the development of power semiconductor devices is the key to the technological improvement in power electronics.

Generally speaking, power semiconductor switches are three terminal devices. The signal applied to the control terminal makes the switch either block voltage or conduct current between the other two terminals. In the early 1950s, the first controllable power semiconductor switch, Bipolar Junction Transistor (BJT), was developed [1]. Since then, power BJTs were used widely in power electronics systems. This was followed by the invention of the Gate Turn-off Thyristor (GTO) that has the gate turn-off capability unlike the conventional thyristor which can only be turned off by reversing the voltage across it. Since the power BJT is a current controlled device, increasing the current gain for a given blocking voltage became the primary design goal in order to simplify the base driving circuit design. However, there exists a fundamental tradeoff between the collector-emitter breakdown voltage and the current gain due to the conflicting requirements on the base width and collector drift region thickness.

In the late 1970s, with the development of the MOS IC technologies, power MOSFET was introduced. The power MOSFET is a voltage-controlled device that can be turned on and turned off with a voltage signal. This simplifies the gate control circuit and makes the power

electronics system integration easier. In addition, when the blocking voltage is below 200 volts, the on-resistance, hence the conduction loss of a power MOSFET can be made very small by using high channel density design. The power MOSFETs also exhibit excellent switching speed and large Safe Operation Area (SOA). These features have made the power MOSFET widely used in low voltage and high frequency applications. However, the on-resistance of the power MOSFET increases very rapidly with increased voltage ratings due to the lack of conductivity modulation, and this makes it unsuitable for high-voltage applications.

In the late 1980s, the integration of the MOSFET and the bipolar transistor resulted in a new power device called the Insulated Gate Bipolar Transistor (IGBT) [2]. The important features of the IGBT are its high forward conduction current density, low drive power due to its MOS gate-controlled structure, MOS gate-controlled turn-off and turn-on capabilities and wide safe operation area. This has led to its wide applications in power electronics systems immediately after its commercial introduction. On the other hand, the forward voltage drop in the IGBT increases gradually when the blocking voltage increases. Hence the on-state power dissipation of the high voltage IGBTs therefore is still higher than thyristor devices, such as the GTOs. Therefore, a new class of power semiconductor device with the integration of the MOSFET into the thyristor structure has emerged in the 1990s. MOS-gated thyristors like the MOS Controlled Thyristor (MCT) belongs to this power device class. The topology of the MCT is basically a high-voltage thyristor with two MOSFETs integrated into the cathode structure. One of the MOSFETs, the ON-FET, is responsible for turning the MCT on, and the other MOSFET, the OFF-FET, is responsible for turning the MCT off. The MCT therefore combines the low forward voltage drop and large current carrying capability of a thyristor with the advantages of MOS-controlled turn-on and turn-off. MCTs therefore provide both an easy gate drive, due to the high input impedance of the MOS gate, and a low on-state loss, due to the strong conductivity modulation effect of the thyristor. They are expected to compete with IGBTs in high power applications. However, the MCT lacks the current saturation capability so it is difficult to control the turn on and turn off in a required manner and protect the device from short circuit fault.

In order to overcome the problem of lacking the current saturation capability in the MCT, many MOS gated thyristor structures with current saturation feature have been reported, e.g., the Dual Channel Emitter Switched Thyristor (DC-EST) [3], the Dual MOS Gate Controlled Thyristor (DMGCT) [4] and the Emitter Controlled Thyristor (ECT). In these new devices, The ECT exhibits superior on-state characteristic even at a blocking voltage of 4.5 kV and excellent high voltage current saturation capability [5]. A brief description of the ECT structure and operation is provided in Chapter 2. This thesis discusses operation and development of the ECT at Virginia Tech.

1.2 Organization of the Thesis

The research work reported here focuses on the following two tasks.

1). Development of a novel 1200 V ECT with superior current saturation capability.

2). Development of a novel hybrid ECT (HECT) with 4 kV blocking capability.

The first part of this thesis covers the development of a 1200 V ECT. This part of work includes analysis of the ECT using numerical simulation tools, device optimization, processing design for the proposed 1200 V device, fabrication of the device and experimental characteristic analysis of the fabricated devices.

The second part of the thesis focuses on the development of a 4 kV HECT. The design goal of the HECT is to obtain lower forward voltage drop and achieve superior current saturation capability at the same time when blocking voltage increases to 4 kV. In the HECT structure, an external low voltage power MOSFET was packaged with a high voltage thyristor structure. Due to the hybrid integration, the complexity of device fabrication decreases therefore a lower cost and a higher yield can be obtained. This part of work also covers the device optimization, processing design and fabrication of the device. It also covers the experimental characteristic analysis of the fabricated devices.

The major contributions of the research work described in this thesis are listed below.

1). Presented a new ECT structure compatible with the IGBT fabrication process. The new operation concept is verified by simulation and experiment.

2). Proposed a novel hybrid ECT structure, and fabricated a 4 kV HECT using only seven masks aluminum gate process. Experimental characteristic was analyzed to verify the hybrid integration concept. Lower forward voltage drop and current saturation capability are achieved comparing to the same voltage rating IGBT.

The thesis is divided into five chapters with an introduction at the beginning. Chapter 2 provides the background material on power semiconductor devices. That will help us to understand the evolutional development of power devices from the bipolar transistor to MOS-gated thyristor. The principle, basic structure and operation concept of the ECT are then introduced in Chapter 2.

Chapter 3 investigates a new IGBT-compatible ECT structure. Numerical simulations are used to optimize the device characteristics and analyze the operating principle of the device. A novel processing is proposed for the ECT. Device fabrication is conducted at Cornell Nano-fabrication Facility and experimental results are reported.

In Chapter 4, the concept and operation principle of the hybrid ECT structure are analyzed first. Then the processing design and layout design are discussed in order to fabricate the device. Then, a set of detailed experimental data is provided to describe the characteristics of the fabricated device. A test circuit is also presented to verify the switching capability of the fabricated device.

Finally, conclusions are obtained based on the research work and some suggestions for future work are outlined in Chapter 5.

Appendix provides the details of the device fabrication steps.

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Chapter 2 Introduction to Emitter Turn-off Thyristor

2.1 Desirable Characteristics of a Power Switch

The field of power electronics deals with the processing of electrical power using solid state semiconductor devices. The switching converter is a key element that connects a power input to a power output and a control input. The raw input power is processed as specified by the control input signal and yields the conditioned output power. One of several basic functions can be performed by the switching converter. A dc-dc converter can convert the dc input voltage to a dc output voltage having a larger or smaller magnitude. An ac-dc rectifier can rectify an ac input voltage to produce a dc output voltage. A dc-ac inverter can transform a dc input voltage into an ac output voltage of controllable magnitude and frequency. Fig. 2.1 shows a popular application of power electronics [1], a dc-3ϕac inverter system. The inverter produces three-phase ac output voltages of controllable frequency and controllable magnitude from a dc voltage source. This system allows accurate control of the ac machine. Applications of this system include speed control of industrial processes, such as control of fans and pumps; transportation applications such as subways and locomotives; and motion control applications such as computer peripherals and industrial robots.

The system shown in Fig. 2.1 has three switch pairs or phase legs: a (s1 and s2), b (s3 and s4) and c (s5 and s6). The magnitude and frequency of the three phase voltages V_{an}, V_{bn} and V_{cn} can be controlled by changing the switching duty cycle of the three switch pairs *a*, *b* and *c*. The switches are typically realized by power semiconductor transistors and their anti-parallel diodes. Therefore, in a typical 3ϕ inverter, each branch or phase leg consists of two switches and two diodes. The parallel of a switch and a diode allows bi-directional current conducting and

unidirectional voltage blocking. Combination of S1 and S2 forms a phase leg, or a single-pole, double throw switch that can chop the input power in pulsed form, and store it in a magnetic element (inductor), then feed to the output. Fig. 2.2(a) shows the realization of one branch in the dc-3ϕac inverter system, such as the switch pair *a* and its load voltage V_{an}. In Fig. 2.2(a), if the load current is positive, only the diode D2 is used in switch S2 location while switch S1 only uses the transistor Q1. When the current reverse the direction, switch S1 uses the diode D1, while switch S2 needs the transistor Q2. In the following discussion, we'll discuss the case when the load current is positive, therefore the only meaningful component in the phase leg is a transistor and a diode, such as that shown in Fig. 2.2(b). Since both transistor and diode are periodically 'on' and 'off', they themselves are also frequently called switches. A transistor is a switch with forced turn-off capability, while a diode is a switch that can only be turned off by commutation of the current. The load current, within one switching cycle, can be considered constant because the existence of filter inductor. Hence in many discussions the load current is considered a current source.

When transistor Q1 is on, it conducts current of inductor load L and diode D2 blocks the DC voltage V_{source}. When Q1 is turned off, diode D2 conducts the current of inductor L and transistor Q1 blocks the DC voltage V_{source}. If these switches are ideal, it will take no time to turn on and turn off, so there is no turn on and turn off losses. But in reality, non-ideal transistors and diodes are used to fulfill the switch function. This causes some issues worth discussion here.

Forward Voltage Drop (V_F): When the transistor or diode conducts certain amount of currents, a minimum voltage must exist on the transistor or diode. This voltage is defined as device's forward voltage drop (V_F). The product of V_F and forward conducting current constitutes the conduction power loss.

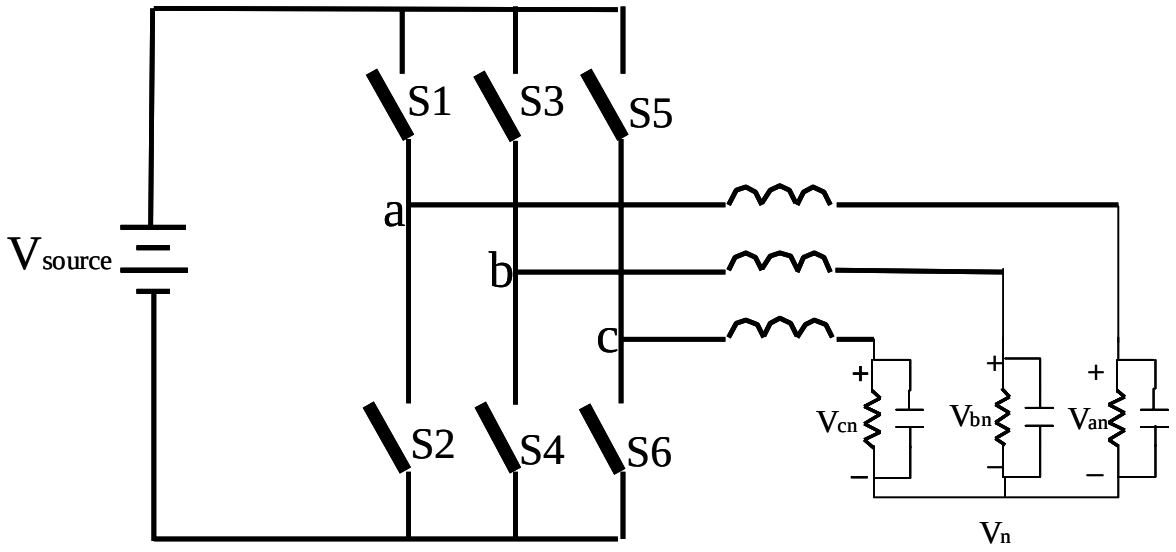


Fig. 2.1 The dc-3ϕac inverter system.

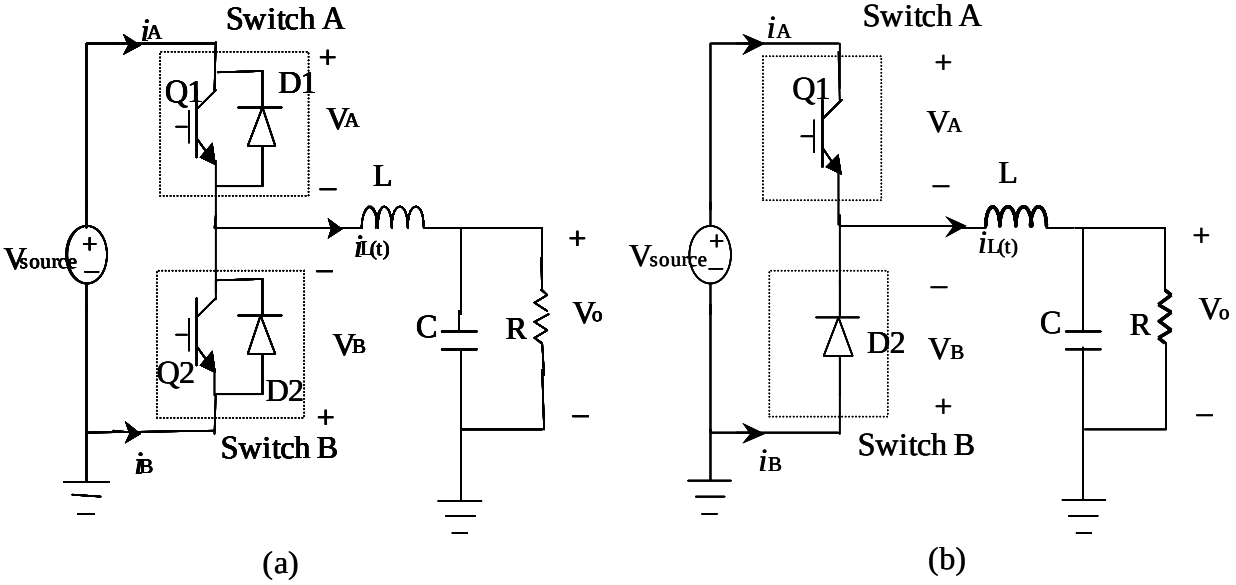
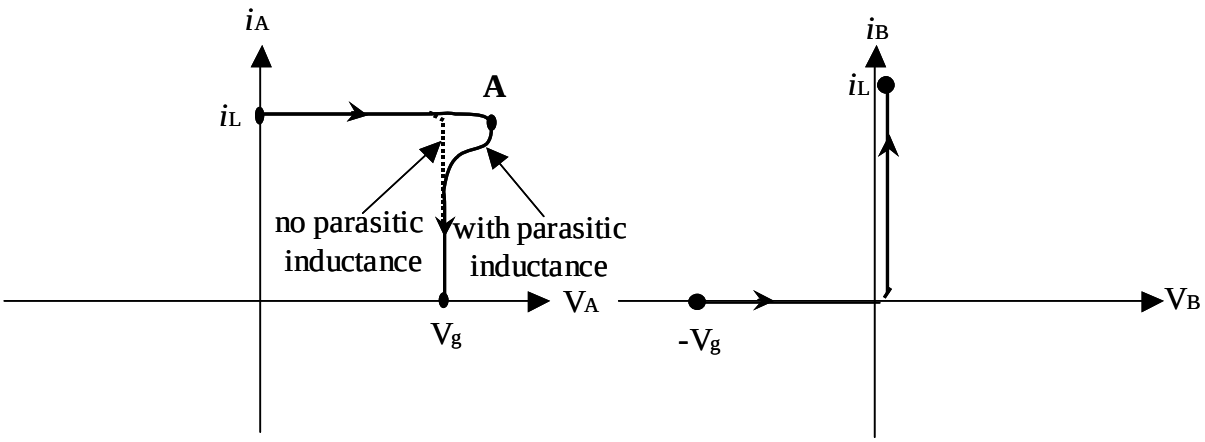


Fig. 2.2 The circuit realization branch in the dc-3ϕac inverter system (a) the transistor realization and (b) the simplified circuit when the load current is positive .

Turn-off Process and RBSOA: Due to the inductive load nature of power electronics application, such as the inverter system shown in Fig.2.2(b), the transistor Q1 and diode D2 both are subject to high power stress during turn-off operation. During the turn-off of Q1, the voltage across Q1 increases until it reaches V_{source} and then the current of Q1 decreases because D2 starts to turn on. Fig. 2.3 shows the locus (trajectory) of Q1 during turn-off and the corresponding locus of D2 during its turn-on. Fig. 2.4 shows the corresponding time-domain voltage and current waveforms of Q1 and D2. From Fig. 2.3, it is clear that during the turn-off of Q1, because of the voltage overshoot caused by parasitic inductance, voltage on the Q1 will exceed the DC voltage V_{source} while the current is still the inductor current I_L. The reverse biased safe operation area (RBSOA) [2,3] of a transistor refers to the current-voltage boundary within which the device can be turned off without failure. That means if the highest voltage and highest current point A of Q1 exceeds the RBSOA of Q1, the device will fail. It is important to emphasis that the RBSOA, such defined is a collection of failure points in the V-J plane. Practical system design require device de-rating to allow the device be turned off well within the RBSOA.

Turn-off Energy (E_{off}): From Fig. 2.4, the integration of the product of the device voltage and current during the turn-off is defined as the device's turn-off energy loss (E_{off}).

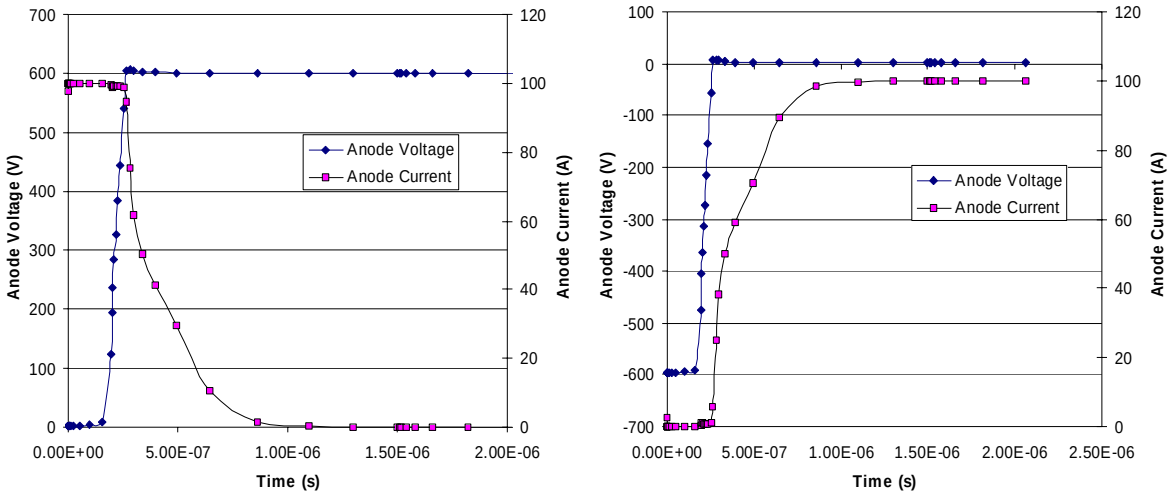
Turn-on Process and FBSOA: During the turn-on of the Q1, diode D2 turns off. If there is no other inductance presented in the system beside the load inductor L in Fig. 2.2(b), the switch Q1 current will increase very rapidly to the load current I_L. At the same time, the diode current decreases to zero. During this time, the voltages on Q1 and D2 are unchanged. Due to the reverse recovery property of semiconductor diode, which refers to the temporary current conduction capability of the diode in the reverse direction, the current in D2 will reverse direction and the current in Q1 will exceed I_L. Due to the high dI/dt in this current commutation process, diode reverse recovery current can be extremely high, causing a high current overshoot in Q1. Fig. 2.5 shows the locus of Q1 during turn-on. From Fig. 2.5, during the Q1 turn-on, because of the reverse recovery of the diode D2, the current of Q1 will exceed the inductor current I_L. A large locus or trajectory exists for the transistor Q1.



(a). The dynamic switching locus of Q1 during turn-off, large stress is experienced

(b). The dynamic switching locus of D2 during turn-off small stress is experienced

Fig. 2.3 The locus of the Q1 and D2 during turn-off of Q1.



(a). Turn-off waveforms of Q1

(b). Turn-on waveforms of D2

Fig. 2.4 The current and voltage waveforms of Q1 during turn-off and D2 during turn-on.

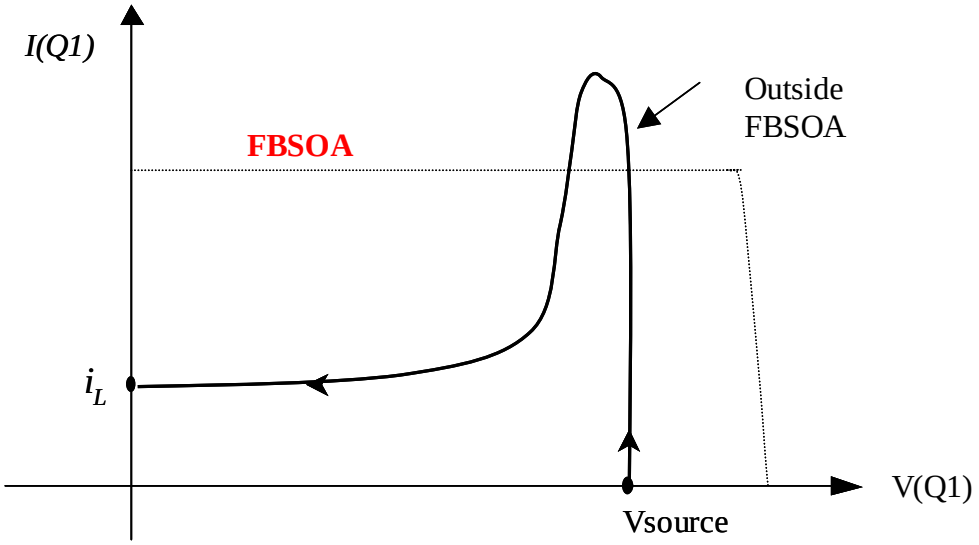


Fig. 2.5 The voltage-current trajectory of Q1 during its turn-on (large current overshoot exists due to diode D2 reverse recovery).

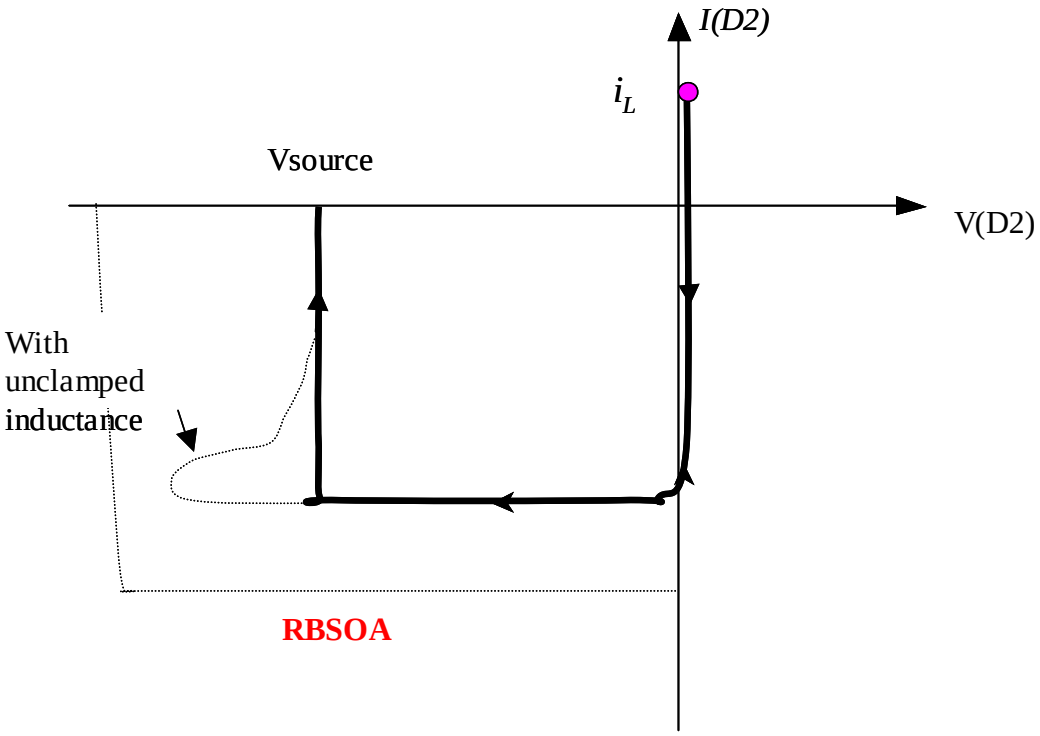


Fig. 2.6 The diode D2 trajectory during its turn-off (a definition of RBSOA can be made for the diode and the effect of unclamped inductance will result in voltage overshoot).

The forward biased safe operation area (FBSOA) of Q1 is defined as the maximum voltage-current boundary it can operate without destruction during DC or pulsed forward biased operation. Q1's turn-on locus therefore passes through its FBSOA region with a speed determined by the current commutation rate from D2 to Q1 (i.e. dI/dt). A square and large FBSOA is useful to allow high dI/dt commutation and to protect the transistor Q1 when abnormal situation occurs, such as to support the turn-on when the load is short circuited (i.e. L_{load} =0). If the device has no FBSOA or too small FBSOA, when it turns on with high dI/dt or when the load is short-circuited, the current will increase to large values exceeding its FBSOA and the device will fail. But as for the devices with large FBSOA, it can support a large voltage and current during forward conduction mode (typically in short pulses) and the turn-on would be safe.

It is therefore clear that a large FBSOA is desirable for a switching transistor from the turn-on point of view. It is also important to emphasis that the FBSOA defined here refers to the collection of failure points in forward biased condition. Due to the impact of the temperature rise, FBSOA is frequently plotted for DC and pulsed conditions. The turn-on process requires the device having a large pulsed FBSOA or FBSOA determined without considering thermal coupling effect since the turn-on process typically finishes within sub-microseconds.

Power semiconductor transistors can be classified into two groups based on whether it has a FBSOA or not. Devices such as BJT, IGBT and power MOSFET have FBSOA because they all have an active region in which the device can operate at high voltage and high current. Devices like thyristor and MCT have no FBSOA region because they can only work in the latched forward conduction mode (low voltage and high current) or cut-off mode (low current, high voltage). They cannot operate in the active region or high voltage and high current region, even for a very short pulse. Figure 2.7 shows the I-V characteristics of an IGBT, clearly showing the stable operation point available in the high voltage, high current region (active region). The avalanche points are used to define the short pulse (<10 us) FBSOA boundary.

During the turn–on of Q1, diode D2 turns off and suffers a strong stress as indicated by the large locus shown in Fig.2.6. A definition of diode's RBSOA can therefore be made similar

to the situation of the switch Q1. On the other hand, when diode turns on, it has a very small trajectory shown in Fig. 2.3(b), therefore, there is no requirement for diode to have a FBSOA (it indeed does not have one).

Modern Definition of FBSOA: The FBSOA definition above corresponds to the collection of failure points in device forward active region. This definition has been widely used in the 70s when the only power device with FBSOA is the power BJT. The FBSOA failure points in the BJT correspond to the BV_{CEO} points at high currents, typically limited by the second breakdown.

Modern power device such as IGBT and power MOSFET can withstand high voltage and high current up to the avalanche breakdown voltage point. The highest current achievable in the IGBT or MOSFET, on the other hand, corresponds to the saturation current $I_{sat(max)}$ when the gate voltage is at its maximum. This gate voltage is typically +15V in order to avoid gate oxide breakdown. Under such situation, the maximum current achieved, $I_{sat(max)}$, is not the failure current, but rather the self-limiting current at V_{gmax}. Device manufactures frequently use this current as the FBSOA's current boundary. It is therefore important to notice that this FBSOA definition is a practical one because it means the device cannot reach higher current due to current limiting. Fig.2.8 shows this practical, modern definition of the FBSOA.

SCSOA: Since modern devices such as IGBT and power MOSFET has a FBSOA defined by the avalanche voltage and the saturation current at V_{gmax}, the current boundary portion of the FBSOA corresponds to a non-failure limiting boundary. This allows device to operate in short circuit for a short period of time. The only limitation here is the length of the time because the device temperature will rise quickly due to high power stress since $P_{short\text{-}circuit} = V_{source} * I_{sat(max)}$. Eventually the device temperature will rise above a critical temperature at which the junction disappears. This temperature is typically $600^{o}C$ for silicon devices. Modern power device therefore defines the short-circuit SOA (SCSOA) as the time allowed (in microseconds) in short circuit operation. Since $P_{short\text{-}circuit} = V_{source} * I_{sat(max)}$, a large SCSOA requires lowering $I_{sat(max)}$. This would mean that a small or a flat rectangular FBSOA, based on the modern definition shown in Fig. 2.8, is desirable.

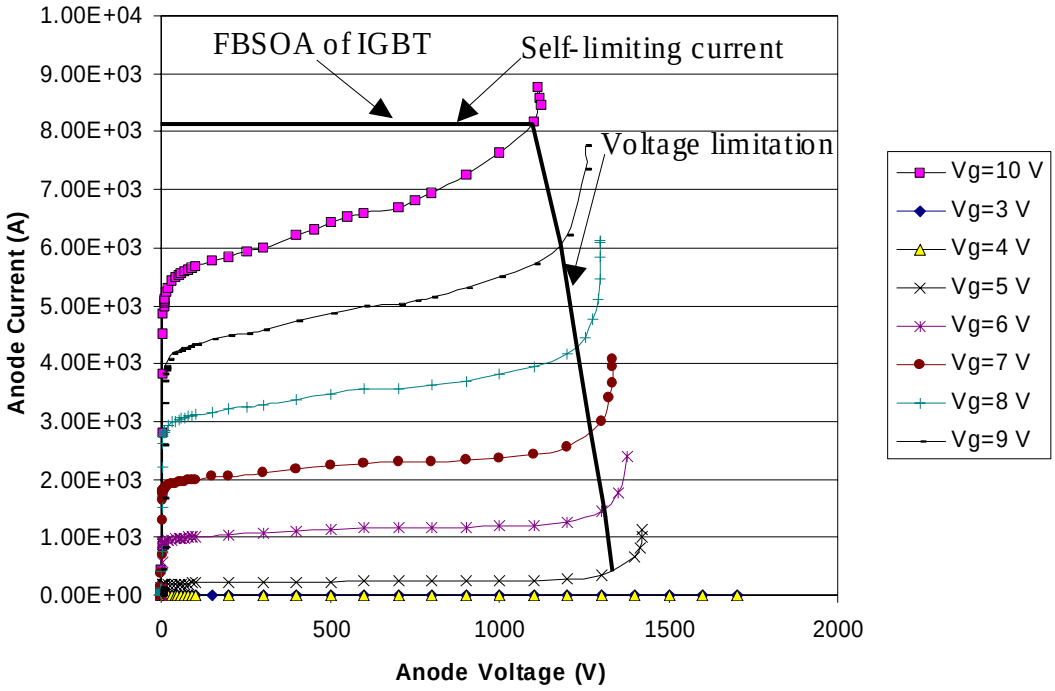


Fig. 2.7 An IGBT forward I~V characteristics showing the definition of the FBSOA determined by the avalanche voltage at high current (this FBSOA is only achievable in small pulse condition).

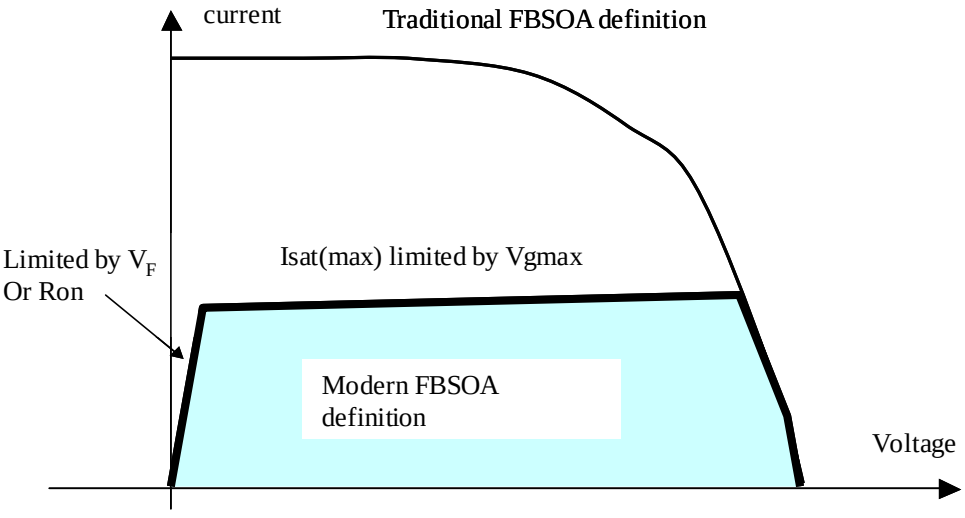


Fig. 2.8 Modern and tradition FBSOA definition.

Turn-on Energy (E_{on}): The integration of the product of device voltage and current during the turn-on is defined as device's turn-on energy loss (E_{on}). Device using external dI/dt snubber has very low turn-on energy because a small V-I trajectory or V-I overlaps in the time-domain.

2.2 Insulated Gate Bipolar Transistor (IGBT)

In order to combine the low forward voltage drop of the power BJT and the high input impedance of the power MOSFET, a new power device, the Insulated Gate Bipolar Transistor (IGBT), was invented [4,5]. The cross section view of an IGBT is shown in Fig. 2.9. It is fabricated using the self-aligned DMOS process. The IGBT is composed of a wide base PNP bipolar transistor and a lateral N channel MOSFET between the bipolar transistor's base and collector (the emitter terminal of the IGBT). The equivalent circuit of the IGBT is also shown in Fig. 2.9.

The IGBT not only has the forward blocking capability, but also the reverse blocking capability. When the voltage between the gate and the emitter is zero, a positive bias can apply to the collector of the IGBT with no current through the device. That is the forward blocking. The voltage is supported through the junction J2 shown in Fig. 2.9. At the same gate and emitter voltage condition a negative voltage can also apply to the collector of the IGBT. That is the reverse blocking state. The voltage is supported through the junction J3. In DC or voltage source inverter applications, the reverse blocking of the IGBT is not needed. This enables the optimization of only the forward blocking capability. An N+ buffer layer can be added adjacent to the P+ collector. The N+ buffer layer enables the use of a shorter N- region thickness and the punch through operation during the forward blocking state.

A positive gate bias can create an inversion layer on the surface of the P region and electrons will inject into the N- region from the N+ emitter for positive collector voltages. The IGBT enters its forward conduction mode. These injected electrons provide the base drive current of the vertical PNP transistor and induce the holes be injected from the P+ collector into the N- region. If the current density becomes large, the injected electrons and holes concentration

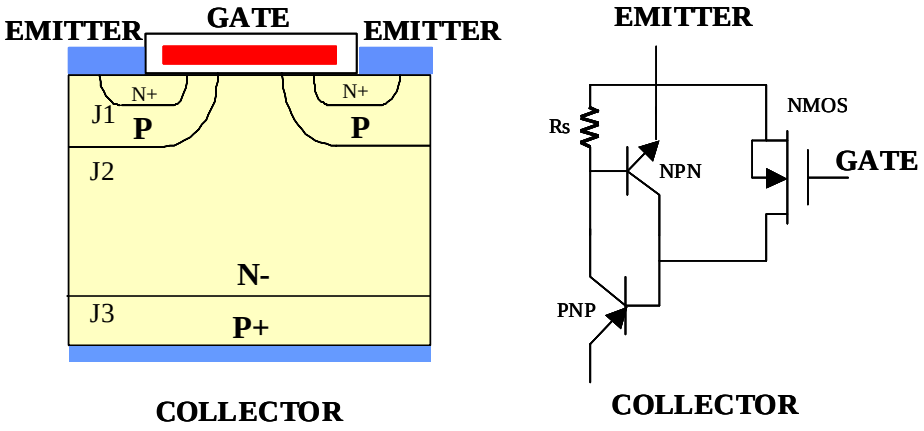
become large and exceed the N- region doping concentration. Charge neutrality requires that the concentrations of holes and electrons become equal. These concentrations can therefore become far greater than the background doping level and hence significantly lowers the resistivity of the device. This phenomenon is called conductivity modulation and is extremely important to allow a high current density through the power device with low forward drop. Because of the conductivity modulation, the forward voltage drop of the IGBT is approximately that of a P-I-N diode plus a series MOSFET. As long as the gate bias is large enough to ensure the MOSFET working in its triode region, the IGBT exhibits an excellent current carrying capability. If the MOSFET enters its saturation region, the voltage drop across the MOSFET becomes significant and the current is limited by the MOSFET too. This causes the IGBT to enter its saturation region (active region). Once saturated, the current will no longer increase with the voltage and a high voltage can be applied to the IGBT. This high voltage is supported by the main junction J2. A typical simulated output characteristics of a 1200 V IGBT is shown in Fig. 2.10(a) and the low voltage region when the gate voltage is 10 V is shown in Fig. 2.10(b). The current saturates at higher current density when the gate voltage increases. At a current density of 100 A/cm^2 the simulated IGBT exhibits a forward drop of only 1.8 V. Fig. 2.11 shows the typical carrier distribution of the 1200 V IGBT at current density of 100 A/cm^2. Compare with the N- drift region background doping concentration of 5×10^{13} cm^{-3} it is clear that the conductivity modulation happened in the N- drift region and the electron and hole concentration became much larger than the native doping level. And in order to keep the charge balance in the N- drift region, the hole and electron concentration are forced to be the same. However, since the injection from the N+ emitter of the IGBT is through a series NMOSFET, the injected electrons level is much less than the holes injected from P+ collector into the N- drift region. That is why the carrier concentration close to the collector (distance above 110 um) is much larger than that near the emitter (distance below 15 um). This type of carrier profile in IGBT is the major reason why forward voltage drop of a high voltage IGBT can increases significantly. Increase carrier lifetime is needed to maintain low forward voltage drop for very high voltage IGBTs. However, a high lifetime will cause the turn-off energy loss, E_{off}, to increase. Therefore a fundamental trade-off

between V_F and E_{off} exist. This trade-off curve is frequently referred as technology curve because it represents the technology of different IGBT design. Punch-through (PT) IGBT design typically will result in a better trade-off than non-punch-through (NPT) IGBT. PT IGBT, a shorted N- region can be used because of the use of an N+ buffer layer. In PT IGBT, the N+ buffer layer also serves the purpose of reducing the heavily doped P+ collector injection efficiency. To adjust the device speed (E_{off}), lifetime control is also used in PT IGBT. In the NPT IGBT, long N- region is used with no lifetime control. P+ collector concentration is lowed to control the injected holes to adjust the device speed (E_{off})

To turn off the IGBT, the gate voltage is reduced to zero. This cuts off the channel of the MOSFET and stops providing the base current for the PNP transistor. The device starts to turn off. Because of the conductivity modulation of the N- region, the turn-off can be separated into two parts. When the gate voltage is suddenly removed, the channel electron current of MOSFET is cut off suddenly. That makes the voltage rise quickly followed by a sudden collector current drop. After this point, there is a current tail caused by the stored minority carriers in the undepleted N- region. These carriers support the continouse flow of the open-base PNP current and can be removed only by the recombination.

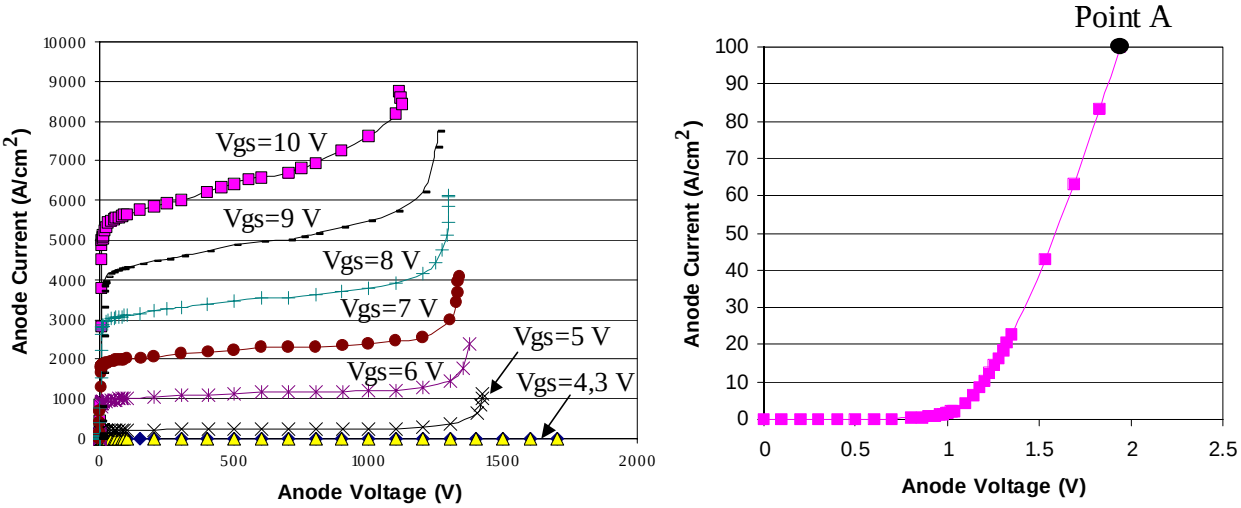
A parasitic thyristor exists in the structure of the IGBT shown in Fig. 2.9. It is formed by the junctions J1, J2 and J3. This thyristor structure can be triggered into latch up state at high current density and makes the IGBT gate lose its control capability. The trigger condition is reached when the hole current flowing in the P region is large enough to forward bias the junction J1. In order to decrease such possibility N+ emitter in IGBTs is shorted to the P region by the emitter contact as shown in Fig. 2.9. Adding a deep P+ region under the N+ emitter also helps suppressing the latch up of the parasitic thyristor by reducing the P region resistance.

Low forward voltage drop, high input impedance and gate controlled output characteristic of the IGBT make it a superior power device compared to the power BJT and power MOSFET. However, if the blocking voltage increases to above 2 kV, the forward conduction loss of IGBT will become large and not competitive with other power devices such as the GTO.



(a) (b)

Fig. 2.9 The cross-section view of the IGBT (a) and its equivalent circuit (b).



(a) (b)

Fig. 2.10 The IGBT output characteristics of the high voltage current saturation region (a) and the low voltage region (b).

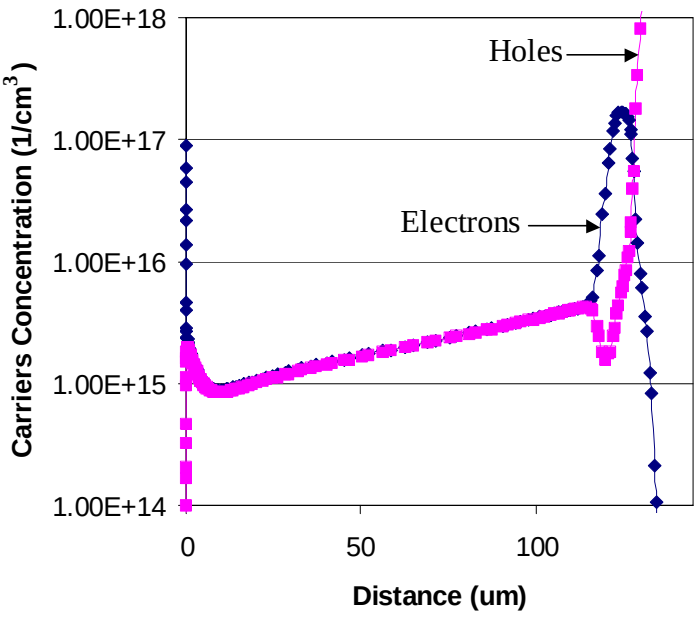


Fig. 2.11 Typical carriers distribution of a 1200 V IGBT when the current density is 100 A/cm^2 shown in Fig. 2.10 as point A.

2.3 MOS-Controlled Thyristor (MCT)

IGBT's conductivity modulation relies mostly on the anode (collector) side carrier injection. The injection from the cathode (emitter) side is very weak. This causes high V_F for high voltage IGBT. 600 V IGBT has a forward voltage drop at 2 V or lower, for 6 kV IGBT, the forward voltage drop increases to more than 6 V.

This situation can be improved if the cathode side injection of electrons can be enhanced. This results in the proposal of using a four-layer thyristor structure with MOS control. One of such proposals is the MCT. The cross section of the MCT [6,7] and its equivalent circuit are shown in Fig. 2.12. A thyristor structure is formed by the junction J1, J2 and J3 in the MCT. The current flows through the thyristor when the device is on and can be switched between the on and off state by applying different gate bias. An n-channel and a p-channel MOSFET with a shared gate are integrated on the surface in the P region. When a positive voltage is applied to the gate, an inversion layer is formed in the n-channel MOSFET. Electrons inject into the N- region from the N+ cathode through the inversion layer. That provides the base current for the vertical PN-P+ bipolar transistor. At the same time, the holes collected by the reverse biased junction J2 flow through P region. This hole current raises the potential of the P region and forward biases the junction J3. The thyristor enters its latch up state. After the thyristor is triggered into latch up state, the n-channel MOSFET loses the control over the MCT. The IV characteristic of MCT is therefore independent of the gate voltage when it exceeds the threshold voltage of the n-channel MOSFET. Fig. 2.13 shows the IV characteristics of the MCT at different gate voltage. No current saturation is observed in the on-state, hence there is no FBSOA in the MCT. When the gate voltage is above the threshold voltage of the MCT, the device changes from off-state into on-state in an uncontrolled manner (dI/dt controlled by external inductor instead of the transconductance g_m. Fig. 2.14 shows the typical carrier concentration distribution of 1200 V MCT comparing with that of the IGBT at current density of 100 A/cm^2. Because the thyristor structure in the MCT enters its latching state, the electrons injected from N+ cathode is almost the same as the injection from the P+ anode into the N- drift region.

Therefore a MCT is a double injection bipolar device while an IGBT is a single injection device. It is clear the carrier modulation of the IGBT is much less than that of the MCT. Hence, at the same current density the MCT has lower forward voltage drop than that of the IGBT. This is also true for all thyristor based devices because of the stronger conductivity modulation. Because of the stronger conductivity modulation in MCT, the MCT has better E_{off}–V_F trade-off than an IGBT. Fig. 2.15 shows calculated technology trade-off curve for 1200 V MCT and IGBT. This conclusion holds true for other thyristor based power device.

Applying a negative voltage to the gate can turn off the MCT. A negative gate voltage creates an inversion layer in the p-channel MOSFET. The N+ cathode is then shorted to the P region and the electron injection from N+ stops. This inversion layer also diverts the hole current from the P region into the cathode. The holding current of the thyristor increases and the thyristor is forced to turn off [8].

Because the MCT conducts current through a thyristor structure, the forward conduction characteristic is close to a conventional thyristor. Hence, the current carrying capability is better than that of the IGBT. However, the MCT is a five-layer device and requires a triple diffused fabrication process. This makes the fabrication difficult. Furthermore, the MCT lacks the FBSOA, hence lacks the full gate control capability found in the power MOSFET and the IGBT.

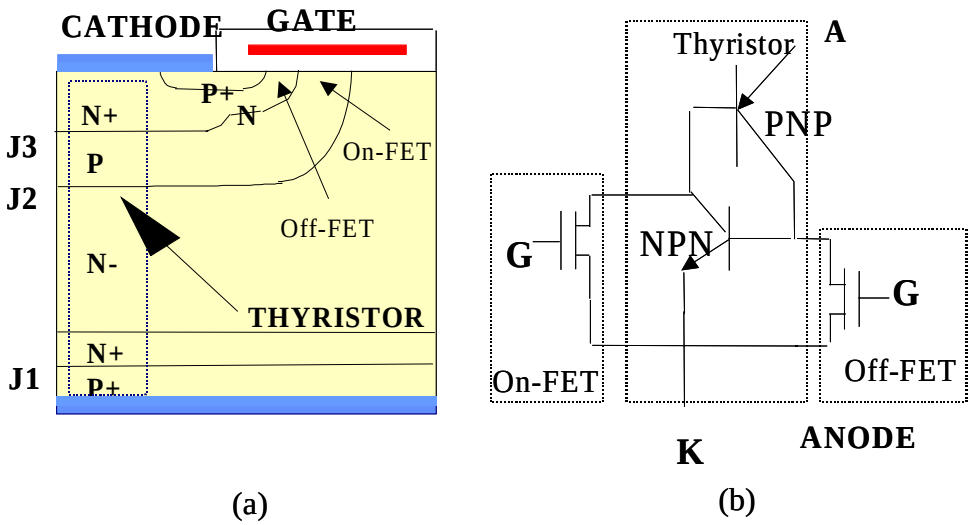


Fig. 2.12 The cross-section view of the MCT (a) and its equivalent circuit (b).

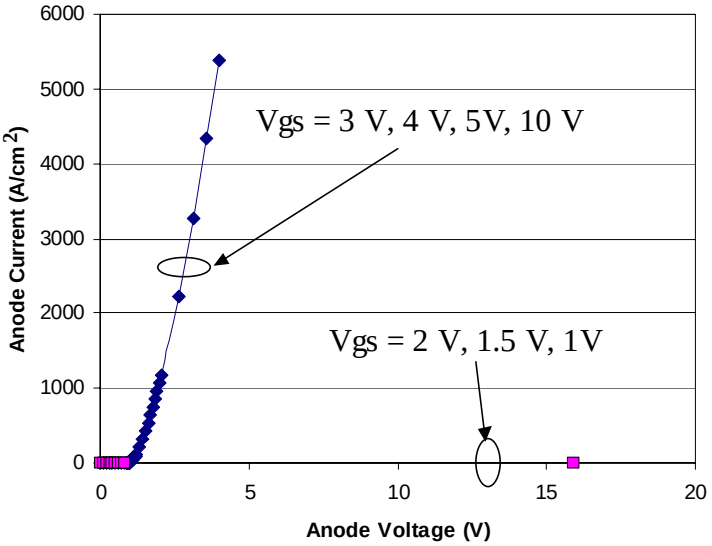


Fig. 2.13 The output characteristics of the MCT.

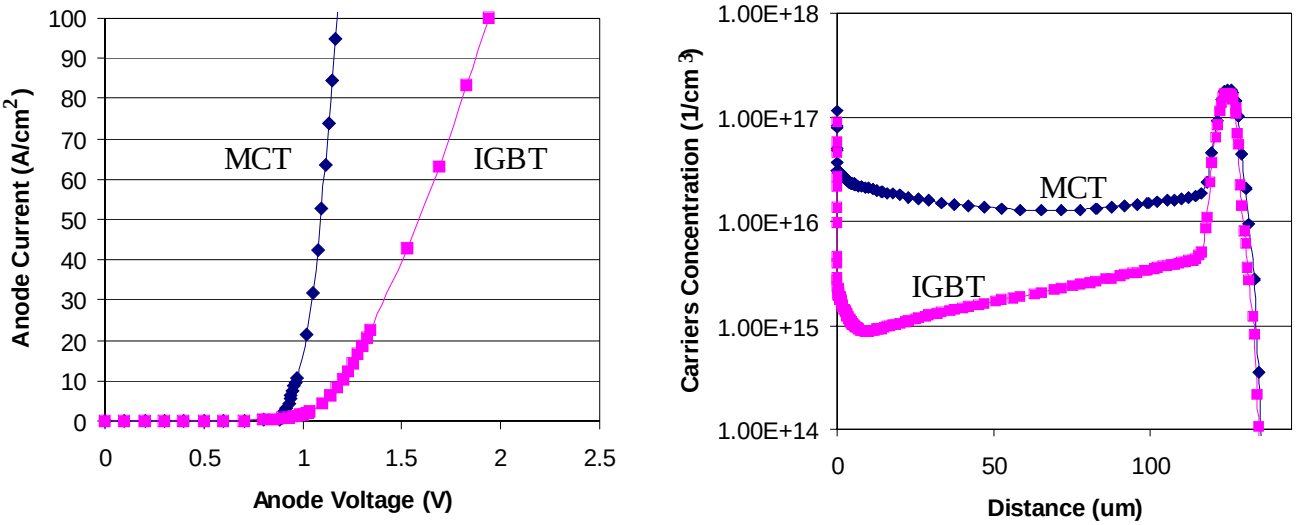


Fig. 2.14 The forward voltage drop (a) and the typical carriers concentration distribution (b) of 1200 V MCT when the current density is 100 A/cm^2 comparing with the IGBT.

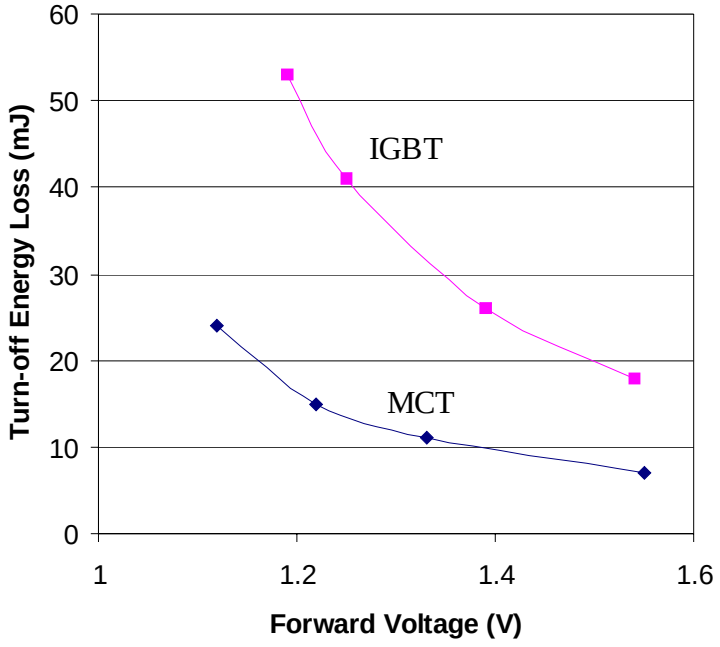


Fig. 2.15 Tradeoff between forward voltage drop and the turn-off loss per cycle when the current density is 100 A/cm^2 and turn-off voltage is 600 V.

2.4 Emitter Controlled Thyristor (ECT)

The MCT discussed above allows current flow through a thyristor structure to obtain a lower on-state voltage drop. However, it lacks the FBSOA, hence the controlled turn-on characteristic and current saturation capability. The MCT is therefore susceptible to current filament during both device turn-off and turn-on. For a high current MCT using multi-cell structure, if a non-uniform gate delay happens, there will be a small number of unit cells that will be turned off a little later than the other unit cells. The anode voltage of those unit cell rises while they are still in the on-state. High current filament will happen in these slower cells. Fig. 2. 16 shows the difference between what happens in the MCT and that of the IGBT when the anode voltage rises. Current filament in the MCT is formed along path A' to B', while that happens in the IGBT along A to B. A much larger voltage ΔV(IGBT) is needed to form a smaller ΔI(IGBT) current filament, while a much smaller ΔV(MCT) is enough to form a very large ΔI(MCT) current filament. Therefore, the existence of the FBSOA is very important to the large area power device in order to survive a non-uniform turn-off. In other words, the FBSOA is important for achieving a large RBSOA.

In order to obtain the current saturation capability hence the FBSOA and at the same time keep the forward voltage drop low, many improved MOS gated thyristors have been invented. The Emitter Switched Thyristor (EST) [9] uses emitter-switch for current turn-off and offers current saturation capability. The current saturation capability in the EST is, however, limited by the breakdown voltage of a series n-channel MOSFET in its top structure, and its FBSOA is therefore very small due to low voltage limitaion. A modified EST structure, known as the Dual-Channel EST (DC-EST) [10,11] has a better FBSOA because the lateral n-channel MOSFET is replaced by two double diffused n-channel MOSFETs in series. However, the DC-EST's current can only saturate at a gate voltage slightly higher than the threshold voltage of the n-channel MOSFETs. Further, both the EST and the DC-EST [12,13] have a parasitic thyristor which affects their FBSOA as well as their RBSOA.

The Emitter Controlled Thyristor (ECT) is a new MOS gate controlled thyristor which exhibits superior on-state characteristic even at high voltage ratings and excellent current saturation capability [14]. The ECT represents a new concept to realize the control of thyristor, which is different from the MCT and EST. There are two major requirements in an ECT. An ECT must have a emitter switch in series with the thyristor, and a emitter-short switch in parallel with the emitter junction of the thyristor. Therefore two MOSFETs are needed. First, an emitter FET is needed to connect in series with the emitter of the thyristor. Second, another FET is needed to short the emitter to the cathode during turn-off. This latter switch is the so-called emitter-short switch. In some cases, a turn-on FET is needed to trigger the thyristor into the latching condition. Therefore, three FETs together with the thyristor are typically needed to realize the ECT.

According to how these FETs are integrated with the thyristor to realize the ECT, there are four different ECT structures proposed [15,16]. Fig. 2.17 shows the ECT with a MOS turn-on gate region similar to that of the MCT that wasn't shown here. The main thyristor is formed by junction J2, J3 and J4. The N+ emitter of the thyristor is connected to the cathode via a p-channel MOSFET (PMOS1) which is integrated on the top N region. A Floating Ohm Contact (FOC) shorts the N+ emitter and the P+ region acting as the source of the PMOS1. The FOC floating contact can transfer the N+ emitter electron current into P+ region hole current and make it flow through the PMOS1 channel into cathode. The upper P base region is connected to the cathode via another p-channel MOSFET (PMOS2) and the gate of the PMOS2 is tied to the cathode. Therefore the PMOS1 acts as the emitter switching FET and PMOS2 acts as the emitter short FET. Fig. 2.18 shows another ECT structure with a depletion mode n-channel MOSFET as the turn-on FET and an n-channel MOSFET as the emitter switching FET. The main thyristor is composed of the N+ emitter, P base region, N- drift region and the P+ anode. A FOC is also used to connect the N+ emitter of the thyristor with the drain of the NMOS1 to make the current flow through the NMOS1 into cathode. The upper P base region is connected to the cathode via the PMOS2 to realize the emitter short function. In this structure, NMOS1 acts as the emitter switching FET, NMOS2 acts as the turn-on FET and PMOS2 acts as the emitter short FET. Fig.

2.19 shows another ECT structure with a depletion mode n-channel FET as the turn-on FET and a p-channel MOSFET as the emitter switching FET. A FOC is also used to connect the N+ emitter of the thyristor with the source of the PMOS1. The upper p base region is connected to the cathode via PMOS2. Fig. 2.20 shows the fourth ECT structure with an external MOSFET as the emitter switching FET. The main thyristor is still composed of the junction J1, J2 and J3. Depletion mode NMOS1 is also used as the turn-on FET. The external NMOS2 connects the emitter of the thyristor to the cathode acting as the emitter switching FET. The emitter short function is realized using PMOS1.

The structures shown in Fig. 2.19 and in Fig. 2.20 will be studied in detail in the following two chapters. The devices are analyzed using numerical simulations and experimental device fabrication.

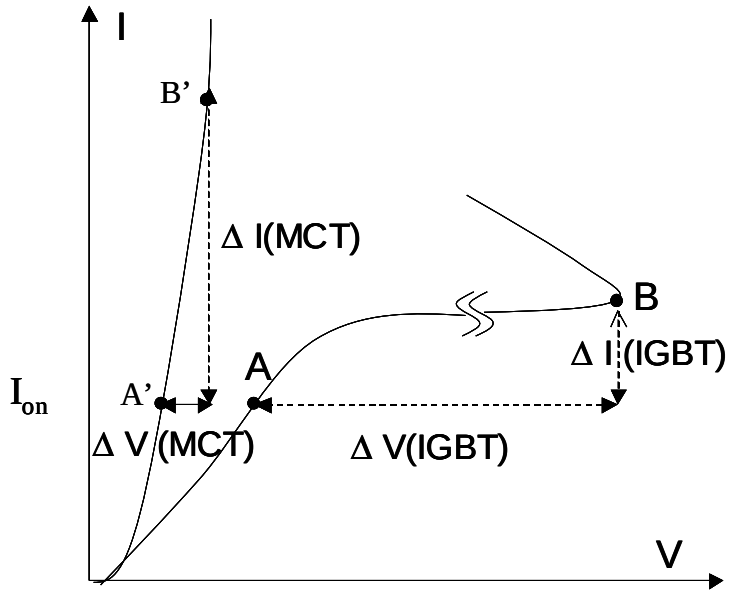


Fig. 2.16 The difference between what occurs in the gate delay cells of the MCT and that of the IGBT when the anode voltage rises.

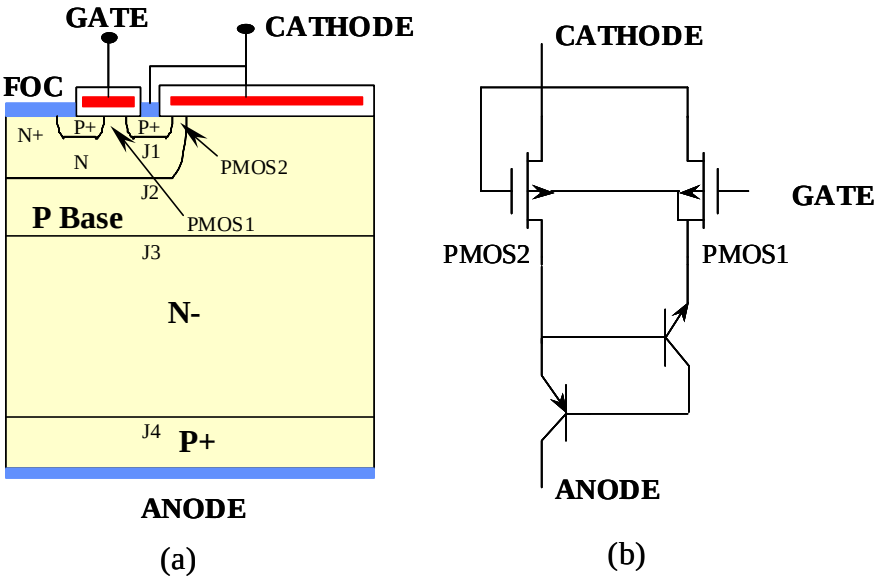


Fig. 2.17 The cross-section view of the ECT (a) and its equivalent circuit (b).

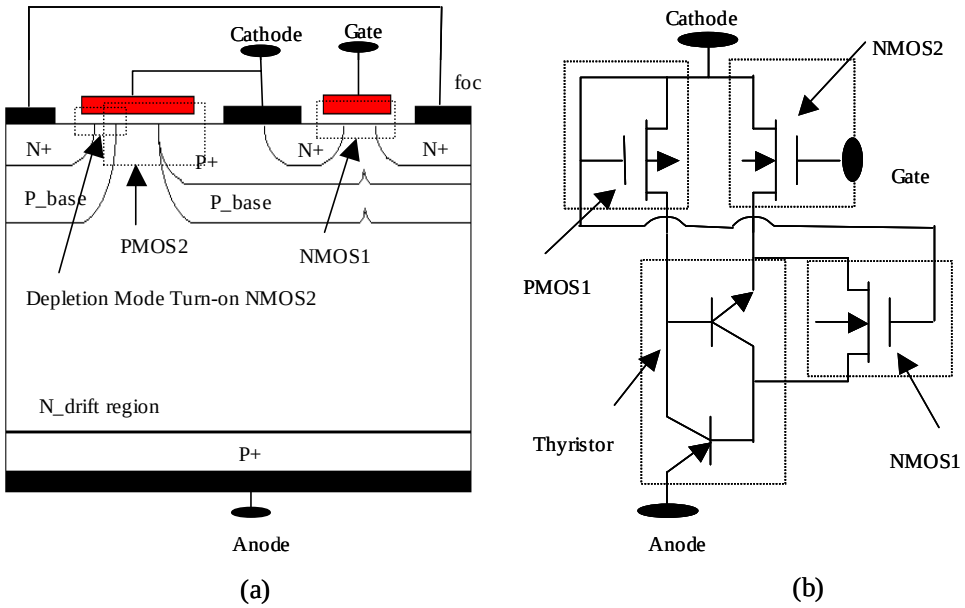


Fig. 2.18 The cross-section view of the ECT with an n-channel emitter switching FET (a) and its equivalent circuit.

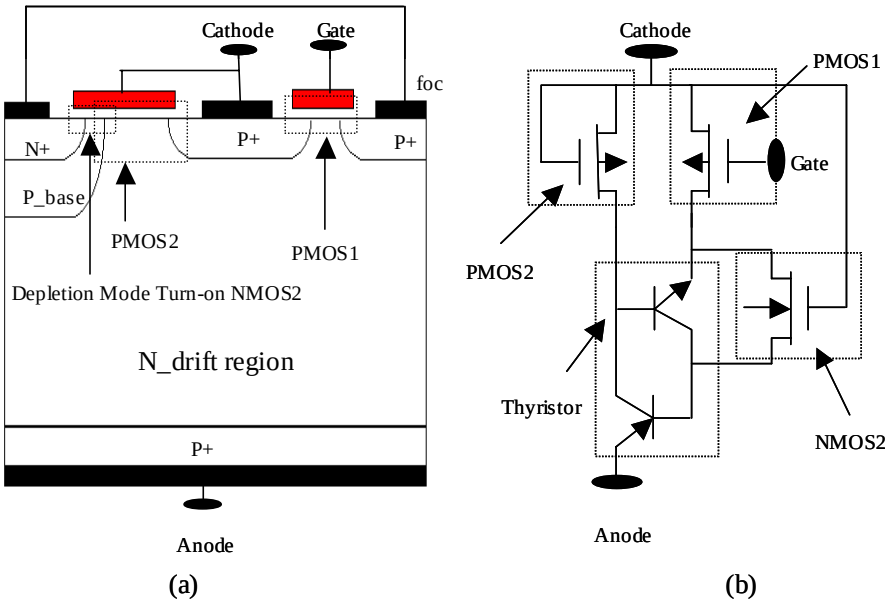


Fig. 2.19 The cross-section view of the ECT with a p-channel emitter switching FET (a) and its equivalent circuit.

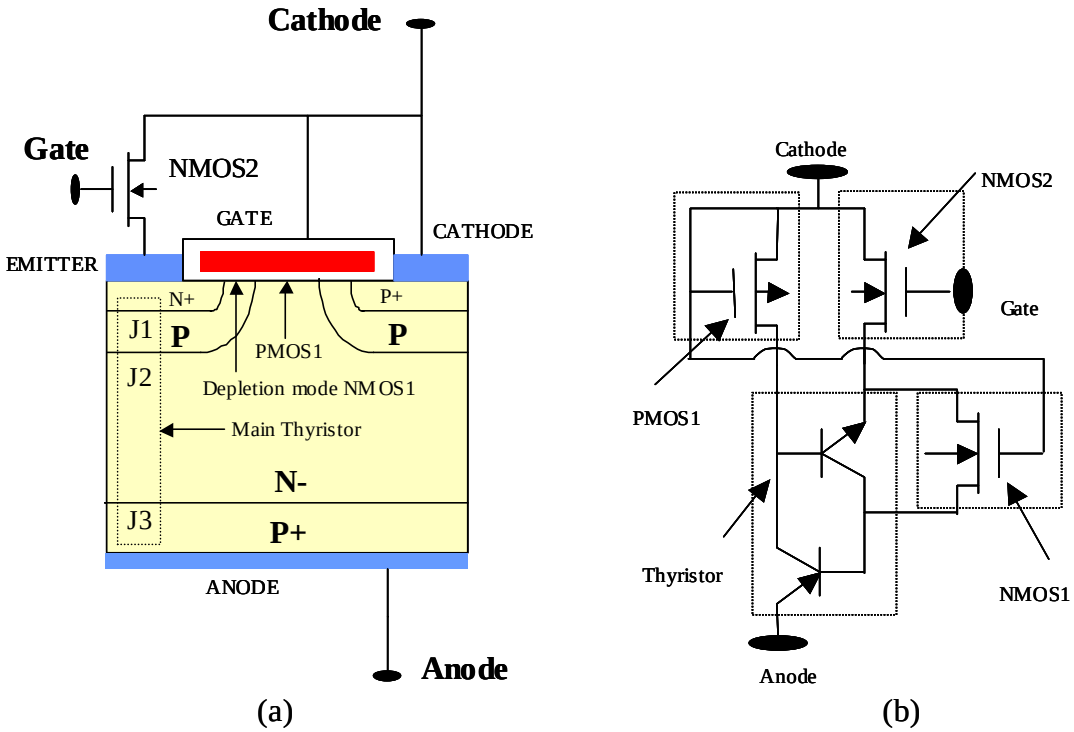


Fig. 2.20 The cross-section view of the ECT with external emitter switch FET (a) and its equivalent circuit (b).

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Chapter 3 Design and Fabrication of the 1200 V Emitter Controlled Thyristor

3.1 Introduction

For any power electronics application, the current saturation capability or FBSOA is one of the most important features for a power switch. It enables the device to be turned on and off in a controlled manner by changing the gate signal and it also provides the short circuit protection for the switch. Power semiconductor devices can be classified into two groups based on whether it has a FBSOA or not. Devices such as BJT, IGBT and MOSFET have FBSOA because they all have an active region. That means the device can operate at high current and high voltage simultaneously, and only limited by the thermal dissipation of the device. However, for the IGBT, enhancement in FBSOA can only be achieved by decreasing the channel density at the cost of a higher on-state voltage drop [1,2]. Devices like thyristor and MCT [3] have no FBSOA region because they can only work in the latched forward conduction mode (low voltage and high current) or cur-off mode (low current and high voltage). They cannot operate in the active region or high voltage and high current region, even for a very shot pulse. Comparing with the IGBT, the MCT has a much lower on-state voltage drop, but lacks the FBSOA [4,5]. That makes it difficult to protect the MCT under short-circuit condition. Also the gate voltage of the MCT cannot control the speed of the turn-on process. The turn-on of the MCT is usually too fast which results in a snappy reverse recovery in the associated diode.

When the IGBT is in its active region, the saturated current is given by [6]:

$$I_{sat} = \frac{1}{1-\alpha_{PNP}} \frac{\mu_{ns} C_{ox} W_{CH}}{L_{CH}} (V_G - V_T)^2 \qquad (3\text{-}1)$$

From this equation, the transconductance of the IGBT in the active region can be achieved by differentiation with respect to V_G:

$$g_m = \frac{dI_D}{dV_G} = \frac{1}{1-\alpha_{PNP}} \frac{\mu_{ns} C_{ox} W_{CH}}{L_{CH}} (V_G - V_T) \qquad (3\text{-}2)$$

The on-state voltage drop for the IGBT is given by [6]:

$$V_F = \frac{2kT}{q} \ln\left(\frac{I_C d}{2qW_{CH} D_a n_i F(d/L_a)}\right) + \frac{(1-\alpha_{PNP}) I_C L_{CH}}{\mu_{ns} C_{ox} W_{CH} (V_G - V_T)} \qquad (3\text{-}3)$$

It can be seen from the above three equations, for a given channel length (L_{CH}), the saturation current and transconductance of the IGBT is proportional to the channel density. Here, channel density is defined as the total channel width (W_{CH}) within a unit area. The saturation current of the IGBT can be lowered by reducing the channel density, so does the transconductance. However, the on-state voltage drop of the IGBT will increase. Hence there is a trade-off between V_F and I_{sat}.

When the MCT is in its on-state, it can maintain such state by the regenerative action between the two coupled transistors within the MCT structure as long as the current is above its holding current. Usually the holding current of the MCT is far below the operating current density, so the anode current level of the MCT is independent to the gate bias during the turn-on transient. In order to provide controllable turn-on and short-circuit capability, novel devices with FBSOA should be developed.

In this chapter, a novel ECT is studied which achieves superior current saturation capability and lower forward voltage drop at the same time. First, the device structure and operation are discussed with the help of numerical simulations. Then a fabrication process is developed. Results from device fabrication are then shown and discussed.

3.2 ECT Characteristics

3.2.1 Device Structure and Current Saturation Mechanism

The cross-section view of the novel, three terminal ECT [7] is shown in Fig. 3.1. The ECT has a 4-layer PNPN thyristor structure. A p-channel MOSFET (PMOS1) is integrated on the top of the N- drift region which provides emitter switch function. A Floating Ohmic Contact (FOC) metal strap is used to connect the P+ source of the PMOS1 and the upper N+ emitter of the PNPN thyristor. The FOC provides the bridge for transferring emitter currents of the upper NPN transistor into source of the PMOS1, which then flows through PMOS1 channel and into the cathode contact. An n-channel MOSFET (NMOS2) is also formed at the surface of the ECT. This MOSFET needs to be depleted and acts as the turn-on FET. Between the turn-on NMOS2 and the PMOS1 there is another P channel MOSFET (PMOS2) with the upper P base as its source. PMOS2 provides the emitter short function. The PMOS2 and the NMOS2 share the same gate that is tied to the cathode contact. Therefore, the ECT is a three-terminal MOS-gate controlled power device and can be controlled easily by applying a signal on the gate just as the IGBT.

If a negative voltage whose value is larger than that of the threshold voltage of the PMOS1 is applied to the gate electrode and another positive voltage is on the anode electrode, the ECT will be turned on. The depletion mode NMOS2 is in its on state all the time and will inject electrons into the lower N- drift region of the thyristor. Then the thyristor is triggered into the latch-up state. The current of the thyristor collected by the upper N^+ emitter first flows laterally into the cathode through the FOC metal strap and then into the PMOS1. Therefore, the forward voltage drop of the ECT is that of a thyristor plus that of the PMOS1.

With the increase of the current, the voltage at the FOC metal strap, V_{FOC}, will increase because of the channel resistance of the PMOS1. The voltage of the upper P base of the thyristor, V_{Pbase}, will increase too because $V_{Pbase}=V_{FOC}+0.7$ V. So will V_{Nbase}, the voltage of the lower N drift region of the thyristor adjacent to the P base region. When the V_{Nbase} is larger than $-V_{PT1}$ (the threshold voltage of PMOS2 which is less than zero), the PMOS2 turns on automatically. Hole current will then be diverted from the upper base through PMOS2 into the cathode. The upper NPN transistor's gain, α_{npn}, hence reduces because of the decrease of the base current of

the transistor. If the reduction of the upper NPN transistor current gain, $\Delta\alpha_{npn}$, can't be compensated by an increase of the lower PNP transistor current gain, $\Delta\alpha_{pnp}$, so that:

$$\alpha_{npn0} + \alpha_{pnp0} - \Delta\alpha_{npn} + \Delta\alpha_{pnp} \leq 1 \qquad (3\text{-}4)$$

the ECT will come out of its latch-up state. Then the current of the thyristor will tend to decrease, and so will the V_{FOC}. However, the decrease of the V_{FOC} means a reduction of the diverted hole current and the reduction of the $\Delta\alpha_{npn}$. Hence, the ECT enters latch-up state again. Such a negative feedback mechanism therefore requires the main thyristor to operate at the boundary of the latching condition. Under this condition, the anode voltage keeps increasing without significant anode current increase. The increased anode voltage is supported by the main junction of P base and N- drift region. Hence, the current saturation capability is obtained in the proposed ECT. Once entering the saturation region, the NPN and PNP transistor operates in their active regions instead of their saturation regions. The emitter FET PMOS1 and emitter short FET PMOS2 are both in conduction in the ECT saturation region.

The ECT can be turned off by increasing the gate voltage to zero or a positive value in the PMOS1, which cuts off the emitter current path. All currents are then forced to divert to the cathode by the PMOS2. Unlike the EST and the DC-EST [8], no uncontrolled parasitic thyristor limits the RBSOA of the ECT.

3.2.2 Device Simulation

A punch-through (PT) type ECT is investigated by the two-dimensional device simulator MEDICI [9]. The thickness of the N- drift region is 120 um with a doping concentration of 1×10^{14} cm^{-3} in order to obtain the 1200 V blocking capability. The P+ region has a surface concentration of 2×10^{19} cm^{-3} to form the PMOS1. The P base region doping is critical that must satisfy the requirement of the blocking capability and at the same time make the NMOS2 depleted. A surface concentration of 2×10^{16} cm^{-3} and junction depth of 10 um was finally chosen to satisfy the design. The upper N+ emitter of the thyristor has a surface concentration of 2×10^{19} cm^{-3} and a junction depth of 2 um. The threshold voltage of the depletion PMOS1 was designed to be – 1.8 V. In the simulation, a minority carrier lifetime of 1.75 us was used to describe the N-

drift region. The doping profile along the cut line AA' shown in Fig. 3.1(a) is shown in Fig. 3.2. Fig. 3.2(a) shows the doping profile of the top cell and Fig. 3.2(b) shows the doping profile of the buffer layer and anode region.

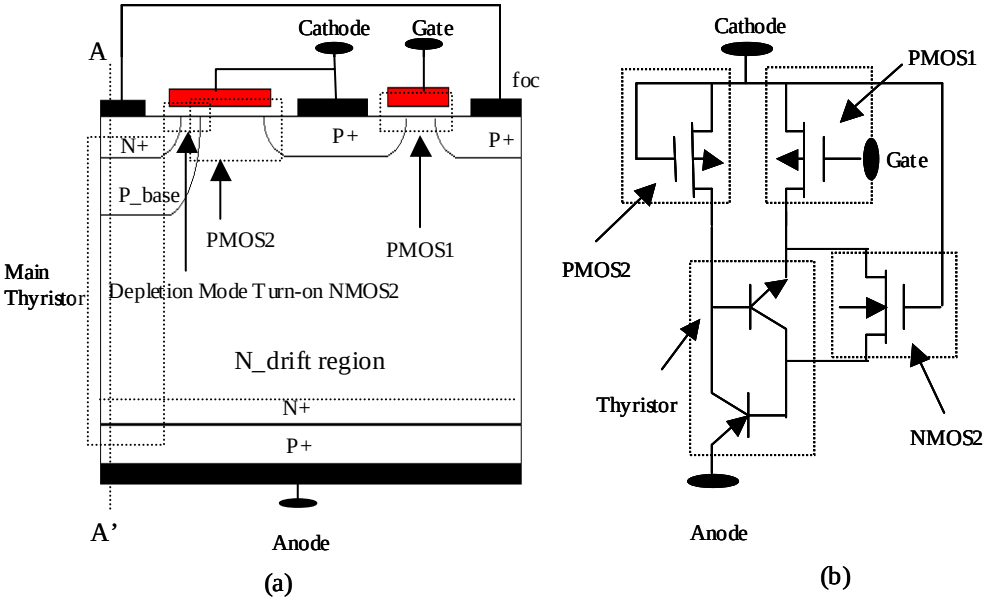


Fig. 3.1 Device structure of the three terminal ECT (a) and its equivalent circuit (b).

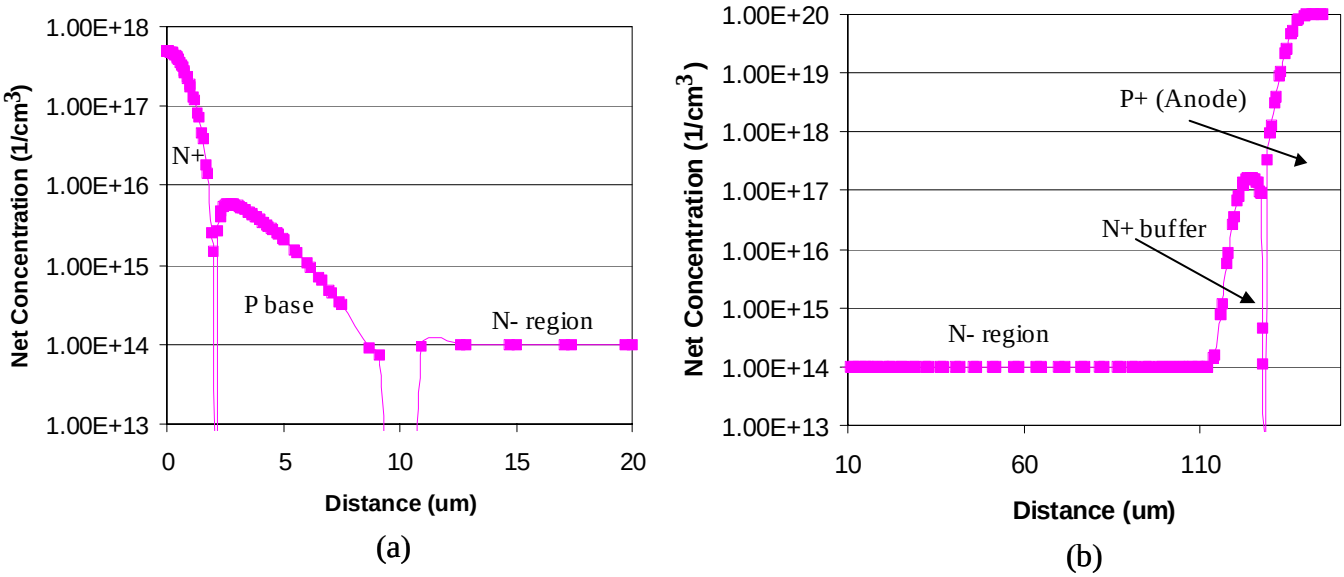


Fig. 3.2 1-D doping profile of the top cell (a) and anode region (b) of the 1200 V ECT along the cut line of AA' shown in Fig. 3.1.

(a). Forward I~V Characteristics

The forward I-V curves of the studied ECT are shown in Fig. 3.3. The forward voltage drop of the ECT at a current density of 100 A/cm^2 is different at different gate voltage. When the gate voltage is –15 V, the forward voltage drop is only 1.74 V. At the gate voltage of –10 V and –5 V the forward voltage drop increases to 2 V and 2.75 V. Fig. 3.4 shows the typical carrier distribution of the ECT when the current density is 100 A/cm^2. This is compared with that of the IGBT and the MCT. The conductivity modulation of the MCT is strongest among the three devices. The ECT is better than the IGBT, but worse than the MCT. Therefore, the forward voltage drop of the ECT is smaller than that of the IGBT, but higher than that of the MCT.

The high voltage output I-V characteristics of the ECT obtained from MEDICI are also shown in Fig. 3.5. For a gate voltage of –5 V, the current density of the anode saturates at about 1800 A/cm^2 and the anode voltage reaches 1300 V before breakdown happens. For a gate voltage of –15 V, the current density of the anode saturated at about 4000 A/cm^2 and the anode voltage went to 1100 V. It is clear that there exist a trade-off between the saturation current level and the forward voltage drop for the ECT. A lower gate voltage results in a lower saturation current, but a higher forward voltage drop. Change the ECT device dimension (especially the PMOS2 channel length) will also change V_F and I_{sat}.

From Fig. 3.5, it is also found that for the same gate voltage, the anode current increases slightly with the increase of the anode voltage after the device enters the saturation region. When the anode voltage increases, the substrate of the PMOS1 and PMOS2 increases too since it is connected to the anode. The value of the threshold voltage of the PMOS1 and PMOS2 will increase according to the equation below [10]:

$$|V_{th}| = |V_{th0}| + \gamma \cdot \left[\sqrt{2\phi_b + |V_{sb}|} - \sqrt{2\phi_b}\right] \qquad (3\text{-}4)$$

$$\text{where } \gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_A} \text{ and } \phi_b = \frac{kT}{q}\ln\left(\frac{N_A}{N_i}\right)$$

Therefore, with the increase of the anode voltage, the threshold voltage of the PMOS1 and PMOS2 will increase. That means the current diverted through PMOS2 decreases at the

same drain voltage. This will reduce the emitter short's effectiveness hence the anode current will increase due to a stronger thyristor path through PMOS1.

Fig. 3.6 shows the current flowlines of the ECT at different conduction modes. Fig. 3.6(a) shows the current flow when the ECT is in its forward conduction mode. The thyristor operates in its latch up state. Most of the current goes through the vertical thyristor structure and then laterally flows into the cathode through the FOC and the series PMOS1. So the forward voltage drop of the ECT is that of the thyristor plus that of the PMOS1. Fig. 3.6(b) shows the current flowlines when the ECT is in the saturation region. There are still lots of current going through the thyristor. However, the PMOS2 was clearly turned on because of the increase of the V_{FOC}. Some of the current are diverted into the cathode via PMOS2. According to the analysis mentioned above this current will keep the thyristor working at the boundary of the latching condition. The total current keeps almost constant and both NPN and PNP transistors are in their active regions.

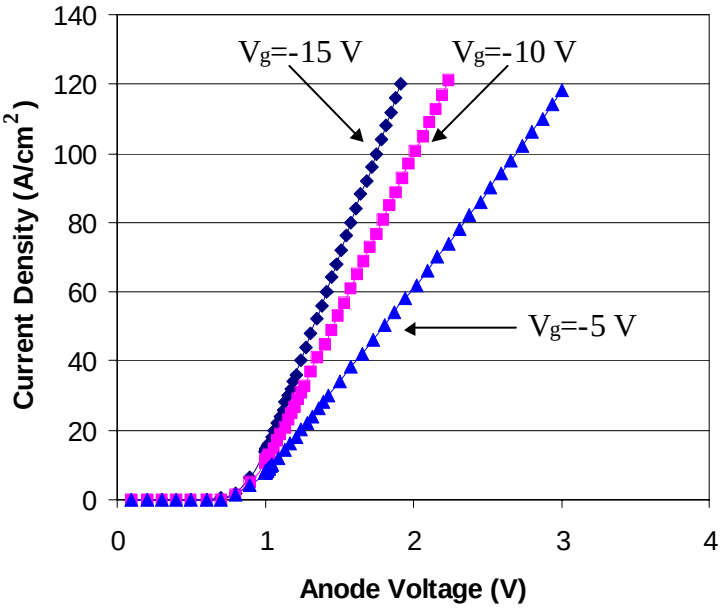


Fig. 3.3 The forward I~V characteristics of the 1200 V ECT obtained by device simulation.

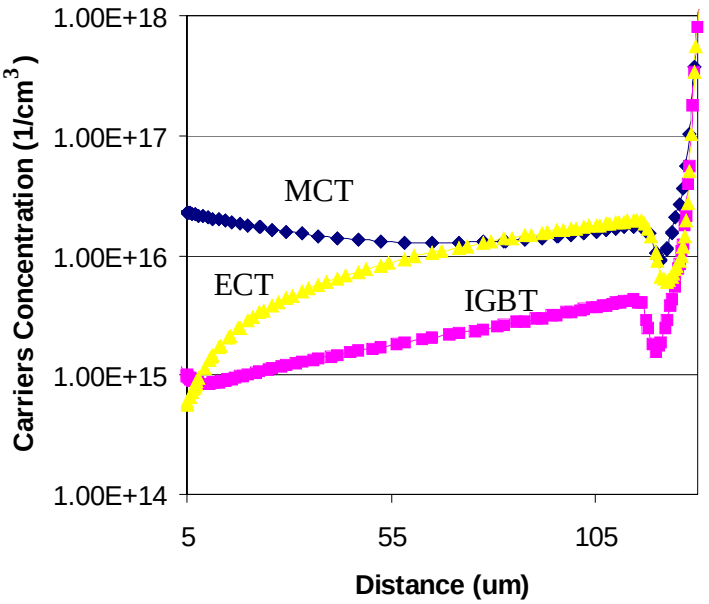


Fig. 3.4 The typical carriers concentration distribution of 1200 V ECT when the current density is 100 A/cm^2 comparing with that of the IGBT and MCT.

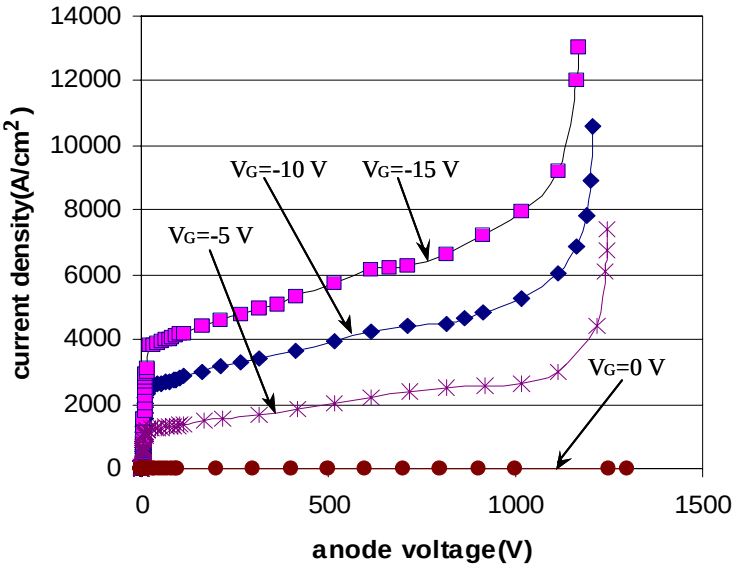


Fig. 3.5 The output characteristics of the ECT obtained by device simulation.

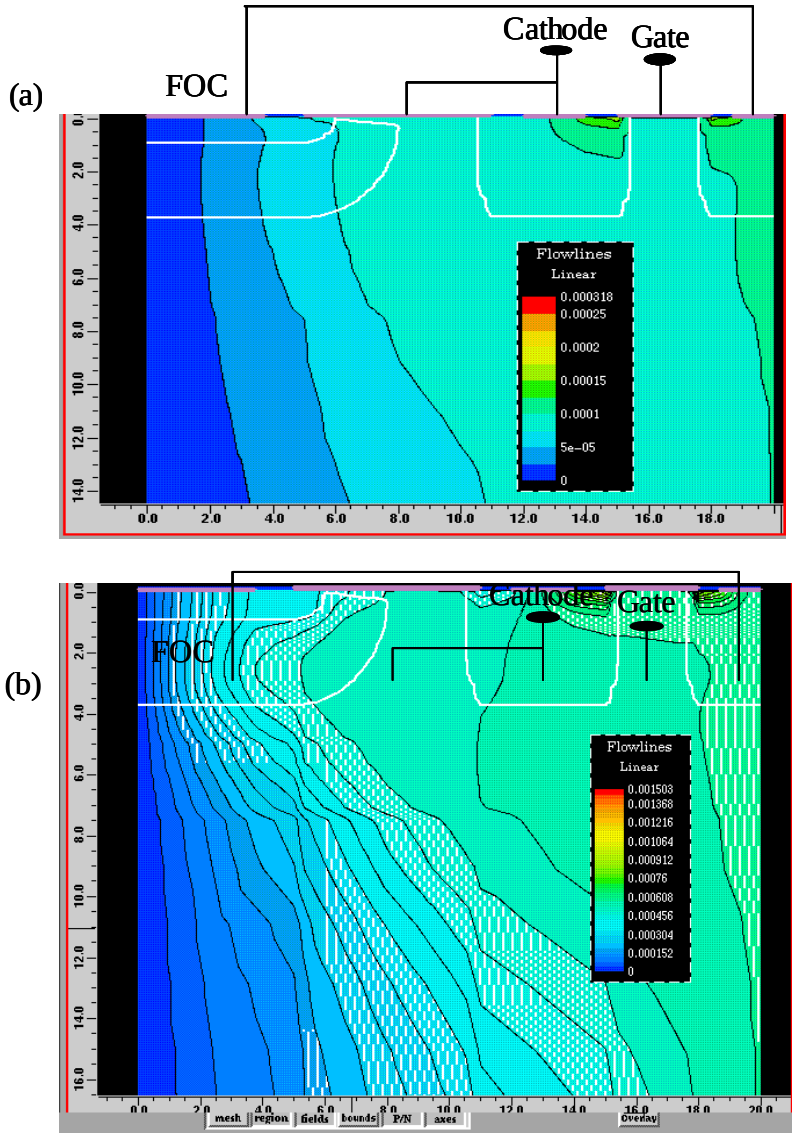


Fig. 3.6 The current flowlines of the ECT (a) in the forward conduction mode and (b) in the high voltage current saturation mode.

(b). FBSOA and RBSOA of the ECT

From the output characteristics of the ECT shown in Fig. 3.5, the FBSOA of the ECT can be obtained. In Fig. 3.5, there are two distinct changes of the slope in the I-V curves that separates the ECT operation area into three parts. In the region before the first slope change, the anode voltage is small and the current increases very fast. That means the thyristor is latched, but the PMOS2 is not turned on and the reduction of α_{npn} is too small to satisfy the equation (3-4). Therefore the current increases quickly just like a thyristor plus a series PMOS1. In the second region, the PMOS2 is turned on automatically because of the increase of the V_{FOC}. The equation (3-4) is satisfied and forces the thyristor works at the boundary of the latching condition. Hence the current saturated and the anode voltage keeps increasing. At the second slope change point, the increased α_{pnp} makes equation (3-4) unsatisfied and the thyristor enters deep latching state again instead of at the boundary state. The current starts to increase, and so does the V_{foc}, until the PMOS1 breaks down. According to the FBSOA definition, the second slope change point is the FBSOA point for each gate voltage.

Fig. 3.7 shows the calculated FBSOA of the 1200 V ECT in comparison with the FBSOA of a 1200 V IGBT. The simulated IGBT structure has the same N- drift region and backside P+ layer. It is clearly shown that the ECT has a much wider FBSOA than that of the IGBT mainly because the parasitic thyristor structure in the IGBT limits the large current operation of the IGBT.

Fig. 3.8 shows the circuit diagram used to calculate the RBSOA of the ECT. The gate voltage was ramped up from –15 V to 15 V within 100 ns in the turn-off simulations. A forced current source was used to model the inductive load. Fig. 3.9(a) shows the voltage and current waveform of the ECT during the turn-off. After the gate voltage changes from –15 to 15, the anode voltage begins to rise and the anode current keeps the initial value. After the anode voltage exceeds the source voltage, the free-wheeling diode begins to bypass the load current and the anode current decreases to zero. The turn-off in this case is successful. However, during the process of building up the voltage, after a certain time the electric field generated by the voltage may be high enough to initiate avalanche [11]. With the onset of avalanche at a high electric

field, the constant load current across the depletion region can then be supported by the drift of carriers generated by the avalanche multiplication. If the free carriers generated in the depletion region can carry the load current, the load current will stop extracting stored minority carriers. Therefore, the depletion region will no longer expand, and the anode voltage will stop rising. If the terminal voltage of the ECT enters a saturation state before it exceeds the voltage source value, as in the case 1400 V and 1000 A shown in Fig. 3.9(b), the turn-off is considered unsuccessful due to the dynamic avalanche.

Failure points of the simulation were collected as the RBSOA of the ECT. Fig. 3.10 shows the calculated RBSOA of the ECT comparing with that of the IGBT. The IGBT structure used here has the same N- drift region doping and P+ anode. It is clear that the ECT also has a wider RBSOA than that of the IGBT.

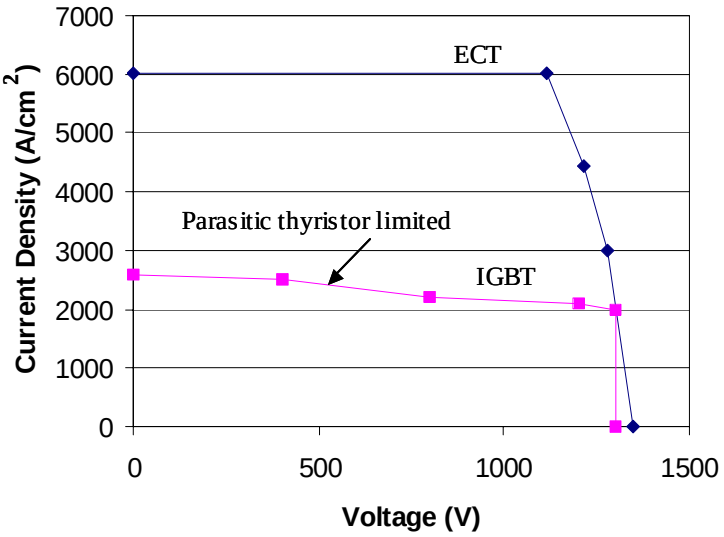


Fig. 3.7 The FBSOA of the ECT in comparison with the FBSOA of the IGBT.

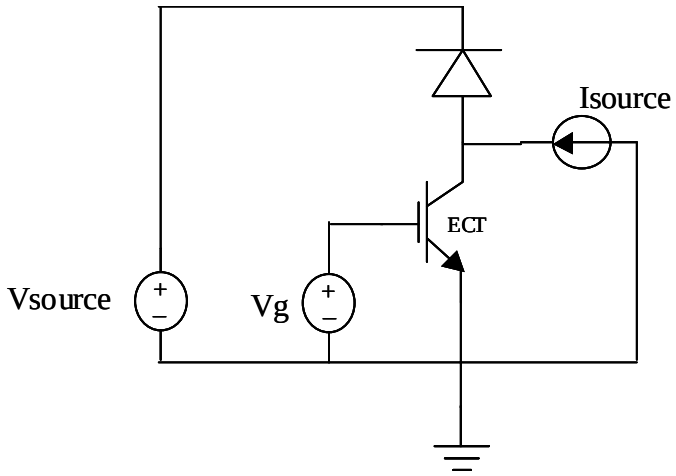
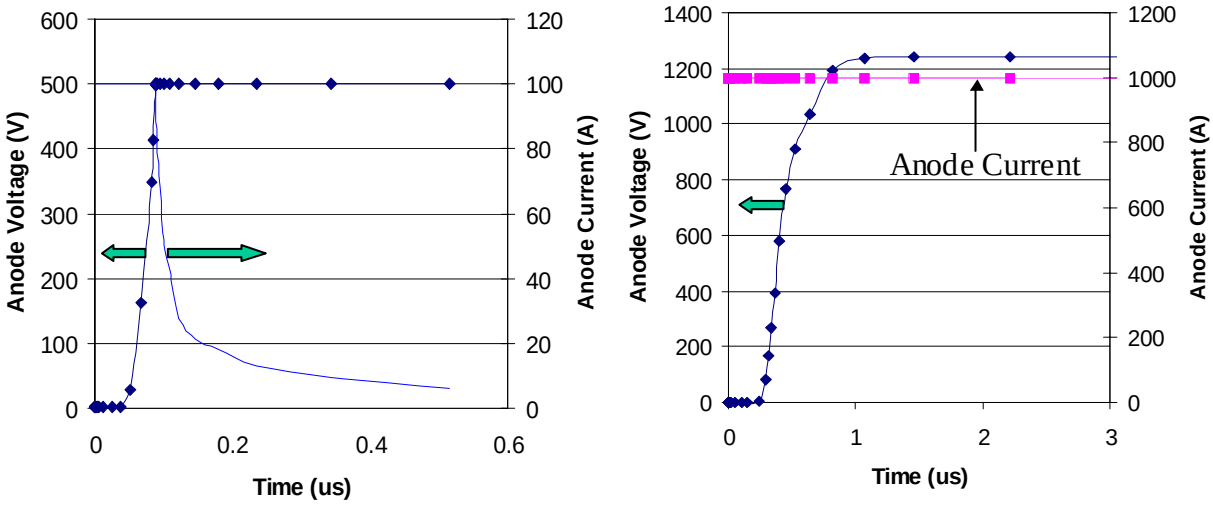


Fig. 3.8 Circuit diagram used to calculate the RBSOA using mixed mode MEDICI simulator.



(a). Successful turn-off (b). Turn-off failed

Fig. 3.9 The voltage and current waveform during turn-off.

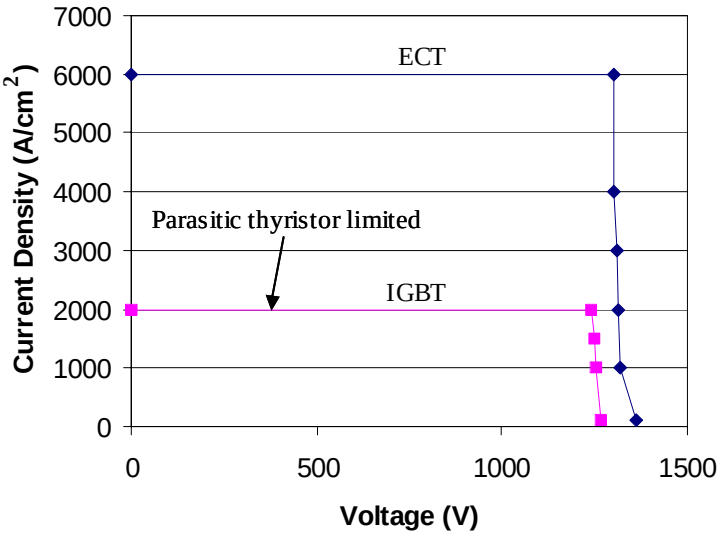


Fig. 3.10 Simulated RBSOA of the ECT in comparison with the RBSOA of the IGBT.

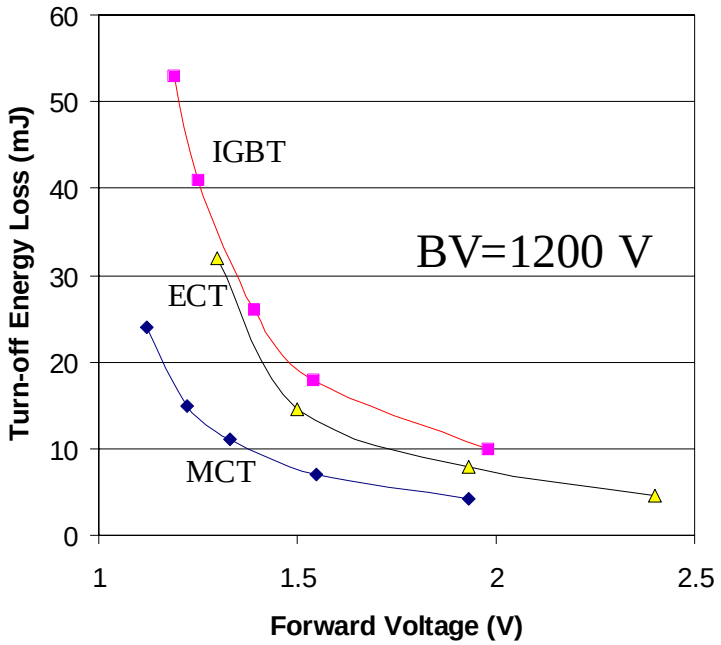


Fig. 3.11 Tradeoff between forward voltage drop and the turn-off loss per cycle when the current density is 100 A/cm^2 and turn-off voltage is 600 V.

(c). Turn-off Loss and Trade-off

Table 3.1 compares the main characteristics of the 1200 V ECT with those of the IGBT. The values of the conduction power loss were the on-state loss at a current density of 100 A/cm^2, and the switching loss (turn-on and turn-off) energy losses were obtained at a bias of 600 V and a current density of 100 A/cm^2 under inductive load switching conditions. From Table 3.1, it is clear that the ECT is better than the IGBT. The reason for this is because the ECT uses both emitter switch (PMOS1) and the emitter short (PMOS2) in the turn-off process.

Table 3.1 Comparison of 1200 devices main characteristics.

	Conduction power loss (w/cm^2)	turn-on energy loss (mJ/cm^2)	turn-off energy loss (mJ/cm^2)	switch energy loss (mJ/cm^2)
IGBT	182.7	57.0	2.08	59.1
ECT	173.2	51.8	2.02	53.8

In order to evaluate the performance of the 1200 V ECT, the trade-off between the turn-off energy loss and the forward voltage drop was also obtained by varying the minority carrier lifetime. Fig. 3.11 shows the calculated technology trade-off curve for 1200 V ECT comparison with that of the IGBT and the MCT. It is clear that the ECT has a better trade-off curve than the IGBT but worse than the MCT. That is because the conductivity modulation of the ECT is between those of the IGBT and the MCT. Therefore, the trade-off curve of the ECT is also between those of the IGBT and the MCT.

(d). Turn-on Characteristics

Fig. 3.12 shows the circuit diagram used for turn-on study. The value of the voltage source is 600 V, half of the voltage rating. The current source is 100 A and the device area is 1 cm^2, so the current density is 100 A/cm^2. Different gate resistors were used during the simulation to control the rise of the gate voltage at the switch gate. The gate voltage source V_g changes from 15 V to –15 V within 100 ns. The dV/dt of the gate voltage $V_g(t)$ is therefore different for different gate resistors. When the gate resistor increases, the dV/dt of the actual gate voltage

$V_g(t)$ will decrease. Fig. 3.13 shows the anode current waveform of the ECT during turn-on at different gate resistors. Fig. 3.14 shows the current rise rate dI/dt of the ECT in comparison with that of the IGBT and the MCT. It is clear that the change of the gate resistor of the MCT will not change the dI/dt and the dI/dt of the MCT is very large. But as for the ECT and the IGBT, things are different. The dI/dt is small and will decrease when the gate resistor increases. In actual applications, the gate resistor can therefore be used to control the dI/dt during turn-on for both the ECT and the IGBT, this however can not be done for the MCT. The dI/dt of ECT shown in Fig. 3.14 is lower than the IGBT. This is another evidence of excellent FBSOA (lower g_m, at lower V_F) in the ECT.

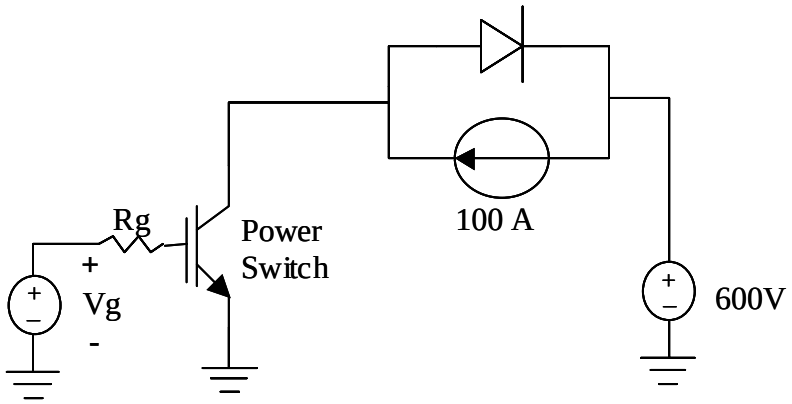


Fig. 3.12 Turn-on circuit with varying gate resistor used in the simulation.

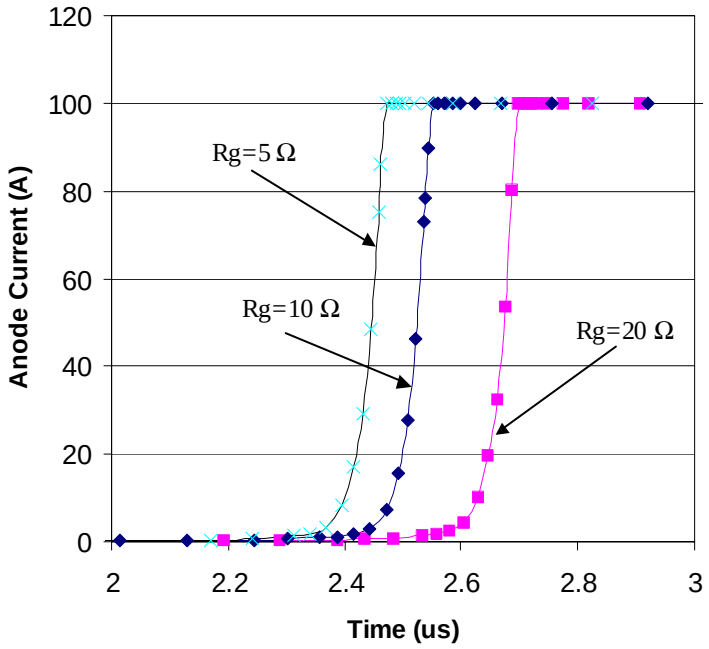


Fig. 3.13 The ECT turn-on waveforms with different gate resistance.

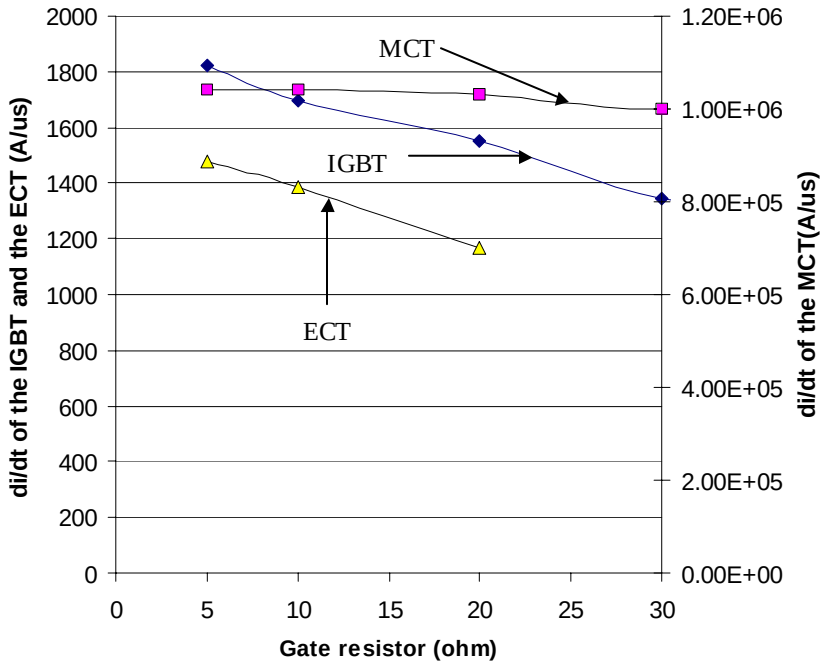


Fig. 3.14 The di/dt of the ECT at different gate resistor comparison with that of the IGBT and the MCT.

3.3 Design and Fabrication of the 1200 V ECT

3.3.1 Device Design

After verifying the concept and operation of the ECT through the two-dimensional numerical simulations, ECT devices were designed in order to experimentally demonstrate their operation. A ten-mask process was developed to fabricate the ECT. The masks in this design were designed using Cadence layout tool. Fig. 3.15 shows the photomicrograph of a typical multi-cell ECT die. The total area of the die is 1000 um×1000 um including the device termination region. The active region of the ECT is about 500 um ×250 um. The basic dimensions of the ECT unit cell are shown in Fig. 3.16. The control gate length is 3um and the automatic turn-on gate length is 15 um. The N+ emitter length is set to 5 um (half of the total length).

The termination region shown in Fig. 3.15 is formed by four P+ floating rings and one channel stop ring with field plates. The cross-section view of the edge termination is shown in Fig. 3.17 together with the dimensions in order to achieve the designed breakdown voltage.

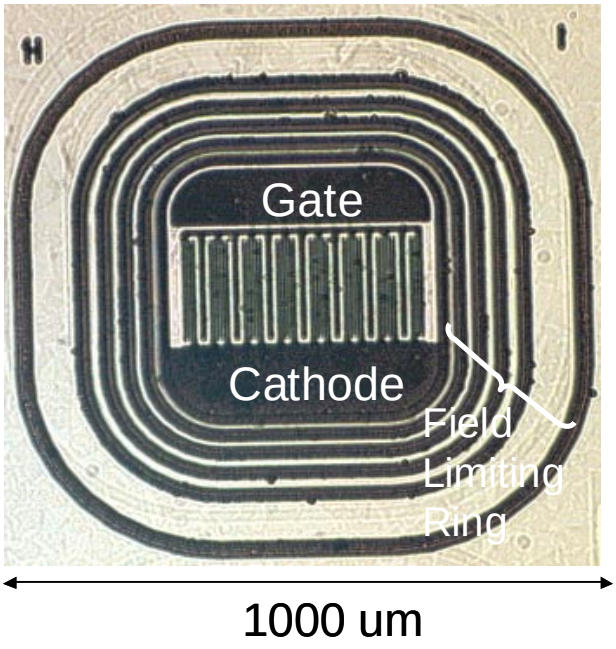


Fig. 3.15 The test structure of ECT with gate length of 3 um and width of 1500 um.

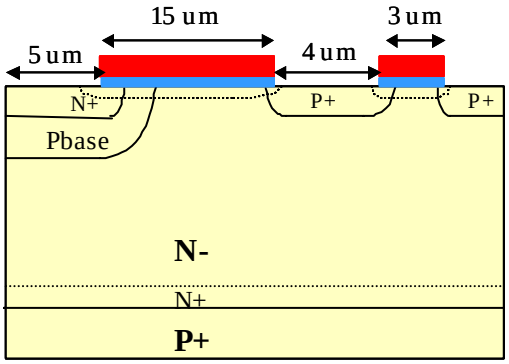


Fig. 3.16 The dimensions of the ECT unit cell.

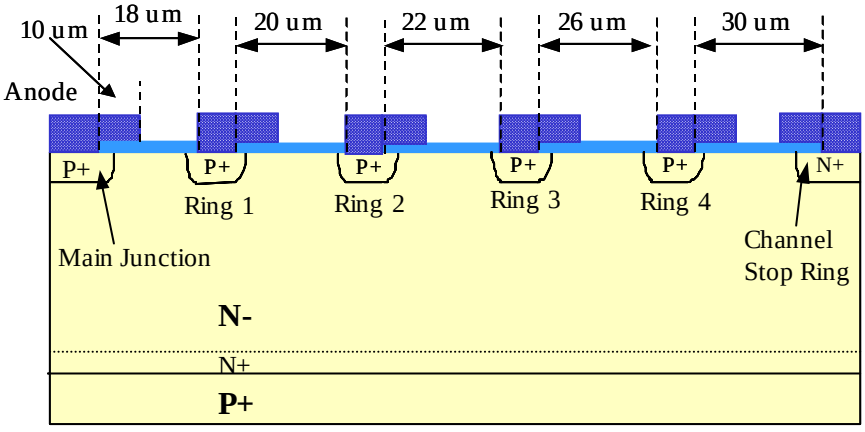


Fig. 3.17 The cross-section view of the ECT edge termination region.

3.3.2 Major Fabrication steps

The ECT test structures were fabricated using <100> oriented P+ substrate wafers with a 100 um thick, 52 ohm-cm N- epitaxial layers as the starting material. A complete process flow list is given in Appendix A. Fig. 3.18 shows the major steps of the self-aligned ECT process. The fabrication is carried out at Cornell Nanofabrication Facility.

The wafers were initially grown with a 1 um field oxide using wet oxidation. The first mask (ACTIVE) was used to open the active region, such as devices active region and termination ring region. The oxide in the open area was removed by the buffer acid while the oxide in the remaining area was protected by photo resist.

Next, a screen oxide was grown and one mask (JFET) was used to pattern the wafers for the threshold voltage adjustment implantation like that shown in Fig. 3.18(a). Arsenic was used for the N implantation. After the implantation, the photo resist was stripped and the wafers were driven in high temperature furnace.

The gate oxide was then grown. After that a poly layer was grown to form the gate. The thickness of the poly layer was 0.5 um. Mask (POLY) was used to pattern the gate shown in Fig. 3.18(b). After the gate is formed, another mask (PWELL) was used to open the termination ring area and Boron was implanted in such area to form the P+ termination ring.

The fifth mask (PBASE) was used to open the window for the implantation of the Pbase region and Boron was then implanted to form the Pbase junction shown in Fig. 3.18(c) followed by the drive in operation. The sixth mask (PDIV) was used to open the window for the implantation of the P+ region and the seventh mask (NPLUS) was then used to open the window for the implantation of the N+ emitter region shown in Fig. 3.18(d). These three implantations are all self-aligned to the poly gate. That makes the double diffusion junction formed easily.

After all the implantation and the form of the junction, a thick oxide layer was grown to protect the gate and other active region. Then another mask (CONTACT) was used to open the contact hole shown in Fig. 3.18(e). Then the aluminum layer was sputter immediately after the contact hole was formed in order to obtain a good ohmic contact between the aluminum and the P+ or N+ region shown in Fig. 3.18(f). The thickness of the aluminum was 1um. The aluminum

layer then undergoes the wet etching also using a mask (METAL) to form the pattern and photo resist for the protection. The last step is to form a silicon nitride layer about 0.5 um thick to protect the aluminum and make the top surface of the wafers passive. Then the last mask (PAD) was used to open the pad region and expose the aluminum on the surface for wire bonding connection.

After all the surface processing steps were finished, photo resist was spread on the surface for the protection. Then the substrates of the wafers were lapped until the remaining thickness was around 250 um. A multi-layer metal, Cr-Ni-Ag, was deposited to provide good ohmic contact and good adhesion to the substrate.

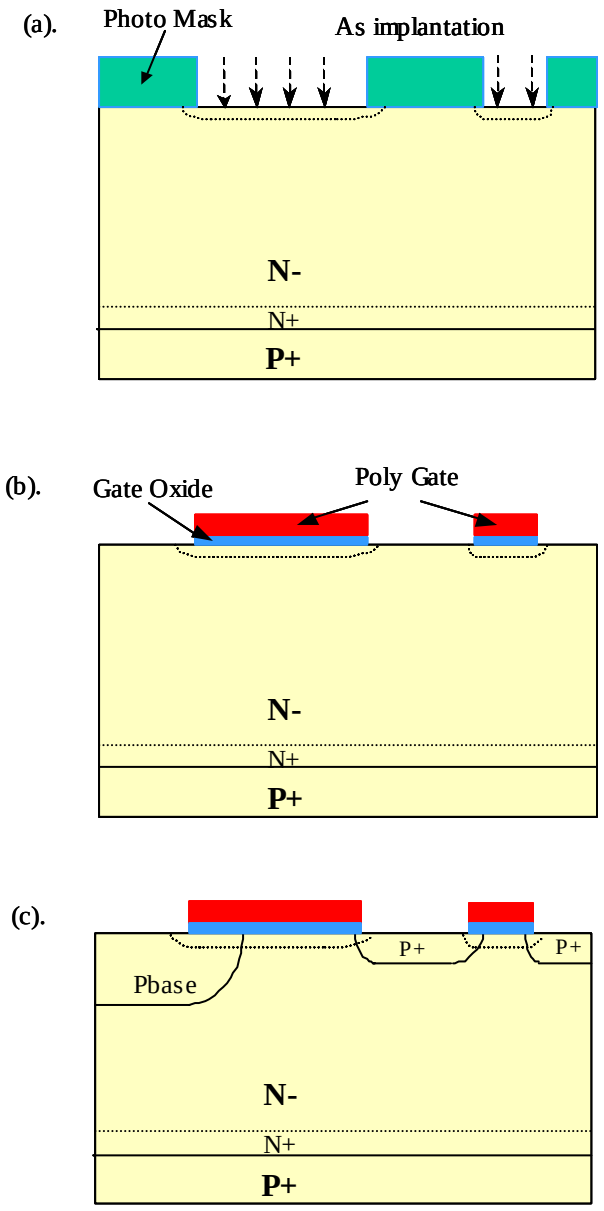


Fig. 3.18 Major steps of the proposed ECT fabrication process.

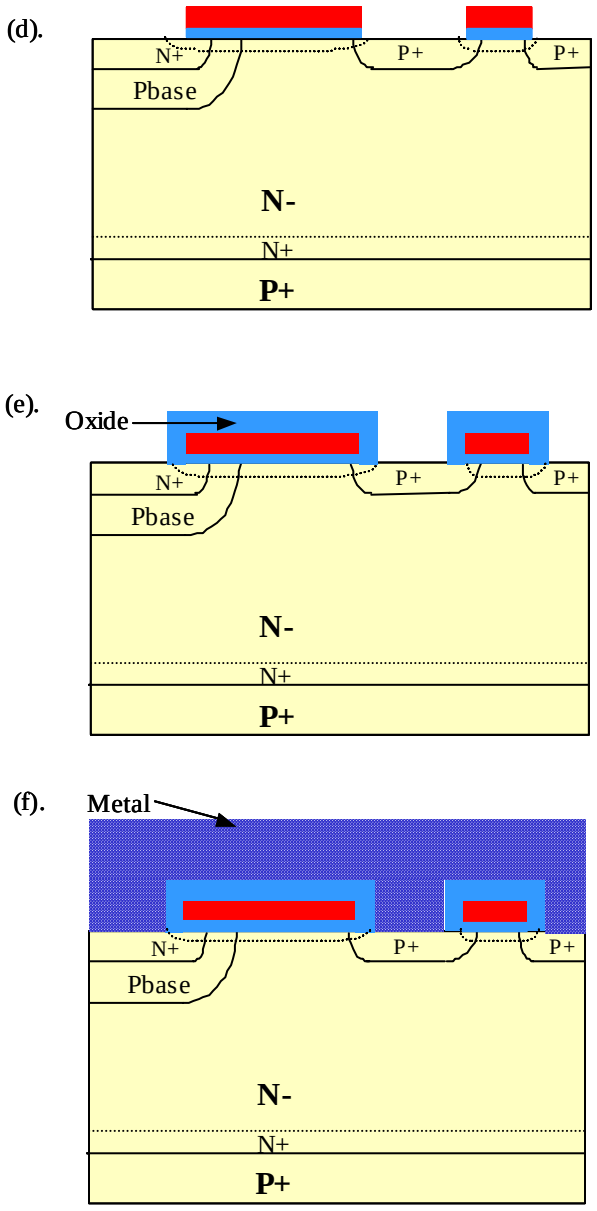


Fig. 3.18 Major steps of the proposed ECT fabrication process (continued from previous page).

3.4 Experimental Results and Discussion

The ten-mask ECT test structure discussed above was fabricated in Cornell University. Fig. 3.19 shows the measured breakdown voltage of the ECT. The leakage current is small and the breakdown voltage is around 1100 V. This demonstrates the effectiveness of the junction termination. Fig. 3.20 shows the measured output characteristics of the device at room temperature. The on-state voltage drop (V_F) of the device is about 1.8 V at 100 A/cm^2. This compares favorably with the planar DMOS-based 1200 V IGBT, whose V_F typically is above 2 V at the same current density [13]. The device possesses an excellent current saturation capability as shown in Fig. 3.20. The current saturation mechanism discussed above is therefore proved.

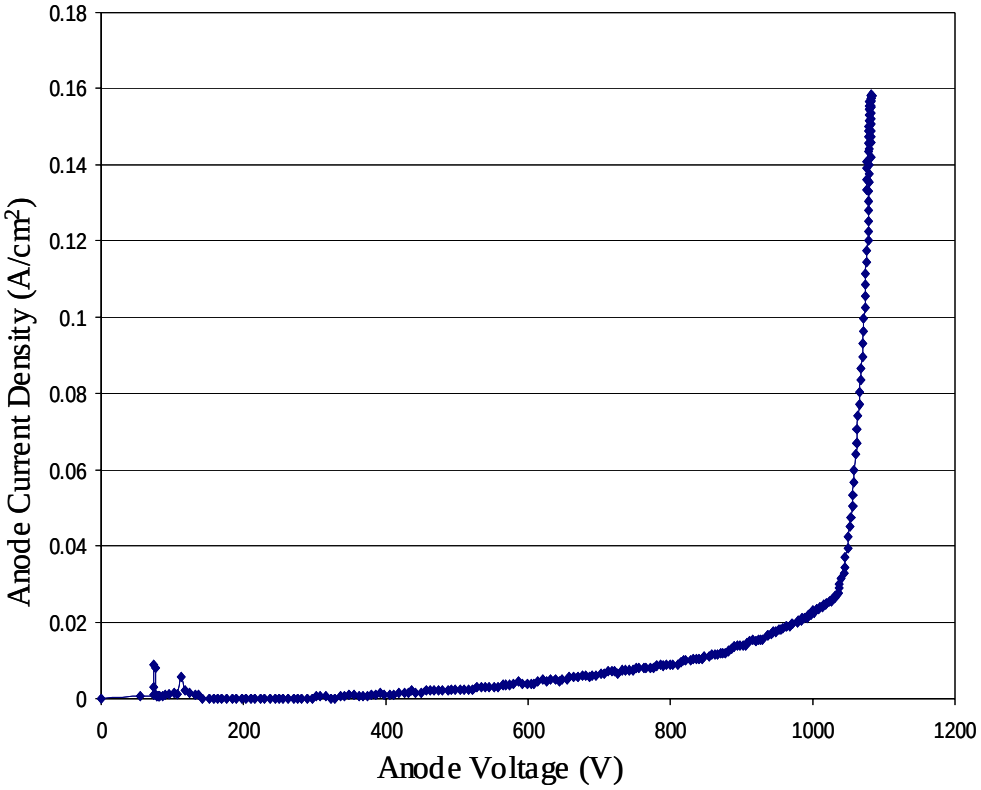


Fig. 3.19 The measured breakdown voltage of the ECT.

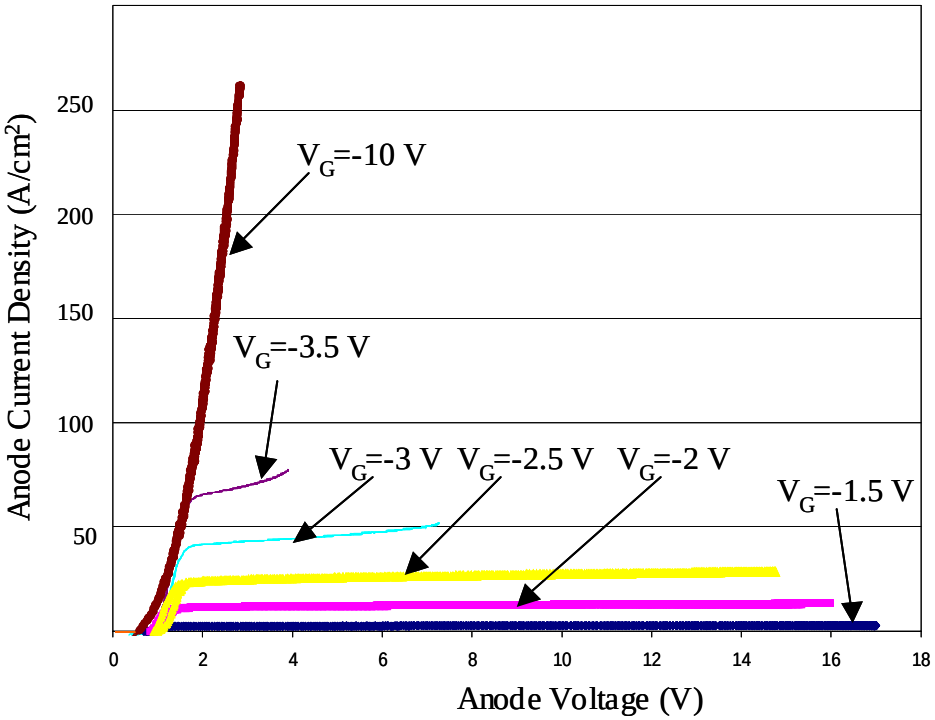


Fig. 3.20 Experimental output characteristics of the ECT.

Fig. 3.21 shows the output characteristics of the IGBT fabricated on the same wafer. The IGBT has the same anode doping and buffer layer. The N+ region and P base region of the top cell of the IGBT are the same as the ECT. Fig. 3.22 shows the forward voltage drop comparison when the gate voltage of the ECT is –10 V and the gate voltage of the IGBT is 10 V. The difference is small similar to that shown in the Table 3.1. The benefit of the ECT over the IGBT is not significant because the blocking rating isn't high enough. On the other hand, the advantage of the thyristor operation is clearly shown in Fig. 3.22 even though there is a voltage drop on the emitter FET, PMOS1.

For both the ECT and the IGBT, the anode voltage can't go very high when the devices enter the saturation region. In this fabrication, the isolation between the poly gate and the active region is not good and a leakage current exists when a voltage signal applies to the gate. This makes it impossible to test the device under high current condition. More works need to be done to improve the device design and the fabrication process to avoid such problem.

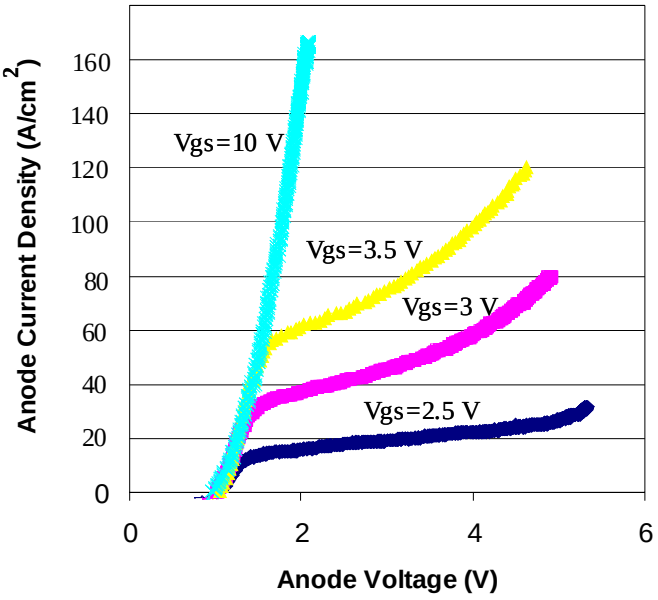


Fig. 3.21 Experimental output characteristics of the IGBT.

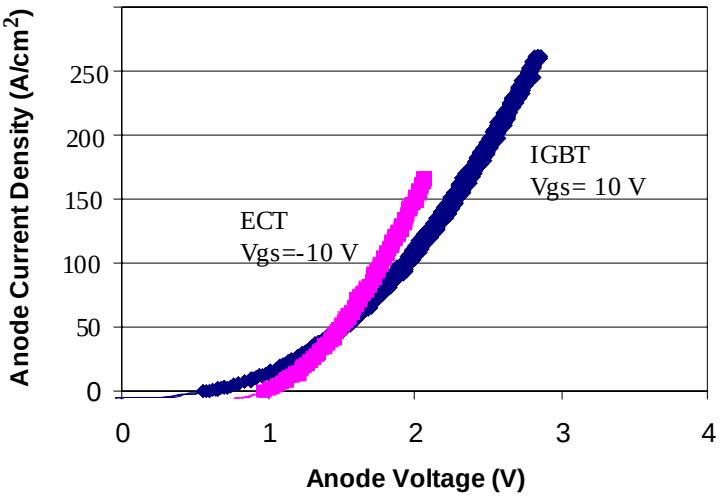


Fig. 3.22 Experimental forward voltage drop of the ECT comparing with the IGBT.

References

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Chapter 4 Design and Fabrication of the 4 kV Hybrid Emitter Controlled Thyristor

4.1 Introduction

In the previous chapter, a novel ECT was studied. Numerical simulation was used to demonstrate the operation of the new device. A 1200 V ECT was designed and fabricated using a process compatible with IGBT [1]. Because the voltage range is still not high, the benefits that the ECT can obtain are not very obvious. So in this chapter, a 4kV Hybrid-ECT (HECT) structure is proposed. The HECT is actually a hybrid integration of a low voltage packaged power MOSFET with a high voltage thyristor structure, similar to the ETO [2] except in the HECT MOS turn-on FET is integrated while the ETO requires a separate current source for turn-on. The low voltage power MOSFET is connected externally and the high voltage thyristor structure with turn-on FET and emitter short FET is fabricated using a novel high voltage process. The hybrid integration separates a complicated fabrication issue into two easy ones. Due to hybrid integration, the fabrication becomes easier. Only seven masks are needed to fabricate the device. The cost will decrease and the yield will increase because of the simplified processing. Device optimization also becomes easier since the thyristor structure can be optimized separately. Another motivation of the HECT is to make it easy to fabricate high current devices because the structure shown in Chapter 3 is not easy to scale the chip size unless two metal layers are used.

The device structure and operation principle of the HECT was studied first by the numerical simulation. Then the processing design was obtained in order to fabricate the device.

Some variations were discussed for optimization of the design. At last, the fabricated device was tested and results were discussed.

4.2 Device Design

The cross-section view of the high voltage part of the HECT is shown in Fig. 4.1. It is also a 4-layer PNPN thyristor structure. A p-channel MOSFET (PMOS1) is integrated on the top of the N- drift region which provides emitter short function. A depletion n-channel MOSFET is also integrated on the surface in the p region, which acts as the turn-on FET. The main thyristor structure is formed by the junction J1, J2 and J3. The high voltage part of the HECT has four terminals: anode, emitter, gate and cathode. Since the turn-on FET is a depletion mode MOSFET, the gate can be tied directly to the cathode resulting in only three terminals. After connecting an external low voltage MOSFET, the final structure of the HECT is shown in Fig. 4.2. The external MOSFET (NMOS2) is used to connect the emitter to the cathode of the HECT. The external MOSFET therefore acts as the emitter switch of an ECT. So the HECT is still a three-terminal power device. The signal on the gate can control the power flow between the cathode and the anode to realize the function of a power switch.

If a positive voltage which is larger than the threshold voltage of the NMOS2 is applied to the gate electrode of NMOS2 and another positive voltage is applied to the anode electrode, the HECT will be turned on. The positive voltage on the gate turns on the NMOS2 which connects the emitter to the cathode. Since the depletion mode NMOS1 is in its on state when the emitter potential is low, once a path is created for the NMOS1, it will conduct current. And the emitter will then inject electrons into the lower N- drift region of the thyristor through NMOS1 channel and the main current path becomes the vertical thyristor. Then the thyristor is triggered into the latch-up state. The current of the thyristor collected by the upper N+ emitter flows into the cathode through the NMOS2. Therefore, the forward voltage drop of the HECT is that of the main thyristor plus that of the NMOS2.

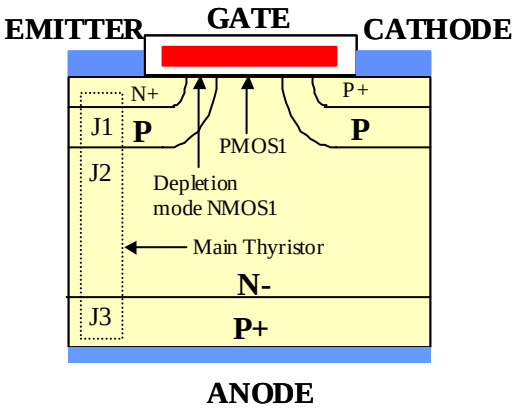


Fig. 4.1 The cross-section view of the high voltage part of the HECT and IGBT.

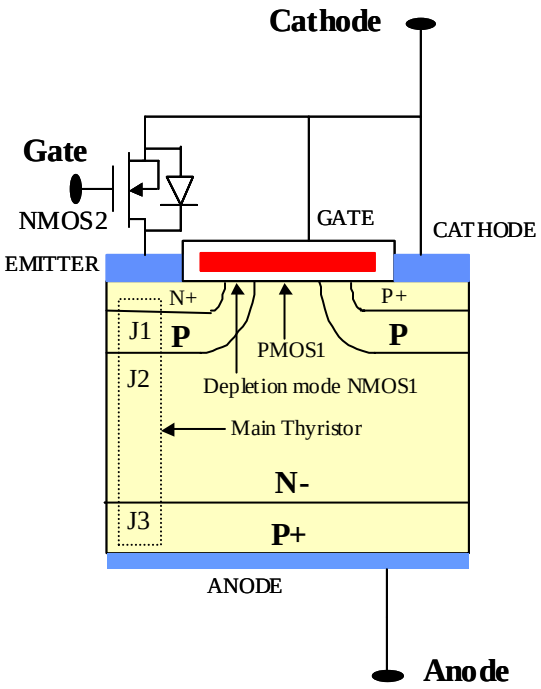


Fig. 4.2 The overall structure of the HECT.

In order to study the characteristics of the HECT, a 4 kV non-punch-through (NPT) type HECT is investigated by the two-dimensional device simulator MEDICI. The length of the N-drift region is 550 um with the doping concentration of 5×10^{13} cm^{-3} in order to obtain 4kV blocking capability. The P+ region has a surface concentration of 2×10^{19} cm^{-3} to form the ohmic contact. The deeper p region on the surface is a critical one that must satisfy the requirement of the blocking voltage and at the same time to make the NMOS1 depleted. A surface concentration of 2×10^{16} cm^{-3} and a junction depth of 12 um were finally chosen in the design. The upper N+ emitter of the main thyristor has a the surface concentration of 2×10^{19} cm^{-3} and a junction depth of 1.5 um. In the simulation, the minority carrier lifetime of 1.75 us was used to describe the N-drift region. The NMOS2 is represented by an idea MOSFET model in the mixed-mode simulation.

Fig. 4.3(a) shows the simulated forward voltage-current characteristics of the 4 kV HECT and IGBT. When the anode voltage is around 1.1 V, the main thyristor is triggered into its latch-up state. The forward voltage drop of the HECT is only 1.9 V at a current density of 100 A/cm^2 while the forward voltage drop of the IGBT is 2.6 V. At the same blocking voltage rating, V_F of the HECT is therefore lower than that of the IGBT [3,4]. Fig. 4.3(b) shows the technology trade-off between the turn-off energy loss and the forward voltage drop. It is clear that the HECT has a better trade-off than that of the IGBT, due to stronger modulation.

With the increase of the current, NMOS2 will enter its saturation region at a fixed gate voltages. The current through NMOS2 stays at a certain value and the voltage of the emitter ($V_{emitter}$) increases. So does the voltage of the upper P base region of the main thyristor (V_{pbase}). When $V_{pbase}>|V_p|$, where $V_p<0$ is the threshold voltage of the PMOS1, the PMOS1 turns on automatically and hole current will be diverted from the upper base of the man thyristor via PMOS1 into the cathode. This reduces the current gain of the upper NPN transistor of the main thyristor. If the total current gain of the upper NPN transistor and the lower PNP transistor of the main thyristor becomes less than 1, the main thyristor will come out of the latching state. Then, the current flow through NMOS2 decreases, so does the $V_{emitter}$. A reduced $V_{emitter}$ means a reduction of the diverted current and an increase of the current gain of the upper NPN transistor;

hence the main thyristor enters latching state again. Such negative feedback mechanism makes the main thyristor to operate at the boundary of the latching condition in which both NPN and PNP are in the active region. Therefore, the anode voltage continues to increase without significant anode current increase. The increased anode voltage is supported by the junction of the upper P base region and the N- drift region. The output I~V characteristics of the simulated 4 kV HECT are shown in Fig. 4.4(a). For a gate voltage of 5 V, the current density of the anode saturates at about 450 A/cm^2 and the anode voltage increases to 3.6kV. While for a gate voltage of 3 V, the current density of the anode saturated at about 40 A/cm^2 and the anode voltage went to 3.8kV. From Fig. 4.4(a), it is also shown that for the same gate voltage, the anode current increases slightly with the increasing of the anode voltage after the device enters its active region. The reason is the same as the one discussed in Chapter 3 by using equation (3-4) [5]. Here, another explanation is presented in order to understand this phenomenon well. When the anode voltage increases, the depletion region in the N- drift region expands. So the base width of the lower PNP transistor of the main thyristor decreases. To keep the main thyristor operate at the boundary of the latching condition, the current gain of the upper NPN transistor must decreases by diverting more hole current via PMOS1. Then, the $V_{emitter}$ will increase and results in the increase of the total current. At very high anode voltages, the $V_{emitter}$.will reach the breakdown voltage of the NMOS2 and the current will increase significantly as shown in Fig. 4.4(a). Fig. 4.4(b) shows the emitter voltage when the anode voltage increases.

Fig. 4.5 shows the schematic of the circuit used to calculate the RBSOA of the HECT. The gate voltage was ramped down from 15 V to –15 V within 100 ns in the turn-off simulations. A forced current source was used to model the inductive load. Failure points of the simulation were collected as the RBSOA [6,7] of the HECT. Fig. 4.6 shows the calculated RBSOA of the HECT.

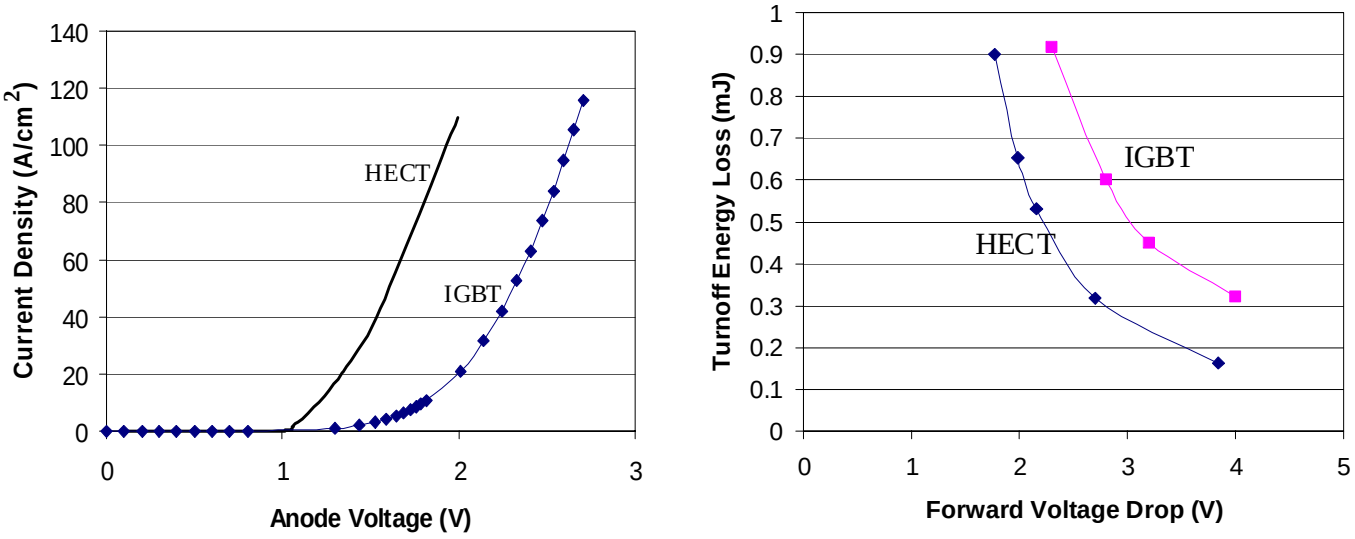


Fig. 4.3 Forward I~V characteristics (a) and technology trade-off curve (b) of the 4K V HECT comparing with that of the IGBT.

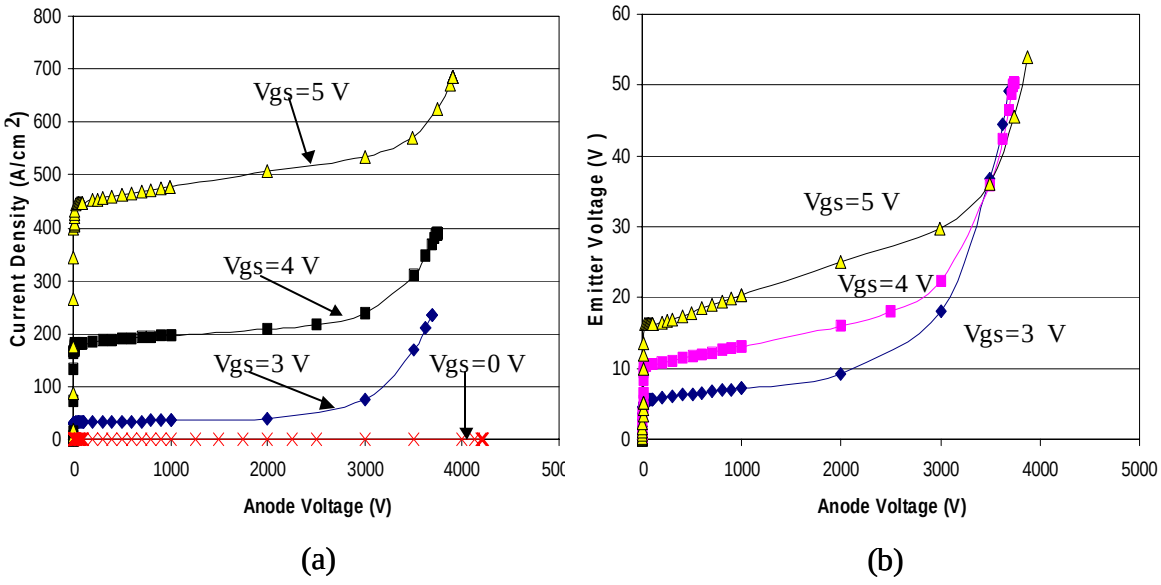


Fig. 4.4 The output characteristics of the HECT (a) and the emitter voltage (b).

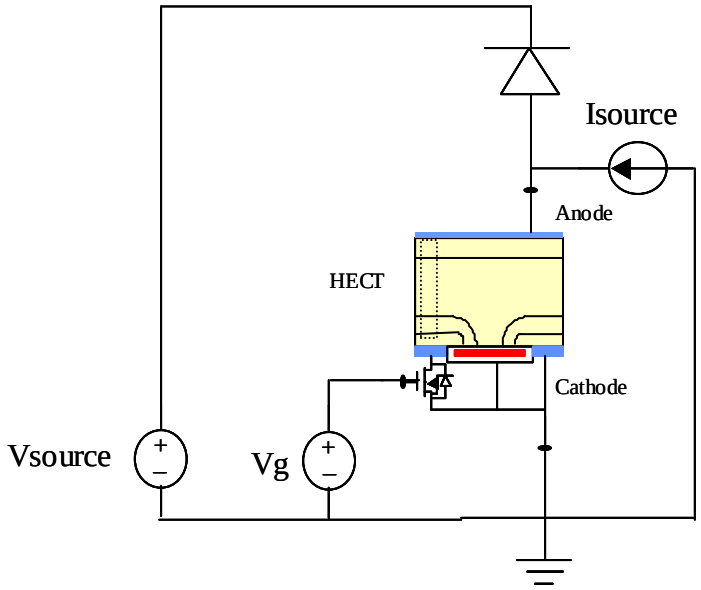


Fig. 4.5 Schematic of the simulation circuit to calculate the RBSOA.

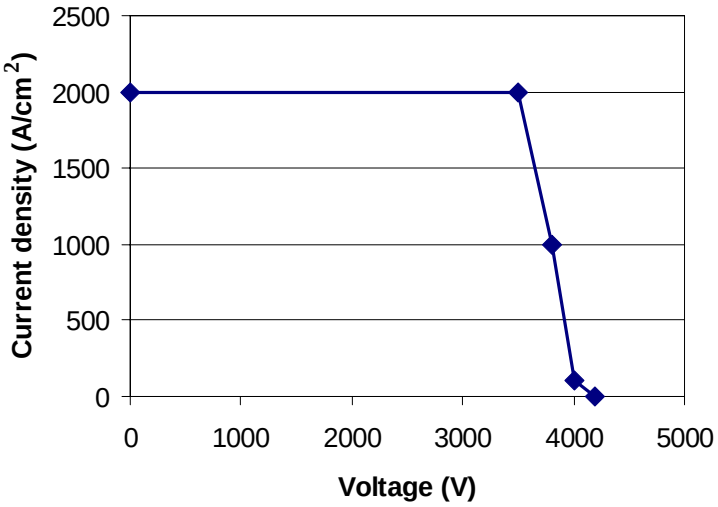


Fig. 4.6 The RBSOA of the HECT.

4.3 Processing Design

4.3.1 Layout Design

After verifying the concept of the HECT through two-dimensional numerical simulations, devices were designed in order to experimentally demonstrate HECT operation. A seven-mask novel process was developed to fabricate the HECT. The layout was designed using Cadence tools. Fig. 4.7 shows the photomicrograph of the multi-cell HECT die. The total area of the die is 4000 um×8000 um including the edge termination region. There are two emitter pads at the edges of the device and each one can carry 2 A current. There are also five cathode pads on the other side of the device. The JTE corner part of the device is labeled in Fig. 4.7 and will be discussed in the next section.

Fig. 4.8 shows the Cadence layout of the row cell part specified in Fig. 4.7. The cathode is connected together through a big surface metal plate. This will make the current flow through the metal uniformly and decrease the current crowding. The emitter is also connected together via a big metal plate and the width of the metal path increases gradually in order to carry more current. Fig. 4.9 shows the basic cell which formed the large HECT. The cathode and the emitter have a finger layout. The emitter length is 40 um and the gate length is 30 um.

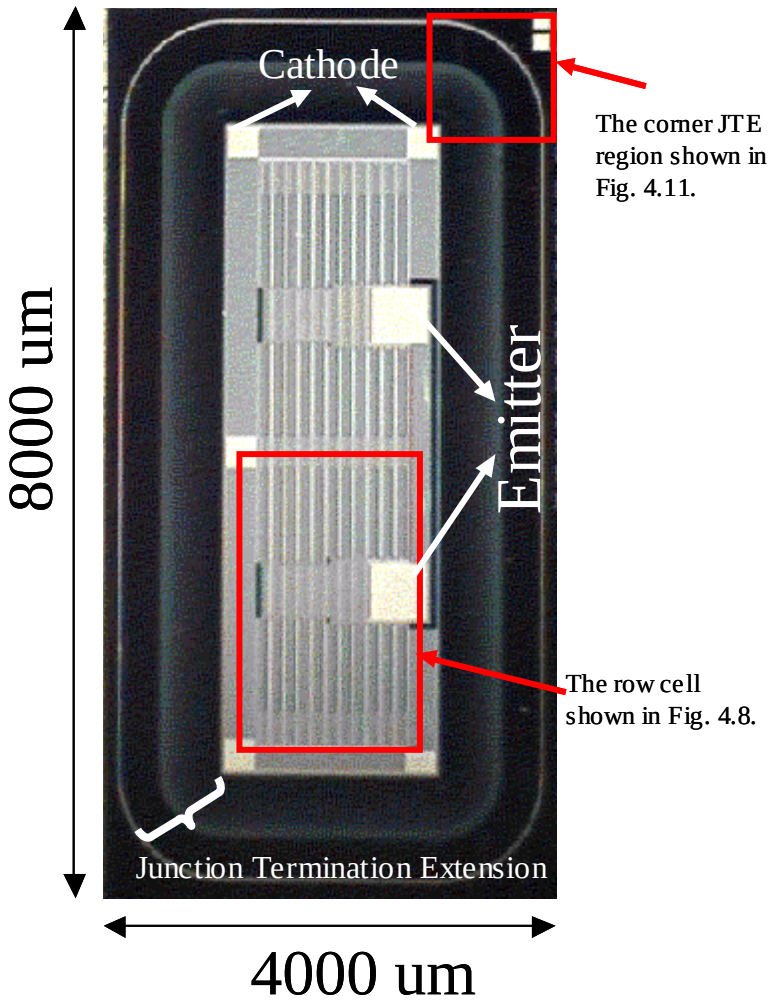


Fig. 4.7 The test structure of HECT with gate length of 30 um.

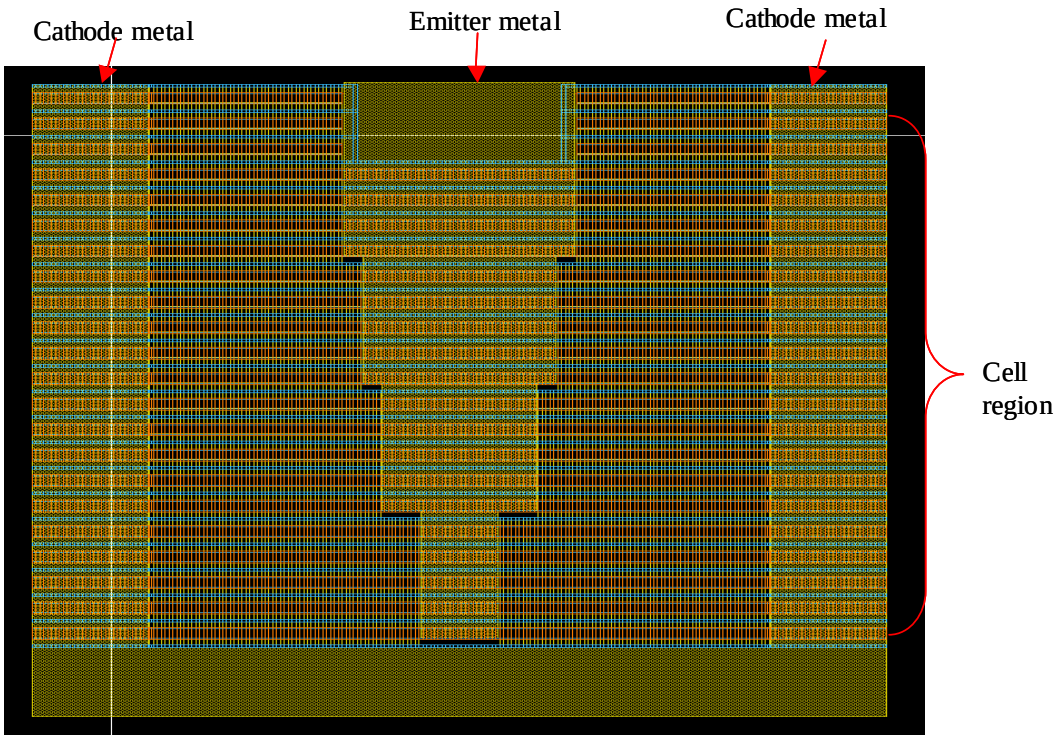


Fig. 4.8 The row cell of the test structure.

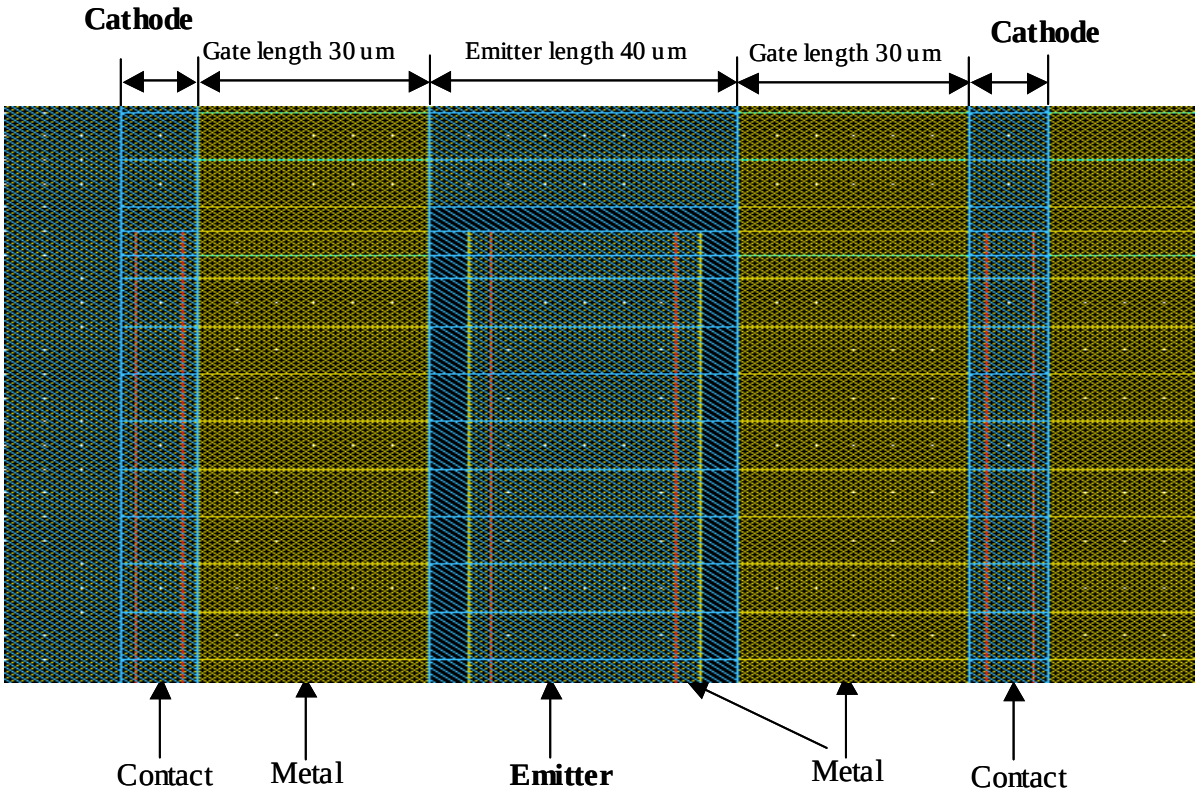


Fig. 4.9 Basic cell dimension of the test structure.

4.3.2 Edge Termination Design

Junction Termination Extension (JTE) [8] is used as the edge termination for this high voltage device. The cross-section view and dimension of the JTE is shown in Fig. 4.10. The zone consists of a P region 600 um wide in order to protect the main junction. Beyond the P zone, there is a N+ channel stop ring. The metal over the stop ring is floating but should have the same potential as the anode when the anode voltage increases. The layout of the JTE region specified in Fig. 4.7 is shown in Fig. 4.11. The JTE region is formed by a single Boron implantation. One mask is used to form the implantation window. The implantation opening window varies according to distance from the main junction in order to realize an optimized dose distribution in the JTE region, such as linear distribution or ellipse distribution [9,10,11].

The total charge of the implantation is a critical parameter for high breakdown voltage. Simulations have been used to optimize the implantation charge in order to achieve a required breakdown voltage. Fig. 4.12 shows the different breakdown voltage of the JTE at different implantation charge. Based on this, a process variation was made to obtain the best breakdown voltage.

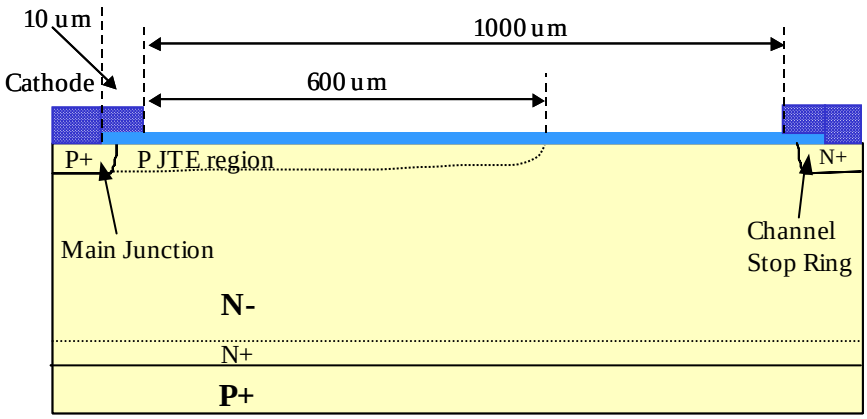


Fig. 4.10 The cross-section view of the JTE termination region.

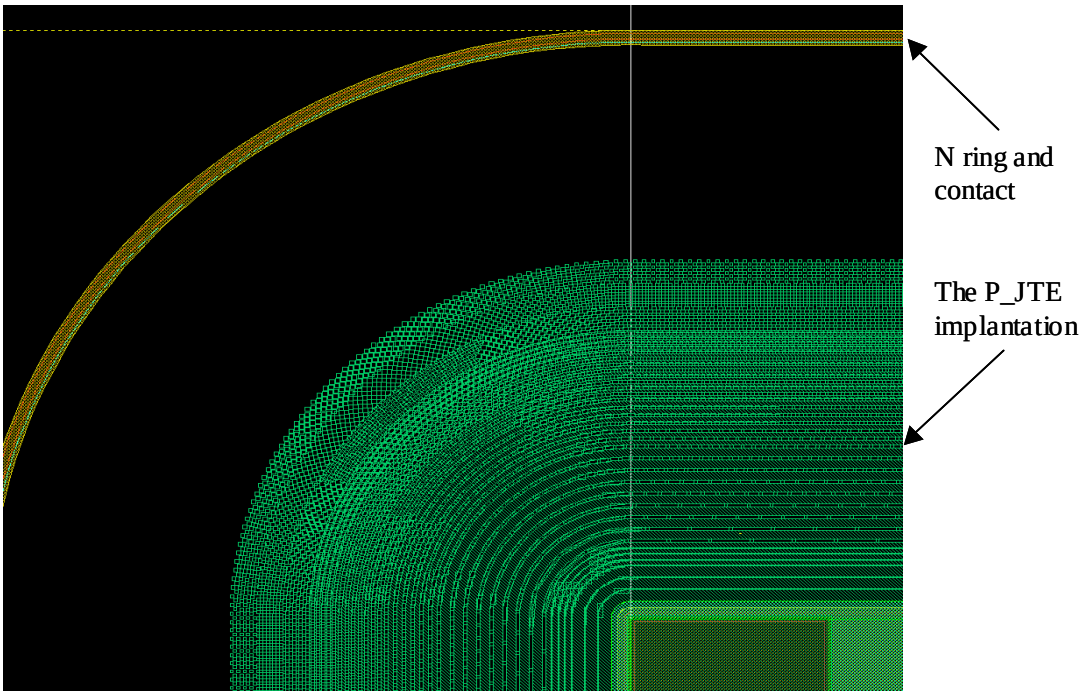


Fig. 4.11 The layout of the JTE region.

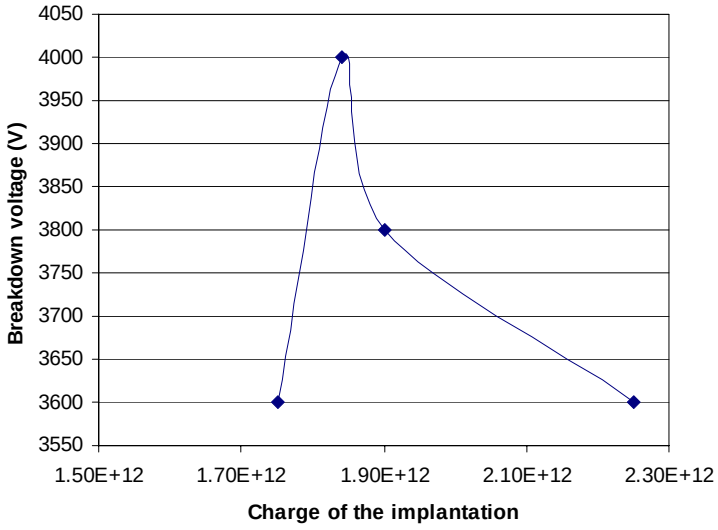


Fig. 4.12 The breakdown voltage at different implantation charge of the JTE.

4.3.3 Process Flow

In order to achieve the depletion mode NMOS1, an additional threshold adjustment Arsenic implantation must be used. The charge of the implantation decides the threshold voltage of the depletion mode NOMS1. If the implantation charge is not high enough, the HECT has poor turn-on characteristics and will result in a snap-back in the forward conduction characteristic. Fig. 4.13 shows the I~V characteristics at different Arsenic implantation charges. According to these curves, a processing split can be used to optimize the device.

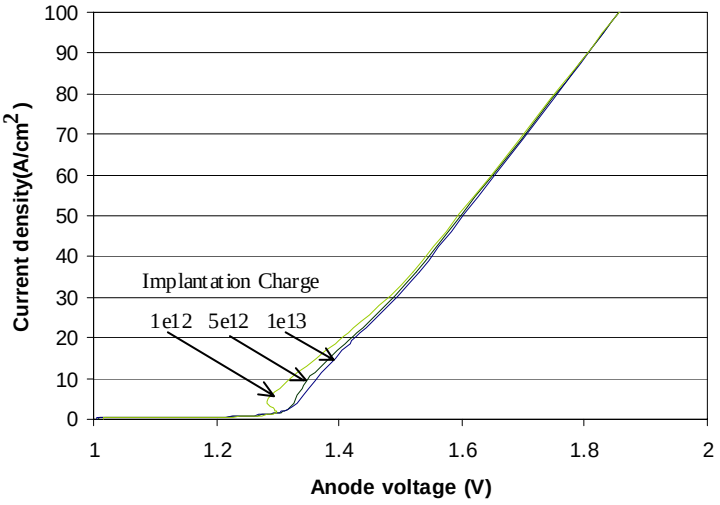


Fig. 4.13 The anode voltage and current curves at different threshold voltage adjustment implantation charges.

The HECT test structures were fabricated using <100> oriented N- substrate wafers with a thickness of 550 um. The doping concentration of the N- region is about 5×10^{13} cm^{-3} in order to obtain 4kV breakdown voltage. The complete processing flow is given in Appendix B. Fig. 4.14 shows the major steps of the HECT process.

The wafers were initially grown with a 1 um oxide using wet oxidation. Then photo resist was used to protect the front polished surface, while the backside oxide was etched. A heavy Boron implantation on the backside was followed to form the P+ anode region. After 12 hours high temperature drive, a 16 um deep junction was formed on the back of the wafers shown in Fig. 4.14(a). Then first mask (P_JTE) was used to open the windows in the JTE region followed by the JTE Boron implantation. After the implantation a high temperature drive was used to form the JTE junction. Another thick oxide was grown after this.

The second mask (Pbase) was used to open the window for the P base region implantation. Fig. 4.14(a) shows the structure after the window is opened. Boron implantation was again used to form the junction. Followed by the third mask (Pdiv) to open the window for the implantation of the P+ region. Fig. 4.14(b) shows the structure after the junction was formed.

Next, mask N+ was used to open the window for the implantation of the N+ emitter region. Fig. 4.14(c) shows the structure after the N+ junction was formed. Then another mask (Active) was used to get rid of the field oxide in the active region while keep the field oxide for the protection in the non-active region. The threshold adjustment implantation was followed to obtain the depletion mode NMOS1. Before that, a screen oxide must be grown for the protection of the surface. After the implantation, the screen oxide was etched and a new gate oxide is grown shown in Fig. 4.14(d).

The Contact mask was used to open the contact hole. The aluminum layer was sputtered immediately after the contact hole was formed to obtain a good ohm contact between the aluminum and the P+ or N+ region. The thickness of the aluminum was 1 um. The aluminum layer then underwent the wet etching using a mast (Metal) to form the pattern and using photo resistor to protect the area there the aluminum need to be remain. An optional mask (PAD) can

be used to open the pad region if a silicon nitride layer was grown for the protection of the aluminum.

After all the surface processing steps were finished, photo resist was spread on the front surface for the protection. Then a multi-layer metal, Cr-Ni-Ag, was deposited to provide a good ohmic contact and good adhesion to the P+ anode region.

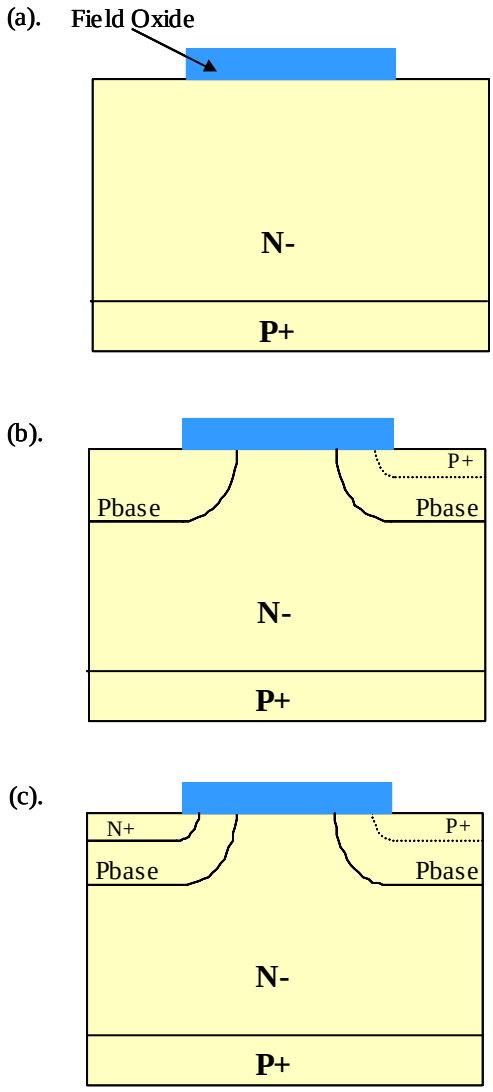


Fig. 4.14 Major steps of the HECT fabrication process.

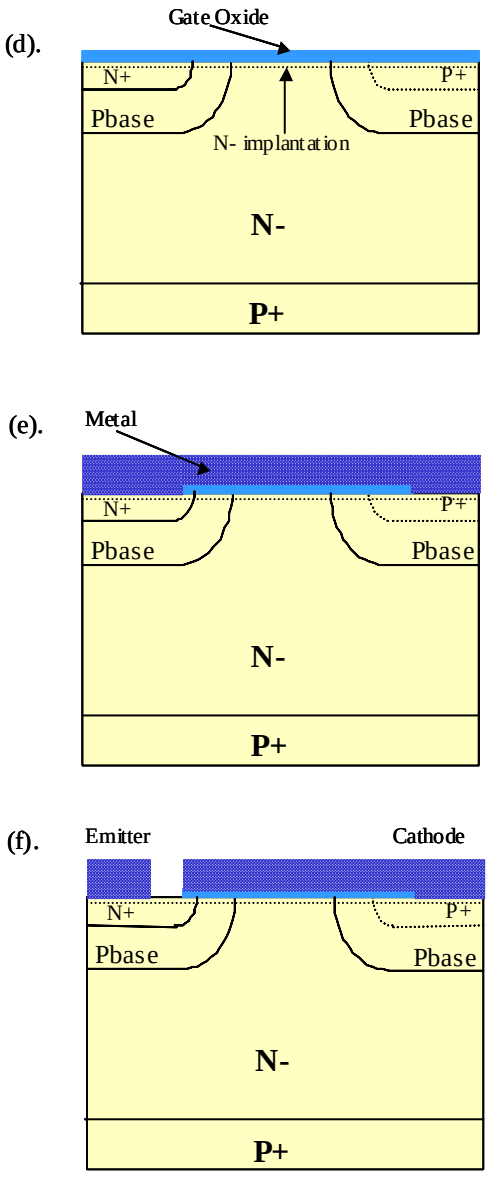


Fig. 4.14 Major steps of the HECT fabrication process (continued from previous page).

4.4 Experimental Results and Discussion

4.4.1 Device Characteristics of the Fabricated Device

The seven-mask HECT test structure was successfully fabricated in Hong Kong University of Science and Technology. The overall structure of the HECT after packaging is shown in Fig. 4.15. A commercial NMOSFET, Intersil HRF3205, is used as the external FET. A 25 um radius Aluminum is used for the wire bond shown in Fig. 4.15. Typical forward I~V characteristic of the HECT measured at room temperature at a gate voltage of 10 V is shown in Fig. 4.16 comparing with the simulation result when the minority carrier life time is 2.5 us. The forward voltage drop is about 4 V at the current density of 50 A/cm^2. It is lower than that of the IGBT at the same voltage range [3].

The current saturation capability of the packaged HECT was shown in Fig. 4.17 and Fig. 4.18. In Fig. 4.17, four different voltages were applied to the gate in order to get different current curve. Fig. 4.18 shows the current curve when the gate voltage is 3.25 V. The current saturated at the current density of 3 A/cm^2 and the anode voltage can go up to 45 V. The current saturation capability of the fabricated HECT can not be obtained at high voltage because the lateral PMOS1 shown in Fig. 4.1 is too weak to divert the hole current from the P base region of the emitter and make the voltage of the emitter increase. When the voltage of the emitter exceeds the breakdown voltage of the emitter and the cathode, the current of the device will increase instead of keeping constant value.

The measured breakdown voltage of the HECT is shown in Fig. 4.19(a) together with the floating emitter voltage. The device can sustain a high voltage up to 2000 V while keeps a small leakage current. Since the JTE termination is very sensitive to the charge implanted, it is hard to obtain the optimized breakdown voltage as simulated. Multiple fabrication is normally needed to obtain the highest BV. Fig. 4.19(b) shows the breakdown voltage between the cathode and the emitter.

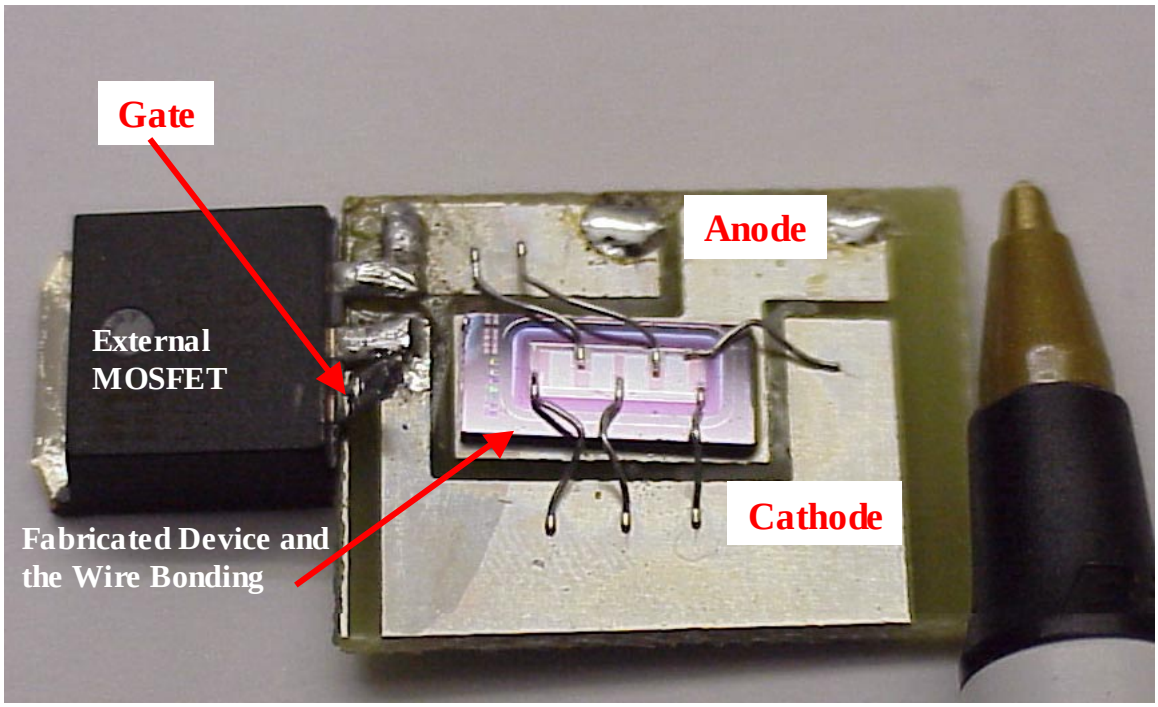


Fig. 4.15 The overall structure of the HECT after packaging.

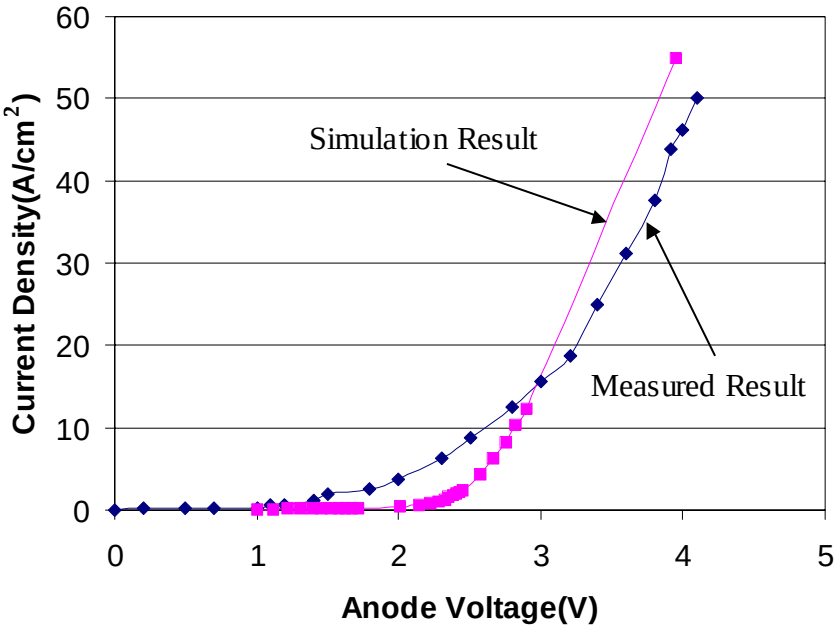


Fig. 4.16 The forward I~V curve of the fabricated device.

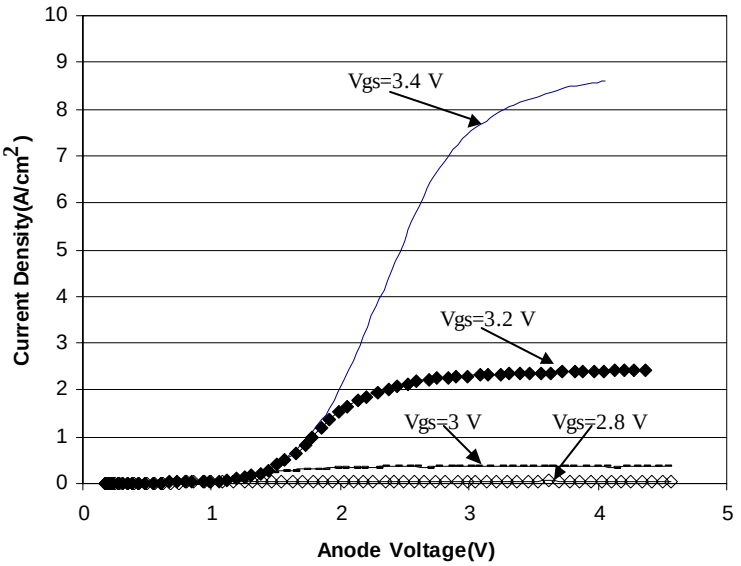


Fig. 4.17 The output characteristics of the fabricated device.

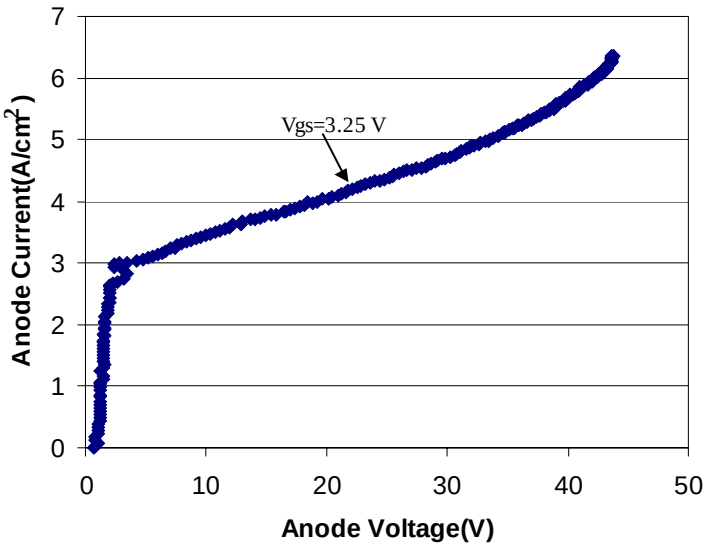
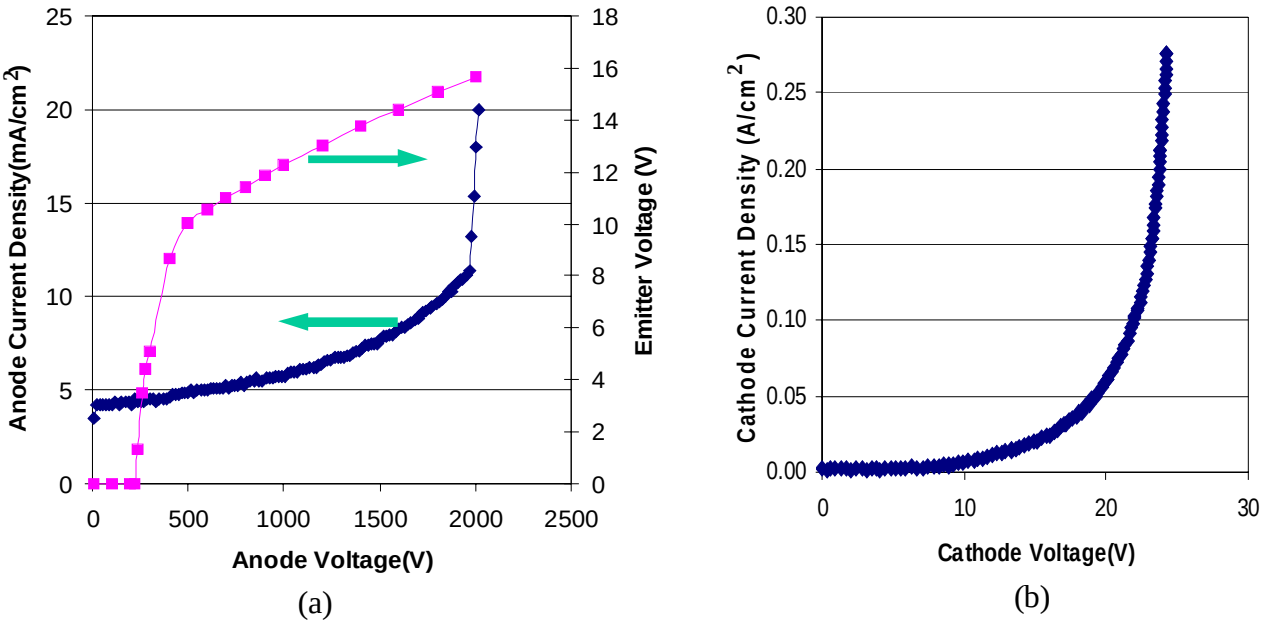


Fig. 4.18 The output characteristics of the fabricated device at high anode voltage.



(a) (b)

Fig. 4.19 The breakdown voltage between the anode and the cathode (a) and the breakdown voltage between the cathode and the emitter (b).

4.4.2 Turn-on and Turn-off Experiments

In order to perform switching measurements for the packaged HECT, a 250 us wide voltage pulse was applied to the gate. The maximum voltage of the pulse is 15 V and the minimum voltage is –5. Fig. 4.20 shows the resistive load switching circuit. The V_{source} is the bus voltage and will be a fixed value during switching. R is the load resistor. The V_R is the voltage on the resistor. The V_g is the gate pulse voltage source that controls the turn-on and turn-off of the device. Fig. 4.21 shows a typical voltage waveform during switching. When the gate voltage is –5 V, the HECT is off. The V_{anode} equals to the V_{source} and there is no current through the R. The emitter of the HECT will float and stay at a value decided by the anode voltage as shown in Fig. 4.19. Then, when the gate voltage increases to 15 V, the HECT turns on and the V_{anode} decreases to a low value. Since the V_{source} keeps constant, there will be a current through the R and the device. The current value is decided by the source voltage and the forward voltage drop of the HECT. When the gate voltage pulse is finished, the HECT is turned off and the V_{anode} goes up again to approach the source voltage. Fig. 4.22 shows the voltage waveform during turn-off. V_R is the voltage on the resistor. When the turn-off finished, the V_{anode} should equal to the source voltage and there is no current through R and the device. At the beginning of the turn-off, the $V_{emitter}$ increases to a high value, then decreases to the initial level. That is because the emitter of the HECT is floating when the device is turned off. It keeps collecting hole current and makes the voltage increasing until the PMOS1 shown in Fig. 4.2 turns on and diverts the hole current into the cathode directly. Simulations were done to study this phenomenon and will be discussed later.

The source voltage can be increased when R is fixed until the turn-off failed. Such failure points are the resistive turn-off capability of the device (RBSOA). Fig. 4.23 shows the measured RBSOA of the HECT. It is quite small comparing with the simulated RBSOA shown in Fig. 4.6. A set of turn-off simulations were done to analyze the reason.

Fig. 4.24 shows the simulated current and voltage waveform during turn-off using the turn-off circuit shown in Fig. 4.5. The first one shows the successful turn-off when the anode

voltage is 500 V and current is 100 A. The second one is the failed turn-off at the same anode voltage and current, but the breakdown of the emitter and the cathode is decreased in order to create the failure. The voltage and current point, 500 V and 100 A, is far below the simulated shown in Fig. 4.6. However, the failure can be created if the breakdown of the emitter and the cathode decreases to a certain value. As observed in the measured waveform, Fig. 4.21, the emitter voltage of the HECT will increase to a high level when the turn-off begins partly due to the stray inductance of NMOS2 connection. This is also observed during the simulation shown in Fig. 4.24. When the turn-off is successful, the emitter voltage increases to a high value and decrease during turn-off shown in Fig. 4.24(a). At the same time, the anode voltage keeps increasing till reach the source votlage. In the failed turn-off case, the emitter voltage increases to a high value, but will stay there and the anode voltage stops increasing. The current is still flowing through the device.

Three time instances during turn-off were selected and the current flowlines at the selected points were shown in Fig. 4.25. At point A, the NMOS2 shown in Fig. 4.2 is cut off and the emitter becomes floating. No current can flow out of the emitter, however, the hole current of the main thyristor keeps flowing into the emitter because the thyristor is still in its latching condition. The hole current collected by the emitter will make the voltage of the emitter increase as seen in Fig. 4.24(a) and (b). So does the voltage of the P base of the thyristor. If the voltage of the P base exceeds the value of the threshold voltage of the PMOS1, the PMOS1 begins conducting hole current as shown in Fig. 4.25(b). Therefore, the hole current is diverted into the cathode instead of going into the emitter. The voltage of the emitter will stop rising and begins decreasing because of leakage current of the emitter junction. The thyristor gets out of the latching state because the decrease of the electron injection. The turn-off is successful. If the voltage of the emitter reaches the breakdown of the emitter and the cathode before the PMOS1 diverts all the hole currents, the hole current from the thyristor will flow into the cathode through the breakdown mechanism of the emitter junction. Then the emitter voltage will stay at the breakdown level and the thyristor keeps its latching state. The anode voltage will stop increasing and current will keep flowing through the thyristor. The turn-off then failed as shown in Fig.

4.25(c). In actual test, the device is normally destroyed after such a turn-off failure. It is clear that more works should be done to improve the diverting capability of the PMOS1 in order to get a large RBSOA. The emitter to cathode breakdown voltage should also be improved to realize the potential of the ECT.

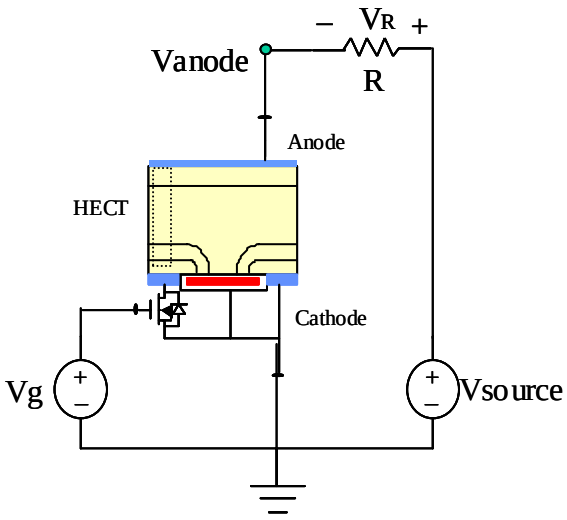


Fig. 4.20 Test circuit used to perform the resistive load switching test.

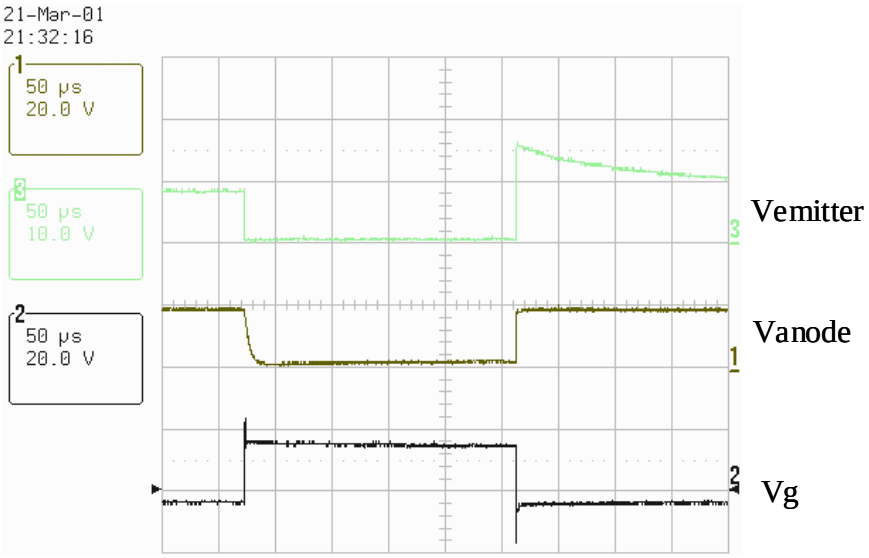


Fig. 4.21 The voltage waveform during switching.

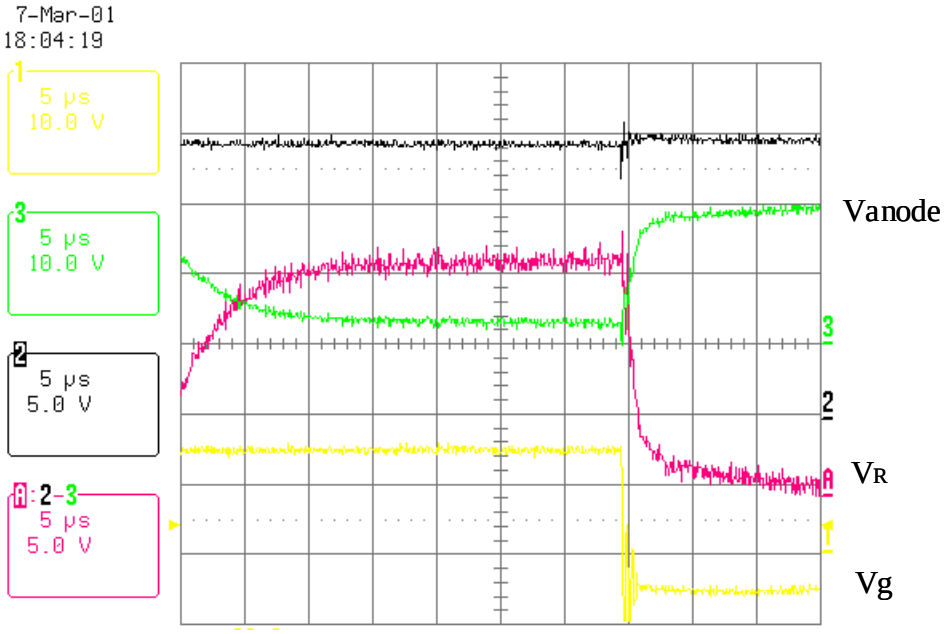


Fig. 4.22 The voltage waveform during turn-off.

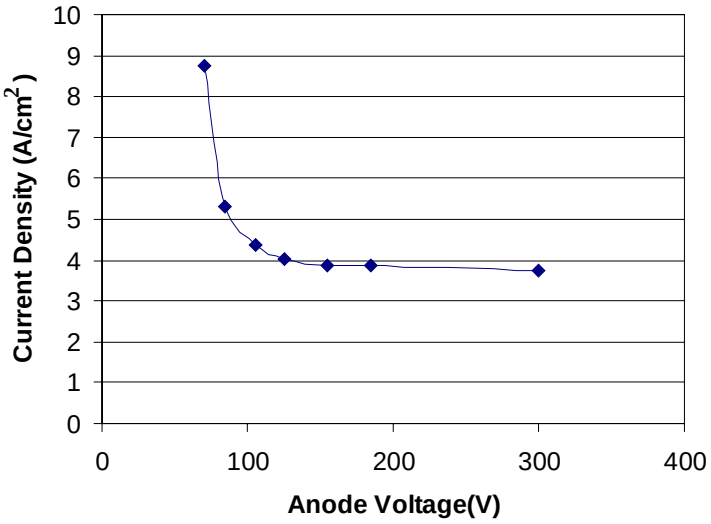


Fig. 4.23 The measured RBSOA of the HECT.

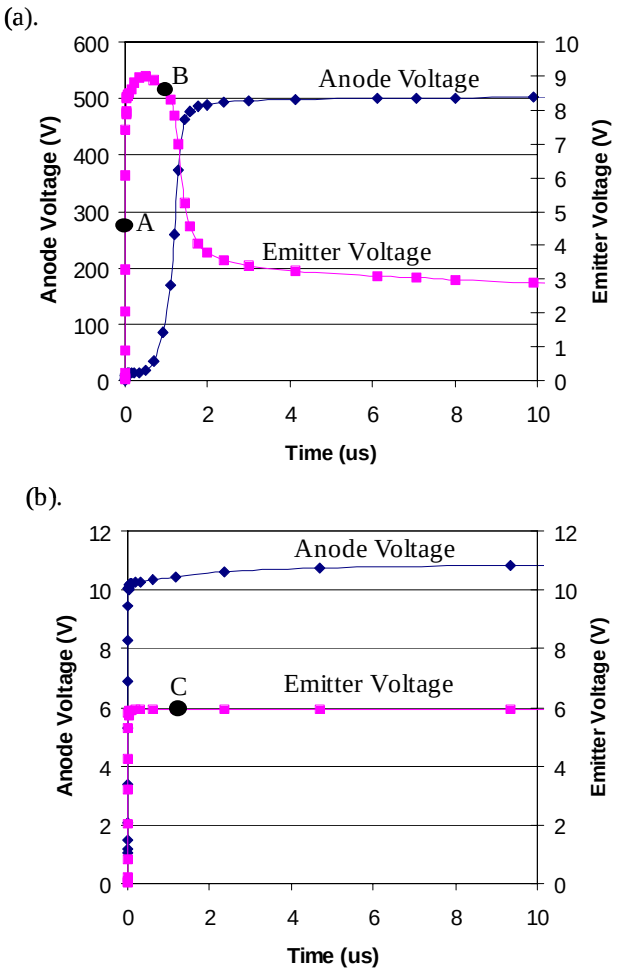


Fig. 4.24 The current and voltage waveform during turn-off (a) successful turn-off (b) turn-off failed.

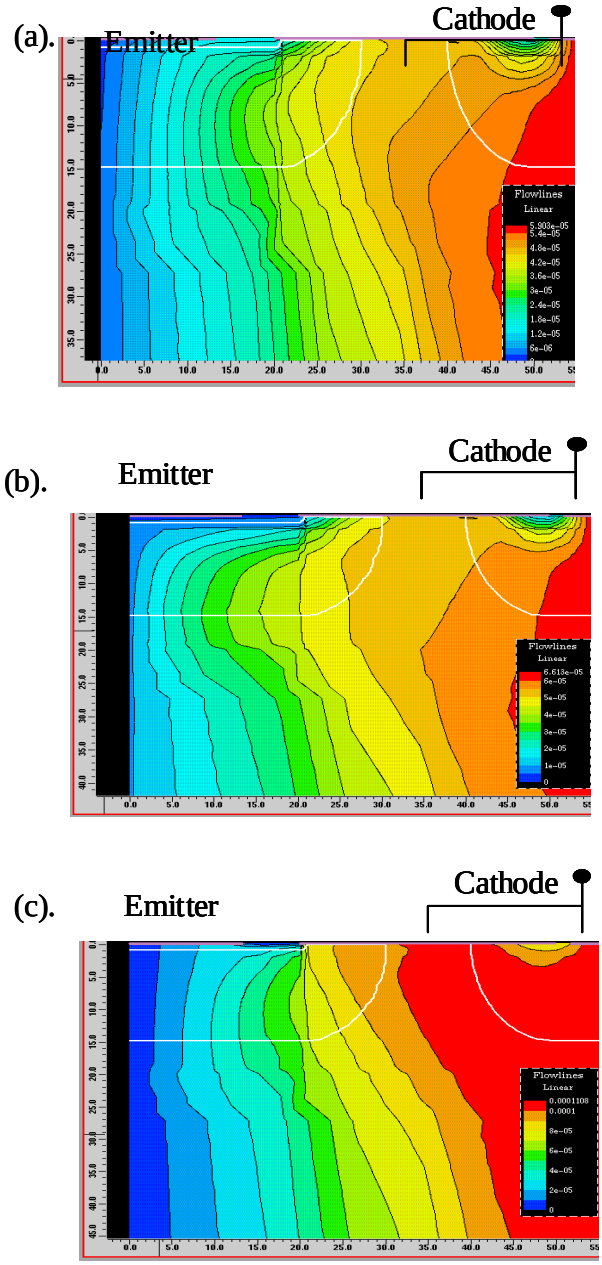


Fig. 4.25 The current flowlines of the HECT during turn-off corresponding to the point A,B,C shown in Fig. 4.24.

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Chapter 5 Conclusions and Future Work

In this research work, a new MOS-gated thyristor called Emitter Controlled Thyristor (ECT) has been developed from a conceptual stage to a fully operation device. The ECT is composed of emitter short FET, emitter switch FET and depletion mode turn-on FET integrated all together with the thyristor in order to obtain a good control over the thyristor. Two novel ECT structures, a monolithic ECT and a hybrid ECT, were demonstrated through numerical simulations and chip fabrications. In this chapter, the research is summarized and potential future work on the subject is suggested.

5.1 Investigation of the Monolithic ECT

A novel monolithic ECT structure that utilizes the ECT concept was proposed first. The emitter short FET, emitter switch FET and turn-on FET are all integrated on the surface of a high voltage thyristor. Numerical simulation results show the ECT has a better conductivity modulation than that of the IGBT. Hence, the forward voltage drop of the ECT is lower than that of the IGBT. It is also shown that the ECT exhibits superior high voltage current saturation capability hence the FBSOA. The technology trade-off curve of the ECT is also better than that of the IGBT because of the stronger conductivity modulation.

A 1200 V monolithic ECT structure was optimized and a ten-mask processing procedure was designed to fabricate the test structure. The fabrication work was completed in Cornell Nano-fabrication Facility. It was experimentally confirmed that the ECT could achieve superior forward voltage drop and high voltage current saturation capability.

5.2 Investigation of the Hybrid ECT

A Hybrid ECT (HECT) structure was also developed in this research work. The HECT uses an external FET to realize the emitter switching function, hence a complicated fabrication issue is separated into two simple one. The cost of the fabrication decreases and the yield increases due to the hybrid integration. Numerical simulations were done to demonstrate the superior on state voltage drop and the high voltage current saturation capability.

A 4 kV HECT then was designed and a seven-mask processing procedure was developed in order to fabricate the test structure. The fabrication was completed in Hong Kong Science and Technology University. Experimental results show that the HECT could achieve the lower forward voltage drop and superior current saturation capability. Resistive switching test was carried out to demonstrate the switching characteristics of the HECT.

5.3 Future Work

(1). The fabricated monolithic ECT devices consist 10~20 unit cells capable of carrying 100~200 mA of current. Larger devices need to be fabricated to carry several amperes of current to observe if the devices exhibit the same behavior when scaled up in dimension.

(2). Due to the functional requirement, the layout of the cathode metal and control gate of the monolithic ECT are finger like. The cathode metalization could not form a large continuous metal plate. This will limit the current capability of the ECT because of the limitation of the metal strip width in the layout design. More works needed to be done to improve the layout of the devices to obtain superior current carrying capability.

(3). The edge termination of the HECT is sensitive to the implanted JTE dose and it is hard to obtain the optimized blocking voltage. A new edge termination design or a new doping distribution needs to be developed to make the blocking voltage of the edge termination stable and optimized.

(4). The current capability of the emitter short FET of the HECT is weak and cannot fulfill the designed function to bypass the whole emitter current directly into the cathode. More

works need to be done to improve the emitter short FET design and obtain the excellent high voltage current saturation capability.

(5). During the operation of power devices, the device temperature is usually higher than the ambient temperature because of the power dissipation. The characteristics of these devices at high temperatures need to be investigated.

Appendix A: Process Flow of the Monolithic ECT

Step	Process Split	Process Description
1	All	Field Oxidation and Active Etch: 1.1 RCA Clean 1.2 Thermal Oxidation: wet oxide, temp=1150°C time=180'WO+10'N, test=1.4um 1.3 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 1.4 Expose Mask No.1 Active (focus=251 expose time=0.5), misalignment key test: less than 0.5 um 1.5 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson 1 min to get rid of PR about 100Å. 1.6 BOE(6:1) etching: 17 min to etch oxide 1.4um. 1.7 Strip PR by using 1165
2	All	JFET Implantation and Diffusion: 2.1 RCA Clean(use HF to get rid of native oxide) 2.2 Grow screen oxide: dry oxide, temp=1000°C time=17'DO+10'N, test=300Å 2.3 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 2.4 Expose Mask No.2 JFET (focus=251 expose time=0.5), misalignment key test: less than 1 um 2.5 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 2.6 Ion Implantation: As dose=1e12 energy=100KeV 2.7 Strip PR bye using 1165 for 1 hour 2.8 RCA Clean 2.9 Diffusion temp=1100°C time=200min 2.10 Strip oxide by using HF for 1 min.
3	All	Gate Oxide and Poly Mask: 3.1 RCA Clean 3.2 Grow Gate Oxide: dry oxide, temp=1000°C time=30min, test=500Å 3.3 LPCVD Poly: n+ type doped, temperature=650 °C, time=110 min, test=0.55 um 3.4 Grow oxide temp=950 °C, time=20 min, test=0.1 um 3.5 Put PR(positive 1813 for 5*stepper): HMDS, spin at

		4000, bake 115°C for 1 min 3.6 Expose Mask No.3 Poly (focus=251 expose time=0.5), misalignment key test: less than 1 um. 3.7 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 3.8 Etch oxide, wet etch (HF, 3.5 min) 3.9 Etch poly, dry etch (5 min) 3.10 Strip PR by using 1165
4	1,5 dose=2e12 2,6 dose=8e12 3,7 dose=2e13 energy=100KeV	Pwell Implantation and Diffusion: 4.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 4.2 Expose Mask No. 4 Pwell (focus=251 expose time=0.5), misalignment key test: less than 0.5 um 4.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 4.4 Ion Implantation: three diverts, Boron 4.5 Strip PR by using 1165 for 1 hour 4.6 RCA Clean 4.7 Diffusion: temp=1150°C time=600min
5	All	Pbase Implantation and Diffusion: 5.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 5.2 Expose Mask No.5 Pbase (focus=251 expose time=0.5), misalignment key test: less than 1 um 5.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 5.4 Ion Implantation: Boron dose=1e14 energy=60KeV 5.5 Strip PR by using 1165 for 1 hour 5.6 RCA Clean 5.7 Diffusion: temp=1100°C time=350min
6	All	Pdiv Implantation and Diffusion: 6.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 6.2 Expose Mask No.6 Pdiv (focus=251 expose time=1.0), misalignment key test: less than 1 um 6.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 6.4 Ion Implantation: Boron dose=1e15 energy=150KeV 6.5 Strip PR by using 1165

		6.6 RCA Clean 6.7 Diffusion: temp=1050°C time=30min
7	All	Nplus Implantation and Diffusion: 7.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 7.2 Expose Mask No.7 Nplus (focus=251 expose time=0.5), misalignment key test: less than 1 um 7.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 7.4 Ion Implantation: Phosphorus dose=5e15 energy=30KeV 7.5 Strip PR by using 1165 7.6 RCA Clean 7.7 Diffusion: temp=1050°C time=60 min
8	All	Deposit Oxide and Contact Mask: 8.1 PECVD Oxide: 1um, time=30 min 8.2 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 8.3 Expose Mask No.8 Contact (focus=251 expose time=0.5), misalignment key test: less than 1 um 8.4 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 8.5 Etch Oxide: dry etch 1.05um oxide, time=27 min 8.6 Strip PR by using 1165
9	All	Metal Mask: 9.1 Sputter Al about 2um 9.2 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 9.3 Expose Mask No.9 Metal (focus=251 expose time=0.5), misalignment key test: less than 1 um 9.4 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 9.5 Etch Al 2um, dry etch, time=25 min 9.6 Strip PR by using 1165
10	5, 6, 7 only	Deposit Nitride and Pad Mask: 10.1 Deposit Nitride 1um 10.2 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 10.3 Expose Mask No.10 Pad (focus=251 expose

		time=0.5), misalignment key test: less than 1 um 10.4 Develop in CD-26 for 1 min, bake 90°C for 30 min, Branson for 1 min to get rid of PR about 100Å. 10.5 Etch Nitride 1um, dry etch, time=30 min 10.6 Strip PR by using 1165

Appendix B: Process Flow of the Hybrid ECT

Step	Process Split	Process Description
1	Split: energy=60KeV dose=1.5E12, 2E12, 3E12;	Backside Diffusion, Field Oxidation and P_JTE Mask: 1.8 RCA Clean(use HF to get rid of the oxide on both surface) 1.9 Thermal Oxidation: wet oxide, temp=1150°C time=180'WO+10'N, thickness=1.5~2um 1.10 Put PR(positive 1813 for 5*stepper) on frontside: HMDS, spin at 4000, bake 115°C for 1 min 1.11 BOE(6:1) etching backside field oxide 1.12 *Backside Diffusion Boron dose=5e15 1.13 *Diffusion time=100min temp=1150°C 1.14 BOE(6:1) etching front field oxide 1.15 RCA Clean 1.16 Grow Screen oxide 400Å 1.17 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 1.18 Expose Mask No.1 P_JTE 1.19 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å 1.20 Strip PR by using Acetone 1.21 *Boron Implantation (split) 1.22 *Diffusion temp=1150 time=200min 1.23 RCA Clean(use HF to get rid of the oxide on both surface) 1.24 Thermal Oxidation: wet oxide, temp=1150°C time=180'WO+10'N, thickness=1.5~2um
2	All	Pbase implantation: 2.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 2.2 Expose Mask No.1 Pbase 2.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å. 2.4 BOE(6:1) etching field oxide 2.5 Strip PR by using Acetone 2.6 RCA Clean 2.7 Grow Screen oxide 400Å

		2.8 Boron Implantation dose=1e14 energy=60KeV 2.9 RCA Clean 2.10 *Diffusion temp=1150 time=600min
3	All	Pdiv Implantation and Diffusion: 3.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 3.2 Expose Mask No.2 Pdiv 3.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å. 3.4 *Ion Implantation: Boron dose=1e15 energy=60KeV 3.5 Strip PR bye using 1165 for 1 hour 3.6 RCA Clean 3.7 *Diffusion temp=1100°C time=60min
4	All	N+ Implantation and Diffusion: 4.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 4.2 Expose Mask No.3 N+ 4.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å. 4.4 BOE(6:1) etching field oxide 4.5 Strip PR bye using 1165 4.6 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 4.7 Expose Mask No.3 N+ 4.8 RCA 4.9 Grow screen oxide about 400Å 4.10 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å. 4.11 *Ion Implantation: Phosphorus dose=5e15 energy=30KeV 4.12 Strip PR bye using 1165 for 1 hour 4.13 RCA Clean 4.14 *Diffusion: temp=1050°C time=60 min
5	Dose=1e12; 5e12; 1e13; Energy=60Kev	Field Oxide Etch and n_vth implant: 5.1 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 5.2 Expose Mask No.4: Active region 5.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å. 5.4 BOE(6:1) etching field oxide

		5.5 Strip PR by using Acetone 5.6 RCA Clean 5.7 Grow screen oxide 400Å 5.8 Ion Implantation (split) 5.9 RCA Clean 5.10 *Diffusion time=30min temp=1000 5.11 Etch oxide by HF
6	All	Gate oxide and contact Mask: 6.1 grow gate oxide 1000Å 6.2 Expose Mask No.5 contact 6.3 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å. 6.4 Etch oxide 6.5 Strip PR by using 1165 for 1 hour
7	All	Metal mask: 7.1 Sputter Al about 2um 7.2 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min 7.3 Expose Mask No.6 Metal 7.4 Develop in CD-26 for 1 min, bake 90°C for 30 min, disgunt for 1 min to get rid of PR about 100Å. 7.5 Etch Al 2um 7.6 Strip PR by using Acetone
8	All(Optional)	Deposit Nitride and Pad Mask: 8.1 Deposit Nitride 1um 8.2 Put PR(positive 1813 for 5*stepper): HMDS, spin at 4000, bake 115°C for 1 min Expose Mask No.10 Pad (focus=251 expose time=1.0) 8.3 Develop in CD-26 for 1 min, bake 90°C for 30 min,disgunt for 1 min to get rid of PR about 100Å. 8.4 Etch Nitride 1um 8.5 Strip PR by using Acetone
9	All(Backside)	Backside metal: 9.1 Laping about 1~2um (smooth) 9.2 Clean 9.3 Metalization, (avoid thermal processing)

Vita

The author, Yin Liu, was born in Anyang, Henan, China, in August 1974. He received the B.S. degree in Electronic Engineering from Xi'an Jiaotong University, Xi'an, China, in 1995, and M.S. in Mircroelectronics from Tsinghua University, Beijing, China, in 1998. Since 1998, he has been with the Virginia Power Electronics Center, now Center for Power Electronics Systems, in the Electrical and Computer Engineering Department of Virginia Tech, as a graduate research assistant. His research interests include power semiconductor devices and integrated circuit.