Advanced High-Frequency Electronic Ballasting Techniques for Gas Discharge Lamps

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(ABSTRACT)

Small size, light weight, high efficacy, longer lifetime and controllable output are the main advantages of high-frequency electronic ballasts for gas discharge lamps. However, power line quality and electromagnetic interference (EMI) issues arise when a simple peak rectifying circuit is used. To suppress harmonic currents and improve power factor, input-current-shaping (ICS) or power-factor-correction (PFC) techniques are necessary.

This dissertation addresses advanced high-frequency electronic ballasting techniques by using a single-stage PFC approach. The proposed techniques include single-stage boost-derived PFC electronic ballasts with voltage-divider-rectifier front ends, single-stage PFC electronic ballasts with wide range dimming controls, single-stage charge-pump PFC electronic ballasts with lamp voltage feedback, and self-oscillating single-stage PFC electronic ballasts.

Single-stage boost-derived PFC electronic ballasts with voltage-divider-rectifier front ends are developed to solve the problem imposed by the high boost conversion ratio required by commonly used boost-derived PFC electronic ballast. Two circuit implementations are proposed, analyzed and verified by experimental results.

Due to the interaction between the PFC stage and the inverter stage, extremely high bus-voltage stress may exist during dimming operation. To reduce the bus voltage and achieve a wide-range dimming control, a novel PFC electronic ballast with asymmetrical duty-ratio control is proposed. Experimental results show that wide stable dimming operation is achieved with constant switching frequency.

Charge-pump (CP) PFC techniques utilize a high-frequency current source (CS) or voltage source (VS) or both to charge and discharge the so-called charge-pump capacitor

in order to achieve PFC. The bulky DCM boost inductor is eliminated so that this family of PFC circuits has the potential for low cost and small size. A family of CPPFC electronic ballasts is investigated. A novel VSCS-CPPFC electronic ballast with lamp-voltage feedback is proposed to reduce the bus-voltage stress. This family of CPPFC electronic ballasts are implemented and evaluated, and verified by experimental results.

To further reduce the cost and size, a self-oscillating technique is applied to the CPPFC electronic ballast. Novel winding voltage modulation and current injection concepts are proposed to modulate the switching frequency. Experimental results show that the self-oscillating CS-CPPFC electronic ballast with current injection offers a more cost-effective solution for non-dimming electronic ballast applications.

To My Parents Rencai Tao and Jingfang Hui

My Wife Zhimei Ding

And Son Liangyu Tao

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Chapter 1 Introduction

1.1 Background

Light is defined as visually evaluated radiant energy, which stimulates man's eyes and enables him to see [F1]. Man has always sought to counter the influence of the darkness by creating artificial light. In ancient times, man had very poor ways of making artificial light. He tried to adapt natural luminous phenomena with the aid of rush lights, torches, oil lamps, candles, etc. to this purpose. During the past 200 years, more systematic research has been carried out, and ever-increasing technological progress has enabled man to make real advances in the difficult search for effective light sources. The discovery of electric power and the possibility of transmitting it in a simple manner facilitated the development of modern lamps.

Today there are nearly 6,000 different lamps being manufactured, most of which can be placed in the following six categories: incandescent, fluorescent, mercury vapor, metal halide, high-pressure sodium (HPS) and low-pressure sodium (LPS). Except for incandescent lamps, all of these light sources can be termed as gas discharge lamps. Fluorescent and LPS lamps operate on low-pressure gaseous discharge, and the mercury vapor, metal halide and HPS lamps operate on high-pressure gaseous discharge. The mercury vapor, metal halide and HPS types are commonly known as high-intensity discharge (HID) lamps.

The major characteristics to be considered when choosing a lamp are its luminous efficacy, life, lumen depreciation and color rendering [F1, pp.190]. Luminous efficacy is the measure of the lamp's ability to convert input electric power, in watts, into output luminous flux, in lumens, and is measured in lumens per watt (lm/w). The luminous flux of a light source is the electromagnetic radiation within the visible part of the electromagnetic spectrum multiplied by the sensitivity of man's eyes to that part of the

light from the source. The visible portion of the spectrum covers the wavelength range from approximately 380 nm to 780 nm (Figure 1-1), and the eye discriminates between different wavelengths in this range by the sensation of color in the manner illustrated by Figure 1-2. The life of a lamp is the number of hours it takes for approximately 50% of a large group of lamps of the same kind to fail. Failure means that the lamp will no longer light or that light output has dropped to a specific percentage value. Lumen depreciation during life is a characteristic of all lamps. This is a process of lamp aging, an important consideration in lighting design. Finally, there is the matter of color rendering. The lamp types do not provide the same nominal "white." Their difference in spectral distribution can produce two effects within a lighted space. Some of the colors of objects within that space can appear unnatural or faded – reds can appear brown, violets nearly black, etc. Second, the entire space may "feel" warm or cool. For example, a mercury lamp, lacking in reds and oranges, makes a space seem cool, whereas an incandescent lamp, with deficiencies in the blue and violets, makes a space feel warm.

Incandescent lamps and gas discharge lamps generate light through two different physical mechanisms of electrical energy conversion [F3]. Incandescent lamps use the Joule-heating process by electrically heating high-resistance tungsten filaments to intense brightness. The electric behavior is simple. The lamp current is determined by the applied voltage and the resistance of the tungsten filament, which is close to the *v-i* characteristic of a linear resistor. The spectrum of energy radiated from incandescent lamps is continuous with good color rendering. However, only about 10% of the electricity flowing through incandescent lamps is converted to light, as shown in Figure 1-3(a), and thus the luminous efficacy of incandescent lamps is low. Electric gas discharge lamps convert electrical energy into light by transforming electrical energy into the kinetic energy of moving electrons, which in turn becomes radiation as a result of some kind of collision process [F5]. The primary process is collision excitation of atoms in a gas to states from which they relax back to the lowest-energy atomic levels by means of the emission of electromagnetic radiation. The emitted electromagnetic radiation is not continuous, instead consisting of a number of more or less separate spectral lines. By modifying the composition of the gas used, the luminous efficacy can be varied considerably.

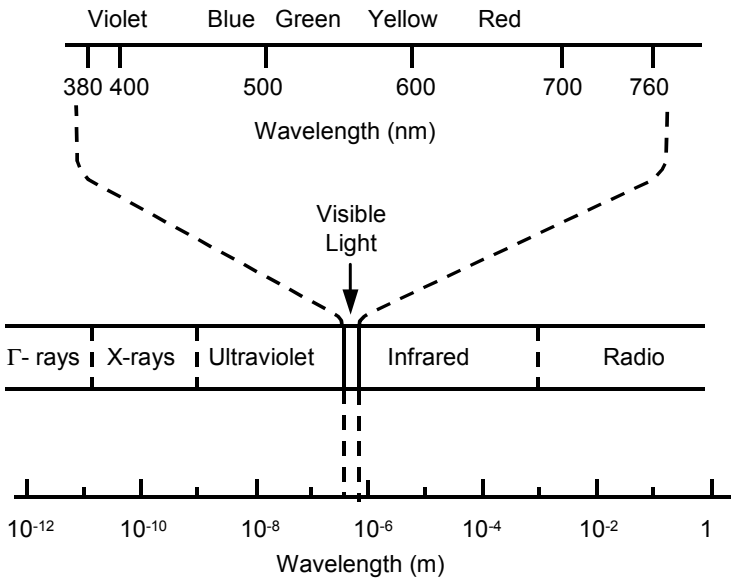


Figure 1-1. The electromagnetic spectrum [F2, p.3].

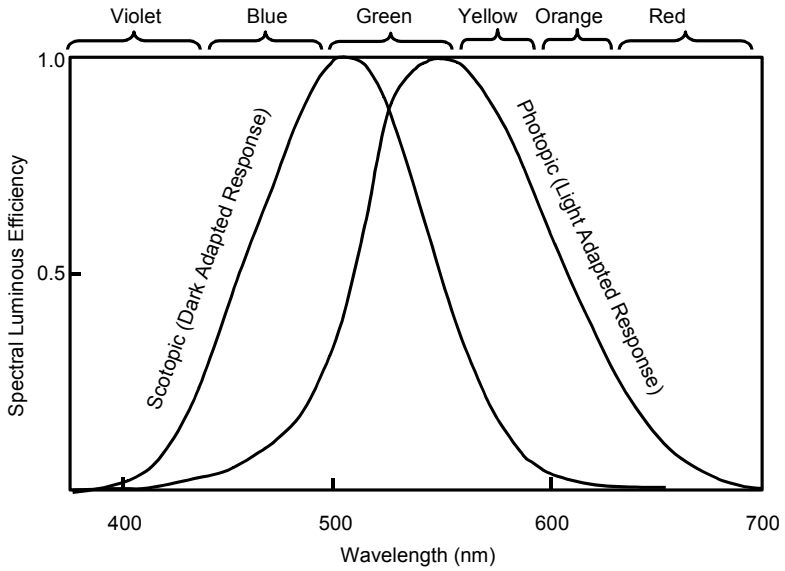


Figure 1-2. Relative response of the eye to light of various wavelengths [F2, p.10].

Compared with incandescent lamps, gas discharge lamps have three great virtues as light sources: They are efficient energy converters, transforming as much as 20% to 30% of the electrical energy input into light energy output, as shown in Figure 1-3(b); they last a long time, 18 times longer than incandescent lamps if fluorescent lamps are taken as an example (rated life up to 20,000 hours); and they have excellent lumen depreciation, typically delivering 60% to 80% of the initial level of light at the end of life.

Although gas discharge lamps have tremendous advantages over incandescent lamps, they require an auxiliary apparatus called a ballast to run with them. It is a well-known fact that gas discharge lamps have negative incremental impedance. Figure 1-4(a) shows a typical curve of discharge potential drop versus current when a lamp is operated from a DC power source. The curve can also be regarded as the locus of points (i,v) for which the time rate of change of electron density, dn_e/dt, is zero. For points above and to the right, dn_e/dt is greater than zero (production exceeds loss), and electron density would increase with time. For points below and to the left, dn_e/dt is less than zero, and electron density would decrease with time. Obviously, the slope of the curve, defined as incremental impedance $r \equiv dv/di$, is negative. The negative increase impedance characteristic poses a circuit problem for operating lamps. In general, a starting voltage V_s that is higher than the steady-state operation voltage is needed to establish ionization in the gas. After the discharge begins, the operating point (i,v) of the discharge would lie somewhere on the line of the constant $V = V_s$, which is in the domain for which the ionization rate exceeds the loss rate, and thus electron density n_e increases continuously with time. Consequently, the discharge current increases without any regulation, and eventually causes system failure.

As a result, gas discharge lamps cannot be directly connected to a voltage source. A certain impedance must be placed between the discharge lamp and the voltage source as a means to limit lamp current. For example, Figure 1-4(b) shows the effect of series resistance in stabilizing lamp current. The dotted lines V_{La} and V_R show the voltage potential across the discharge and resistor, respectively, and the solid line V_{AB} shows the potential across the pair in series.

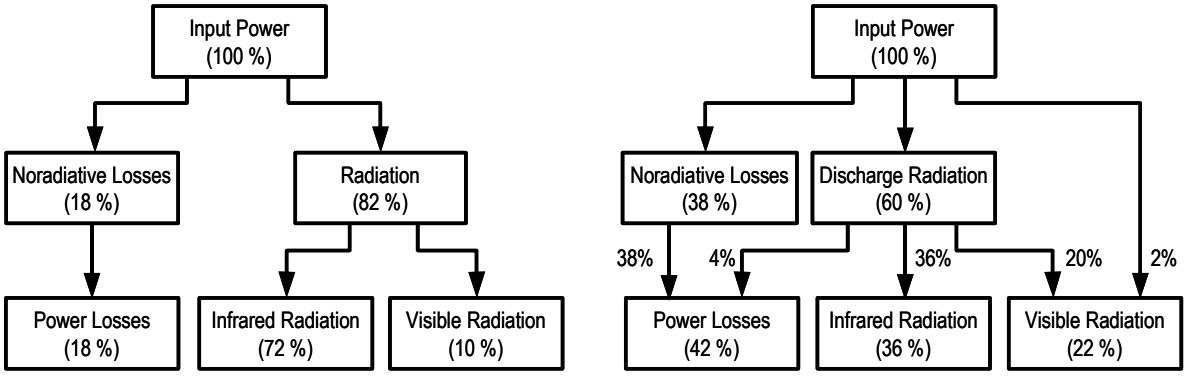


Figure 1-3. (a) Energy distribution of an incandescent lamp. About 10% of the energy is converted to light [F4, p.5]. (b) Energy distribution of a fluorescent lamp. About 22% of the energy is converted to light. Other discharge lamps have a similar percentage [F4, p.18].

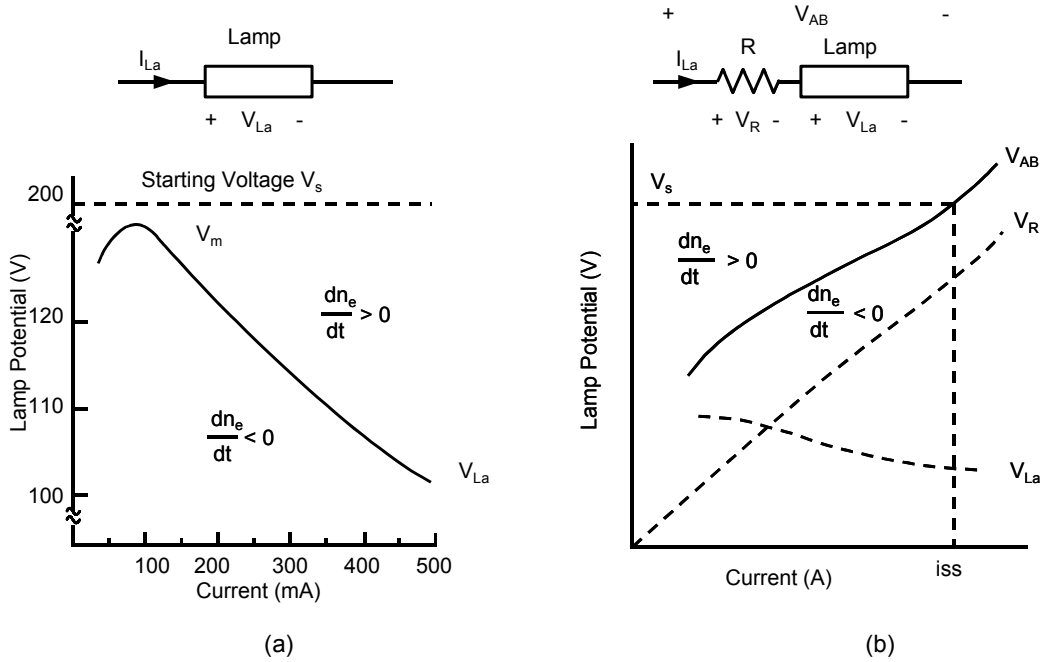


Figure 1-4. (a) Discharge potential drop versus current [F5, p.28]. (b) The effect of series resistance in stabilizing lamp current [F5, p.30].

Upon application of a starting voltage to the lamp-resistor system and establishment of ionization, the operating point (i,v) is in the domain of positive dn_e/dt, increasing the lamp current until it reaches the point (i_{ss},V_s). A further increase in current would move the operating point into the region of negative dn_e/dt, forcing the current back to i_{ss}. The resistor R helps to establish the stable operating point of the discharge lamp and acts as a ballast.

Obviously, the resistive ballast incurs large power loss and significantly reduces the system efficiency. Fortunately, most discharge lamps are operated in alternating-current (AC) circuits so that inductive or capacitive impedance can be used to provide current limitation. AC operation also balances the wearing of two electrodes and maintains a longer lamp life. The inductor (lag) and the inductor-capacitor (lead) ballast represent the conventional ballasting approaches, and are known as magnetic ballasts.

Magnetic ballasts are operated in 50/60Hz line frequency. Every half line cycle, they reignite the lamp and limit the lamp current. Although magnetic ballasts have the advantages of low cost and high reliability, there exist at least three fundamental performance limitations due to the low-frequency operation. First of all, the weight and volume of the ballast must be great. Second, the time constant of the discharge lamps is around a millisecond, which is shorter than the half line period, so the arc is reignited twice each cycle. Figure 1-5 shows the measured voltage and current waveforms of an F40T12 lamp operating at 60 Hz. After every line zero crossing, the lamp voltage waveform has a restrike voltage peak; during the rest of the cycle, the voltage does not vary much. This causes two big problems: The lamp electrode wearing is significant, and the lamp's output light is highly susceptible to the line voltage, which results in an annoying visible flickering [F6]. Finally, there is no efficient and cost-effective way to regulate the lamp power.

These drawbacks led to studying the use of high-frequency AC current to drive the discharge lamps. High-frequency operation not only results in significant ballast volume and weight reduction, but also improves the gas discharge lamp property. Figure 1-6 shows the measured voltage and current waveforms of the lamp operating with the same current level but at high frequency. The voltage and current waveforms are almost

proportional with the same *v-i* characteristic of a resistor, although this resistor is not linear and varies as a function of time and lamp current. The restrike voltage peak no longer exists. The recombination of ions and electrons in the discharge is very low. No reignition energy is needed. The lamp electrodes also sustain the electron density during the transition from cathode to anode function, resulting in additional energy savings. Therefore, the gas discharge itself is more efficient in high-frequency operation, contributing to an increased efficacy. Figure 1-7 shows the curve of fluorescent lamp efficacy versus lamp operating frequency [A2]. It shows that the efficacy increases by about 10% when the operating frequency is above 20 kHz. Other discharge lamps have a similar characteristic. The high-frequency operation also makes the lamp start easily and reliably, and eliminates audible noise and stroboscopic effect. In addition, due to the advances in power electronics, power regulation can be easily incorporated into the ballast, making intelligence and energy management feasible [A3].

Essentially, the high-frequency electronic ballast is an AC/AC power converter, converting line-frequency power from the utility line to a high-frequency AC power in order to drive the discharge lamp. Figure 1-8 shows the circuit diagram of typical high-frequency electronic ballasts. In high-frequency operation, a low lamp current crest factor (CF) is preferred. The CF is the ratio of the peak of the lamp current to the root-mean-square (RMS) value. For high-frequency ballasts, it is a ratio of the peak of the modulated envelope to the RMS value. The CF plays a significant role in ballast performance. As studies show, the electrode life is very sensitive to the CF, and the life of a gas discharge lamp is basically determined by its electrode's life. The higher the CF, the shorter the lamp life. The lamp life will drop to less than half if the CF becomes 2 [F3, pp.138]. A pure sine wave without modulation has a CF of 1.4; a triangular wave has a CF of 1.7. American National Standards Institute (ANSI) specifications recommend that the maximum CF be 1.7 [A4]. The CF is also a matter of lamplight flickering. Unlike in magnetic ballasts where the flickering is caused by the jitter of the ignition angle in a half-line cycle, the flickering is caused by the use of a modulated drive current to the lamp in electronic ballasts. A higher CF means higher current modulation.

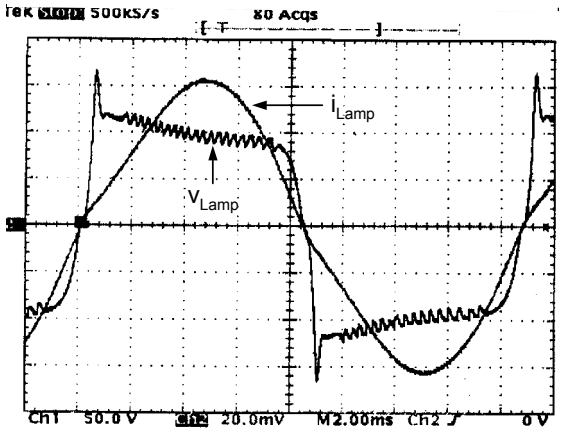


Figure 1-5. Measured lamp voltage and current waveforms at 60 Hz [A1].

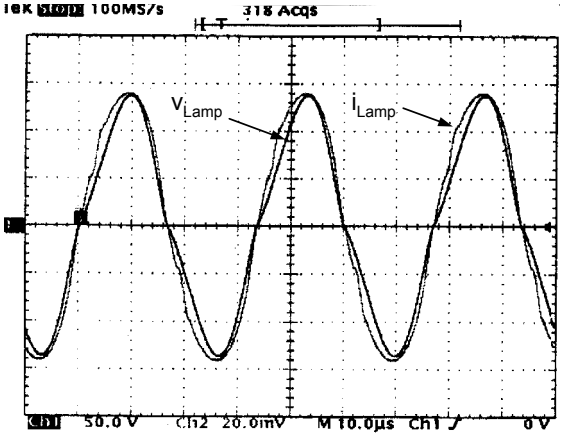


Figure 1-6. Measured lamp voltage and current waveforms at 30 kHz [A1].

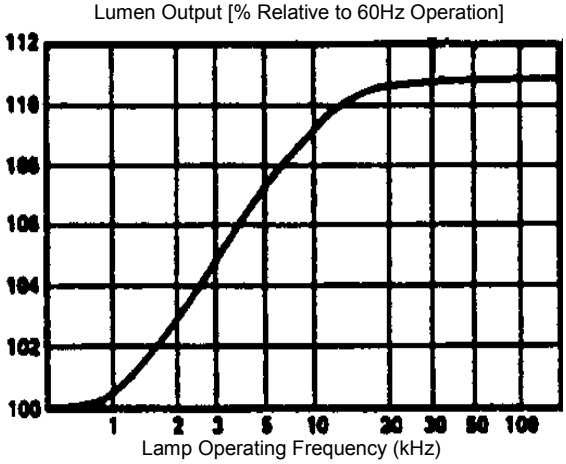


Figure 1-7. Fluorescent lamp efficacy versus lamp operating frequency [A2].

To maintain a low CF, a bulk capacitor is necessary to handle the variations between the input pulsating power and the constant output lamp power. A conventional practice is to locate a bulk capacitor right behind the diode rectifier, as shown in Figure 1-8(b). This is a rather simple solution for improving CF. However such a configuration draws current from the AC line in only a small conduction angle, producing a very poor power factor (PF) with rich harmonic currents. These harmonic currents in an AC utility line will cause a lot of problems, such as voltage distortion, voltage flickering, transformer overheating, generator high-torque rippling, and severe electromagnetic interference (EMI) noise to the telecom/datacom systems and electronic data processing systems.

Lighting equipment represents a significant portion of the total electrical load. As more and more electronic ballasts are put into use, it becomes increasingly important to maintain high PF and low harmonics.

PF is a commonly used measure of power quality, which is defined as the ratio of the average power to the apparent power at the AC terminal, and can be expressed as a product of the distortion factor K_d and the displacement factor K_θ assuming an ideal sinusoidal input voltage, as shown in (1.1). K_d is defined as the ratio of the fundamental RMS current to the total RMS current, and K_θ is defined as the cosine of the displacement angle θ between the fundamental input current and voltage. The PF is required by the building code to be at least 0.9, either leading or lagging [A5]. Usually, a slightly leading PF is preferred. Another important measure of the input-current quality is the total harmonic distortions (THD), defined as (1.2), where I_k is the RMS value of the k^{th} current harmonics. The relationship between PF and THD can be expressed as (1.3), where there is no DC component in the input current.

$$PF \equiv \frac{Average\ power}{Apparent\ power} = \left(\frac{I_{rms,1}}{I_{rms}} \right) \cos\theta = K_d K_\theta \tag{1.1}$$

$$THD \equiv \sqrt{\frac{\sum_{k=2}^{\infty} I_k^2}{I_1^2}} \tag{1.2}$$

$$PF = \frac{K_\theta}{\sqrt{1 + THD^2}} \tag{1.3}$$

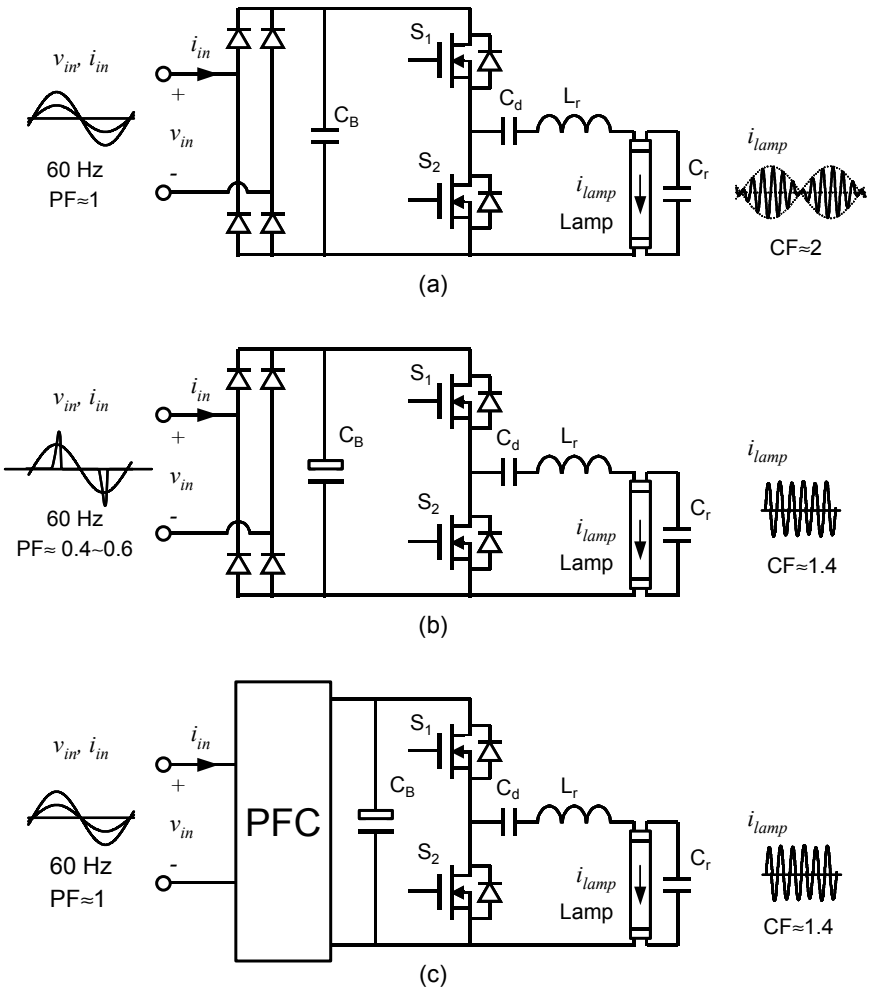


Figure 1-8. Circuit diagrams of high-frequency electronic ballast: (a) with small bus capacitor, (b) with large bus capacitor, and (c) with large bus capacitor and PFC stage.

Table 1-1. Limits for Class C equipment (IEC 1000-3-2).

Harmonic Order n	Maximum Permissible Harmonic Current, Expressed as a Percentage of the Input Current at the Fundamental Frequency %
2	2
3	$30 \bullet \lambda^*$
5	10
7	7
9	5
$11 \le n \le 39$	3
* λ is the Circuit Power Factor	

From (1.1) to (1.3), both the distortion factor and the displacement factor must be large in order to get a high PF. In practice, harmonics are important concerns. Several standards have been established to limit harmonics. The most commonly cited standard in lighting equipment industry is the IEC 1000-3-2 Class C, which sets the harmonic current limits by percentage, as listed in Table 1.1 [F7].

To achieve high PF and low current harmonics, the use of a power-factor-correction (PFC) or input-current-shaping (ICS) method is necessary. One simple approach is to use a passive filter. However, passive filter components are usually bulky and ineffective. A more effective approach is to use active means. A common practice is to employ the so-called two-stage approach, in which a switching mode PFC stage is added to the conventional electronic ballast, providing almost unity PF AC/DC rectification from the utility line, as shown in Figure 1-8(c).

Electronic ballasts can provide dimming capability. Dimming controls have been broadly employed in recent lighting systems to provide energy savings and improved ergonomics. Study shows that energy savings of more than fifty percent can be achieved with dimming controls [C1, C2]. The circuit shown in Figure 1-8(c) can be used as a dimmable electronic ballast when an appropriate control circuit is employed. The dimmable electronic ballast should have all the characteristics required for the non-dimmable electronic ballast. An additional requirement is that the dimming control should be done smoothly without abrupt changes in light levels when transitioning from one light level to another. Flickering and striation should not be observed.

In summary, compared with magnetic ballasts, high-frequency high-PF electronic ballasts provide remarkably improved performances as far as 1) improved circuit efficiency; 2) improved luminous efficacy of lamps; 3) improved lamp lifetime; 4) reduction in size and weight; 5) absence of flickering; 6) elimination of audible noise; 7) high input PF with low THD; 8) better-controlled starting and operating conditions; and 9) facility for energy management, such as remote switching, dimming and photocell control.

However, regardless of these advantages, electronic ballasts have been unable to supersede the magnetic ballasts for over three decades [A6]. There are probably two

major reasons for the long delay. First, it took many years for power devices to evolve. Second, the initial cost of electronic ballasts is much higher than that of magnetic ballasts. In the case of residential applications, one of the most undesirable points is the high initial cost, although the long-run energy savings and lower maintenance costs will offset this problem. Therefore, developing cost-effective electronic ballasts with high performance by using advanced high-frequency electronic ballasting techniques is the main purpose of this dissertation.

1.2 Review of Previous Research

Many efforts have been made previously to develop cost-effective electronic ballasts. Small local silicon-controlled-rectifier (SCR) inverters for each lamp, as well as large ones or even high-frequency rotating AC generators for the large banks of lamps in factories or large office buildings, were considered. But with the rapid drop in transistor and ferrite core prices, DC/AC inverters rectified from the utility line became dominant. Therefore, major DC/AC inverters suitable for electronic ballast application are first analyzed. Then, the PFC techniques and dimming control techniques are reviewed.

1.2.1 Major Electronic Ballast Topologies (DC/AC Inverter Stage)

Electronic ballasts are expected to perform the following functions: supply proper starting and operating voltage for the lamp; maintain a running current at the designed value with a low CF; regulate the lamp current output against supply voltage variations; and have a high overall efficiency. To obtain extra energy savings and/or make intelligent lighting, the controllable light output or dimming feature is expected. In addition, low cost and high reliability are very important considerations.

From a historical perspective, electronic ballasts originated from the solid-state radio frequency (RF) power amplifiers (PAs). RF PAs are usually identified by their classes of operation, that is, Classes A, B, C, D, E, F, G, H and S [F9]. Based on how the transistor is biased and driven, all these classes of PAs are placed in the following three categories:

linear-mode PAs, switching-mode PAs and mixed-mode PAs [F10]. In the linear-mode PAs, the power transistors act as a high-resistance current source to produce a magnified replica of the input signal voltage or current wave. Because of the high voltage and current product (power dissipated) inherent in power transistors, this category of PAs usually has low efficiency. In switching-mode PAs, the power transistors operate as a switch, alternately open-circuited and short-circuited. Ideally, a switch has either zero voltage across it or zero current through it at all times (i.e., zero resistance when on, infinite resistance when off, no associated parasitic capacitance or inductance, and zero transition times). Therefore, this category of PAs can theoretically achieve efficiencies of 100%. In mixed-mode PAs, the power transistors basically act as a current source, but partially also as a low-resistance "on" switch. Compared with linear-mode PAs, this category of PAs can improve efficiency due to operating the power switch into saturation. Obviously, the biggest achievements of switching-mode PAs are their high efficiency, low power dissipation, high reliability, small size and low cost.

Classes D, E and S usually comprise switching-mode PAs in RF engineering. Essentially, Class S PAs are wideband PWM DC/DC converters with low-pass filters to allow only a slowly varying DC or average voltage component to appear on the load. The desired output signal is obtained by controlling the pulse width of the input signal, and for this reason, it requires PWM control. In power electronics, Class S PAs are appropriated for applications in variable-speed AC motor drives and uninterruptible power supplies (UPSs), which use batteries to provide standby AC power. Classes D and E PAs, on the contrary, are essentially resonant power converters with high-frequency AC output voltage and current. This is most favored in electronic ballast applications in which a sinusoidal current source is needed. Actually, Class D and Class E electronic ballasts represent two major categories in today's electronic ballast market.

Class D PAs were invented in 1959 by Baxandall [F11], and have been widely used in various applications. However, the basic idea was probably first presented in 1932 by F. N. Tompkns [F12] and later by G. H. Royer, et al. in 1954 [F13]. The original Royer oscillator is a self-oscillating push-pull inverter generating a square wave voltage, in which the timing was based on the saturation of the power transformer, resulting in relatively high core losses and high switching spikes. The Jensen oscillator, as a modified

Royer oscillator, eliminated these disadvantages by separating the timing and power processing functions by a small additional rectangular B-H loop transformer that served as the base drive transformer [F14]. Class D PAs, however, employ a pair of active switches and a tuned network. The switches are driven to act as a two-pole switch that defines either a rectangular voltage or rectangular current waveforms. The output network is tuned to the switching frequency and removes its harmonics, resulting in a sinusoidal output. This characteristic of Class D PAs easily finds its application in electronic ballasts. With its sinusoidal current drive, the lamp efficacy is highest and the EMI is smallest. Additionally, the tuned network also functions as an impedance match to the lamp. The tuned network is probably the most cost-effective way to generate AC current as well as allowing impedance matching. Figure 1-9 shows the four most commonly used Class D topologies for electronic ballasts. These are voltage-fed and current-fed variations of the push-pull topology for the 120V AC-line input and the half-bridge topology for the 220V AC-line input.

Class D current-fed push-pull (Class D CFPP) electronic ballasts (Figure 1-9(a)) were first discussed by R. J. Haver in 1976 [A7], and recently became an interesting research topic in the areas of cold cathode fluorescent lamp (CCFL) ballasts and automotive HID ballasts [A8-A12]. The Haver version did not use an isolation transformer to drive the lamps, but rather a center-tapped choke connected directly from collector to collector with the lamps across the choke. Since the peak voltage of the resonant tank is constant (πV_B), determined by the volt-second balance of the inductor L_1, in some cases this tank voltage may not be sufficient to ignite the lamp, and a step-up transformer is needed. The transformer is usually center-tapped with magnetizing inductance as the parallel-resonant inductance. A resonant capacitor is in parallel to the primary winding. The turns ratio is set to the specified nominal lamp-striking voltage. A lossless series impedance (such as a coupling capacitor) adjusts the lamp RMS operating current to its specified value. The circuit can be decoupled into two parts (Figures 1-10(a) and 1-10(b)). Due to the tuned network, the output of the inductor L_1 is a rectified sine wave voltage with a peak value of V_p. In steady state, the volt-second product across the inductor must be zero, which leads to $V_p = \pi V_B/2$. Therefore, the switches are subjected to a peak voltage of πV_B.

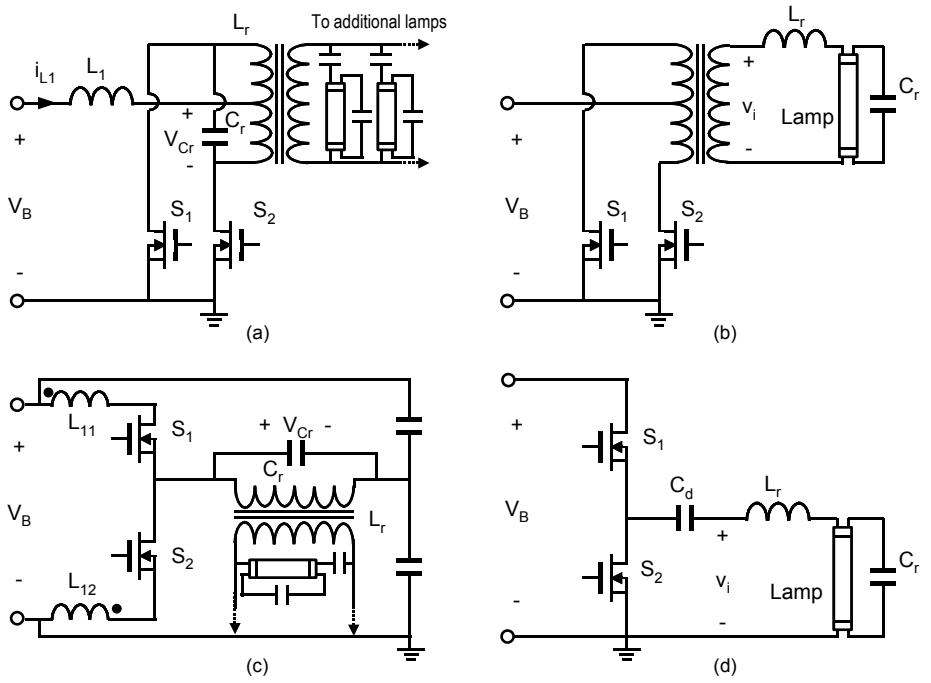


Figure 1-9. Commonly used topologies for electronic ballasts (DC/AC inverter stage): (a) current-fed push-pull parallel resonant ballast; (b) voltage-fed push-pull series-resonant parallel-loaded ballast; (c) current-fed half-bridge parallel resonant ballast; and (d) voltage-fed half-bridge series-resonant parallel-loaded ballast.

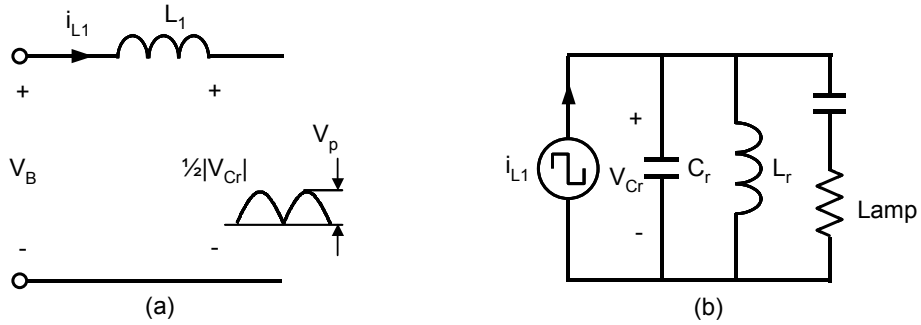


Figure 1-10. Equivalent circuit of current-fed push-pull parallel resonant ballast: (a) input stage, and (b) resonant stage.

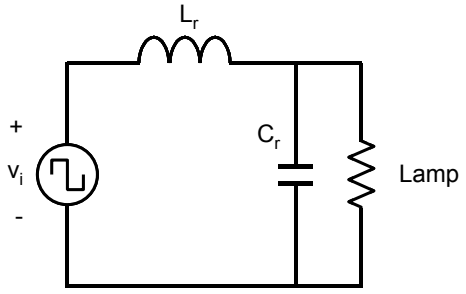


Figure 1-11. Resonant stage of voltage-fed ballasts.

In the Class D voltage-fed push-pull (VFPP) electronic ballasts (Figure 1-9(b)), a square-wave voltage is fed into a series-resonant or series-resonant-derived network, thereby producing sinusoidal resonant current, as opposed to the CFPP electronic ballasts in which a square-wave current is fed into a parallel-resonant or parallel-resonant-derived network, thereby producing sinusoidal resonant voltage such that the voltage and current waveforms are interchanged. Figure 1-11 shows the resonant stage. The voltage stress of the switches is $2V_B$ rather than πV_B.

Class D current-fed half-bridge (CFHB) and voltage-fed half-bridge (VFHB) electronic ballasts are shown in Figures 1-9(c) and (d), respectively. Although the circuit topologies are different, the circuit operations are essentially the same as those of their push-pull counterparts.

Class E PAs are also good candidates for ballasting gas discharge lamps. Since the invention of the Class E PAs by N. O. Sokal and A. D. Sokal in 1975 [F15], they have been a very interesting research topic. In the field of power electronics, the first reported DC/DC converter based on the principle of the Class E PA was proposed by R. J. Gutmann in 1980, in which a 5W, 25V-to-5V DC/DC converter operating at 10 MHz was experimentally demonstrated to have an efficiency of 68% [F16]. R. Redl, et al. proposed a more theoretical analysis and design guideline for Class E DC/DC converters [F17]. The first Class E electronic ballast was proposed by G. Lutteke and H. C. Raets in 1984; in it a high-voltage-rating device BIMOS was used to operate the circuit at 450 kHz and 15W for 120V mains, and later for 220V mains [A14, A15]. Since then, many interesting papers about Class E electronic ballasts have been published. Class E portable ballast systems with high overall efficiency were presented with dimming function [C3, C4]. Other proposed Class E electronic ballasts were integrated with a PFC circuit [B22, B23]. A simple, cost-effective modified Class E electronic ballast was also reported for CCFL applications [A16]. The first Class E electronic ballast to operate well into the MHz region with a self-oscillating mode to drive an electrodeless lamp has also been proposed [E1]. An exact analysis, valid at any duty ratio or circuit Q, with optimization procedures for Class E electronic ballasts has also been reported [E2].

There also exists a family of non-resonant electronic ballasts based on PWM techniques. A flyback converter has been proposed to supply the fluorescent lamps with DC lamp current [A17]. By eliminating the output diode, a bi-directional lamp current is obtained [A18]. Boost-type converters with unidirectional or bi-directional lamp currents were also presented [A19]. The buck-type version was also discussed [A20], in which a voltage-doubler rectifier must be used to facilitate lamp ignition. A family of non-resonant electronic ballasts with tapped inductors was introduced as well [A21].

One of the salient advantages of the PWM-based non-resonant electronic ballasts is their simplicity and low cost. However, the volt-second balance required by the inductor is usually achieved by the lamp voltage, which will incur a high lamp current spike when the switch turns off. This high lamp current spike and/or DC current operation limits their applications to emergency and portable light systems.

In contrast, Class D CFPP electronic ballasts have the best performances. Due to the parallel resonant configuration with current feed, they can operate indefinitely under virtually any load condition, including short, open, and the most severe situation in which a lamp is socketed into a powered fixture. Another important advantage is that they can achieve parallel lamp operation simply by adding a single ballast capacitor per additional lamp, and part of the lamps' replacements might occur while the rest of the lamps are in normal operation. But the downside is that they have the largest component count. The required large inductor and step-up transformer make the circuit bulky and lossy. High voltage stress on the two switches also makes them less attractive, especially when operated after a PFC pre-regulator. The Class D VFHB electronic ballasts, on the contrary, are simple circuits requiring few components. When they operate at the undamped natural frequency, they show current source characteristics such that no step-up transformer is necessary. If isolation is needed, a smaller transformer can be used because the secondary winding voltage is equal to the lamp voltage, unlike the Class D CFPP electronic ballasts in which a separate ballast impedance is necessary to absorb the voltage difference between the winding voltage (striking voltage) and the lamp's normal operating voltage. Another attractive feature is that the voltage stress of the two switches is equal to the bus voltage, which allows low-voltage-rating MOSFETs to be used.

Compared with Class D electronic ballasts, Class Es have several advantages: They are single-ended circuits, which simplifies the drive circuit; the current and voltage waveforms of the switch are displaced with respect to time, such that the voltage does not rise before the current has fallen to zero and the voltage falls to zero again with zero slope before the current begins to rise, resulting in virtually zero switching; the parasitic reactive elements such as transistor output capacitance, inductance capacitance and leakage inductance of the transformer in the isolation version are absorbed in the circuit operation; and input current is usually continuous, which reduces EMI to the source. Because of its extremely low switching losses, the circuit is well suited to high-frequency applications, in which the size of the magnetic components can be reduced significantly. However, all of these advantages are achieved at the penalty of severe voltage and current demands on the devices because of the sinusoidal-like voltage and current waveforms for the switches as well as the passive components [A15]. Currently, they mainly find their applications in compact fluorescent lamps in which they are inserted into conventional incandescent lamp fittings, making critical the size of the ballast.

Considering all of these preceding factors, the Class D VFHB electronic ballasts are chosen in this dissertation.

1.2.2 PFC Techniques in Electronic Ballasts

There are generally two methods for correcting the PF and suppressing harmonic distortion: the passive PFC approach and the active PFC approach. Passive PFC refers to using only line-frequency reactive components plus uncontrolled rectifiers, while the active PFC uses active devices and high-frequency reactive components as well as passive switches such as diodes. The advantages of the passive PFC approach are its simplicity, reliability, robustness, lack of EMI generated, and low cost. Although the input current of the passive approach is not expected to achieve a perfect sinusoidal waveform, in low-wattage applications the circuit can be designed to meet the IEC 1000-3-2 Class C specifications [B1-B3]. However, the physical size and weight of the line-frequency components renders the passive approach very unattractive. The active

approach, on the other hand, not only easily meets the specifications, but also significantly reduces the circuit size and weight. The major issues are circuit complexity, reliability and cost.

In literature, the single-phase active PFC circuits are classified into two categories: the two-stage approach and the single-stage approach. The two-stage approach represents the conventional practice, in which a current-shaping stage (PFC stage) cascades with the DC/AC stage. Good PF and circuit performance can be accomplished simultaneously since the PFC stage is dedicated to achieving high PF and regulating the DC-link output voltage. The PFC stage could be a buck, boost or buck-boost converter. The buck topology is seldom used except for some particular applications due to its step-down characteristic, which incurs a dead angle of the input current when the line voltage falls below the output voltage [B4]. The buck-boost topology can properly shape the input current. However, the high voltage/current stresses and the pulsating input and output currents limit its applications. The boost converter is more suitable for the PFC for the following reasons. The boost inductor is in series with the input line, which gives a lower current ripple, and the power switch is in shunt with the power-flow path with which the converter operates efficiently. However, there is a limitation: The output voltage must be higher than the line peak voltage. This may not be a problem for the single-phase universal line where a cost-effective 450V bus capacitor can be used.

In terms of overall efficiency and EMI filter size, continuous-conduction mode (CCM) is preferred for the boost converter operating as an active PFC stage. However, it needs a complicated control circuit [B5]. Moreover, there exist severe problems caused by the effect of the reverse-recovery characteristic of the boost diode. Some approach, such as the use of a passive or active snubber, must deal with this adverse effect, further complicating the circuit and increasing the cost [B6]. One practical solution is to operate the circuit into the boundary between the continuous- and discontinuous-conduction modes, which lessens the reverse-recovery problems and control complexity. However, a wide range of variable switching frequency controls must be used, causing problems for circuit implementation and design optimization. Discontinuous-conduction-mode (DCM) operation may be a good trade-off for low-power applications. The circuit is simple, with a PFC switch operating at constant duty ratio and constant frequency without sensing

input voltage or current. But the high inductor ripple current not only requires a large EMI filter, it also causes current stress on the devices. Nevertheless, the two-stage approach shows good performances. It represents a mature PFC technique, but is a rather costly and ineffective solution when used in low-power applications for which cost is a sensitive issue.

Great efforts have been made to reduce the component count and circuit cost. The majority of these efforts have focused on incorporating the PFC stage and DC/AC stage into one by allowing them to share the active switches so that neither PFC switch nor controller is needed. This technique is called single-stage PFC approach.

Lots of single-stage PFC circuits were proposed and analyzed in literature. The most original ones are probably as follows: the dither rectifiers proposed by I. Takahashi [B7], the charge-pump power-factor-correction (CPPFC) circuits by W. L. Eaton [B8], the modified valley fill circuit by J. J. Spangler [B9], the dual output PFC circuits by Kheraluwala [B10], the boost integrated with flyback rectifier/energy storage/DC-DC converter (BIFRED) and the boost integrated with a buck rectifier/energy storage/DC-DC converter (BIBRED) by M. Madigan [B11], the voltage-source PFC circuit by S. Teramoto [B12], the P-PFC circuits by Y. Jiang [B13], the single-stage isolated power-factor-correction power supply (SSIPP) by R. Redl [B14], the magnetic switch (MS) PFC circuits by O. R. Schmidt [B15], the voltage-doubler rectifiers by J. Zhang, et al. [B16], the bus voltage feedback circuits by F. Tsai, et al. [B17], and J. Qian, et al [B18], the effective boost duty ratio by L. Huber, et al. [B19], the current-source PFC circuits by G. Hua [B20], and the two-terminal ICS cells and three-terminal ICS cells by J. Zhang, et al. [B17]. Based on these original single-stage PFC techniques, numerous modified circuits were discussed in articles and patents.

The development path of PFC techniques in electronic ballasts is almost the same as that in AC/DC converters. However, there are some special issues in electronic ballast applications. First, electronic ballasts should meet the IEC 1000-3-2 Class C regulations, which are the most stringent harmonic requirements in all classes. Second, as required by the building code, the PF should be higher than 0.9. These two requirements together stipulate almost sinusoidal input current waveform with THD less than 32%. Third, the

power level of electronic ballasts is usually under 100 W, precluding any complicated PFC method. Furthermore, as a mass product, the electronic ballasts should be small, simple, reliable and cheap. Therefore, boost-derived and charge-pump-derived single-stage PFC techniques are the focus of this dissertation.

The conventional single-stage DCM boost PFC electronic ballast is shown in Figure 1-12, in which switch S_2 is shared between the PFC stage and the DC/AC stage [B24]. Since the peak value of the boost inductor current naturally follows the sinusoidal line voltage, the average input current also follows the line voltage when the duty ratio is constant over a half line cycle. PFC is achieved without an additional switch or control.

The operation of the DCM boost converter as PFC rectifier is quite straightforward. For the convenience of discussion, α factor is introduced as

$$\alpha \equiv V_p / V_B \,, \tag{1.4}$$

where V_p and V_B are the line peak voltage and bus voltage, respectively.

The line current, real input power, PF and THD are given by previous work [B25], as follows:

$$i_{in} = \frac{D^2 \pi V_p}{\omega_s L_b} \cdot \frac{1}{1 - \alpha \left|\sin(\omega_l t)\right|} \cdot \sin(\omega_l t) \,, \tag{1.5}$$

$$P_{in} = \frac{D^2 \pi V_p^2}{\omega_s L_b} y \,, \tag{1.6}$$

$$PF = \frac{\sqrt{2} y}{\sqrt{z}} \,, \text{ and} \tag{1.7}$$

$$THD = \frac{\sqrt{2z}}{2y} \cdot \sqrt{1 - \frac{2y^2}{z}} \,, \tag{1.8}$$

where $$y = -\frac{2}{\pi\alpha} - \frac{1}{\alpha^2} + \frac{2}{\alpha^2 \sqrt{1-\alpha^2}} \left[\frac{1}{2} - \frac{1}{\pi} \tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}} \right) \right], \text{ and} \tag{1.9}$$

$$z = \frac{2}{\pi\alpha(1-\alpha^2)} + \frac{1}{\alpha^2} + \frac{2\alpha^2 - 1}{\alpha^2(1-\alpha^2)} \cdot \frac{2}{\sqrt{1-\alpha^2}} \cdot \left[\frac{1}{2} - \frac{1}{\pi} \tan^{-1}\left(\frac{-\alpha}{\sqrt{1-\alpha^2}} \right) \right]. \tag{1.10}$$

The PF and THD are plotted in Figure 1-13 as a function of the α factor. It can be seen that the PF and THD deteriorate as the α factor increases. The α factor should not exceed 0.8 in order to meet the PF and THD requirements. It should be noted that the boost converter is operated in DCM. The DCM condition is given by

$$\alpha \le 1 - D . \tag{1.11}$$

Although the circuit in Figure 1-12 has potential low cost, there exist several problems. First, according to (1.11) the α factor cannot exceed 0.5 since the duty ratio of the PFC stage is determined by the DC/AC inverter stage in which D =0.5. Therefore, the bus voltage should be higher than twice the line peak voltage, which calls for high-voltage-rating devices. Second, DCM operation induces a pulsing line current so that a large input EMI filter is required. Third, switch S_2 needs to tackle the current from the PFC stage and the DC/AC inverter stage so that a higher-current-rating device is necessary. Moreover, high bus voltage stress at light load is inherent and dimming control is not easy to implement.

To solve the first problem imposed by the requirement of high boost conversion ratio, a variable duty-ratio control strategy could be used [B26, B27]. From (1.5), if the duty ratio is controlled according to (1.12), a unity PF is obtained even if the bus voltage is close to the line peak voltage. However, lamp CF is increased and ZVS operation is easily lost.

$$d(t) = k\sqrt{1 - \alpha\left|\sin \omega_l t\right|} , \tag{1.12}$$

where k is a constant which equals the duty ratio at the line zero-crossing.

Another approach is to increase the resetting voltage by using a "magnetic switch," as shown in Figure 1-14 [B29]. By adjusting the turns ratio of the transformer, good PF is achieved as long as the bus voltage is larger than the line peak voltage. However, another magnetic component and four fast-recovery diodes are added, which complicates the circuit and increases cost. Finding a simple approach is one of the goals of this dissertation.

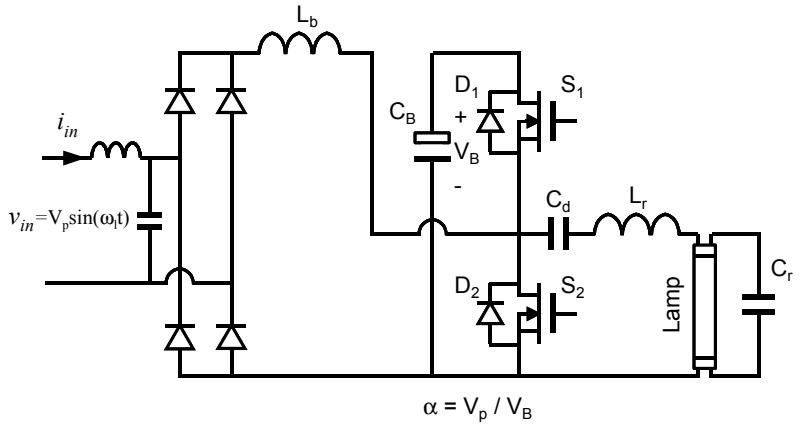


Figure 1-12. Single-stage PFC electronic ballast [B24].

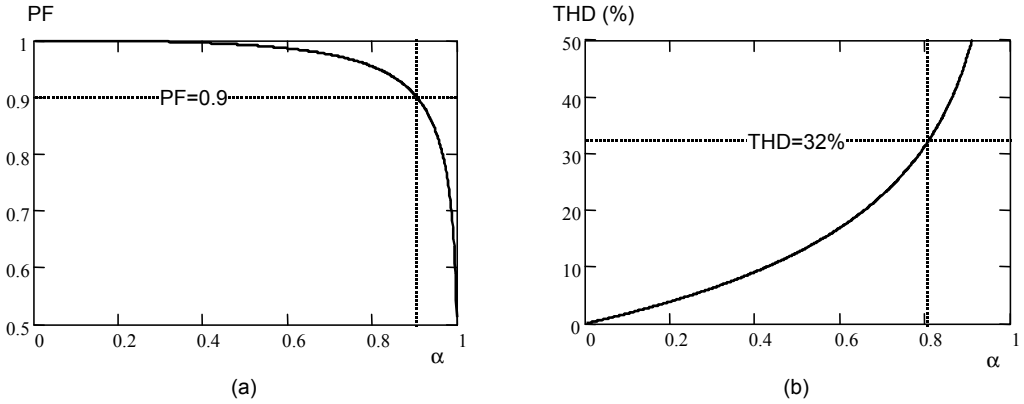


Figure 1-13. (a) PF and (b) THD as a function of the α factor.

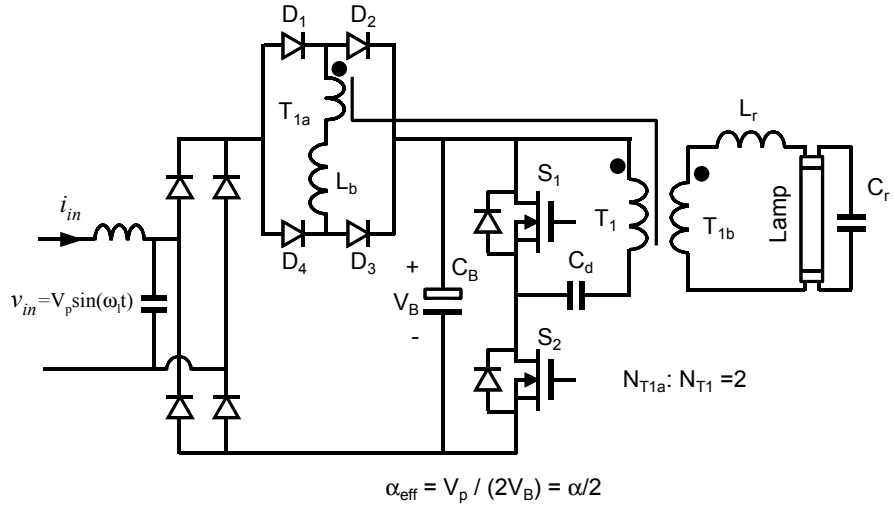


Figure 1-14. Single-stage DCM boost PFC electronic ballast with "magnetic switch" [B29].

Another family of electronic ballasts uses the so-called CPPFC technique to achieve PFC. It has become attractive since the use of a bulky DCM boost inductor is not necessary in these circuits [D1-D21]. The CPPFC circuits employ the capacitor to integrate the PFC stage with the DC/AC inverter stage, by which an inherent PFC is achieved. Figure 1-15 shows the basic CPPFC electronic ballast, in which the resonant inverter is integrated with the PFC stage via C_{in}. Therefore, this family of circuits has potential low cost compared with the boost-derived PFC circuits. The issue is how to evaluate these electronic ballasts since the PFC stage and inverter stage are interrelated. Another issue is how to apply the self-oscillating technique to further reduce the cost.

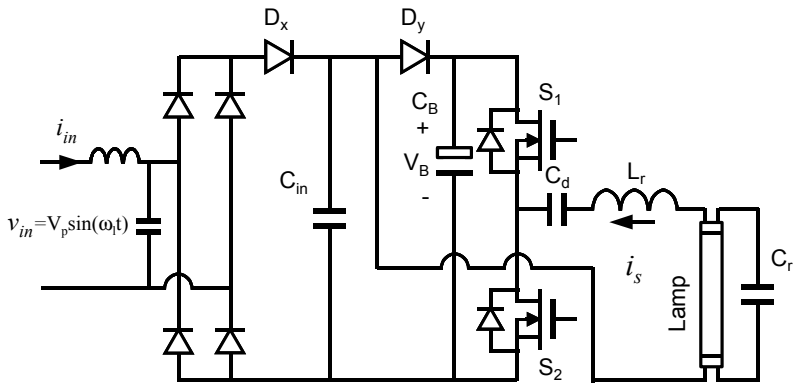


Figure 1-15. Basic CPPFC electronic ballast [D2].

1.2.3. Dimming Control

Most of today's dimming control methods can be placed into four categories: variable switching frequency control, variable duty-ratio control, variable bus voltage control, and their combinations. Accordingly, the power stages may be different for viable operation.

The variable switching frequency control has been popularly adopted in practical implementation because of its simplicity [C5-C12]. When the switching frequency is located further away from the resonance of the tank, less energy is coupled to the lamps, and the lamps dim. The analytical-based analyses for non-PFC electronic ballasts are

given in other work [C5, C7]. An inherent unstable region exists due to the interaction between the negative impedance of the lamps and the output characteristics of the electronic ballast with frequency control [C5]. This analytical result has been verified by experimental tests [C6, C7]. The dimming electronic ballasts with frequency control provide only a limited dimming range, typically 3:1. If one attempts to extend the dimming range, the lamps fail to stay on reliably. They either begin to flicker, or they turn off and remain off.

The stable dimming range could be extended by using DC-link voltage control [C6, C13, C14]. By selecting a switching frequency close to the undamped natural frequency, the electronic ballasts behave as a current source controlled by the bus voltage [A22]. Flicker-free operation can be maintained when the lamp power is reduced to a small value. However, the lamps tend to show striation as the lamp power drops to a certain level. A simplified equation explains this phenomenon [C10]. Without employing a special strategy to reduce the striation, the dimming range typically is about 10:1 [C6].

In practice the DC-link voltage control is only used with a variable bus voltage source such as a PFC pre-regulator. Duty-ratio control can achieve a level of performance similar to that of DC-link voltage control, but with a simple structure. Actually, with the asymmetrical duty-ratio control, a small DC-biased lamp current is formed naturally, which helps to prevent the development of striations [C10, C21-C23]. However, special care must be taken when using the duty-ratio control in a half-bridge inverter, since the switch with the small duty ratio could change its operation from ZVS to ZCS commutation during the dimming control [C15].

Good performance could be achieved in combined control methods. A variable duty-ratio and frequency control in a single-stage PFC electronic dimming ballast with a 3:1 dimming range was reported [C9]. A variable bus voltage and switching frequency control for multiple fluorescent lamps applications in two-stage PFC electronic dimming ballast with a dimming range of 3:1 has also been introduced [C17]. The strategy combining duty-ratio control and switching frequency control with non-linear compensation has been employed [C10]. The reported dimming range is 100:1. However, the control scheme used is very complicated.

1.3. Motivations and Objectives

The preceding discussion of the current electronic ballasting techniques demonstrated the need for further research in this area. Specifically, four areas need to be addressed.

1) The most commonly used PFC topology in low-power applications is the DCM boost converter due to the inherent PFC function. However, when applied in the half-bridge electronic ballast applications, the bus voltage is required to be higher than two times the line peak voltage to ensure DCM operation, which requires designer to resort to impractical high-voltage-rating devices. An important research objective is to develop new single-stage PFC electronic ballasts that only require low boost conversion ratios.

2) Dimming control plays an increasingly important role in modern lighting systems. The marketplace has requested that the light output level be adjustable by a factor of 100. Also the dimmable electronic ballast should meet the IEC 1000-3-2 harmonic requirement. Therefore, it would be important to develop cost-effective single-stage PFC electronic ballasts with continuous wide-range dimming control.

3) The CPPFC techniques eliminate the use of the bulky DCM boost inductor by employing charge-pump capacitors; this approach shows good potential in electronic ballast applications. A family of CPPFC electronic ballasts has been previously proposed. However, because the charge-pump capacitors and the resonant inverter are highly interrelated, the circuit performance is usually hard to analyze. It is very important to understand and compare different CPPFC techniques.

4) The performance and overall cost of electronic ballasts are greatly affected by the control circuits. Self-oscillating operation can reduce the complexity and cost of the control circuit. To achieve good circuit performance, it is necessary to include the control aspect into the self-oscillating circuit. It would be important to understand and develop controllable self-oscillating techniques.

The overall objective of this dissertation is to develop advanced high-frequency electronic ballasting techniques that incorporate these four objectives.

1.4 Dissertation Outline

Chapter 1 introduces the research background and literature reviews. Then it provides the research objectives and outline.

Chapters 2 and 3 cover the single-stage boost-derived PFC techniques. First in Chapter 2, a novel voltage-divider concept is proposed to deal with the high boost conversion ratio problem of the boost-derived DCM PFC circuit. Based on the proposed concept, two new circuits, critical-conduction-mode electronic ballasts and interleaved electronic ballasts, are proposed and analyzed. The proposed circuits are then compared. The circuit analysis and comparison are verified by the experimental results.

Chapter 3 deals with the issues regarding single-stage boost-derived PFC electronic ballasts with wide-range dimming control. First, the problems of the existing single-stage PFC dimmable electronic ballasts are studied. Then, a family of single-stage PFC electronic ballasts with asymmetrical duty-ratio control is proposed, analyzed and implemented. Experimental results show that with the proposed circuits, high PF and low THD, low lamp CF, low bus voltage stress and wide-range dimming control are achieved.

Chapter 4 studies the issues of the single-stage CPPFC electronic ballasts. A family of CPPFC electronic ballast is reviewed and studied. Based on the study, the lamp voltage feedback concept is proposed to suppress the bus voltage stress during light-load operation. Circuit analysis is verified by experimental results.

Chapter 5 deals with the self-oscillating technique for CPPFC electronic ballasts. The winding voltage modulation and current injection concepts are proposed to achieve switching frequency modulation. The proposed concepts are verified by the experimental results.

Chapter 6 summarizes the major results of the work and offers suggestions for future work.

Chapter 2 Boost-Derived Single-Stage Power-Factor-Correction Electronic Ballasts

2.1 Introduction

The DCM boost-derived PFC converter is one of the most commonly used PFC topologies in low-power applications. However, as discussed in Chapter 1, the conventional DCM boost PFC electronic ballast has the problem of small α factor that is required to meet the DCM condition. This chapter proposes the voltage-divider concept to halve the effective α factor so that the DCM condition is automatically satisfied and PF is improved. In addition, the ripple frequency of the input current doubles and the ripple magnitude is reduced so that a smaller EMI filter can be used. Two circuit implementations are proposed, analyzed, compared and verified by the experimental results.

2.2 Voltage-Divider Concept in PFC Electronic Ballasts

Figure 2-1(a) shows the conventional single-stage DCM boost PFC electronic ballast, in which switch S_2 is shared between the PFC stage and the inverter stage. Usually the circuit is operated in constant frequency, constant duty ratio. Therefore, the PFC stage has to be operated in DCM in order to achieve good PF. However, since the duty ratio of the PFC stage is determined by the inverter stage, which usually equals 0.5, the α factor should be less than 0.5 to meet the DCM condition of (1.11). The bus voltage exceeds two times the line peak voltage, which may severely penalize the power stage design and call for a special high-voltage-rating bulk capacitor. To solve this problem, previous work has attempted to reduce the α factor by increasing the resetting voltage of the boost inductor, as shown in Figure 2-1(b), in which the resetting voltage equals the bus voltage

plus the winding voltage V_{T1a}. The effective α factor halves when the turns ratio equals 2. However, this is a rather costly solution since another magnetic component and four fast diodes are added. To simplify the circuit, the approach proposed here is to halve the input voltage using a voltage-divider branch so that the effective α factor is also halved. Figure 2-1(c) shows the conceptual circuit diagram, in which two small DC capacitors form the voltage-divider branch. It can be seen that the two-level rectified line voltage is converted into three-level voltage, which allows simpler and more efficient implementation of the single-stage PFC electronic ballast.

2.3 Voltage-Divider PFC Circuit Implementations

2.3.1 Single-Stage Critical-Conduction-Mode PFC Electronic Ballast

The circuit derivation is shown in Figure 2-2. First the boost inductor is placed in the center leg, as in the conventional DCM boost PFC electronic ballast. Then two fast diodes are placed in the outer legs to form a full-bridge rectifier together with two body diodes of the MOSFETs. Finally the voltage-divider branch is added. As can be seen later, the proposed circuit operates in critical-conduction mode and has almost the same performance as the circuit of Figure 2-1(b), but with simpler configuration. The complete circuit diagram is shown in Figure 2-3.

To establish the circuit operation, some assumptions are made, as follows.

1) S_1 and S_2 operate at constant frequency: 0.5 duty ratio and 180^0 out of phase.
2) The bus capacitance, C_B, is large enough to be considered a voltage source.
3) The bus voltage, V_B, is always higher than the line peak voltage.
4) The output of the input rectifier is simply the rectified AC voltage. The voltage across the voltage-divider capacitors is simply half of the rectified AC voltage.
5) The lamps are modeled as a resistor, R_{la}, at steady state.

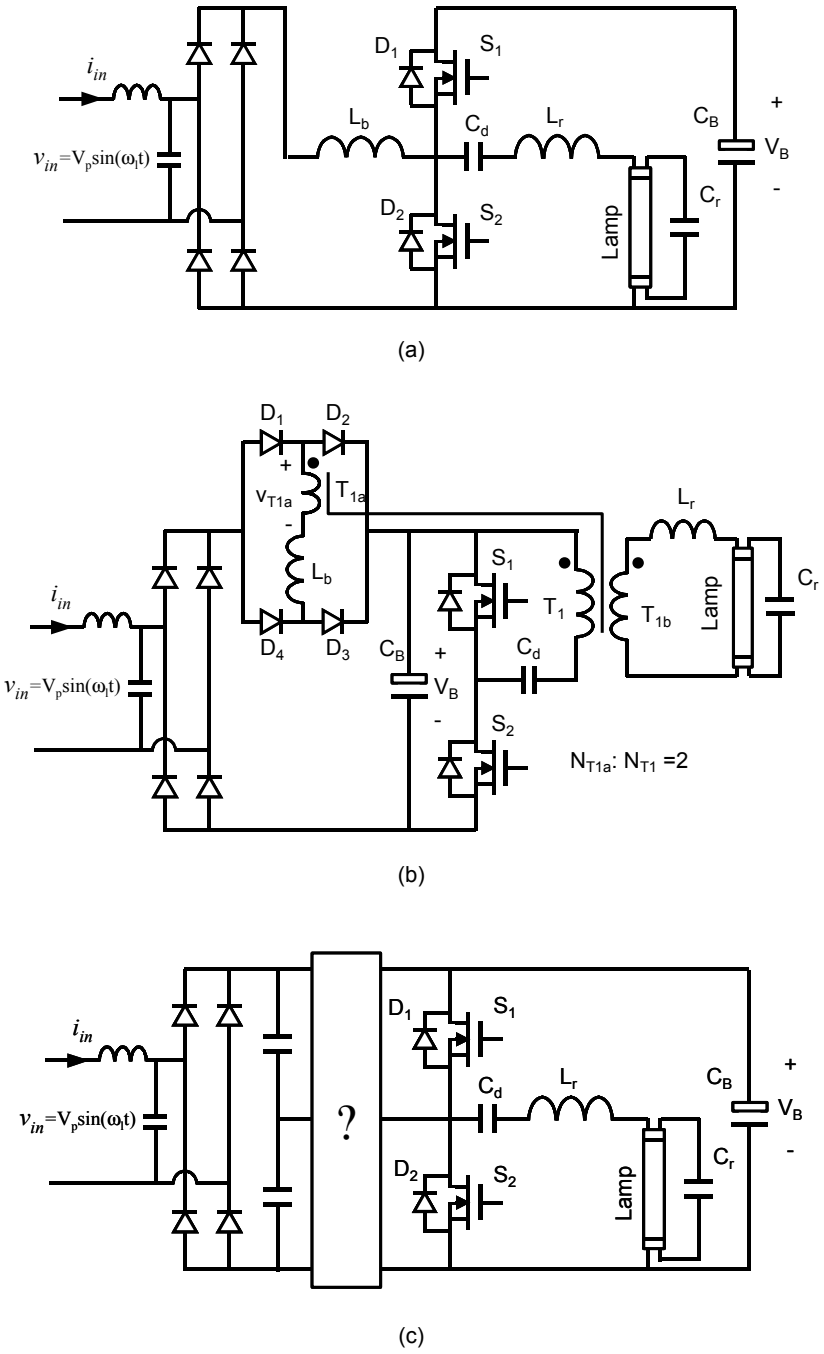


Figure 2-1. (a) Conventional DCM boost PFC electronic ballast [B24] ($\alpha = V_p / V_B$). (b) Boost PFC electronic ballast operating in critical conduction mode [B29] ($\alpha_{eff} = V_p / (2V_B) = \alpha/2$). (c) Conceptual voltage-divider electronic ballast ($\alpha_{eff} = (V_p/2) / V_B = \alpha/2$).

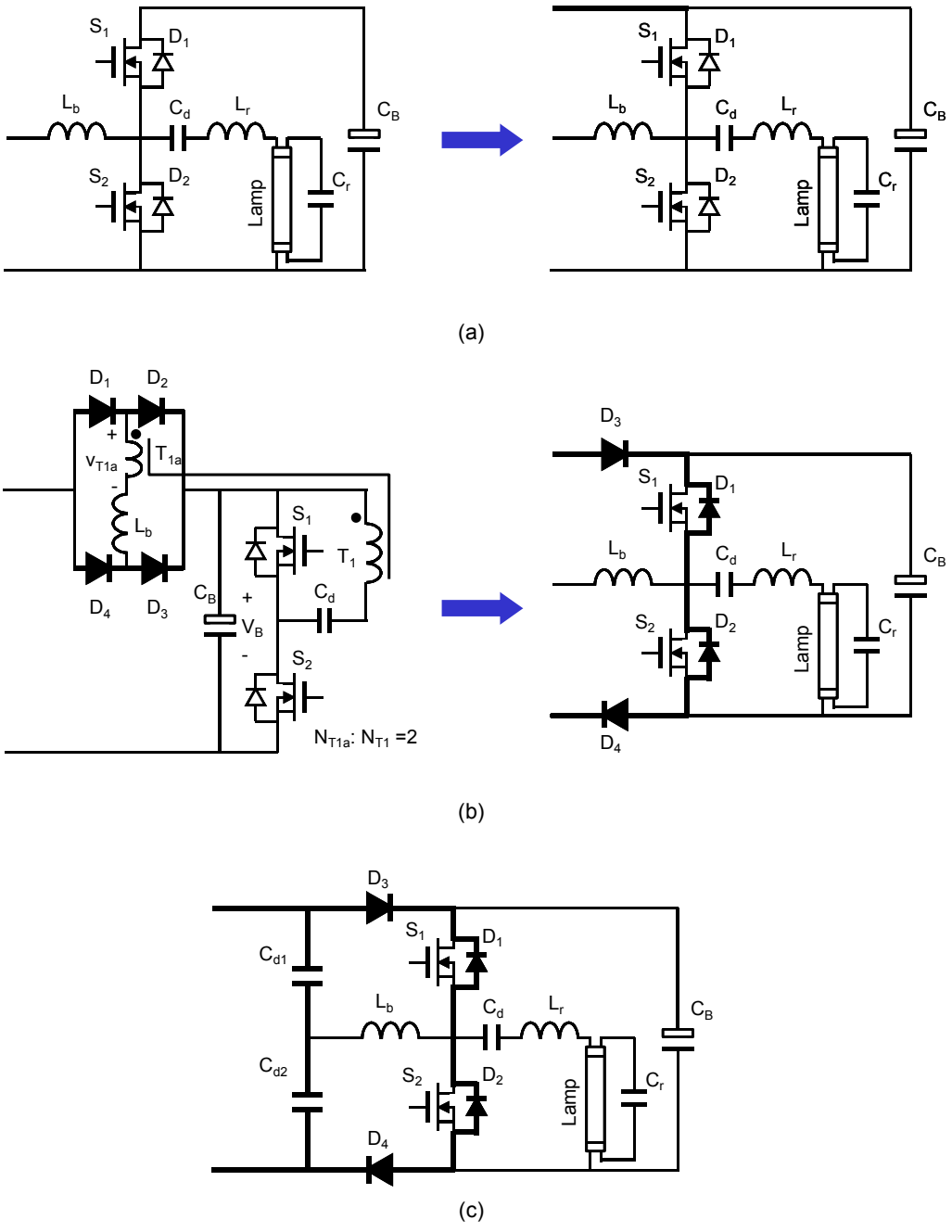


Figure 2-2. Derivation of single-stage critical-conduction-mode PFC electronic ballast: (a) making circuit symmetrical; (b) forming full-bridge rectifier; and (c) adding voltage-divider branch.

In steady state, two conversion stages can be identified for the purpose of analysis: One is a PFC stage, which can be considered as two DCM boost converters operated 180^0 out of phase and sharing one boost inductor (Figure 2-4(a)), and the other is a half-bridge resonant inverter (Figure 2-4(b)). For the PFC stage, there are four topological stages over one switching cycle, as shown in Figure 2-5. Figure 2-6 shows the key waveforms.

Mode 1 [t_0, t_1]: Before t_0, negative boost inductor current i_{Lb} flows through D_1 and D_4. At t_0, i_{Lb} reverses polarity, resulting in turn-off of D_1 and D_4. Since the gate voltage has already been applied to S_1 during the D_1-on period, S_1 is turned on with ZVS. V_{in1} is applied to L_b, and i_{Lb} linearly increases.

Mode 2 [t_1, t_2]: At t_1, S_1 is turned off. The positive i_{Lb} forces the body diode D_2 to turn on. The negative voltage (V_B-V_{in1}) is applied to the inductor, causing i_{Lb} to decrease linearly. This mode ends when i_{Lb} drops to zero at t_2. The gate voltage should be applied to S_2 during this mode.

Mode 3 [t_2, t_3]: At t_2, i_{Lb} reverses polarity, causing turn-off of D_2 and D_3. S_2 is turned on with ZVS. V_{in2} is applied to L_b and i_{Lb} decreases linearly.

Mode 4 [t_3, t_4]: At t_3, S_2 is turned off. Since i_{Lb} is still negative, the body diode of S_1 is forced on. The voltage (V_B- V_{in2}) is applied to L_b, and i_{Lb} increases linearly. This mode ends at t_4 when i_{Lb} becomes zero. A new switching cycle begins.

The analysis shows that the charging voltage is half of the rectified line voltage and the discharging voltage is the bus voltage minus half of the rectified line voltage. Due to the full-bridge rectifier, the boost inductor current never stays at zero. Therefore, the boost inductor is operated in the critical-conduction mode if seen from the line input side. High PF is obtained. For convenience of discussion, an effective α_{eff} factor is defined as

$$\alpha_{eff} \equiv \frac{V_p}{2V_B} = \frac{\alpha}{2}, \tag{2.1}$$

where V_p and V_B are the line peak voltage and bus voltage, respectively.

With the defined α_{eff} factor, the equations of line current, PF, THD and circuit parameters are derived as follows.

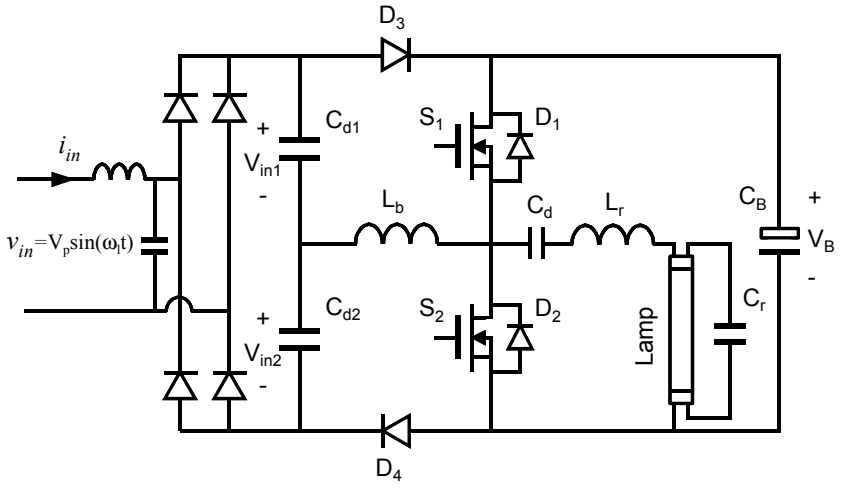


Figure 2-3. Proposed single-stage critical-conduction-mode PFC electronic ballast.

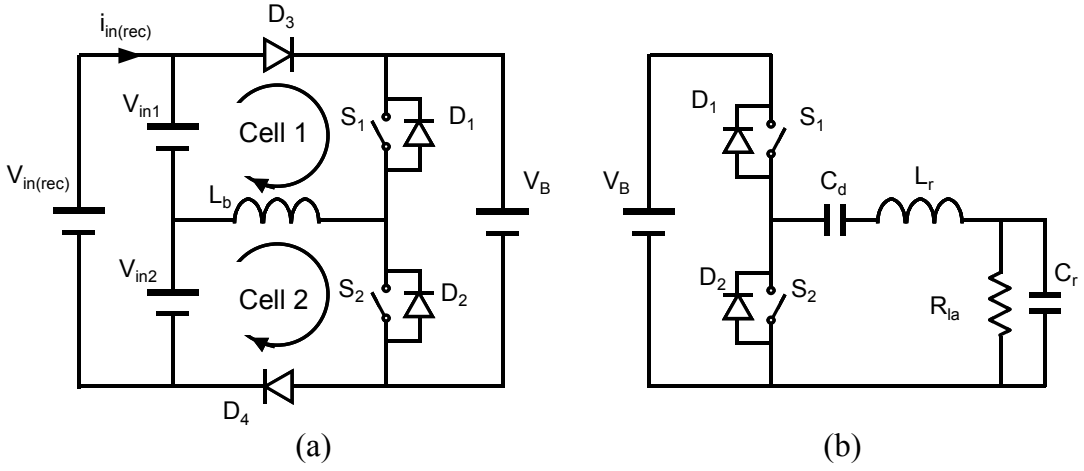


Figure 2-4. Simplified equivalent circuits: (a) PFC stage with two DCM boost cells sharing a common boost inductor, and (b) half-bridge resonant inverter stage.

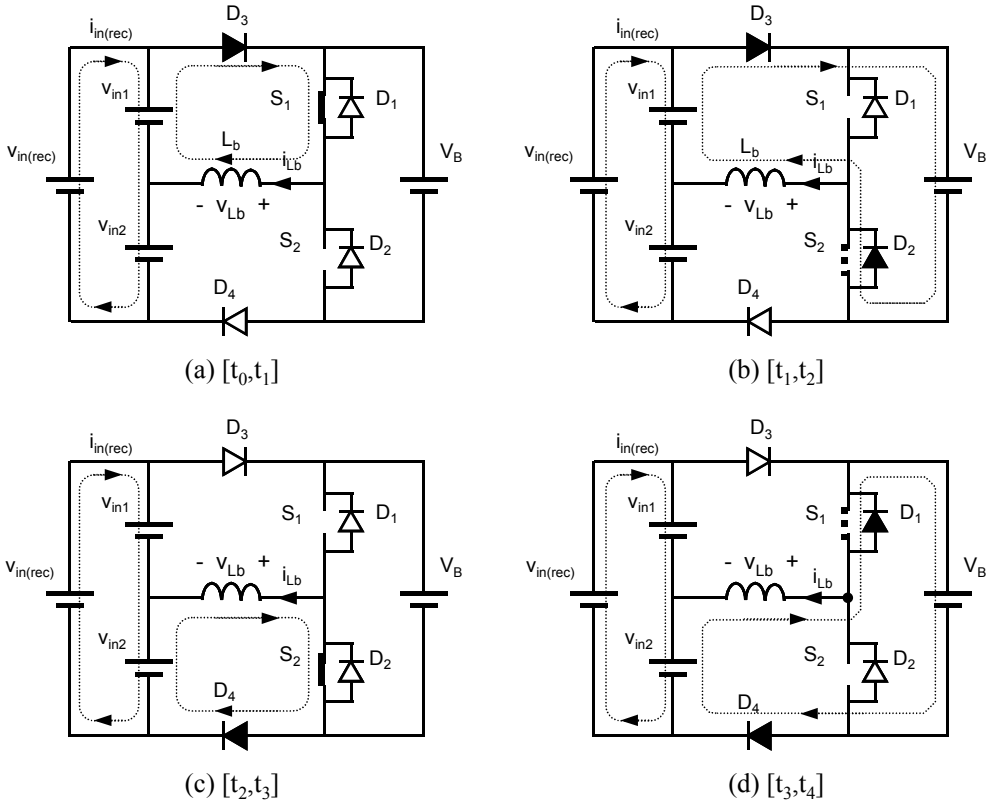


Figure 2-5. Topological stages of the PFC stage.

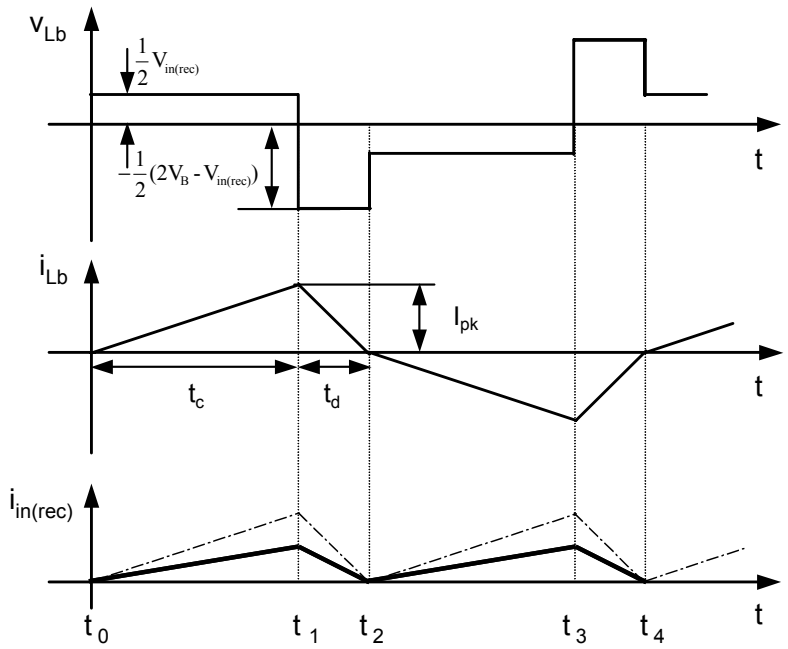


Figure 2-6. Key switching waveforms.

A. Input Current, PF and THD

From Figure 2-6, the peak inductor current I_{pk} is determined by

$$I_{pk} = \frac{V_{in1} t_c}{L_b} = \frac{V_p |\sin \omega_l t| t_c}{2L_b}. \tag{2.2}$$

The discharge time, t_d, is given by

$$t_d = \frac{I_{pk}}{(V_B - V_{in1})/L_b} = \frac{V_p |\sin \omega_l t| t_c}{2V_B - V_p |\sin \omega_l t|} = \frac{\alpha_{eff} |\sin \omega_l t|}{1 - \alpha_{eff} |\sin \omega_l t|} t_c. \tag{2.3}$$

Since $t_c + t_d = \frac{1}{2} T_s$, t_c and t_d can be determined by

$$t_c = \frac{1}{2}(1 - \alpha_{eff} |\sin \omega_l t|) T_s, \text{ and} \tag{2.4}$$

$$t_d = \frac{1}{2} \alpha_{eff} |\sin \omega_l t| T_s, \tag{2.5}$$

where T_s is the switching period.

Substituting (2.4) into (2.2) yields

$$I_{pk} = \frac{V_p T_s}{4L_b}(1 - \alpha_{eff} |\sin \omega_l t|)\sin \omega_l t| = \frac{\pi V_p}{2\omega_s L_b}(1 - \alpha_{eff} |\sin \omega_l t|)\sin \omega_l t|. \tag{2.6}$$

The rectified input current $i_{in(rec)}$ equals half of $|i_{Lb}|$. Therefore, the peak-to-peak ripple current and average current of the rectified line input are determined by

$$i_{ripple}^{pp} = \frac{I_{pk}}{2} = \frac{\pi V_p}{4\omega_s L_b}(1 - \alpha_{eff} |\sin \omega_l t|)\sin \omega_l t|, \text{ and} \tag{2.7}$$

$$i_{in(rec)}^{av} = \frac{I_{pk}}{4} = \frac{\pi V_p}{8\omega_s L_b}(1 - \alpha_{eff} |\sin \omega_l t|)\sin \omega_l t|. \tag{2.8}$$

Due to the high-frequency input filter and rectifier, the instantaneous line current i_{in} is obtained as

$$i_{in} = \frac{\pi V_p}{8\omega_s L_b}(1 - \alpha_{eff} |\sin \omega_l t|)\sin \omega_l t. \tag{2.9}$$

Equation (2.9) shows that the line current will contain a certain amount of distortion due to the non-linear term of $(1-\alpha_{eff}|\sin\omega_l t|)$.

The line RMS current is given by

$$I_{rms}=\sqrt{\frac{1}{\pi}\int_0^{\pi} i_{in}^2 d\theta}=\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{\pi V_p}{8\omega_s L_b}(1-\alpha_{eff}\sin\theta)\sin\theta\right]^2 d\theta}=\frac{\pi V_p}{8\omega_s L_b}\sqrt{z}\,, \tag{2.10}$$

where $z=\frac{1}{\pi}\int_0^{\pi}\left((1-\alpha_{eff}\sin\theta)\sin\theta\right)^2 d\theta=\frac{1}{2}-\frac{8}{3\pi}\alpha_{eff}+\frac{3}{8}\alpha_{eff}^2$. (2.11)

The input real power is given by

$$P_{in}=\frac{1}{\pi}\int_0^{\pi} v_{in} i_{in} d\theta=\frac{1}{\pi}\int_0^{\pi} V_p\sin\theta[\frac{\pi V_p}{8\omega_s L_b}(1-\alpha_{eff}\sin\theta)\sin\theta]d\theta=\frac{\pi V_p^2}{8\omega_s L_b}y\,, \tag{2.12}$$

where $y=\frac{1}{\pi}\int_0^{\pi}\sin^2\theta(1-\alpha_{eff}\sin\theta)d\theta=\frac{1}{2}-\frac{4}{3\pi}\alpha_{eff}$. (2.13)

The PF is defined as the ratio of real power to apparent power, which is given by

$$PF=\frac{P_{in}}{V_{in(rms)}I_{rms}}=\frac{\sqrt{2}y}{\sqrt{z}}. \tag{2.14}$$

If displacement is assumed to be unity, the THD can be obtained by

$$THD=\frac{1}{PF}\sqrt{1-PF^2}=\frac{\sqrt{2z}}{2y}\sqrt{1-\frac{2y^2}{z}}. \tag{2.15}$$

B. RMS MOSFET Current of the PFC Stage

The RMS MOSFET current in the PFC circuit can be approximately calculated using a double integral when the switching frequency is much larger than the AC line frequency [F18]. The square of the MOSFET current is integrated first to find its average over a switching period, and the result is then integrated to find the average over the AC line period. For the proposed PFC stage, the MOSFET current $i_s(t)$ equals the boost

inductor current when the MOSFET conducts, and is zero when it is off. Therefore, the average of $i_s^2(t)$ over one switching period is

$$\left\langle i_s^2 \right\rangle_{Ts} = \frac{1}{T_s}\int_{t}^{t+T_s} i_s^2(t)dt = \frac{t_c}{T_s}\frac{I_{pk}^2}{3} = \frac{I_{pk}^2}{6}\left(1-\alpha_{eff}\left|\sin\omega_l t\right|\right). \tag{2.16}$$

The RMS current $I_{s(rms)}$ is then determined by

$$I_{s(rms)} = \sqrt{\frac{1}{T_l}\int_0^{T_l}\left\langle i_s^2 \right\rangle_{T_s} dt} = \sqrt{\frac{1}{T_l}\int_0^{T_l}\frac{I_{pk}^2}{6}\left(1-\alpha_{eff}\left|\sin\omega_l t\right|\right)dt}\,, \tag{2.17}$$

which can be simplified as

$$I_{s(rms)} = \frac{\sqrt{6}\pi V_p}{12\omega_s L_b}\sqrt{\frac{1}{\pi}\int_0^{\pi}\sin^2\theta\left(1-\alpha_{eff}\sin\theta\right)^3 d\theta} = \frac{\sqrt{6}\pi V_p}{12\omega_s L_b}\sqrt{g}\,, \tag{2.18}$$

where $g = \frac{1}{\pi}\int_0^{\pi}\sin^2\theta\left(1-\alpha_{eff}\sin\theta\right)^3 d\theta = \frac{1}{2}-\frac{4}{\pi}\alpha_{eff}+\frac{9}{8}\alpha_{eff}^2-\frac{16}{15\pi}\alpha_{eff}^3$. (2.19)

C. Boost Inductance

The boost inductance is determined based on the power balance between the input and output, or $P_o = \eta \cdot P_{in}$, where η is the conversion efficiency. Considering the input power equation in (2.12), the boost inductance is determined by

$$L_b = \frac{\eta\pi V_p^2}{8\omega_s P_o}y\,. \tag{2.20}$$

D. Resonant Parameters

The DC/AC inverter stage, shown in Figure 2-4(b) where C_d is a DC-block capacitor, is a second-order series-resonant parallel-loaded tank, which can be described by the following parameters [A22].

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad \text{undamped natural frequency,} \tag{2.21}$$

$$Z_o = \sqrt{\frac{L_r}{C_r}} \qquad \text{characteristic impedance,} \tag{2.22}$$

$$Q_L = \frac{R_{la}}{Z_o} \qquad \text{quality factor, and} \tag{2.23}$$

$$f_r = f_o \sqrt{1 - \frac{1}{Q_L^2}} \qquad \text{resonant frequency.} \tag{2.24}$$

Using fundamental approximation, the amplitude of the resonant inductor current is given by

$$I_{Spk} = \frac{2V_B}{\pi} \cdot \frac{\sqrt{1 + (Q_L f_n)^2}}{Z_o \sqrt{Q_L^2 (1 - f_n^2)^2 + f_n^2}}, \tag{2.25}$$

where f_n ($=f_s/f_o$) is the normalized switching frequency.

The RMS lamp voltage (output voltage) is given by

$$V_{la} = \frac{\sqrt{2}V_B}{\pi} \cdot \frac{1}{\sqrt{(1 - f_n^2)^2 + \left(\frac{f_n}{Q_L}\right)^2}}. \tag{2.26}$$

The RMS lamp current is given by

$$I_{la} = \frac{\sqrt{2}V_B}{\pi} \cdot \frac{1}{Z_o \sqrt{Q_L^2 (1 - f_n^2)^2 + f_n^2}}. \tag{2.27}$$

Substituting (2.23) into (2.26) yields

$$\frac{V_{la}^2}{\left(\frac{\sqrt{2}V_B}{\pi(1 - f_n^2)}\right)^2} + \frac{I_{la}^2}{\left(\frac{\sqrt{2}V_B}{\pi Z_o f_n}\right)^2} = 1. \tag{2.28}$$

So the output characteristic of the resonant circuit is described by a family of elliptic curves in the V-I plane, with a variable f_n.

If f_n equals one, namely $f_s = f_o$, (2.28) reduces to:

$$I_{la} = \frac{\sqrt{2}V_B}{\pi Z_o} = \frac{\sqrt{2}V_B}{\pi \omega_o L_r} = \frac{\sqrt{2}V_B \omega_o C_r}{\pi}. \tag{2.29}$$

Equation (2.29) shows that output current is independent of load resistance at f_o. A current source characteristic is therefore offered. This current source characteristic generates a high voltage to strike the lamp and sets the operating current. Therefore, it is preferable that the resonant circuit operate in the vicinity of its undamped resonant frequency. Considering the ZVS operation, f_s is usually selected to be slightly greater than f_o. Given f_n, quality factor Q_L can be obtained from Equation (2.26), which leads to

$$Q_L = \frac{f_n}{\sqrt{\left(\frac{\sqrt{2}V_B}{\pi V_{la}}\right)^2 - \left(1 - f_n^2\right)^2}}, \tag{2.30}$$

and the characteristic impedance Z_o is given by

$$Z_o = \frac{R_{la}}{Q_L}. \tag{2.31}$$

The lamp can be considered as a pure resistance with negative dynamic impedance at the normal operation. So R_{la} is determined by

$$R_{la} = \frac{V_{la}^2}{P_o}. \tag{2.32}$$

The resonant inductance and capacitance are respectively obtained as

$$L_r = \frac{Z_o f_n}{\omega_S} \text{ and} \tag{2.33}$$

$$C_r = \frac{f_n}{Z_o \omega_S}. \tag{2.34}$$

For a given bus voltage V_B, switching frequency ω_s, lamp voltage V_{la}, lamp power P_o and f_n, the resonant parameters can be calculated from (2.30) to (2.34).

2.3.2 Interleaved Single-Stage PFC Electronic Ballast

The second circuit implementation places two identical boost inductors in the outer legs, as shown in Figure 2-7. As illustrated next, the PFC stage in the resulting circuit consists of two DCM boost cells operating 180^0 out of phase and offers better performance than the previous topology in terms of PF, harmonic distortion, switch current stress and EMI filter size.

In steady state, two conversion stages can be identified for the purpose of analysis. One is the PFC stage and the other is the resonant inverter stage. The resonant inverter stage is the same as that in the critical-conduction-mode circuit. For the PFC stage, four topological stages exist over one switching cycle, as shown in Figure 2-8. Key waveforms are shown in Figure 2-9.

Mode 1 [t_0, t_1]: At t_0, switch S_2 is turned off. Due to the positive inductor current of i_{Lb2}, the body diode of S_1 is forced to turn on, diverting the inductor current from S_2 to diode D_1. Voltage source V_{in1} is applied to the boost inductor L_{b1}, and i_{Lb1} increases linearly. Meanwhile, the negative voltage of (V_B-V_{in2}) is applied to boost inductor L_{b2}, and i_{Lb2} decreases linearly. The equivalent circuit is shown in Figure 2-8a. When i_{Lb1} is greater than i_{Lb2}, D_1 is naturally turned off and the channel of S_1 starts conducting since the gate voltage is applied to S_1 when D_1 conducts current. Because the discharging voltage of (V_B-V_{in2}) is bigger than the charging voltage of V_{in2}, and at the same time the discharging period allowed is the same as the charging period, i_{Lb2} will definitely drop to zero. DCM operation of boost inductor is ensured.

Mode 2 [t_1, t_2]: D_4 is turned off when i_{Lb2} drops to zero. Since the *di/dt* rate of the D_4 current is controlled by $(V_B - V_{in(rec)}/2)/L_{b2}$, the reverse recovery of D_4 is usually not a problem. Due to the positive voltage applied, i_{Lb1} continues increasing during this mode.

Mode 3 [t_2, t_3]: Switch S_1 is turned off at t_2 and the body diode of S_2 is forced on by i_{Lb1}. The negative voltage of (V_B-V_{in1}) is applied to L_{b1}, resulting in a decrease of i_{Lb1}. V_{in2} is applied to L_{b2}, and i_{Lb2} increases linearly. When i_{Lb2} is greater than i_{Lb1}, D_2 is off and S_2 is on. This mode ends when i_{Lb1} decreases to zero.

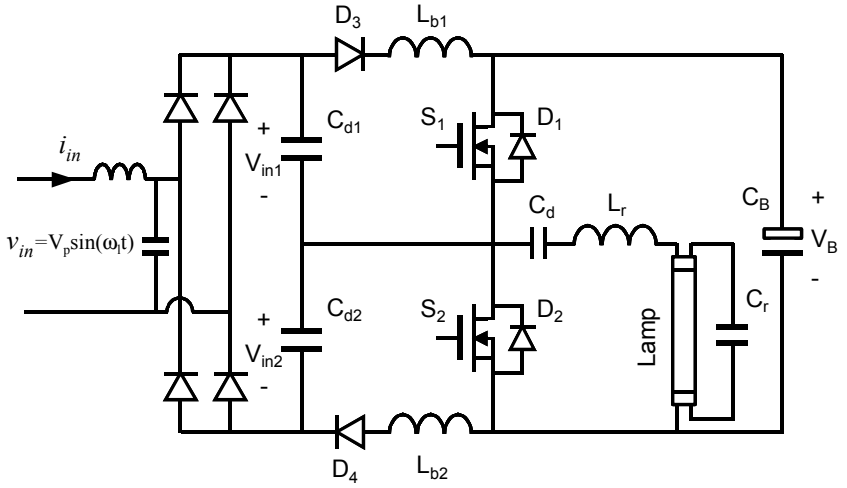


Figure 2-7. Single-stage interleaved PFC electronic ballast.

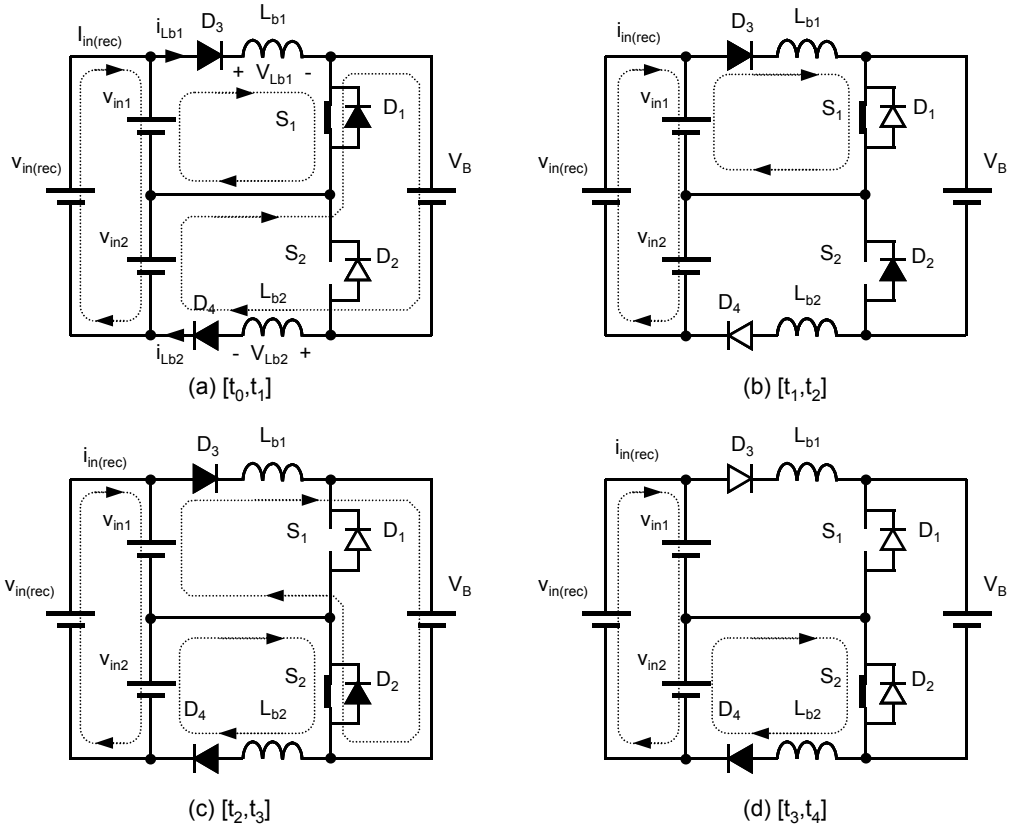


Figure 2-8. Topological stages of the PFC stage.

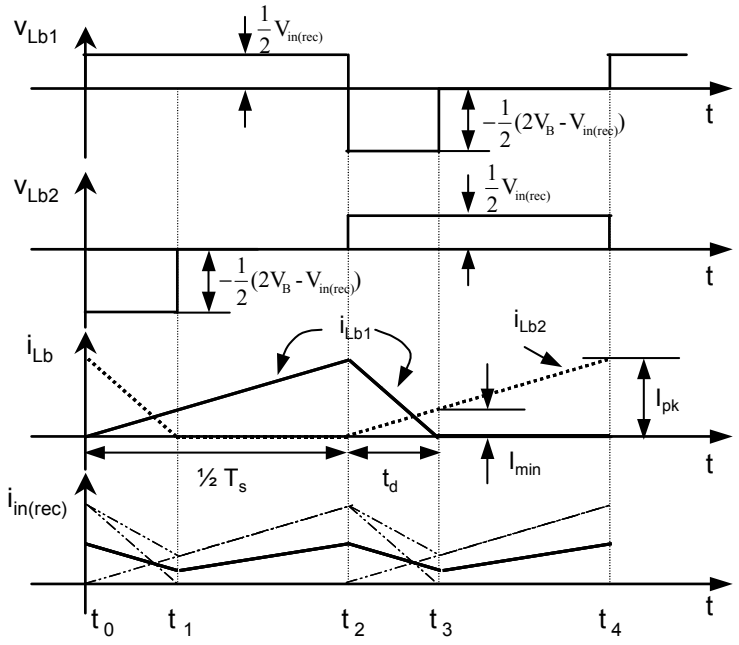


Figure 2-9. Key-switching waveforms.

Mode 4 [t_3, t_4]: D_3 is turned off when i_{Lb1} drops to zero. The i_{Lb2} continues increasing until S_2 is turned off at t_4, and a new switching cycle begins.

This analysis shows that i_{Lb1} and i_{Lb2} operate in DCM and 180^0 out of phase. The rectified input current $i_{in(rec)}$ equals half of the sum of i_{Lb1} and i_{Lb2}. The ripple current is reduced effectively. The line current, PF, THD and circuit parameters can be obtained as follows.

A. Input Current, PF and THD

From Figure 2-9, the peak inductor current I_{pk} is determined by

$$I_{pk} = \frac{V_{in1}}{L_b}\frac{1}{2}T_S = \frac{\pi V_p}{2\omega_s L_b}\left|\sin\omega_l t\right|. \tag{2.35}$$

The discharge time t_d is given by

$$t_d = \frac{I_{pk}}{(V_B - V_{in1})/L_b} = \frac{\alpha_{eff}|\sin\omega_l t|}{1-\alpha_{eff}|\sin\omega_l t|}\frac{T_s}{2}. \quad (2.36)$$

Therefore, the minimum value of (i_{Lb1} + i_{Lb2}) equals

$$I_{\min} = \frac{\frac{1}{2}V_{in(rec)}}{L_b}t_d = \frac{\pi V_p}{2\omega_s L_b}\frac{\alpha_{eff}|\sin\omega_l t|}{1-\alpha_{eff}|\sin\omega_l t|}|\sin\omega_l t|. \quad (2.37)$$

The rectified input current $i_{in(rec)}$ equals half of (i_{Lb1} +i_{Lb2}). Therefore, the peak-to-peak ripple current and average current of the rectified line input are determined by

$$i_{ripple}^{pp} = \frac{1}{2}(I_{pk} - I_{\min}) = \frac{\pi V_p}{4\omega_s L_b}\frac{1-2\alpha_{eff}|\sin\omega_l t|}{1-\alpha_{eff}|\sin\omega_l t|}|\sin\omega_l t|, \text{ and} \quad (2.38)$$

$$i_{in(rec)}^{av} = \frac{I_{pk} + I_{\min}}{4} = \frac{\pi V_p}{8\omega_s L_b}\frac{1}{1-\alpha_{eff}|\sin\omega_l t|}|\sin\omega_l t|. \quad (2.39)$$

Due to the high-frequency input filter and rectifier, the instantaneous line current i_{in} is obtained as

$$i_{in} = \frac{\pi V_p}{8\omega_s L_b}\frac{1}{1-\alpha_{eff}|\sin\omega_l t|}\sin\omega_l t. \quad (2.40)$$

Equation (2.40) shows that the line current will contain a certain amount of distortion due to the non-linear term of $1/(1-\alpha_{eff}\cdot|\sin\omega_l t|)$.

The line RMS current is given by

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_{in}^2 d\theta} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{\pi V_p}{8\omega_s L_b}\frac{\sin\theta}{1-\alpha_{eff}\sin\theta}\right]^2 d\theta} = \frac{\pi V_p}{8\omega_s L_b}\sqrt{z}, \quad (2.41)$$

where $z = \frac{1}{\pi}\int_0^{\pi}\frac{\sin^2\theta}{(1-\alpha_{eff}\sin\theta)^2}d\theta$

$$= \frac{2}{\pi\alpha_{eff}(1-\alpha_{eff}^2)} + \frac{1}{\alpha_{eff}^2} + \frac{2\alpha_{eff}^2 - 1}{\alpha_{eff}^2(1-\alpha_{eff}^2)}\frac{2}{\sqrt{1-\alpha_{eff}^2}}\left[\frac{1}{2} - \frac{1}{\pi}\tan^{-1}\left(\frac{-\alpha_{eff}}{\sqrt{1-\alpha_{eff}^2}}\right)\right]. \quad (2.42)$$

The input real power is given by

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} v_{in} i_{in} d\theta = \frac{1}{\pi}\int_0^{\pi} V_p \sin\theta \frac{\pi V_p}{8\omega_s L_b} \frac{\sin\theta}{1-\alpha_{eff}\sin\theta} d\theta = \frac{\pi V_p^2}{8\omega_s L_b} y\,, \tag{2.43}$$

where $y = \frac{1}{\pi}\int_0^{\pi} \frac{\sin^2\theta}{1-\alpha_{eff}\sin\theta} d\theta$

$$= -\frac{2}{\pi\alpha_{eff}} - \frac{1}{\alpha_{eff}^2} + \frac{2}{\alpha_{eff}^2\sqrt{1-\alpha_{eff}^2}}\left[\frac{1}{2} - \frac{1}{\pi}\tan^{-1}\left(\frac{-\alpha_{eff}}{\sqrt{1-\alpha_{eff}^2}}\right)\right]. \tag{2.44}$$

The expressions of PF and THD are the same as (2.14) and (2.15), respectively.

B. RMS MOSFET Current of the PFC Stage

Note that two MOSFETs operate at ZVS. The current through the channel of the MOSFET can be determined from the boost inductor current waveforms, as shown in Figure 2-10. The time periods τ_1 and τ_2 are determined by

$$\frac{\tau_1}{T_s/2} = \frac{I_a}{I_{pk}} = \frac{t_d - \tau_1}{t_d}, \text{ and} \tag{2.45}$$

$$\tau_2 = \frac{1}{2}T_s - t_d\,. \tag{2.46}$$

Substituting (2.36) into the above two equations leads to

$$\frac{\tau_1}{T_s} = \frac{1}{2}\alpha_{eff}\left|\sin\omega_l t\right|, \text{ and} \tag{2.47}$$

$$\frac{\tau_2}{T_s} = \frac{1-2\alpha_{eff}\left|\sin\omega_l t\right|}{1-\alpha_{eff}\left|\sin\omega_l t\right|}\frac{T_s}{2}\,. \tag{2.48}$$

Therefore, the average of $i_s^2(t)$ over one switching period is

$$\left\langle i_s^2 \right\rangle_{Ts} = \frac{1}{T_s}\int_t^{t+T_s} i_s^2(t)dt = \frac{t_d - \tau_1}{T_s}\frac{I_{\min}^2}{3} + \frac{\tau_2}{T_s}\frac{I_{\min}^2 + I_{\min}I_{pk} + I_{pk}^2}{3}$$

$$= \frac{I_{pk}^2}{6}\left(1 - \frac{\alpha_{eff}^3\left|\sin\omega_l t\right|^3}{\left(1-\alpha_{eff}\left|\sin\omega_l t\right|\right)^2}\right). \tag{2.49}$$

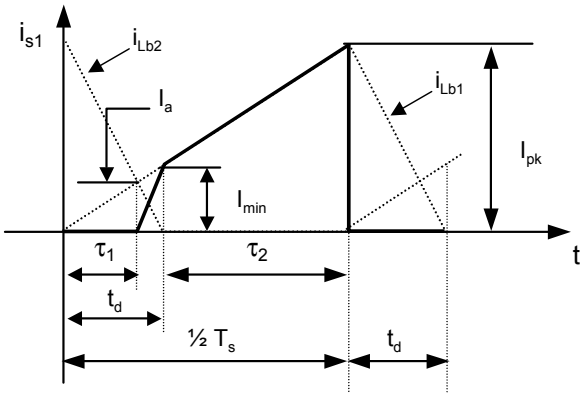


Figure 2-10. MOSFET current waveform.

The RMS current $I_{s(rms)}$ is then determined by

$$I_{s(rms)} = \sqrt{\frac{1}{T_l}\int_0^{T_l} \left\langle i_s^2 \right\rangle_{T_s} dt} = \sqrt{\frac{1}{T_l}\int_0^{T_l} \frac{I_{pk}^2}{6}\left(1 - \frac{\alpha_{eff}^3 \left|\sin \omega_l t\right|^3}{\left(1-\alpha_{eff}\left|\sin \omega_l t\right|\right)^2}\right) dt}\,, \tag{2.50}$$

which can be simplified to

$$I_{s(rms)} = \frac{\sqrt{6}\pi V_p}{12\omega_s L_b}\sqrt{\frac{1}{\pi}\int_0^{\pi}\left(\sin^2\theta - \frac{\alpha_{eff}^3 \sin^5\theta}{\left(1-\alpha_{eff}\sin\theta\right)^2}\right) d\theta} = \frac{\sqrt{6}\pi V_p}{12\omega_s L_b}\sqrt{g}\,, \tag{2.51}$$

where $g = \frac{1}{\pi}\int_0^{\pi}\left(\sin^2\theta - \frac{\alpha_{eff}^3 \sin^5\theta}{\left(1-\alpha_{eff}\sin\theta\right)^2}\right) d\theta = \frac{1}{2} - \frac{\alpha_{eff}^3}{\pi}\int_0^{\pi}\frac{\sin^5\theta}{\left(1-\alpha_{eff}\sin\theta\right)^2} d\theta\,.$ (2.52)

C. Boost Inductance

The boost inductance is determined based on the power balance between the input and output, or $P_o = \eta \cdot P_{in}$, where η is the conversion efficiency. Considering the input power equation, (2.43), the boost inductance is given by

$$L_{b1} = L_{b2} = L_b = \frac{\eta\pi V_p^2}{8\omega_s P_o} y\,. \tag{2.53}$$

D. Resonant Parameters

The DC/AC inverter stage is the same as that of the proposed critical-conduction-mode circuit. Therefore, the design procedure for the resonant parameters is the same as that discussed in Section 2.3.1.

2.3.3 Performance Comparison and Experimental Results

To evaluate the voltage-divider techniques, a circuit comparison and evaluation are made in this section. The circuit in Figure 2-1(b) is used as the benchmark. The comparison has been made in terms of PF, THD, input current ripple and switch RMS current stress.

A. Review of the Benchmark Circuit

Figure 2-11 shows the simplified equivalent circuit and key waveforms of the benchmark circuit. It can be seen that the circuit operates in critical-conduction mode. These waveforms show that the input ripple current, instantaneous line current, RMS current, and input power can be determined by

$$i_{ripple}^{pp} = \frac{\pi V_p}{\omega_s L_b}(1-\alpha_{eff}\left|\sin\omega_l t\right|)\left|\sin\omega_l t\right|, \tag{2.54}$$

$$i_{in} = \frac{\pi V_p}{2\omega_s L_b}(1-\alpha_{eff}\left|\sin\omega_l t\right|)\cdot\sin\omega_l t \text{ , and} \tag{2.55}$$

$$I_{rms} = \frac{\pi V_p}{2\omega_s L_b}\sqrt{z}\ , \tag{2.56}$$

where $z = \frac{1}{\pi}\int_0^{\pi}\left((1-\alpha_{eff}\sin\theta)\sin\theta\right)^2 d\theta = \frac{1}{2}-\frac{8}{3\pi}\alpha_{eff}+\frac{3}{8}\alpha_{eff}^2$, and (2.57)

$$P_{in} = \frac{\pi V_p^2}{2\omega_s L_b}y\ , \tag{2.58}$$

where $y = \frac{1}{\pi}\int_0^{\pi} \sin^2\theta(1-\alpha_{eff}\sin\theta)d\theta = \frac{1}{2} - \frac{4}{3\pi}\alpha_{eff}$. (2.59)

The RMS MOSFET current is given by

$$I_{s(rms)} = \frac{\sqrt{6}\pi V_p}{3\omega_s L_b}\sqrt{g}, \tag{2.60}$$

where $g = \frac{1}{\pi}\int_0^{\pi} \left(1-\alpha_{eff}\sin\theta\right)^3 \sin^2\theta d\theta = \frac{1}{2} - \frac{4}{\pi}\alpha_{eff} + \frac{9}{8}\alpha_{eff}^2 - \frac{16}{15\pi}\alpha_{eff}^3$. (2.61)

The boost inductance is obtained by balancing the power between the input and the output, which yields

$$L_b = \frac{\eta\pi V_p^2}{2\omega_s P_o} y. \tag{2.62}$$

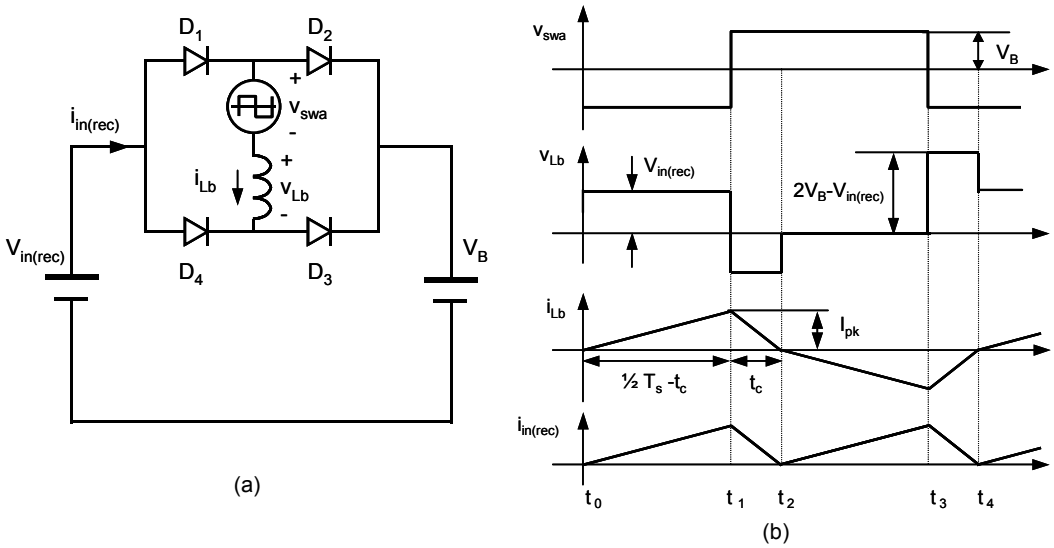


Figure 2-11. (a) Simplified PFC stage, and (b) key waveforms of the benchmark circuit [B29].

B. PF and THD Comparison

The PF and THD are of primary concern in the electronic ballasts. Ideally, the PF is unity and the THD equals zero. However, as analyzed in Sections 2.3.1 and 2.3.2, the line current is not sinusoidal but is instead distorted. The distortion is a function of the α_{eff} factor. For the convenience of discussion, the equations of line current are rewritten as

Benchmark circuit $$i_{in(BM)} = \frac{\pi V_p}{2\omega_s L_b}(1-\alpha_{eff}|\sin\omega_l t|)\sin\omega_l t\,, \qquad (2.63)$$

Critical-conduction circuit $$i_{in(C\_CM)} = \frac{\pi V_p}{8\omega_s L_b}(1-\alpha_{eff}|\sin\omega_l t|)\sin\omega_l t\,, \text{ and} \qquad (2.64)$$

Interleaved circuit $$i_{in(INT)} = \frac{\pi V_p}{8\omega_s L_b}\frac{1}{1-\alpha_{eff}|\sin\omega_l t|}\sin\omega_l t\,. \qquad (2.65)$$

Therefore, the normalized line currents become

Benchmark circuit $$i_{in(BM)\_n} = \frac{1-\alpha_{eff}|\sin\omega_l t|}{1-\alpha_{eff}}\sin\omega_l t\,, \qquad (2.66)$$

Critical conduction circuit $$i_{in(C\_CM)\_n} = \frac{1-\alpha_{eff}|\sin\omega_l t|}{1-\alpha_{eff}}\sin\omega_l t\,, \text{ and} \qquad (2.67)$$

Interleaved circuit $$i_{in(INT)\_n} = \frac{1-\alpha_{eff}}{1-\alpha_{eff}|\sin\omega_l t|}\sin\omega_l t\,. \qquad (2.68)$$

It can be seen that the proposed critical-conduction-mode circuit has a normalized line current equation that is identical to that of the benchmark circuit, which also can be seen from the switching waveforms in Figures 2-6 and 2-11. For all three circuits, the line current waveforms approach an ideal sinusoidal waveform when α_{eff} approaches zero, and becomes more and more distorted as α_{eff} increases. Figure 2-12 shows the waveforms as a function of the α_{eff} factor.

The PF is the ratio of real power to apparent power, which can be represented by a uniform formula defined in (2.14) and rewritten as

$$PF = \frac{P_{in}}{V_{g(rms)} I_{rms}} = \frac{\sqrt{2}y}{\sqrt{z}}. \tag{2.69}$$

THD is a function of PF, which is given by

$$THD = \frac{1}{PF}\sqrt{1-PF^2} = \frac{\sqrt{2z}}{2y}\sqrt{1-\frac{2y^2}{z}}. \tag{2.70}$$

With the derived y and z parameters in (2.11), (2.13), (2.42), (2.44), (2.57) and (2.59) the PFs and THDs are plotted in Figure 2-13 for the three circuits. It can be seen that for a given α_{eff}, the interleaved circuit has the best PF with lowest THD. The proposed critical-conduction-mode circuit has the same PF and THD as the benchmark circuit. It also shows that even when the bus voltage is near the line peak voltage ($\alpha_{eff} \approx 0.5$), the PFs of all three circuits are close to 0.99.

C. Input-Current Ripple Comparison

Input-current ripple frequency and ripple magnitude are related to the differential EMI filter size and weight. A higher ripple frequency and lower ripple magnitude are preferred. As discussed in Sections 2.3.1 and 2.3.2, the ripple frequencies in the proposed two circuits are twice the switching frequency. However, the magnitudes are different. For the convenience of discussion, the equations of the ripple current are rewritten as

Benchmark circuit $$i_{ripple(BM)}^{pp} = \frac{\pi V_p}{\omega_s L_b}(1-\alpha_{eff}\left|\sin\omega_l t\right|)\sin\omega_l t, \tag{2.71}$$

Critical-conduction circuit $$i_{ripple(C\_CM)}^{pp} = \frac{\pi V_p}{4\omega_s L_b}(1-\alpha_{eff}\left|\sin\omega_l t\right|)\sin\omega_l t, \tag{2.72}$$

Interleaved circuit $$i_{ripple(INT)}^{pp} = \frac{\pi V_p}{4\omega_s L_b}\frac{1-2\alpha_{eff}\left|\sin\omega_l t\right|}{1-\alpha_{eff}\left|\sin\omega_l t\right|}\sin\omega_l t. \tag{2.73}$$

If the average input line current is used as the base value, the normalized peak-to-peak ripple current is obtained as

Benchmark circuit $$i_{ripple(BM)\_n}^{pp} = 2, \tag{2.74}$$

Critical-conduction circuit $i_{ripple(C\_CM)\_n}^{pp} = 2$, and (2.75)

Interleaved circuit $i_{ripple(INT)\_n}^{pp} = 2\left(1 - 2\alpha_{eff}\left|\sin\omega_l t\right|\right)$. (2.76)

Figure 2-14 shows the normalized line peak-to-peak ripple current comparison. It can be seen that the ripple magnitude in the interleaved circuit is smaller than other two circuits and increases as the α_{eff} factor decreases.

D. RMS MOSFET Current Comparison

The RMS current determines the conduction loss. The power switches carry both the PFC and inverter stage currents in these three circuits. To simplify the analysis, only the PFC stage current is considered since the inverter stages can be assumed to be identical. The equations of RMS MOSFET current have been derived as follows:

Benchmark circuit $I_{s(BM)}^{rms} = \dfrac{\sqrt{6}\pi V_p}{3\omega_s L_b}\sqrt{g}$, (2.77)

Critical-conduction circuit $I_{s(C\_CM)}^{rms} = \dfrac{\sqrt{6}\pi V_p}{12\omega_s L_b}\sqrt{g}$, and (2.78)

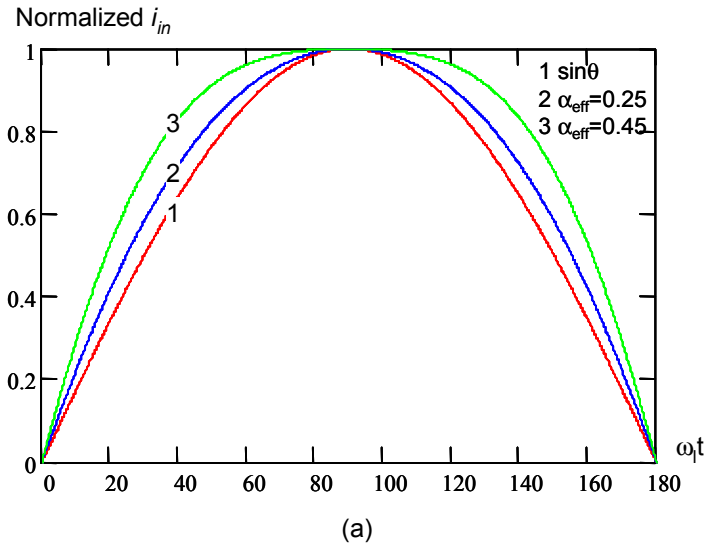
Interleaved circuit $I_{s(INT)}^{rms} = \dfrac{\sqrt{6}\pi V_p}{12\omega_s L_b}\sqrt{g}$. (2.79)

Therefore, the normalized RMS MOSFET currents can be represented by

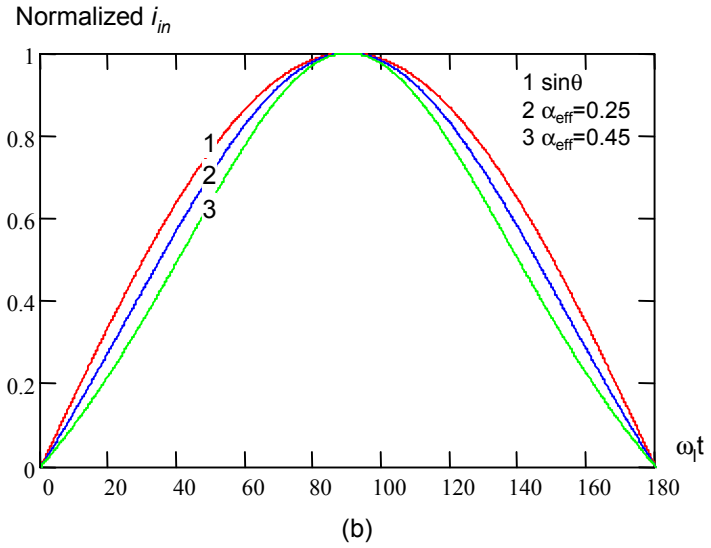
$$I_{s\_n}^{rms} = \frac{I_{s(rms)}}{I_{base(rms)}} = \frac{2\sqrt{3}}{3}\frac{\sqrt{g}}{y}, \tag{2.80}$$

where $I_{base(rms)} = \dfrac{P_{in}}{V_p/\sqrt{2}}$. (2.81)

With the derived *y* and *g* parameters in (2.13), (2.19), (2.44), (2.52), (2.59) and (2.61) the normalized RMS MOSFET currents are plotted in Figure 2-15. It shows that the interleaved circuit has smaller current stress than do the other two circuits, and this difference increases as α_{eff} increases.



(a)



(b)

Figure 2-12. Normalized line current waveforms as a function of α_{eff} within a half line cycle: (a) benchmark circuit and proposed critical-conduction-mode circuit, and (b) proposed interleaved circuit.

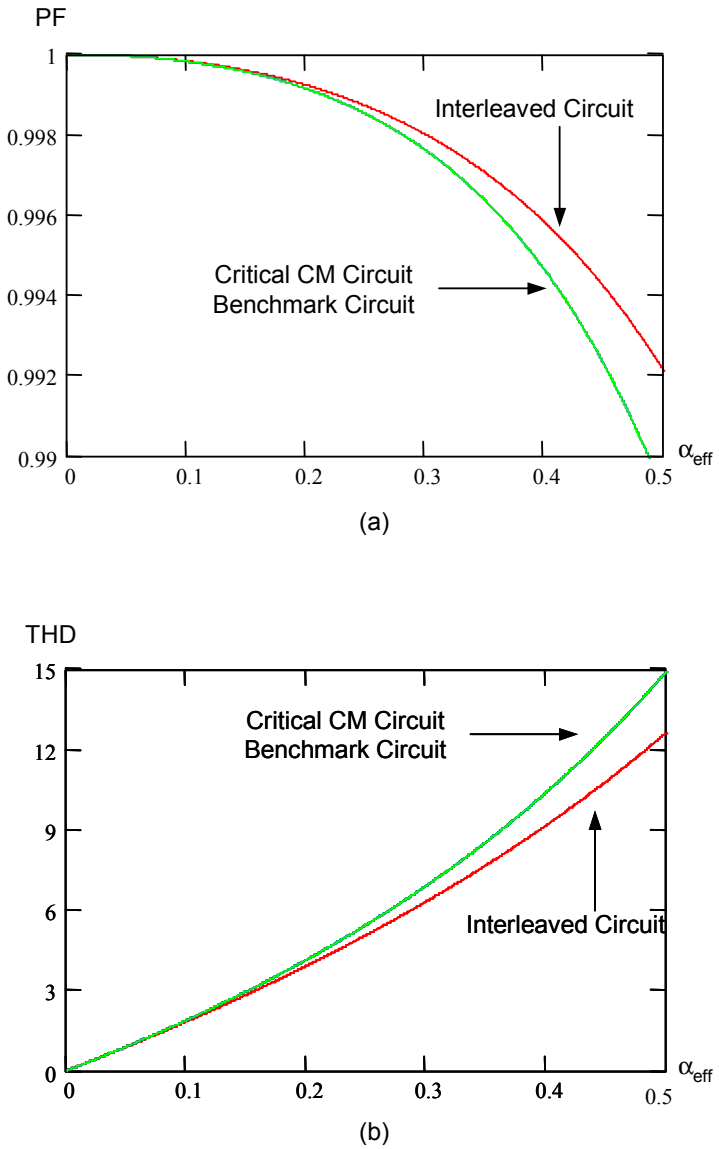


Figure 2-13. Comparison of (a) PF and (b) THD.

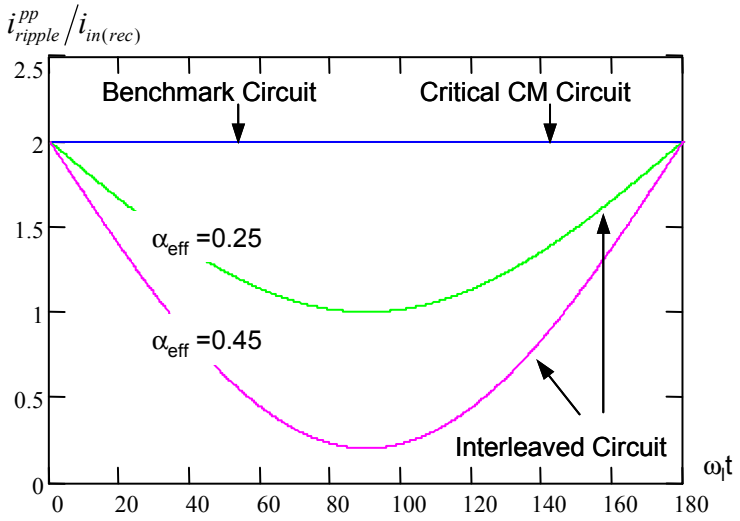


Figure 2-14. Normalized ripple current comparison over a half-line cycle

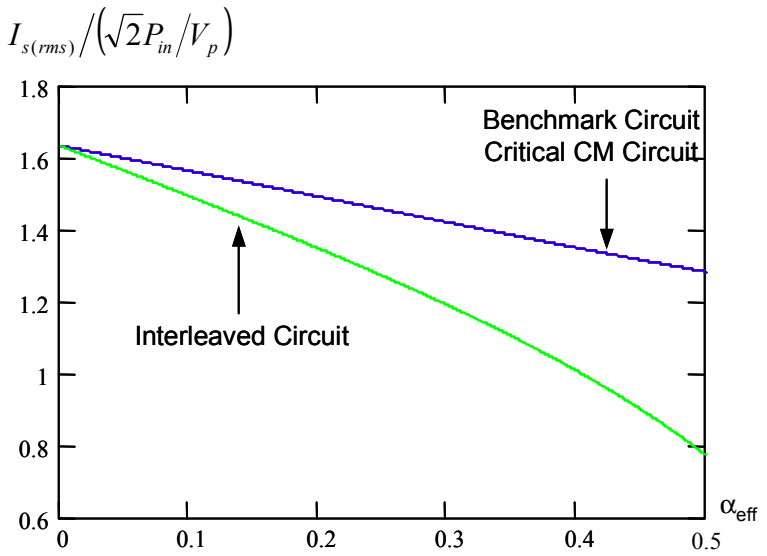


Figure 2-15. Normalized switch RMS current comparison.

E. Experimental Results

Two prototypes are implemented to verify the analysis with 200V input and 85W lamp power. The full-load bus voltage is selected to be 1.1 times the line peak voltage, or 311 V. The lamp voltage is 230 V_{rms}, and the equivalent resistance is 620 Ω with two lamps in series. If the switch frequency is 52 kHz, and f_n =1.05, the resonant tank parameters are calculated from (2.30) – (2.34) as L_r =1.14 mH and C_r =9.2 nF. The boost inductances are calculated from (2.20) and (2.53), assuming η =85% for the critical-conduction mode and interleaved electronic ballasts, respectively. The calculated results are 323 μH and 757 μH, respectively. The voltage-divider capacitance is 0.33 μF, which is sufficient for it to be considered a voltage source at a switching frequency of 52 kHz. The EMI filter is C_f =0.22 μF, and L_f =3 mH and 1 mH for the critical-conduction mode and interleaved electronic ballasts, respectively. Figure 2-16 shows the measured line current waveforms with 0.969 PF and 21.2% THD for the critical-conduction mode and 0.994 PF and 9.2% THD for the interleaved ballast. At the same boost conversion ratio, the measured harmonics could meet the IEC 1000-3-2 Class C requirement by a small margin for the critical-conduction mode, but by a sufficient margin for the interleaved ballast, as shown in Figure 2-17. The measured boost inductor current waveforms are shown in Figure 2-18, and are in good agreement with the theoretical models. Figure 2-19 shows the switch current waveforms. The magnitude of switch current is larger in critical-conduction mode than in the interleaved circuit. The measured efficiencies are 83% and 83.7%, respectively, if the filament losses are included. Because the resonant tank is not modulated by any switching mode, the lamp current CF is about 1.4, as shown in Figure 2-20.

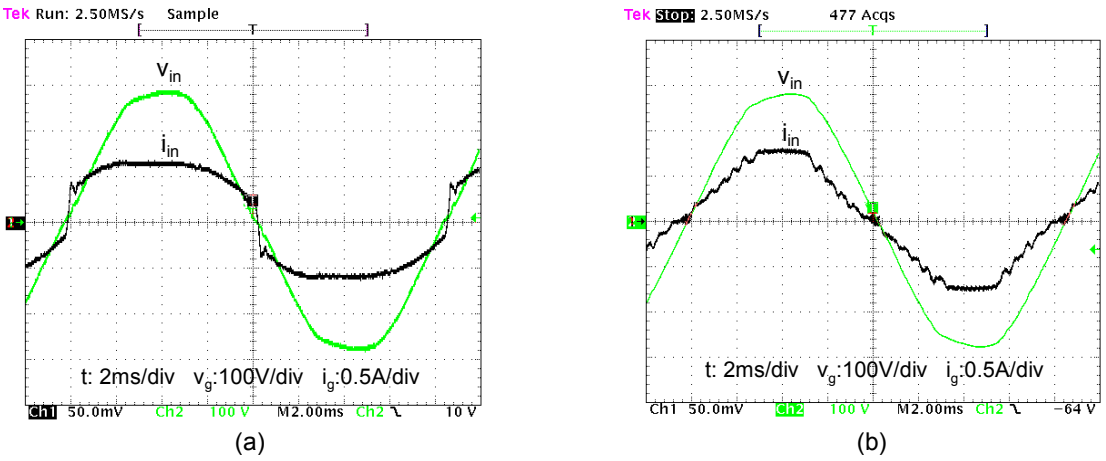


Figure 2-16. Measured input line current waveforms: (a) critical-conduction-mode electronic ballast, and (b) interleaved electronic ballast.

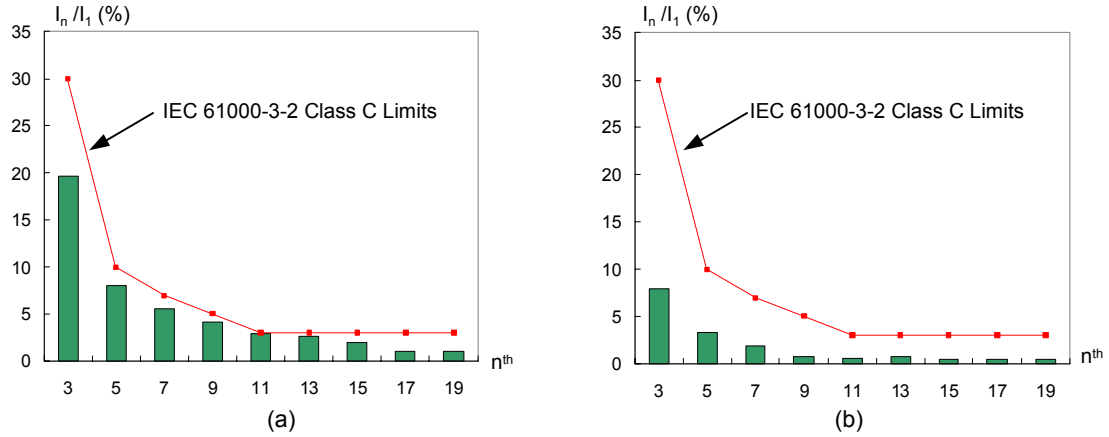


Figure 2-17. Measured input harmonic currents: (a) critical-conduction-mode electronic ballast, and (b) interleaved electronic ballast.

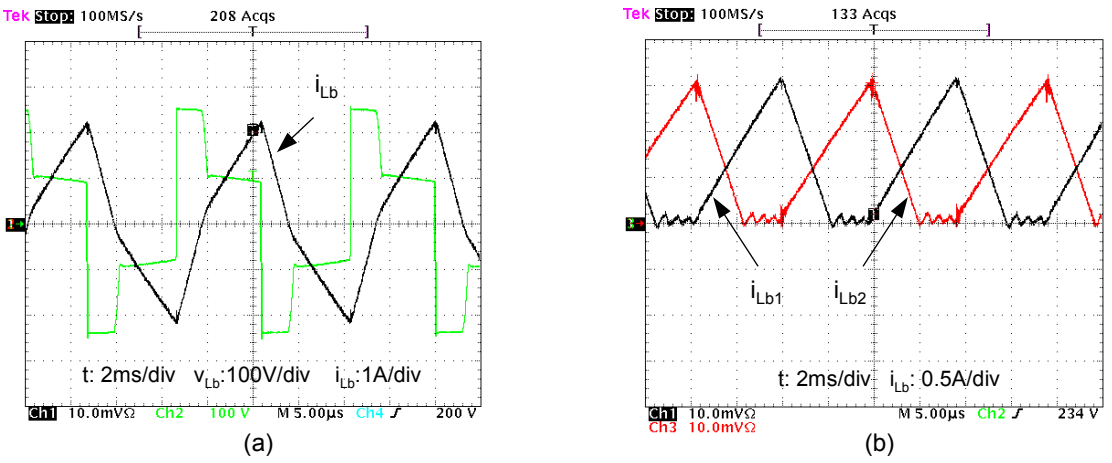


Figure 2-18. Measured boost inductor currents: (a) critical-conduction-mode electronic ballast, and (b) interleaved electronic ballast.

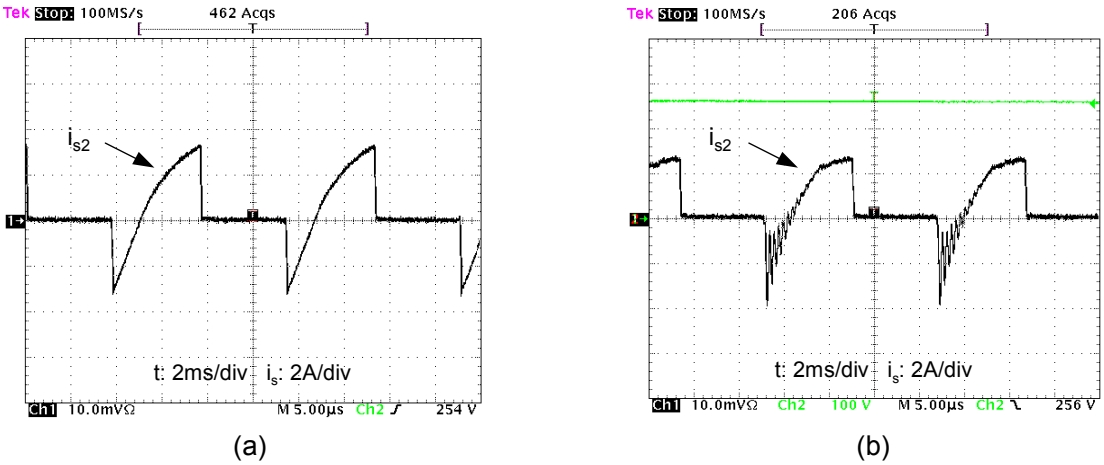
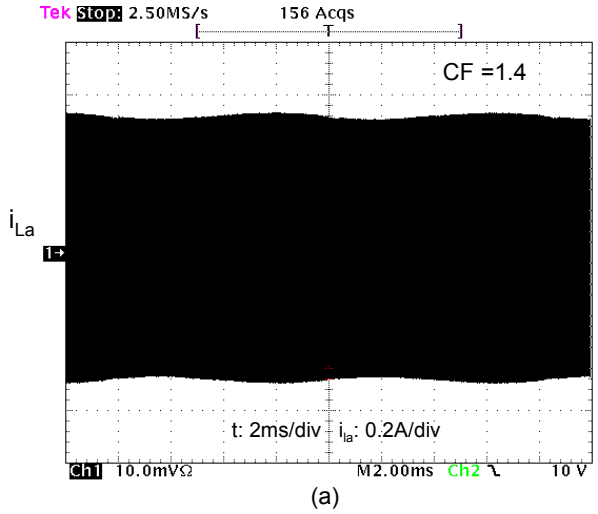
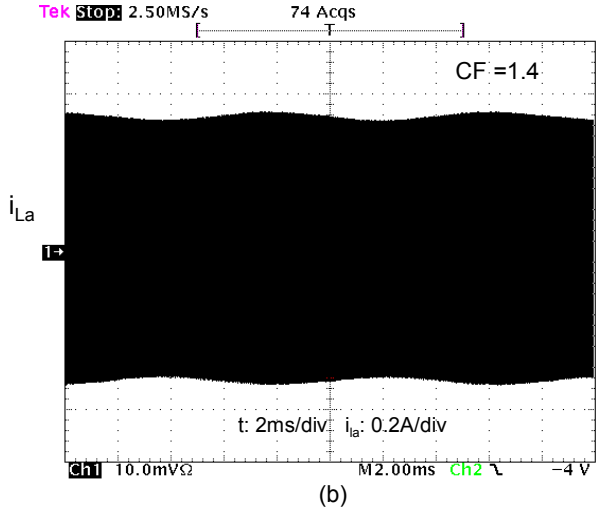


Figure 2-19. Measured switch current waveforms: (a) critical-conduction-mode electronic ballast, and (b) interleaved electronic ballast.



(a)



(b)

Figure 2-20. Measured lamp currents over a line cycle: (a) critical-conduction-mode electronic ballast, and (b) interleaved electronic ballast.

2.4. Summary

For the conventional single-stage boost-derived electronic ballast the bus voltage is required to exceed two times the peak line voltage in order to achieve DCM operation, which may severely penalize the power stage design. This chapter proposed a novel voltage-divider concept to halve the effective α factor so that a high PF can be achieved as long as the bus voltage is higher than the line peak voltage. In addition, the ripple frequency of the line current is doubled and the ripple magnitude is reduced so that a small input filter can be used. Two circuit implementations, a critical-conduction-mode PFC electronic ballast and an interleaved PFC electronic ballast, have been proposed and analyzed.

A comparative study has been done to evaluate the proposed concept. The results show that with the voltage divider, the proposed critical-conduction-mode circuit has almost the same performance as the benchmark circuit while the proposed interleaved circuit has better performance in terms of PF, THD, input ripple current and RMS MOSFET current stress. However, two boost inductors are needed. The proposed critical-conduction-mode electronic ballast is more suitable for low-power applications, while the interleaved circuit is attractive for medium-power applications.

Chapter 3 Boost-Derived Single-Stage PFC Electronic Ballasts with Wide-Range Dimming Control

3.1 Introduction

In general, electronic ballasts can provide dimming capability when matched with an appropriate control system. Figure 3-1 shows the circuit diagram of a conventional two-stage PFC dimmable electronic ballast, in which frequency control is used. The dimming operation is fulfilled by adjusting the inverter switching frequency while the input current waveform and bus voltage are well regulated by the PFC stage.

The circuit shown in Figure 3-1 represents a mature dimming practice. However, the circuit cost is usually high. To reduce the cost, one approach is to employ a single-stage PFC technique. Figure 3-2 shows an example if the proposed critical-conduction-mode ballast operates in dimming mode. However, the control freedoms are reduced due to the integration of the PFC and inverter switches into one switch. Although the line input inherently has high PF, the bus voltage is no longer regulated. Besides, the lamp characteristic is nonlinear with negative incremental impedance. The equivalent resistance varies with different dimming levels. As a result, interactions exist between the lamp and the inverter stage as well as the inverter stage and PFC stage.

To study the interaction between the lamp and the inverter stage, a lamp model is proposed, and is then used to study the system. The results are adjusted according to the boundary conditions between the inverter stage and the PFC stage. Using this approach, it is found that high bus voltage stress exists when the previously proposed two electronic ballasts operate in dimming mode. To suppress the bus voltage and expand the dimming range, a new single-stage PFC dimmable electronic ballast with asymmetrical duty ratio control is proposed, analyzed, designed and implemented. Finally, the circuit is verified by experimental results.

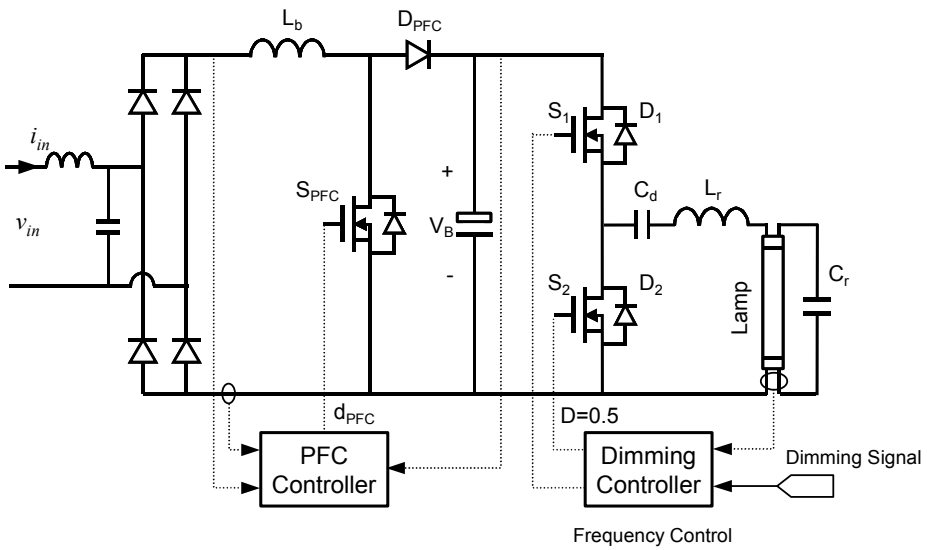


Figure 3-1. Conventional dimmable electronic ballast.

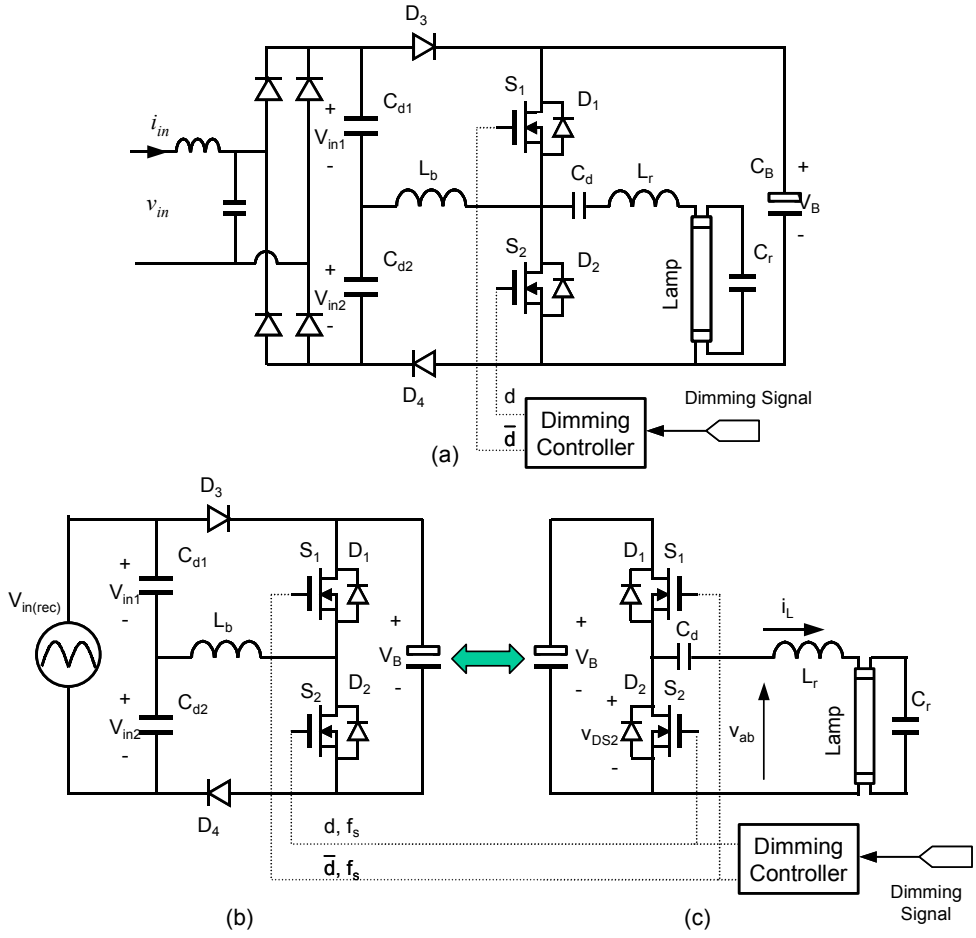


Figure 3-2. (a) Single-stage PFC electronic ballast with dimming control; (b) PFC stage; and (c) inverter stage with boundary conditions (V_B, d, f_s).

3.2 Modeling of Fluorescent Lamps for Dimming Operation

At high-frequency operation, the gas discharge lamp can be approximated as a pure resistance whose value changes with dimming operation. Figure 3-3(a) shows the measured Matsushita FHF32 fluorescent lamp's RMS voltage versus RMS current. It can be seen that the lamp resistance is smaller at higher lamp current and higher at lower lamp current. Using a constant resistance obtained from the rated voltage over the rated current will lead to considerable errors in the analysis of lamp-dimming operation.

The curve shown in Figure 3-3(a) implies that the lamp resistance is current-dependent. However, the relationship between the lamp voltage and current is highly nonlinear. It is found that lamp voltage increases almost linearly with the decrease of lamp power, as shown in Figure 3-3(b). Based on this observation, a lamp power-dependent mode is proposed in (3.1). To account for the positive impedance characteristic in the low lamp power range, an exponential term is added, as follows:

$$V_{la}(P_{la}) = a_0 + a_1 \cdot P_{la} + a_2 \cdot \exp(a_3 \cdot P_{la}), \tag{3.1}$$

$$I_{la}(P_{la}) = \frac{P_{la}}{V_{la}(P_{la})}, \text{ and} \tag{3.2}$$

$$R_{la}(P_{la}) = \frac{V_{la}^2(P_{la})}{P_{la}}, \tag{3.3}$$

where P_{la}, V_{la}, I_{la} and R_{la} are the lamp power, lamp RMS voltage, lamp RMS current and equivalent lamp resistance, respectively. The terms a_0-a_4 are the parameters for the units of volt, volt per watts, volt, and per watts, respectively.

The parameters a_0-a_3 can be experimentally determined from the measured data of the lamps. Usually, the curve-fitting function of *genfit* in Mathcad is used to extract the parameters from the measured data. For Matsushita FHF32 lamps, these parameters are obtained as a_0= 174.06 V, a_1= -1.43 V/W, a_2= -51.44 V, and a_3= -0.54 /W. As shown in Figure 3-4, the calculation results agree very closely with the measured data.

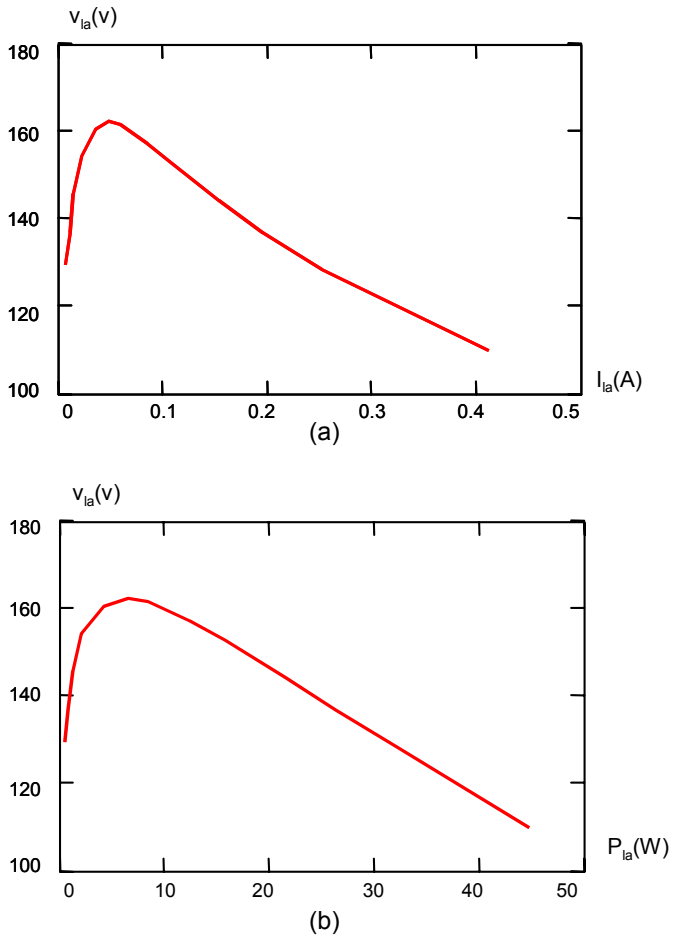


Figure 3-3. (a) Measured lamp voltage versus lamp current, and (b) measured lamp voltage versus lamp power.

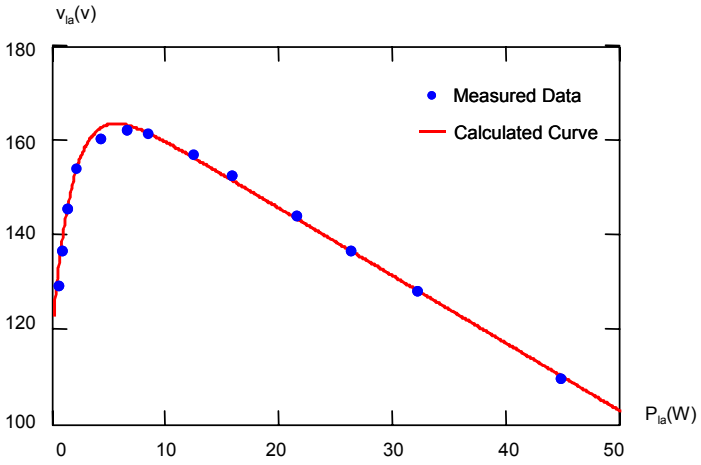


Figure 3-4. Curve-fitting with Equation (3.1).

3.3 Study of Boost-Derived Single-Stage PFC Dimmable Electronic Ballasts with Frequency Control

It is a common practice to use frequency control in the resonant converters to regulate the output power. Although the proposed single-stage PFC circuits consist of both a PFC stage and an inverter stage, these two stages can be first studied separately. The analysis results are then adjusted according to the boundary conditions. Using the developed lamp model, circuit performance of the critical-conductor mode and interleaved single-stage electronic ballasts with switch frequency control are analyzed as follows.

3.3.1 Dimming Operation of the Inverter Stage with Frequency Control

The inverter stage being studied is shown in Figure 3-2(c). By symmetrically driving two MOSFETs, a square-wave voltage source with amplitude of $\pm V_B/2$ is applied to the resonant circuit. Assume that only fundamental component is present in the resonant circuit. The inverter circuit can be represented by an equivalent circuit with lamp mode $R_{la}(P)$ and filament resistance r_f, as shown in Figure 3-5. From Figure 3-5, the lamp RMS voltage can be expressed as

$$V_{la}(P_{la}) = V_{ab1}\left|\frac{Z_p(P_{la})}{Z_s + Z_p(P_{la})}\right| = \frac{\sqrt{2}V_B}{\pi}\left|\frac{Z_p(P_{la})}{Z_s + Z_p(P_{la})}\right|, \tag{3.4}$$

where $Z_s = r_f + j\omega_s L = r_f + jZ_o f_n$, (3.5)

$$Z_p(P_{la}) = R_{la}(P_{la}) // \left(r_f + \frac{1}{j\omega_s C_r}\right) = \frac{R_{la}(P_{la})\left(1 + j\frac{f_n}{Z_o}r_f\right)}{1 + j\frac{f_n}{Z_o}\left(R_{la}(P_{la}) + r_f\right)}, \text{ and} \tag{3.6}$$

$f_n = f_s / f_o = \omega_s / \omega_o$ and $Z_o = \sqrt{L_r / C_r}$.

Since the filament resistance r_f is usually much smaller than R_{la} and Z_o, Equation (3.4) can be simplified into

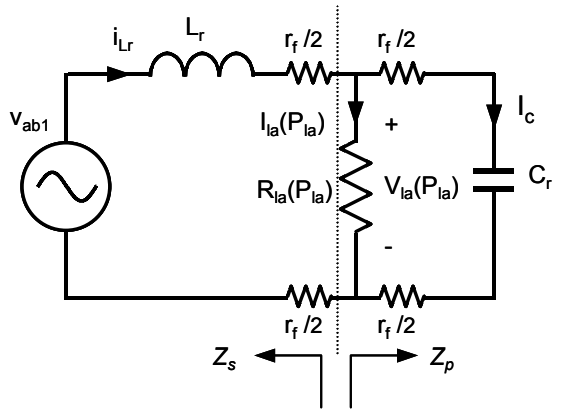


Figure 3-5. Equivalent circuit of the inverter stage.

$$V_{la}(P_{la}) \approx V_{ab1}\frac{1}{\sqrt{\left(1-f_n^2\right)^2+\left(\frac{f_n Z_o}{R_{la}(P_{la})}\right)^2}} = \frac{\sqrt{2}V_B}{\pi}\frac{1}{\sqrt{\left(1-f_n^2\right)^2+\left(\frac{f_n Z_o}{R_{la}(P_{la})}\right)^2}}. \quad (3.7)$$

From (3.7), the required frequency that gives the lamp power P_{la} is determined by

$$f_n(P_{la}) = \sqrt{1-\frac{1}{2}\left(\frac{Z_o}{R_{la}(P_{la})}\right)^2+\sqrt{\left[1-\frac{1}{2}\left(\frac{Z_o}{R_{la}(P_{la})}\right)^2\right]^2-\left[1-\left(\frac{\sqrt{2}V_B}{\pi V_{la}(P_{la})}\right)^2\right]}}. \quad (3.8)$$

Therefore, using the lamp mode developed in (3.1) to (3.3), the relationship between the lamp power and the control parameter f_s (or f_n) can be obtained from (3.8) for a given bus voltage and circuit parameter Z_o. Figure 3-6 shows the calculated P_{la}–f_n curves with different Z_o, and with V_B =410 V. It can be seen that frequency control can be improved when Z_o is large. However, the frequency sweeping range becomes wider, which is not good for circuit design.

Besides the control characteristic consideration, there is another important aspect: that of how the filament heating current is varied during the dimming operation. It is recommended that the filament current be maintained at a constant level over the entire dimming range. As shown in Figure 3-5, there are two sources that contribute to filament heating: the lamp arc current I_{la} (self-heating) and the parallel capacitor current I_c

(external heating). A filament current that is too large may shorten the lamp life; if the filament current is too small, it may not maintain a stable lamp arc. For the FHF32 lamps, the filament current is recommended to be around 0.4 A.

From Figure 3-5, the parallel capacitor current can be approximated by

$$I_c \approx (j\omega_s C_r) V_{la}(P_{la}) = j\frac{f_n}{Z_o} V_{la}(P_{la}). \tag{3.9}$$

The lamp arc current and parallel capacitor current are almost orthogonal to each other; therefore, the filament current can be determined by

$$I_f = \sqrt{I_{la}^2(P_{la}) + 2I_c^2} = \sqrt{\left(\frac{P_{la}}{V_{la}(P_{la})}\right)^2 + 2\left(\frac{f_n}{Z_o} V_{la}(P_{la})\right)^2}, \tag{3.10}$$

where f_n is determined from (3.8).

Figure 3-7 illustrates the variation of the filament current in relation to lamp power. It can be seen that the filament current variation range is not wide during the dimming operation due to the fact that the lamp voltage increases as lamp power is reduced. It also shows that the filament current increases with smaller Z_o. Z_o is chosen to be around 550 Ω to provide the recommended value.

To verify the preceding analysis, a prototype is built, in which the bus voltage is 410 V, full load switching frequency is 40 kHz and the resonant components L_r and C_r equal 1.56 mH and 5.6 nF, respectively. The characteristic impedance Z_o equals 528 Ω. The test results are shown in Figure 3-8. It can be seen that the experimental results agree closely with the theoretical prediction.

It should be noted that from the experimental observation, the striation phenomena occur when the lamp is dimmed to below about 10% of full output power. The mechanisms that cause striation are not completely understood, but a small DC current along the order of 1 mA could eliminate the striation effect [C21-23]. However, due to the symmetrical operation, no DC lamp current exists in the frequency control.

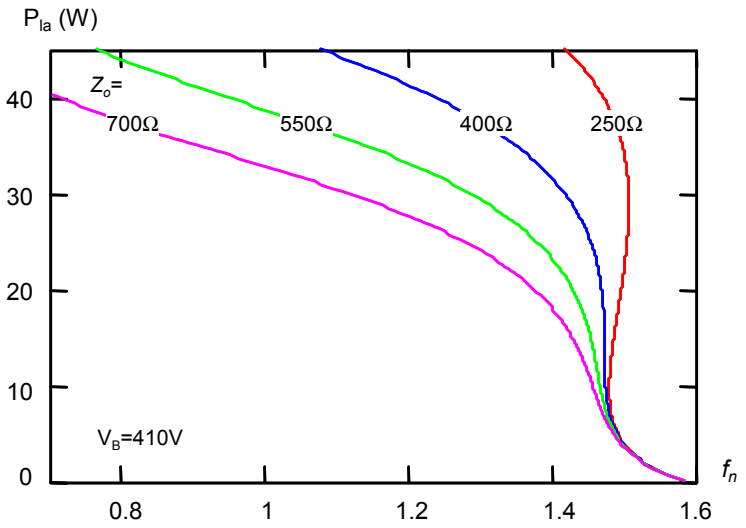


Figure 3-6. Lamp power versus switching frequency.

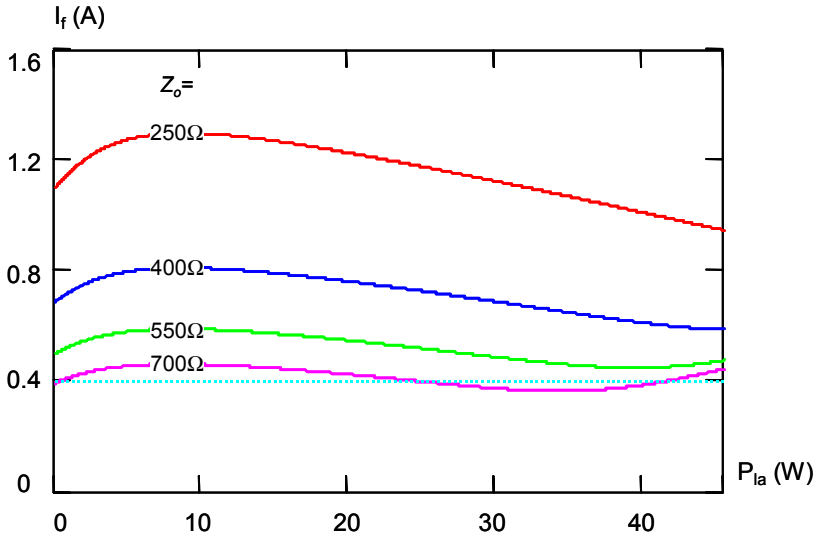


Figure 3-7. Filament current variation during dimming operation in frequency control.

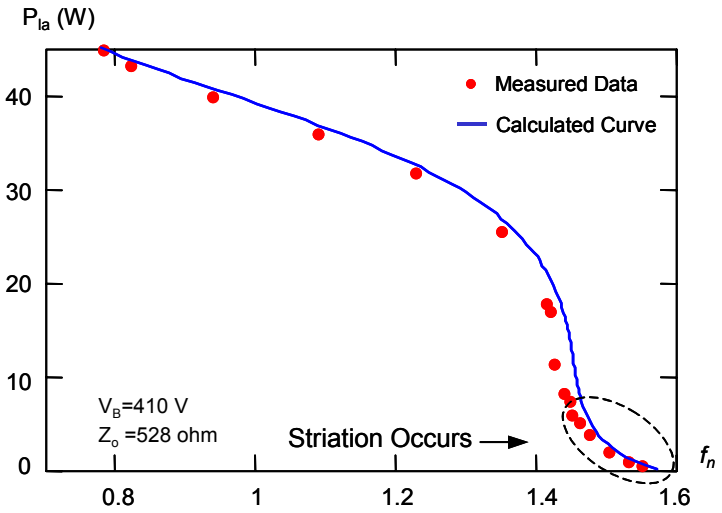


Figure 3-8. Experimental results of the lamp power versus switching frequency.

3.3.2 Bus Voltage Stress with Frequency Dimming Control

The dimming operation of the inverter stage is not independent in the single-stage PFC electronic ballast. The boundary condition between the PFC stage and inverter stage should be considered. Using equations derived in Section 3.3.1 and Chapter 2, the bus voltage stress with frequency dimming control is studied as follows.

A. Bus Voltage Stress in the Critical-Conduction-Mode PFC Electronic Ballast with Frequency Dimming Control

The average input power of the critical-conduction-mode electronic ballast is given by (2.12) and can be rewritten as

$$P_{in} = \frac{\pi V_p^2}{8 f_n \omega_o L_b}\left(\frac{1}{2} - \frac{4}{3\pi}\frac{V_p}{2V_B}\right). \tag{3.11}$$

Based on the power balance between the input and output,

$$P_{la} = \eta P_{in}, \tag{3.12}$$

where η is the conversion efficiency. The switching frequency f_n can be determined by

$$f_n = \frac{\eta}{P_{la}} \frac{\pi V_p^2}{8\omega_o L_b} \left(\frac{1}{2} - \frac{4}{3\pi} \frac{V_p}{2V_B} \right). \tag{3.13}$$

Substituting (3.13) into (3.8), the bus voltage is determined by

$$\frac{\eta}{P_{la}} \frac{\pi V_p^2}{8\omega_o L_b} \left(\frac{1}{2} - \frac{4}{3\pi} \frac{V_p}{2V_B} \right) = \sqrt{1 - \frac{1}{2}\left(\frac{Z_o}{R(P_{lp})} \right)^2 + \sqrt{\left[1 - \frac{1}{2}\left(\frac{Z_o}{R(P_{la})} \right)^2 \right]^2 - \left[1 - \left(\frac{\sqrt{2}V_B}{\pi V_{la}(P_{la})} \right)^2 \right]}}. \tag{3.14}$$

Obviously, (3.14) is complicated. It is hard to get a closed-form solution of V_B. Instead, a numerical solution of V_B can be obtained through Mathcad software. Figure 3-9 is the numerical curve obtained from (3.14), which shows that V_B increases as the lamp power is reduced. Since the bus voltage increases during the dimming operation, the sweeping range of the switching frequency becomes wider, as shown in Figure 3-10. If the bus voltage is limited to below 450 V, the dimming range is from full lamp power to about 62% of full power, which is too narrow to be practical.

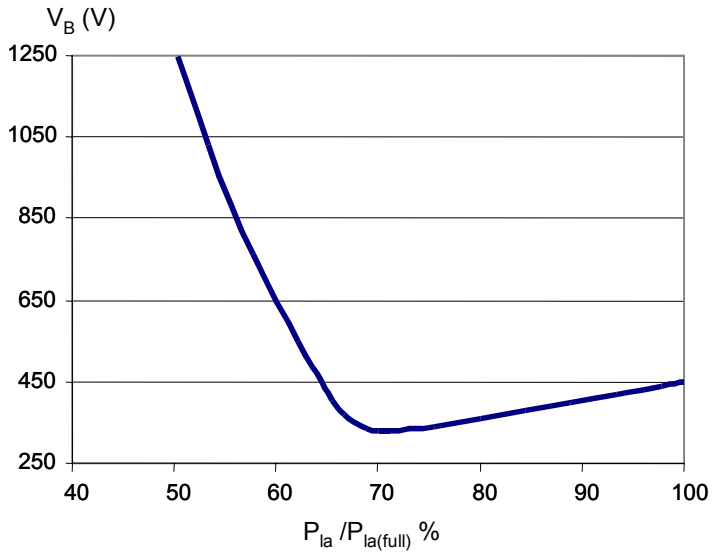


Figure 3-9. Calculated bus voltage of the critical-conduction-mode electronic ballast with frequency dimming control.

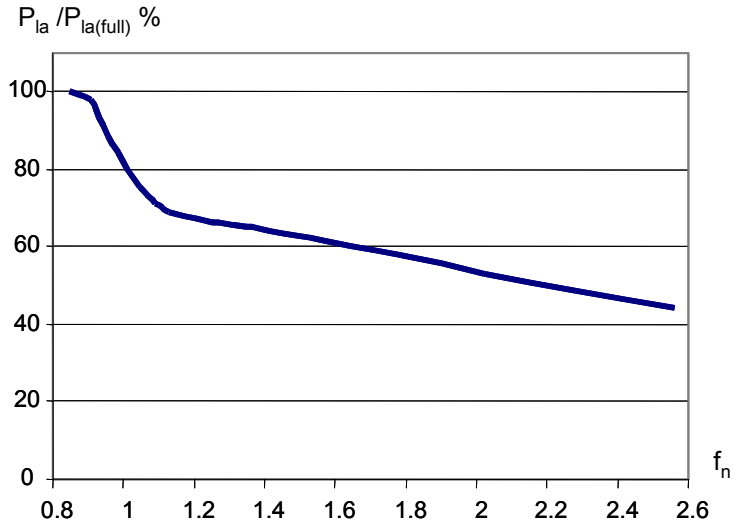


Figure 3-10. Lamp power versus switching frequency.

B. Bus Voltage Stress in the Interleaved PFC Electronic Ballast with Frequency Control

The average input power of the interleaved PFC electronic ballast is given by (2.43) and can be rewritten as

$$P_{in} = \frac{V_p^2}{8 f_n \omega_o L_b}\left(\int_0^{\pi} \frac{\sin^2\theta}{1 - V_p \sin\theta/(2V_B)} d\theta\right). \tag{3.15}$$

Based on the power balance between the input and output, or $P_{la} = \eta P_{in}$, the switching frequency f_n can be determined by

$$f_n = \frac{\eta}{P_{la}} \frac{V_p^2}{8\omega_o L_b}\left(\int_0^{\pi} \frac{\sin^2\theta}{1 - V_p \sin\theta/(2V_B)} d\theta\right). \tag{3.16}$$

Substituting (3.16) into (3.8), the bus voltage is determined by

$$\frac{\eta}{P_{la}} \frac{V_p^2}{8\omega_o L_b}\left(\int_0^{\pi} \frac{\sin^2\theta}{1 - V_p \sin\theta/(2V_B)} d\theta\right) = \sqrt{1 - \frac{1}{2}\left(\frac{Z_o}{R(P_{lp})}\right)^2} + \sqrt{\left[1 - \frac{1}{2}\left(\frac{Z_o}{R(P_{la})}\right)^2\right]^2 - \left[1 - \left(\frac{\sqrt{2}V_B}{\pi V_{la}(P_{la})}\right)^2\right]}. \tag{3.17}$$

It is also hard to get a closed-form solution of V_B from (3.17). However, a numerical solution can be used. Figure 3-11 shows the calculated V_B curve, and Figure 3-12 shows the control curve. It can be seen that V_B increases as the lamp power is reduced. If the upper limit of the bus voltage is set to be 450 V, the dimming range is from full lamp power to around 40% of full lamp power, which is still too narrow to be practical.

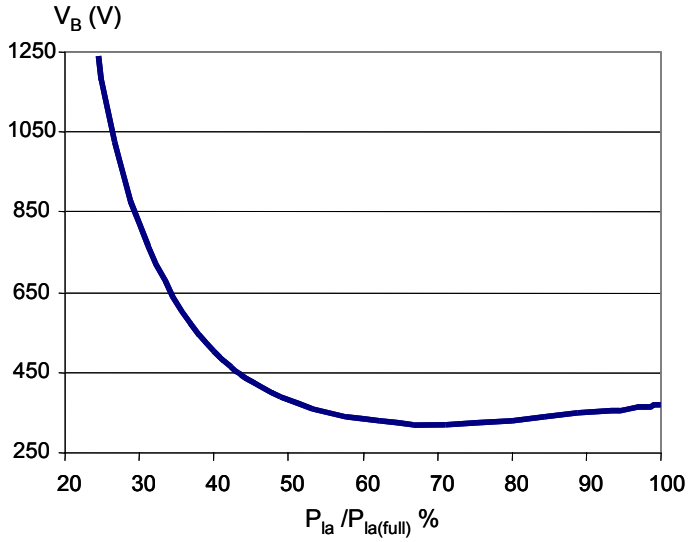


Figure 3-11. Calculated bus voltage of the interleaved electronic ballast with frequency dimming control.

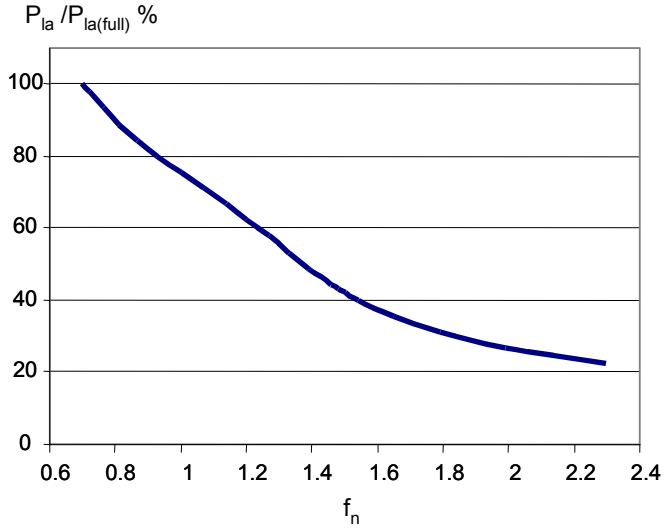


Figure 3-12. Lamp power versus switching frequency.

3.4 Study of Boost-Derived Single-Stage PFC Dimmable Electronic Ballasts with Asymmetrical Duty Ratio Control

Besides switching frequency control, duty ratio control is also usually employed to regulate output power in the resonant converters. Duty ratio control has the advantage of fixed-frequency operation, which can facilitate the design and utilization of magnetic components. Usually there are two types of duty ratio control: symmetrical and asymmetrical. However, the symmetrical duty ratio control was thought to be unsuitable for dimming operation due to the highly distorted output voltage in the half-bridge circuits [C16]. The asymmetrical duty ratio control is therefore studied.

3.4.1 Dimming Operation of the Inverter Stage with Asymmetrical Duty Ratio Control

The inverter stage under study is the same circuit as that shown in Figure 3-2(c). The duty ratios of two MOSFETs are controlled in a complementary manner, which is the so-called asymmetrical duty ratio control. Accordingly, the duty ratios of S_1 and S_2 are 1-D and D, respectively. By driving two MOSFETs asymmetrically, an asymmetrical square-wave voltage source with amplitudes of -(1-D)V_B and +DV_B is applied to the resonant circuit. Assume that only fundamental component is present in the resonant circuit. The RMS value of the fundamental component of V_{ab} is given by

$$V_{ab1} = \frac{\sqrt{2}V_B}{\pi}\sin(\pi D). \tag{3.18}$$

Substituting (3.18) into (3.7) yields

$$V_{la}(P_{la}) = \frac{\sqrt{2}V_B}{\pi}\sin(\pi D)\frac{1}{\sqrt{\left(1-f_n^2\right)^2+\left(\frac{f_n Z_o}{R_{la}(P_{la})}\right)^2}}. \tag{3.19}$$

From (3.19), the required duty ratio that gives the lamp power P_{la} is determined by

$$D(P_{la}) = \frac{1}{\pi}\arcsin\left[\frac{\sqrt{2}\pi\sqrt{\left(1-f_n^2\right)^2 + f_n^2\left(\frac{Z_o}{R_{la}(P_{la})}\right)^2}}{2V_B}V_{la}(P_{la})\right]. \qquad (3.20)$$

Therefore, using the lamp mode developed in (3.1) to (3.3), the relationship between the lamp power and the control parameter D can be obtained from (3.20) for a given bus voltage V_B, switching frequency f_n and circuit parameter Z_o. For V_B =410 V and f_n=1.08, P_{la}–D curves with different values of Z_o are calculated, as shown in Figure 3-13. It can be seen that the lamp power increases with duty ratio in a parabolic shape.

The variation of the filament current in relation to the lamp power can be determined by (3.10) since the switching frequency is fixed in the duty ratio control. Figure 3-14 shows the calculation results with f_n=1.08. It can be seen that the filament current remains almost constant during the dimming operation since the increase of the parallel capacitor current compensates for the loss of the "self-heating" current. To provide the recommended filament current value, a suitable Z_o is around 550 Ω.

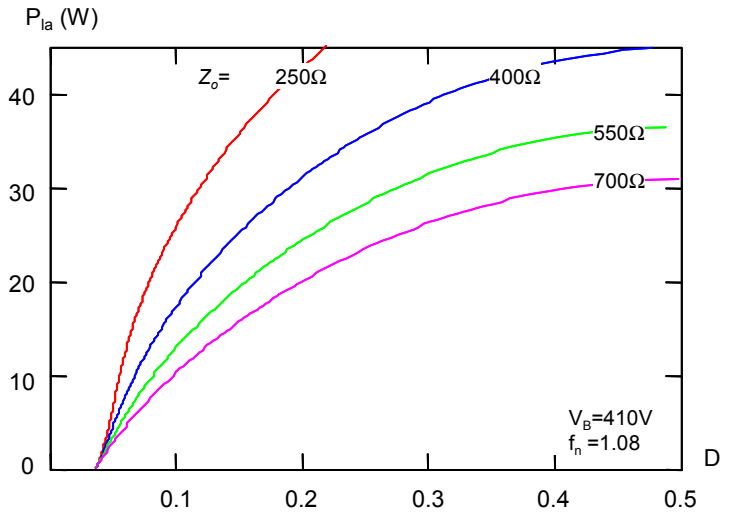


Figure 3-13. Lamp power versus duty ratio of S_2.

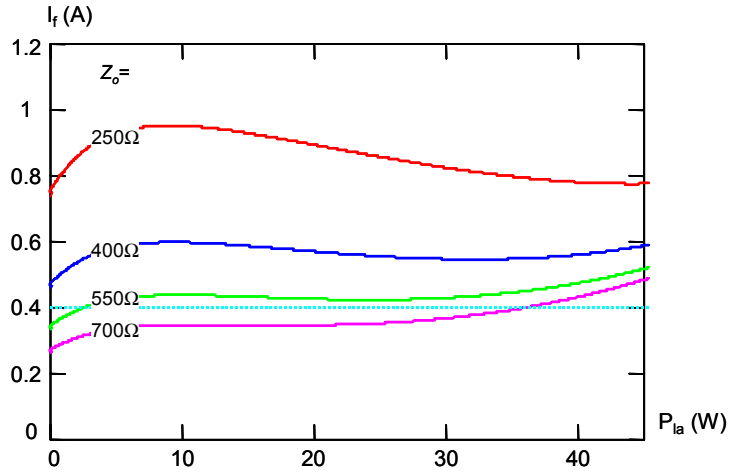


Figure 3-14. Filament current variation during dimming operation in duty ratio control.

Theoretically, the asymmetrical duty ratio control can achieve full-range dimming control if the duty ratio can arbitrarily be any value between zero and one. However, for the inverter in Figure 3-2(c), the maximum duty ratio is 0.5 and the minimum duty ratio is limited to preserve the ZVS operation of the MOSFETs. Figure 3-15 shows the waveforms of drain-source voltage v_{DS2}, resonant circuit input fundamental component v_{ab1} and resonant inductor current i_{Lr} at two different duty ratios. When the duty ratio of switch S_2 is set to be low in order to reduce lamp power, the prolonged conduction of S_1 may allow the resonant inductor current to resonate from positive into negative and flow through the body diode D_1 before switching off S_1. As a result, S_2 cannot be turned on with ZVS and suffers from the severe reverse-recovery-related problems of the body diode D_1. Therefore, the dimming range is limited by the ZVS operation of S_2.

To verify this analysis, a prototype with L_r=1.56 mH and C_r=5.6 nF is built. The bus voltage is 410 V and the switching frequency is 55 kHz. The experimental results are shown in Figure 3-16. It can be seen that the dimming range is limited by the minimum duty ratio, which is around 0.22 for this particular design.

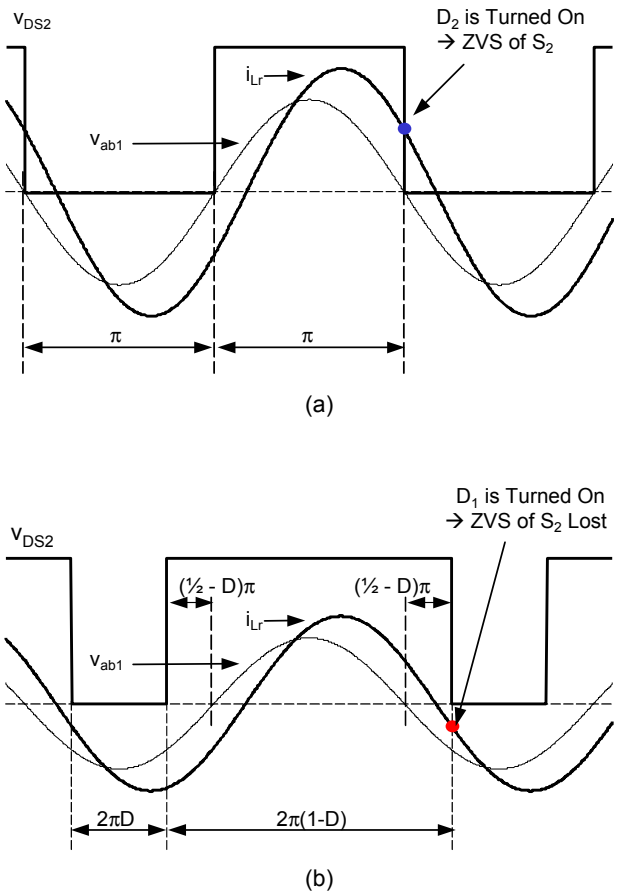


Figure 3-15. Waveforms of drain-source voltage v_{DS2}, resonant circuit input fundamental voltage v_{ab1} and resonant inductor current i_{Lr} at (a) D =0.5 and (b) D <0.5.

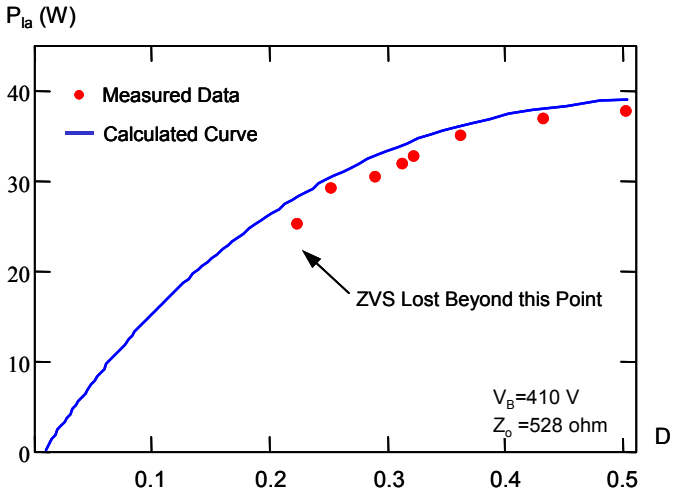


Figure 3-16. Experimental results of the lamp power versus duty ratio.

3.4.2 Development of Asymmetrical Duty-Ratio-Controlled Inverter with ZVS Operation

Wide-range dimming operation can potentially be achieved with asymmetrical duty ratio control if a suitable ZVS technique is employed. One ZVS approach is to add an inductive branch in parallel with the capacitive load so that the overall impedance becomes inductive [F21]. Figure 3-17(a) shows the circuit implementation. By properly sizing the inductance L_o, sufficient circulating current is generated for ZVS operation, as shown in Figure 3-17(b). This solution is simple and effective. It does not affect the characteristics of the original circuit. However, ZVS operation is achieved at the penalty of increasing the conduction losses. Actually, the derived circuit bears a resemblance to the well-known QSW buck DC/DC converter [F20]. Figure 3-17(c) shows the redrawn circuit diagrams of the derived circuit and the QSW buck converter if the resonant tank is regarded as an AC load. In DC/DC applications, the load requires a DC output voltage and the load is usually in parallel with the output capacitor. In ballast applications, on the other hand, the load requires an AC output voltage and the AC load can be in parallel with the inductor. Due to the volt-second balance on the inductor, no DC voltage component exists in the load. Based on this resemblance, a family of ZVS DC/AC inverters can be derived from their QSW DC/DC counterparts, as shown in Figure 3-18.

To understand the characteristics of the derived ZVS inverters, the voltage conversion gain is studied. For the derived inverters, the voltage conversion gain is defined as the fundamental component of output RMS voltage $v_{ab1(rms)}$ over $2/\pi$ times input voltage V_B. With the duty ratio D and voltage reference direction in Figure 3-18, two types of voltage gain exist as follows.

The type I inverter (for the buck-derived inverter) is

$$M_{V(I)} = \frac{v_{ab1(rms)}}{(2/\pi)V_B} = \sin(D\pi)\text{, and} \tag{3.21}$$

the type II inverter (for the rest of the inverters) is

$$M_{V(II)} = \frac{v_{ab1(rms)}}{(2/\pi)V_B} = \frac{\sin(D\pi)}{1-D} \approx 4D\,. \tag{3.22}$$

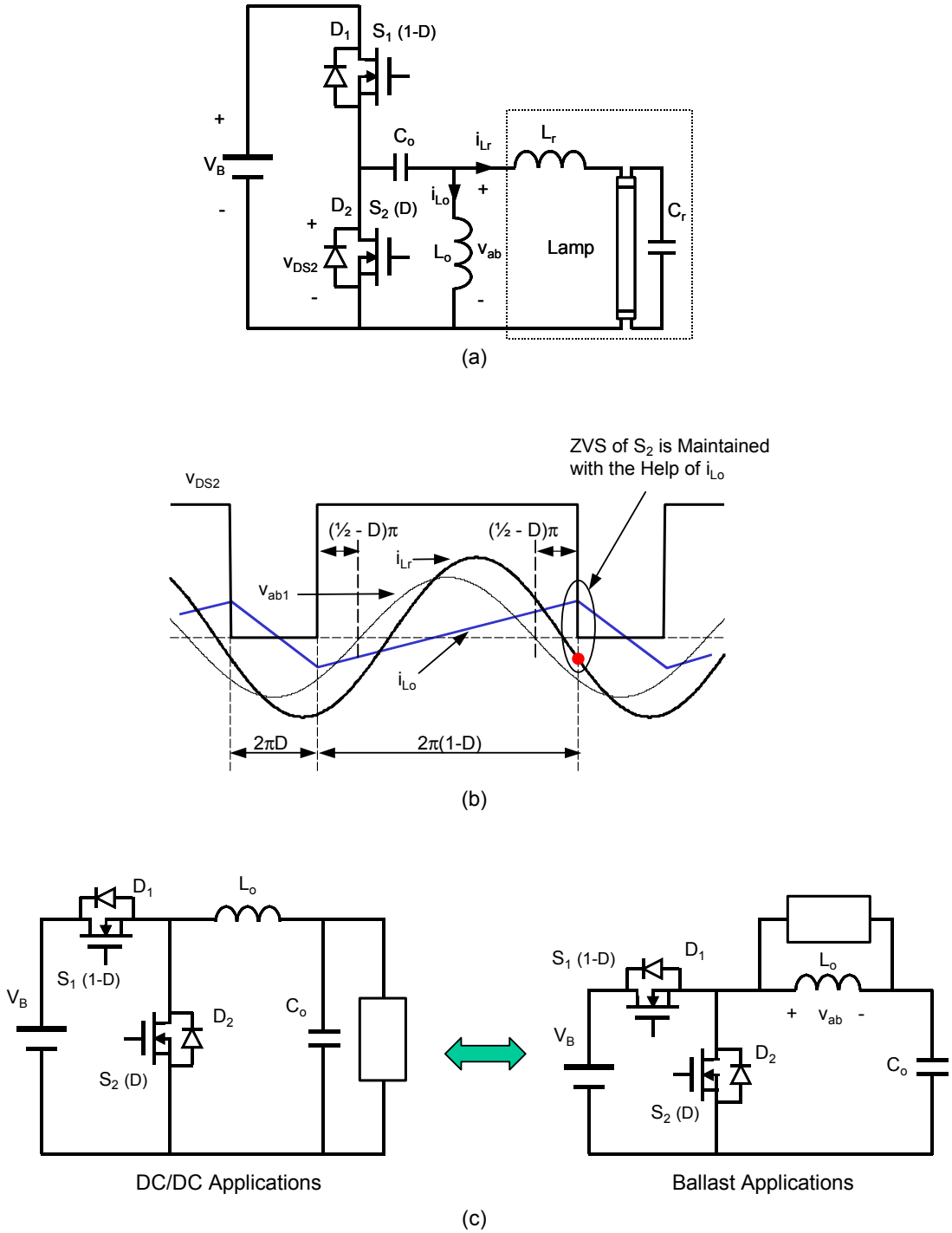
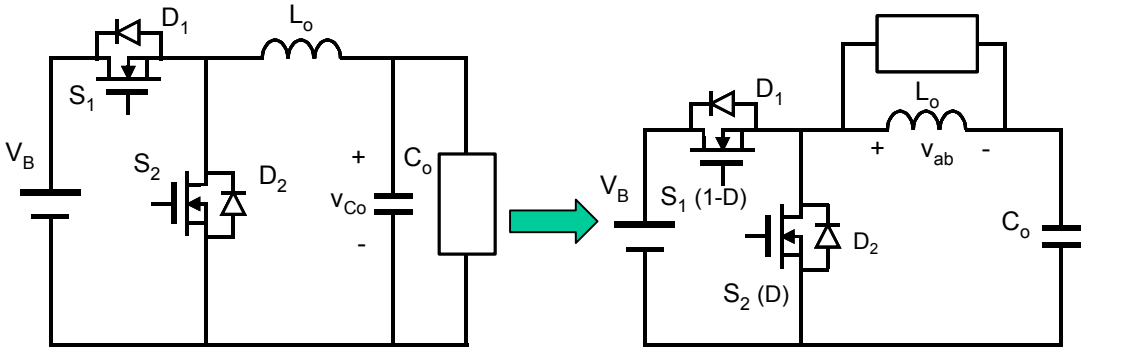
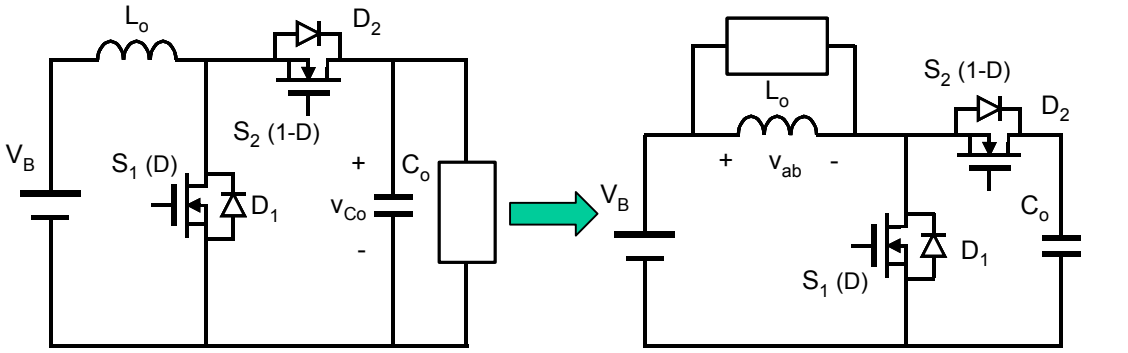


Figure 3-17. (a) The inverter stage of Figure 3-2(c) with inductor L_o; (b) waveforms of drain-source voltage v_{DS2}, inductor L_o fundamental voltage v_{ab1}, resonant inductor current i_{Lr} and inductor current i_{Lo} at D <0.5; and (c) circuit diagrams of QSW buck converter and the derived ZVS inverter.



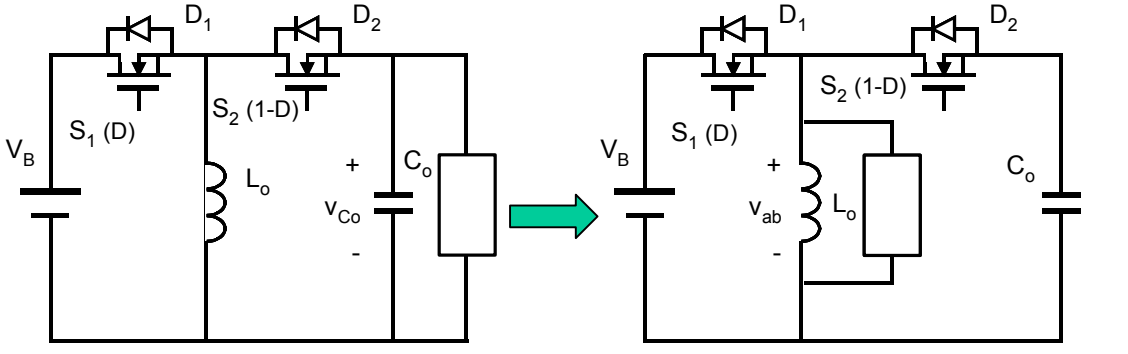
$0 \le t \le DT_s$: $v_{ab} = -(1-D)V_B$, $DT_s \le t \le (1-D)T_s$: $v_{ab} = DV_B$

(a)



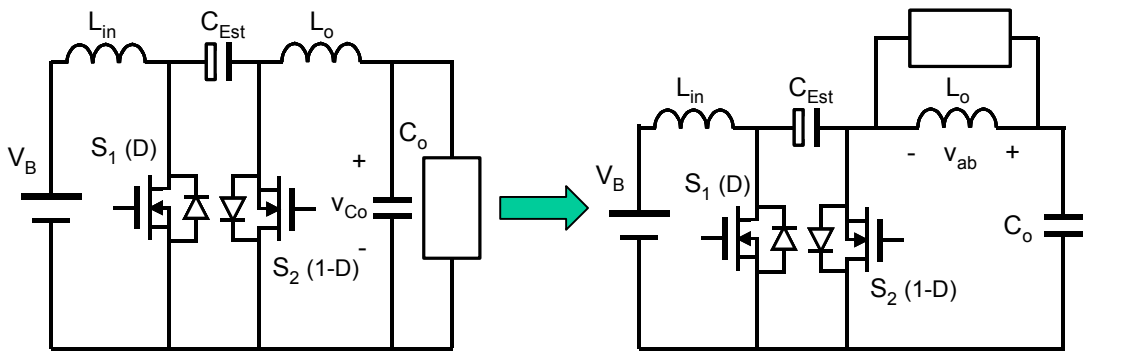
$0 \le t \le DT_s$: $v_{ab} = V_B$, $DT_s \le t \le (1-D)T_s$: $v_{ab} = -DV_B/(1-D)$

(b)



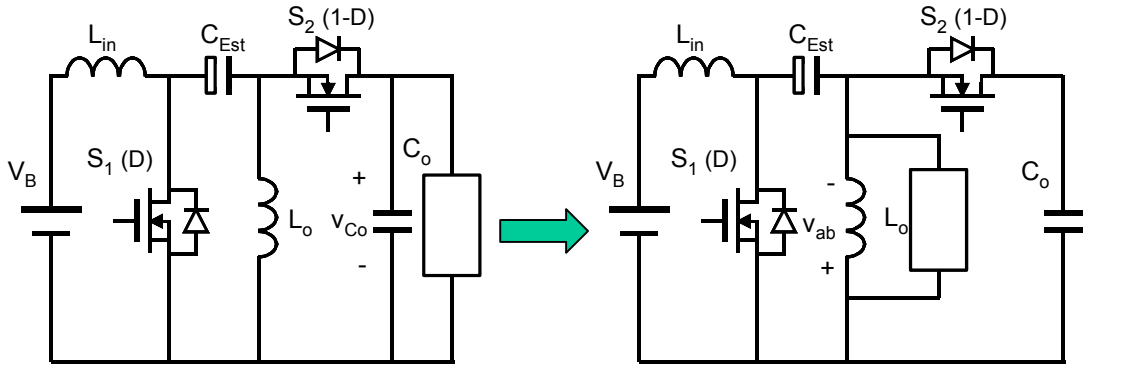
$0 \le t \le DT_s$: $v_{ab} = V_B$, $DT_s \le t \le (1-D)T_s$: $v_{ab} = -DV_B/(1-D)$

(c)



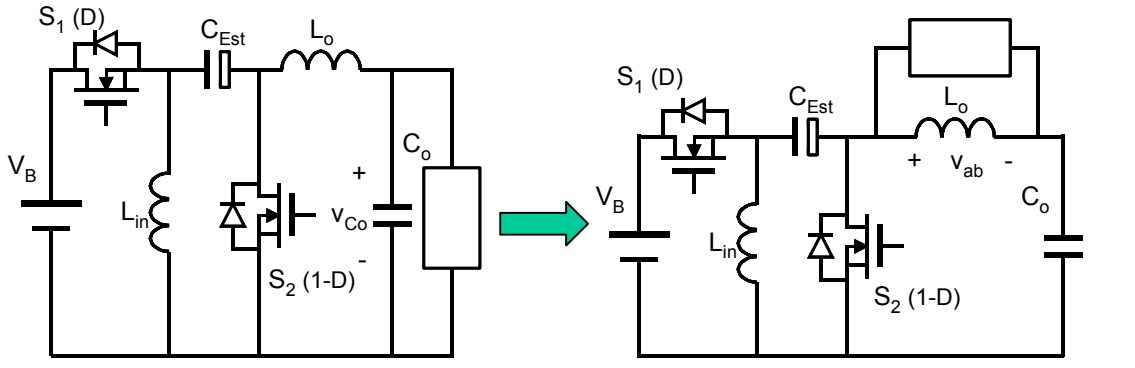
$0 \le t \le DT_s$: $v_{ab} = V_B$, $DT_s \le t \le (1-D)T_s$: $v_{ab} = -DV_B/(1-D)$

(d)



$0 \le t \le DT_s$: $v_{ab} = V_B$, $DT_s \le t \le (1-D)T_s$: $v_{ab} = -DV_B/(1-D)$

(e)



$0 \le t \le DT_s$: $v_{ab} = V_B$, $DT_s \le t \le (1-D)T_s$: $v_{ab} = -DV_B/(1-D)$

(f)

Figure 3-18 Derivation of a family of ZVS inverters: (a) QSW buck converter and QSW buck-derived inverter, (b) QSW boost converter and QSW boost-derived inverter, (c) QSW buck/boost converter and QSW buck/boost-derived inverter, (d) QSW cuk converter and QSW cuk-derived inverter, (e) QSW sepic converter and QSW sepic-derived inverter, and (f) QSW zeta converter and QSW zeta-derived inverter.

Figure 3-19 shows the voltage conversion gain curves as a function of duty ratio. It can be seen that the gain of the type I inverter shows a parabolic shape and the gains of the type II inverters show an almost linear curve over a wide range of D. Therefore, type II inverters have a wider control range than type I inverters.

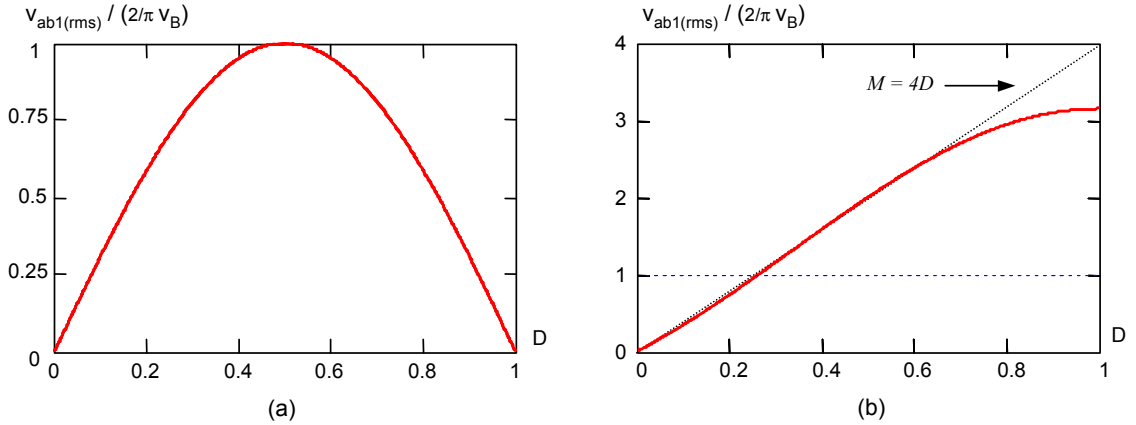


Figure 3-19. Voltage gains of the derived inverters as a function of duty ratio: (a) for type I inverter, and (b) for type II inverters.

3.4.3 Zero-Voltage-Switching Condition

Theoretically, ZVS operation of the derived inverters can always be fulfilled if the inductance L_o is arbitrarily small. However, a smaller inductance induces a larger circulating current, which increases conduction losses and may cause thermal problems. One good approach is to use the maximum inductance that can achieve ZVS operation for the required dimming range. The maximum inductance allowed is called the critical inductance $L_{o(crit)}$. By using the developed lamp model, $L_{o(crit)}$ can be derived as follows.

Figure 3-20 shows the circuit diagram and key waveforms of the buck-derived inverter, in which MOSFET output capacitances are not neglected. To achieve ZVS, S_1 or S_2 should be switched on while its corresponding anti-parallel body diode is conducting. In other words, C_{ds1} and C_{ds2} should be completely discharged by (i_{Lo}+i_{Lr}) before the gate voltage is applied to the respective MOSFET, and the gate voltage should be applied to

the corresponding MOSFET before (i_{Lo}+i_{Lr}) changes the polarity. There are dead-time boundaries for gate voltages. Assume the T_c is the MOSFET output capacitance discharging time period and that T_x is the time period from which the switch is turned off to the instant at which (i_{Lo}+i_{Lr}) changes the polarity. Therefore, the ZVS condition is given by

$$T_c \le t_d \le T_x, \tag{3.23}$$

where t_d is the dead time between the application of gate voltages to S_1 and S_2. As derived later, T_c and T_x are functions of L_o. $L_{o(crit)}$ is determined when $T_x = T_c$.

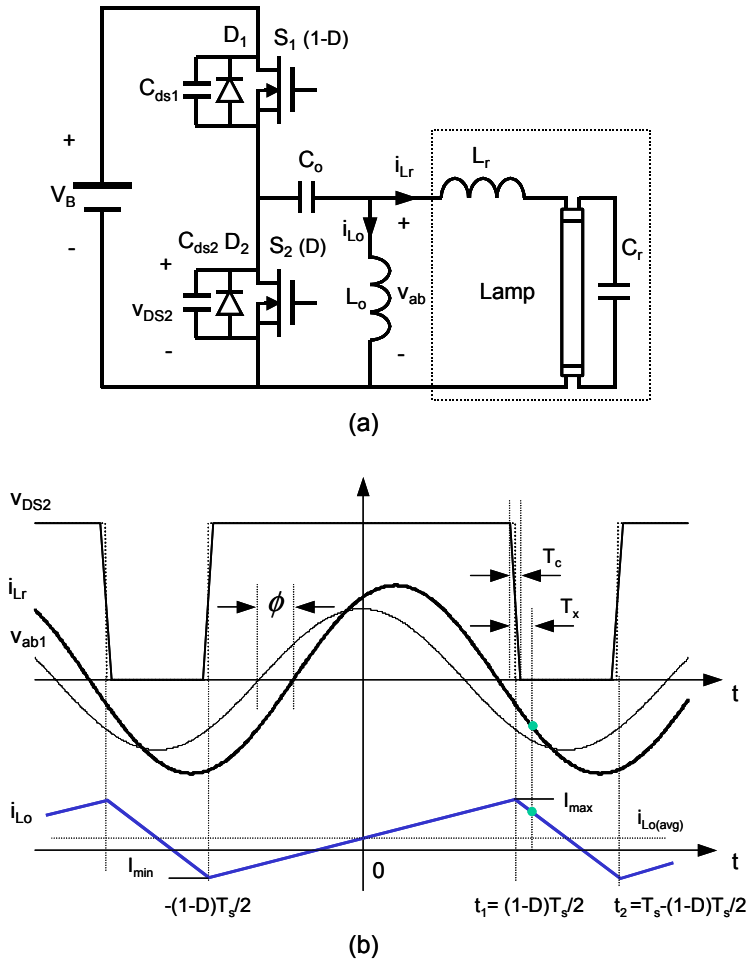


Figure 3-20. (a) Circuit diagram of ZVS buck-derived inverter showing reference directions of currents and voltages, and (b) key waveforms.

From the waveforms in Figure 3-20, the fundamental component of output voltage v_{ab1} and the resonant inductor current i_{Lr} can be expressed by

$$v_{ab1} = \frac{\sqrt{2}V_B}{\pi}\sin(D\pi)\cos(\omega_s t), \text{ and} \tag{3.24}$$

$$i_{Lr}(t) = I_m \cos(\omega_s t - \phi), \tag{3.25}$$

where I_m and ϕ are the magnitude of the resonant current and phase lag of i_{Lr} with respect to v_{ab1}, respectively. From Figure 3-5, I_m and ϕ can be expressed as a function of lamp power P_{la} when the lamp power-dependent model is used, as follows:

$$I_m(P_{la}) = \sqrt{2}\sqrt{I_{la}(P_{la})^2 + I_c^2} = \frac{\sqrt{2}V_{la}(P_{la})}{R_{la}(P_{la})}\sqrt{1+\left(\frac{f_n}{Z_o}R_{la}(P_{la})\right)^2}, \text{ and} \tag{3.26}$$

$$\phi(P_{la}) = \arccos\frac{1}{\sqrt{1+\left[\frac{R_{la}(P_{la})}{Z_o}f_n\left(f_n^2+\left(\frac{Z_o}{R_{la}(P_{la})}\right)^2-1\right)\right]^2}}. \tag{3.27}$$

Unlike i_{Lr}, inductor current i_{Lo} changes linearly in two subintervals, as shown in Figure 3-20. During the first subinterval, with the on-period of S_1, i_{Lo} is given by

$$i_{Lo}(t) = I_{\min} + \frac{DV_B}{L_o}\left(t + \frac{1-D}{2}T_s\right), \quad t \in \left[-\frac{1-D}{2}T_s, \frac{1-D}{2}T_s\right), \tag{3.28}$$

where I_{min} is the minimum value of i_{Lo}. During the second subinterval, with the on-period of S_2, i_{Lo} is given by

$$i_{Lo}(t) = I_{\max} - \frac{(1-D)V_B}{L_o}\left(t - \frac{1-D}{2}T_s\right), \; t \in \left[\frac{1-D}{2}T_s, T_s - \frac{1-D}{2}T_s\right), \tag{3.29}$$

where I_{max} is the maximum value of i_{Lo}, which is given by

$$I_{\max} = I_{\min} + \frac{D(1-D)V_B}{L_o}T_s. \tag{3.30}$$

The average DC-link current $i_{dc(avg)}$ is determined by

$$i_{dc(avg)} = \frac{P_{in}}{V_B} = \frac{1}{T_s}\int_{-\frac{1-D}{2}T_s}^{T_s-\frac{1-D}{2}T_s} i_{dc}(t)dt = \frac{1}{T_s}\int_{-\frac{1-D}{2}T_s}^{\frac{1-D}{2}T_s}\left(i_{Lo}(t)+i_{Lr}(t)\right)dt$$

$$= (1-D)i_{Lo(avg)} + \frac{I_m}{\pi}\sin(D\pi)\cos\phi\,. \tag{3.31}$$

Based on the power balance between the input and output, the average inductor current $i_{Lo(avg)}$ is determined by

$$i_{Lo(avg)} = \frac{P_{la}}{(1-D)\eta_i V_B} - \frac{I_m}{(1-D)\pi}\sin(D\pi)\cos\phi\,, \tag{3.32}$$

where η_i is the conversion efficiency of the inverter stage.

By noting that $I_{\min} + I_{\max} = 2i_{Lo(avg)}$, and considering (3.30), one obtains

$$I_{\min} = \frac{P_{la}}{(1-D)\eta_i V_B} - \frac{I_m}{(1-D)\pi}\sin(D\pi)\cos\phi - \frac{D(1-D)V_B}{2L_o}T_s\,, \text{ and} \tag{3.33}$$

$$I_{\max} = \frac{P_{la}}{(1-D)\eta_i V_B} - \frac{I_m}{(1-D)\pi}\sin(D\pi)\cos\phi + \frac{D(1-D)V_B}{2L_o}T_s\,. \tag{3.34}$$

Using the derived I_{max}, time intervals T_c and T_x can be determined as follows.

Let Q_c be the amount of charge stored in the output capacitances, which is given by

$$Q_C = (C_{ds1} + C_{ds2})V_B\,. \tag{3.35}$$

During period T_c, the amount of charge Q_L that is extracted by (i_{Lo}+i_{Lr})

$$Q_L = \int_{\frac{1-D}{2}T_s-\frac{1}{2}T_c}^{\frac{1-D}{2}T_s+\frac{1}{2}T_c}\left(i_{Lo}(t)+i_{Lr}(t)\right)dt\,, \tag{3.36}$$

which can be simplified; since T_c<<T_s, then

$$Q_L \approx [I_{\max} + I_m\cos((1-D)\pi-\phi)]T_c\,. \tag{3.37}$$

Applying Q_L =Q_c leads to

$$T_c = \frac{(C_{ds1}+C_{ds2})V_B}{I_{\max} + I_m\cos((1-D)\pi-\phi)}\,. \tag{3.38}$$

Referring to the waveforms in Figure 3-20, T_x is determined from the following equation:

$$I_{\max} - \frac{(1-D)V_B}{L_o} T_x + I_m \cos\left[\omega_s\left(\frac{1-D}{2}T_s + T_x\right) - \phi\right] = 0. \tag{3.39}$$

Considering $\cos(x) \approx \frac{\pi}{2} - x$, when x is close to $\frac{\pi}{2}$, T_x is obtained as

$$T_x \approx \frac{I_{\max} + I_m[\phi - (1-D)\pi/2]}{(1-D)V_B/L_o + I_m\omega_s}. \tag{3.40}$$

Figure 3-21 shows the dead-time boundaries with respect to the lamp power P_{la} when L_o =0.5 mH. It can be seen that the critical inductance is around 0.5 mH for the full dimming range. Figures 3-22(a) and (b) show the measured switching waveforms with maximum duty ratio D =0.5 and minimum duty ratio D =0.1, respectively. ZVS operation is maintained within this range. Figure 3-23 shows the measured lamp power versus duty ratio. Compared with the results shown in Figure 3-16, the dimming range is greatly expanded. However, due to the minimum dead-time limit, the controllable duty ratio of S_2 cannot be arbitrarily small. From the experimental results, the minimum controllable duty ratio is around 0.04, which corresponds to an effective duty ratio of 0.1. The measured dimming range is around 5:1, far from the required 100:1.

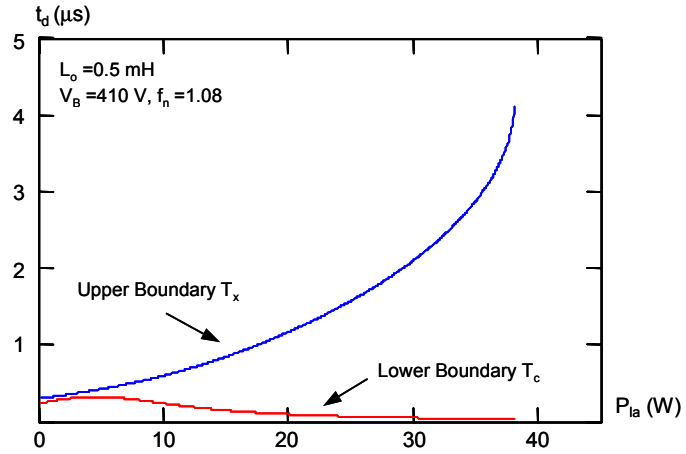


Figure 3-21. Dead-time boundaries for ZVS of buck-derived inverter.

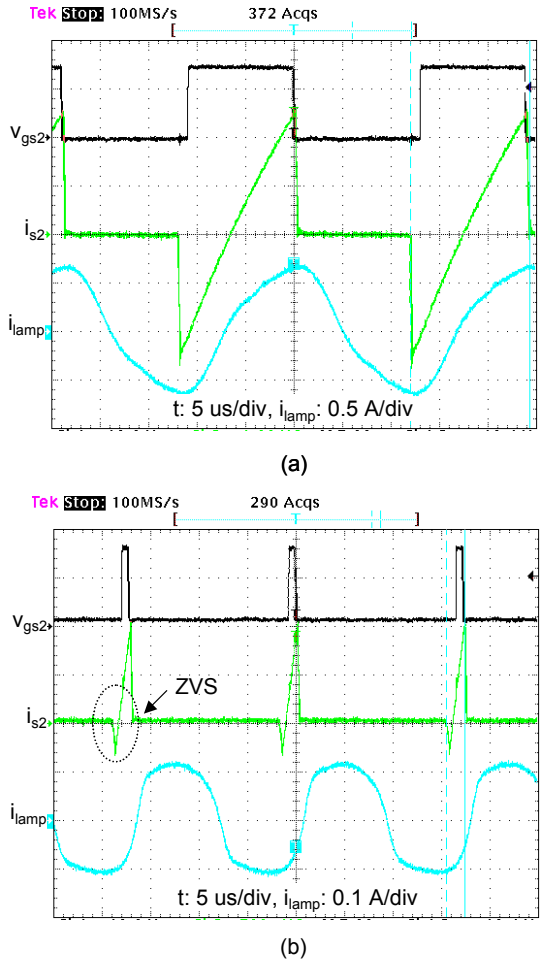


Figure 3-22. Measured switching current waveforms of ZVS buck-derived inverter at two different duty ratios, (a) D =0.5, and (b) D =0.1.

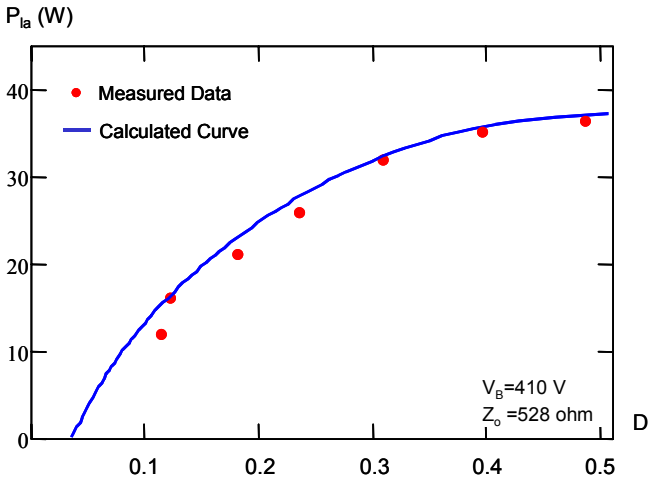


Figure 3-23. Experimental results of lamp power versus duty ratio.

From the analysis given in Section 3.4.2, type II inverters exhibit better voltage conversion gain than does the buck-derived inverter. It is possible to achieve wide-range dimming control for type II inverters. Since buck/boost-derived inverter is relatively simple, the dimming operation is studied as follows.

Referring to the circuit diagram in Figure 3-18(c), one obtains

$$v_{ab} = \begin{cases} V_B & t \in [0, DT_s) \\ -DV_B/(1-D) & t \in [DT_s, T_s) \end{cases}. \tag{3.41}$$

Therefore, the RMS value of the fundamental component of v_{ab} equals

$$V_{ab1} = \frac{\sqrt{2}V_B}{\pi}\frac{\sin(\pi D)}{1-D} \approx \frac{\sqrt{2}V_B}{\pi}4D\,. \tag{3.42}$$

Substituting (3.42) into (3.7) leads to

$$D(P_{la}) = \frac{\sqrt{2}\pi\sqrt{(1-f_n^2)^2 + f_n^2\left(\frac{Z_o}{R_{la}(P_{la})}\right)^2}}{8V_B}V_{la}(P_{la})\,. \tag{3.43}$$

Therefore, for the given bus voltage V_B, switching frequency f_n and circuit parameter Z_o, the required duty ratio that gives the lamp power P_{la} can be calculated from (3.43). The calculated P_{la}–D curves with different values of Z_o are shown in Figure 3-24. The minimum duty ratio required is increased to around 0.1. It should be noted that the bus voltage is adjusted to be 160 V since the circuit operation is different from that of the buck-derived inverter. The switch voltage stress becomes $V_B/(1-D)$.

The derivation of ZVS condition is similar to that of the buck-derived inverter. The major results are given by

$$T_c = \frac{(C_{ds1}+C_{ds2})V_B/(1-D)}{I_m\sin[\phi-(1-2D)\pi/2]-I_{\min}}, \text{ and} \tag{3.44}$$

$$T_x = \frac{I_m[\phi-(1-D)\pi/2]-I_{\min}}{V_B/L_o + I_m\omega_s}, \tag{3.45}$$

where I_m is given by (3.26), ϕ is given by (3.27), and I_{min} is given by

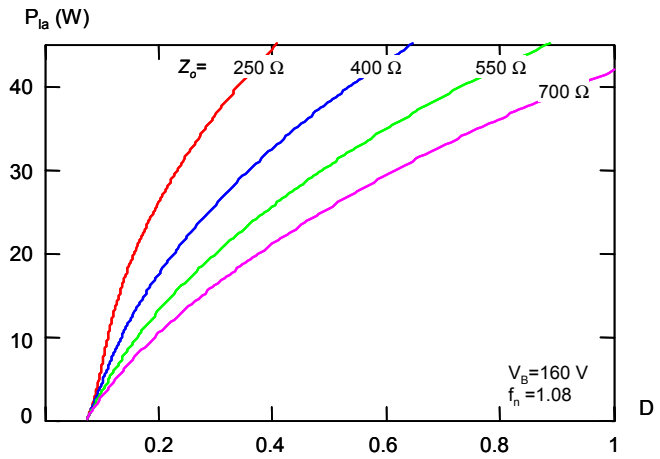


Figure 3-24. Calculated lamp power versus duty ratio with different values of Z_o.

$$I_{\min} = \frac{P_o}{D\eta V_B} - \frac{I_m}{D\pi}\sin(\pi D)\cos\phi - \frac{V_B}{2L_o}DT_s . \tag{3.46}$$

Figure 3-25 shows the dead-time boundaries with respect to the lamp power. The critical inductance is around 0.7 mH.

To verify the calculation results, a circuit prototype is built and tested with the same resonant tank. Figure 3-26 shows the measured lamp power versus duty ratio. It can be seen that the dimming range is expanded to almost the full range. From the experiments, another phenomenon is observed. A small amount of DC current, which helps to prevent the development of striation, appears in the lamp current. The magnitude of the DC current increases as the lamp power is reduced, which helps to maintain lamp life and eliminate lamp striation. Figures 3-27(a) and (b) show the measured lamp current waveforms at 70% and 4% of full lamp power, respectively. Obviously, the lamp current becomes asymmetrical with asymmetrical driving voltage. From the experimental observation, the striations do not occur until the lamp is dimmed to about 0.3% of full lamp power. Excellent dimming performance is achieved with the help of the DC current.

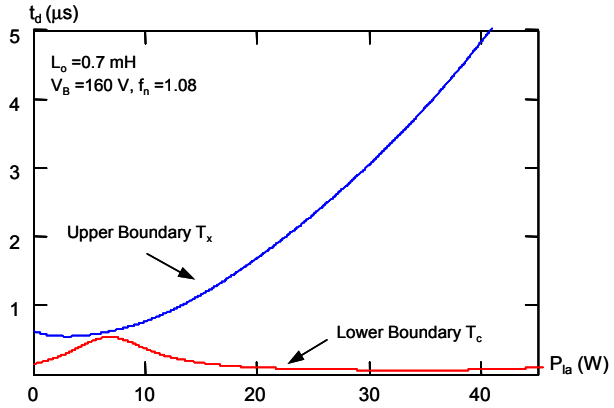


Figure 3-25. Dead-time boundaries for ZVS of buck/boost-derived inverter.

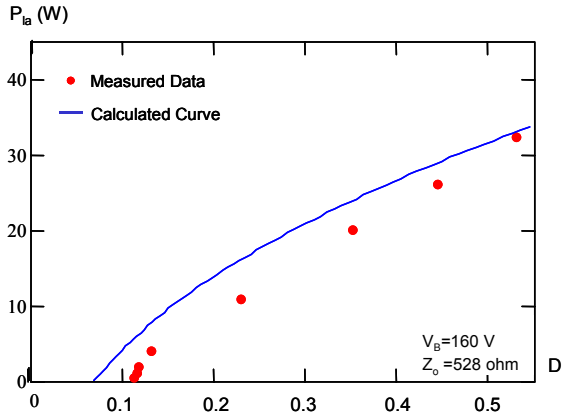


Figure 3-26. Experimental results of lamp power versus duty ratio.

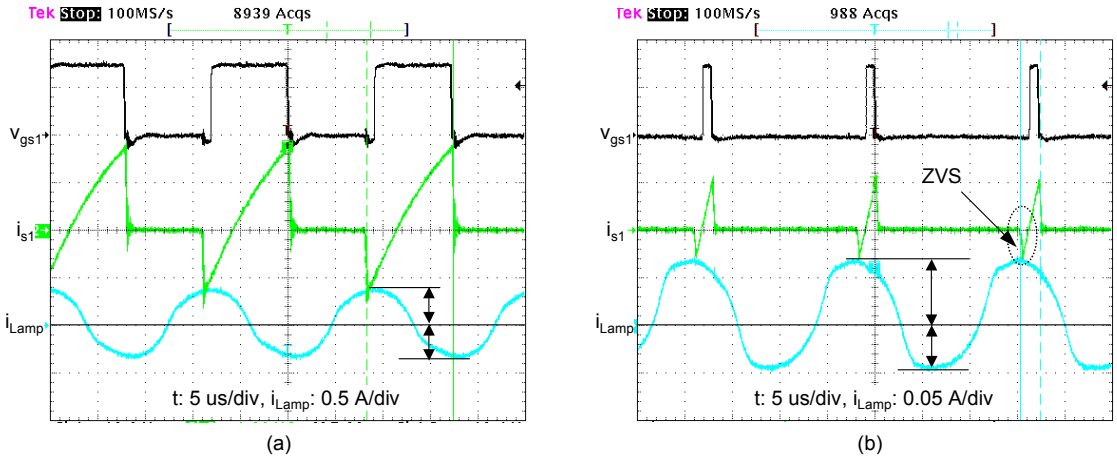


Figure 3-27. Measured lamp current waveforms showing a small amount of DC current in the lamp: (a) 70% of full lamp power, and (b) 4% of full lamp power.

3.4.4 Bus Voltage Stress with Asymmetrical Duty Ratio Control

During dimming operations, the bus voltage is the result of the interaction between the PFC stage and the inverter stage. The characteristics of an inverter stage with asymmetrical duty ratio control are studied in Section 3.4.3. The characteristics of the critical-conduction-mode PFC stage and interleaved PFC stage with asymmetrical duty ratio control are studied as follows.

The equations of average input power for two PFC stages are derived in Chapter 2 under the condition of D =0.5. However, the input current waveforms change with the duty ratio. Figure 3-28 shows the boost inductor current waveform of the critical-conduction-mode PFC circuit when D <0.5. From the waveform in Figure 3-28, the average line current and average input power can be respectively derived as

$$I_{p1} = \frac{\frac{1}{2}V_{in(rec)}}{L_b}\left(DT_s - t_{d1}\right) = \frac{V_B - \frac{1}{2}V_{in(rec)}}{L_b}t_{d2}, \text{ and} \tag{3.47}$$

$$I_{p2} = \frac{\frac{1}{2}V_{in(rec)}}{L_b}\left(D' - t_{d2}\right) = \frac{V_B - \frac{1}{2}V_{in(rec)}}{L_b}t_{d1}. \tag{3.48}$$

From (3.47) and (3.48), I_{p1}, I_{p2}, t_{d1} and t_{d2} can be obtained as

$$I_{p1} = \frac{\pi V_p}{\omega_s L_b}\frac{D - \alpha_{eff}\left|\sin\omega_l t\right|}{1 - 2\alpha_{eff}\left|\sin\omega_l t\right|}\left(1 - \alpha_{eff}\left|\sin\omega_l t\right|\right)\left|\sin\omega_l t\right|, \tag{3.49}$$

$$I_{p2} = \frac{\pi V_p}{\omega_s L_b}\frac{D' - \alpha_{eff}\left|\sin\omega_l t\right|}{1 - 2\alpha_{eff}\left|\sin\omega_l t\right|}\left(1 - \alpha_{eff}\left|\sin\omega_l t\right|\right)\left|\sin\omega_l t\right|, \tag{3.50}$$

$$t_{d1} = \frac{D' - \alpha_{eff}\left|\sin\omega_l t\right|}{1 - 2\alpha_{eff}\left|\sin\omega_l t\right|}\alpha_{eff}\left|\sin\omega_l t\right|T_s, \text{ and} \tag{3.51}$$

$$t_{d2} = \frac{D - \alpha_{eff}\left|\sin\omega_l t\right|}{1 - 2\alpha_{eff}\left|\sin\omega_l t\right|}\alpha_{eff}\left|\sin\omega_l t\right|T_s. \tag{3.52}$$

Therefore, the line input current and average line power are determined by

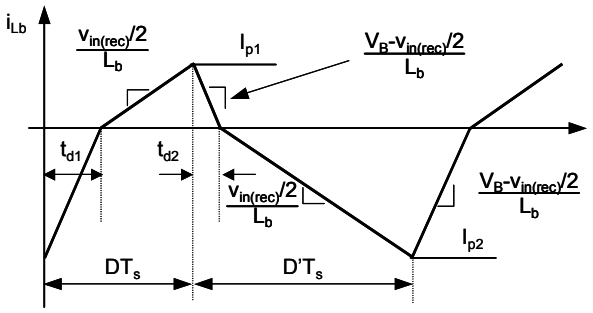


Figure 3-28. Boost induction current waveforms of the critical-conduction-mode PFC electronic ballast operating in asymmetrical duty ratio control.

$$i_{in} = \left\langle \frac{1}{2} i_{Lb} \right\rangle = \frac{\pi V_p}{8\omega_s L_b}\left(1-\alpha_{eff}\left|\sin\omega_l t\right|\right)\left[1+\frac{4(D-0.5)^2}{\left(1-2\alpha_{eff}\left|\sin\omega_l t\right|\right)^2}\right]\sin\omega_l t \text{ , and} \qquad (3.53)$$

$$P_{in} = \frac{\pi V_p^2}{8\omega_s L_b}\left[y_1 + 4y_2(D-0.5)^2\right], \qquad (3.54)$$

where $y_1 = \frac{1}{2} - \frac{4}{3\pi}\alpha_{eff}$, and (3.55)

$$y_2 = \frac{1}{\pi}\int_0^{\pi} \frac{\left(1-\alpha_{eff}\sin\theta\right)\sin^2\theta}{\left(1-2\alpha_{eff}\sin\theta\right)^2} d\theta \,. \qquad (3.56)$$

Equation (3.54) shows that the input power increases with the decrease of duty ratio, which makes the bus voltage even higher than the frequency control. Therefore, the critical-conduction-mode electronic ballast, which is proposed in Chapter 2 for non-dimming applications, is not suitable for dimming operation.

Similar characteristics can be found in the interleaved electronic ballast. Figure 3-29 shows the boost inductor current waveform with an asymmetrical duty ratio. From the waveform, the line input current and input real power become

$$\begin{aligned} i_g &= \frac{\pi V_p}{4\omega_s L_b}\left[D^2 + D'^2\right]\frac{1}{1-\alpha_{eff}\left|\sin\omega_l t\right|}\sin\omega_l t \\ &= \frac{\pi V_p}{8\omega_s L_b}\left[4(D-0.5)^2+1\right]\frac{1}{1-\alpha_{eff}\left|\sin\omega_l t\right|}\sin\omega_l t \text{ , and} \end{aligned} \qquad (3.57)$$

$$P_{in} = \frac{\pi V_p^2}{8\omega_s L_b} y\left[4(D-0.5)^2 + 1\right], \tag{3.58}$$

where $$y = -\frac{2}{\pi\alpha_{eff}} - \frac{1}{\alpha_{eff}^2} + \frac{2}{\alpha_{eff}^2\sqrt{1-\alpha_{eff}^2}}\left[\frac{1}{2} - \frac{1}{\pi}\tan^{-1}\left(\frac{-\alpha_{eff}}{\sqrt{1-\alpha_{eff}^2}}\right)\right]. \tag{3.59}$$

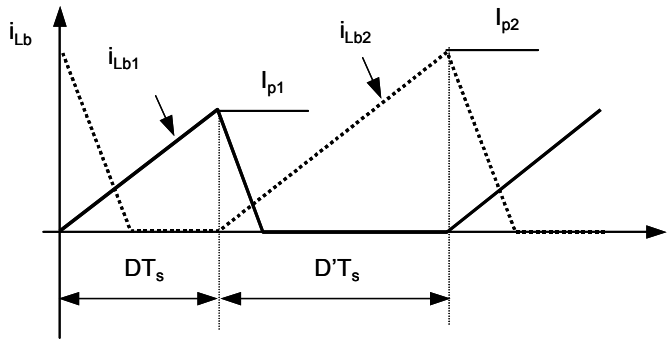


Figure 3-29. Boost inductor current waveforms of interleaved PFC electronic ballast operating in asymmetrical duty ratio control.

From the preceding study, it can be concluded that the critical-conduction-mode and interleaved PFC electronic ballasts are not suitable for asymmetrical duty ratio control due to their symmetrical structures. The conventional DCM boost PFC stage, on the other hand, becomes attractive for asymmetrical duty ratio applications. Since the duty ratio is not limited to be 0.5 in the asymmetrical duty ratio applications, there is a tradeoff between the full-load bus voltage and the dimming range. Therefore, a new family of single-stage PFC circuits is derived, which integrates the DCM boost PFC stage with the ZVS inverters of Section 3.4.2, as shown in Figure 3-30. It should be noted that since there are two inductors and an energy-storage-transfer capacitor in the cuk-derived and sepic-derived ZVS inverters, the corresponding PFC circuits are derived by utilizing the input inductor as the PFC inductor and the energy-storage-transfer capacitor as the DC-link capacitor. Thus, the cuk-derived PFC circuit is degraded to the DCM boost PFC stage plus the buck-derived inverter, while the sepic-derived PFC circuit is degraded to the DCM boost PFC stage plus the buck/boost-derived inverter.

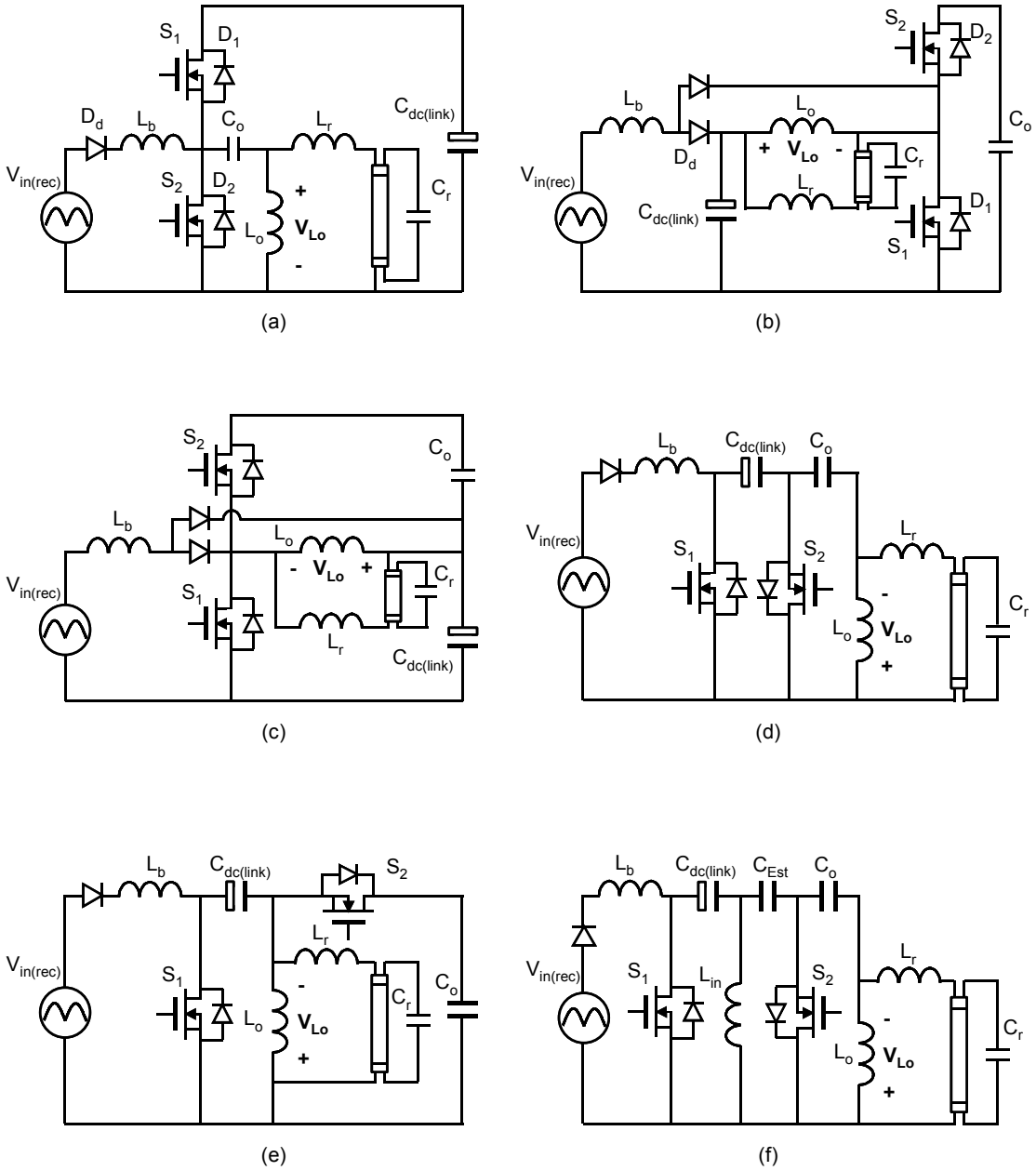


Figure 3-30. A family of dimmable single-stage PFC electronic ballasts with asymmetrical duty ratio control: (a) DCM boost PFC + ZVS buck-derived inverter, (b) DCM boost PFC + ZVS boost-derived inverter, (c) DCM boost PFC + ZVS buck/boost-derived inverter, (d) ZVS cuk-based circuit, (e) ZVS sepic-based circuit, and (f) DCM boost PFC + ZVS zeta-derived inverter.

From the analysis given in Section 3.4.2, type II inverters are more suitable for wide-range dimming operations. Therefore, the PFC circuits shown in Figure 3-30(a) and (d) (based on the buck-derived inverter) are not considered. Since the zeta-derived circuit of Figure 3-30(f) has many more components than the other three circuits, it is ruled out from consideration. Among the remaining three circuits, the PFC circuit of Figure 3-30(e) (ZVS sepic-based) has the simplest topology. Therefore, the sepic-based PFC electronic ballast is selected as the proposed dimmable electronic ballast.

The average input power of the DCM boost PFC stage is given as follows from previous work [B25]:

$$P_{in} = \frac{D^2 V_p^2}{\omega_s L_b}\left(\int_0^{\pi} \frac{\sin^2\theta}{1 - V_p \sin\theta / V_B} d\theta\right). \tag{3.60}$$

Based on the power balance between the input and output, or $P_{la} = \eta P_{in}$, the duty ratio D can be determined by

$$D = \sqrt{\frac{P_{la}\omega_s L_b}{\eta V_p^2 \int_0^{\pi} \frac{\sin^2\theta}{1 - V_p \sin\theta / V_B} d\theta}}. \tag{3.61}$$

The duty ratio D can also be expressed from the inverter stage. It should be noted that the input voltage of the inverter stage is the DC-link voltage. The relationship between the bus voltage and the DC-link voltage $V_{dc(link)}$ is given by

$$V_B = V_{dc(link)} + V_{Co} = \frac{1}{1 - D} V_{dc(link)}. \tag{3.62}$$

From (3.43), the duty ratio D is determined by

$$D = \frac{\sqrt{2}\pi \sqrt{\left(1 - f_n^2\right)^2 + f_n^2 \left(\frac{Z_o}{R_{la}(P_{la})}\right)^2}}{8 V_B (1 - D)} V_{la}(P_{la}). \tag{3.63}$$

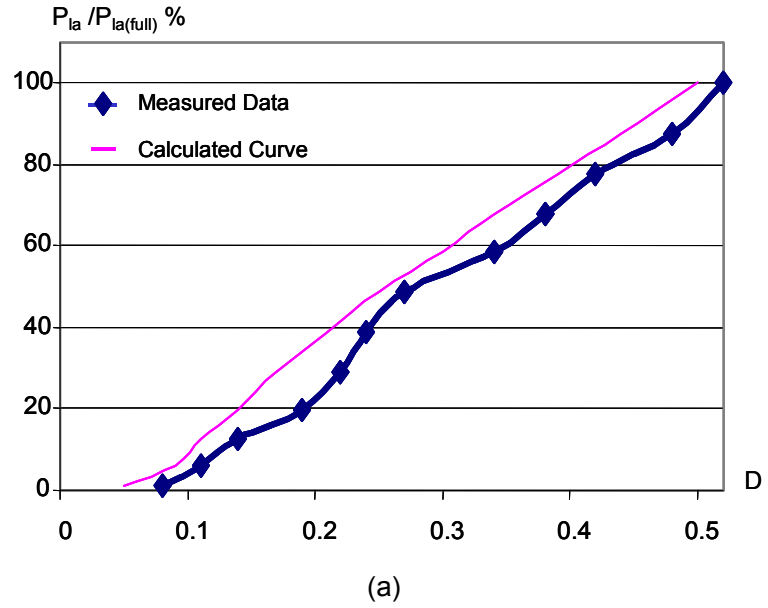
Therefore, the numerical solutions of V_B and D can be obtained from (3.61) and (3.63) for a given lamp power P_{la}. The calculation results are shown in Figure 3-31. It can be seen that no bus voltage stress occurs during the dimming operation.

3.4.5 Experimental Results

To verify the analysis results, a sepic-based electronic ballast is implemented with the following parameters:

L_r =1.56 mH, C_r =5.6 nF, L_b =1.14 mH, L_o =0.7 mH, and C_o =0.33 μF

The electronic ballast operates a 32watt lamp with $110V_{rms}$ line input. The experimental results are shown in Figures 3-31 to 3-33. It can be seen that the experimental results agree closely with the theoretical predictions. Dimming operation from 32 W to 0.1 W was obtained by controlling the duty ratio from 0.52 to 0.06. In this dimming range, no striation or flickering is observed, and the circuit meets the IEC 1000-3-2 Class C regulation. The measured maximum bus voltage and DC-link voltage are lower than 400 V and 210 V, respectively so that 500V-rating MOSFETs can be used as switches, and a 250V-rating electrolytic capacitor can be used as the DC-link capacitor, which reduces the cost. The proposed circuit is shown to be a good alternative for electronic ballasts with wide-range dimming controls.



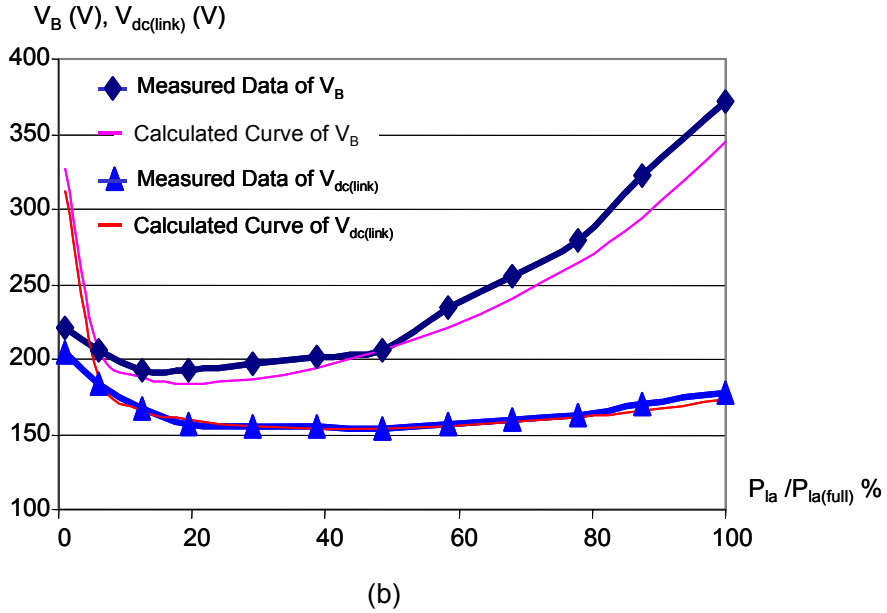


Figure 3-31. (a) Measured and calculated lamp power versus duty ratio, and (b) measured and calculated bus voltage and DC-link voltage during dimming operation.

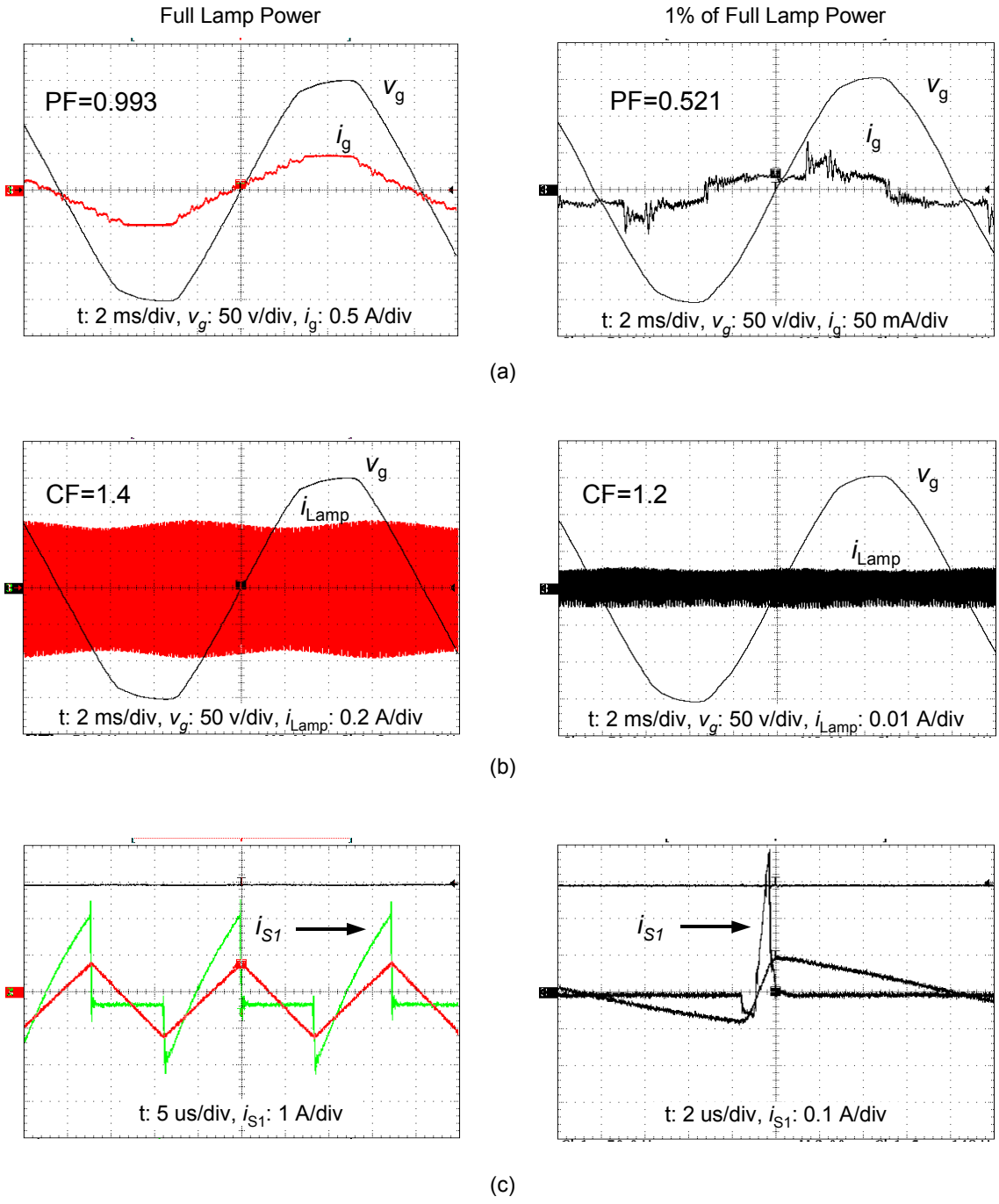
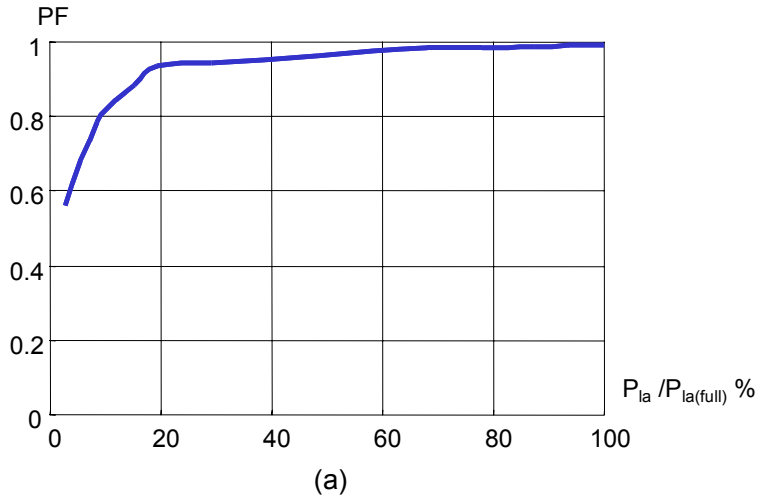
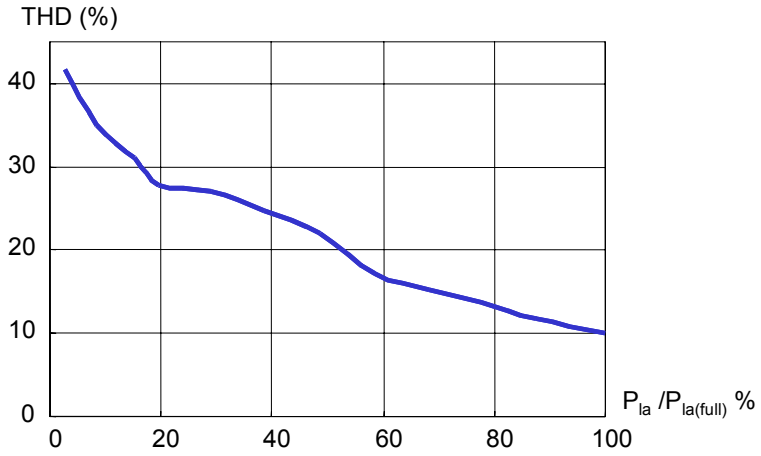


Figure 3-32. Measured waveforms at two different lamp power levels (full, left; 1%, right): (a) input line current waveforms, (b) lamp current waveforms, and (c) switch waveforms.



(a)



(b)

Figure 3-33. (a) Measured PF and (b) THD during dimming operations.

3.4. Summary

The dimming operation of a family of boost-derived single-stage PFC electronic ballasts is studied in this chapter.

To describe the electrical behavior of fluorescent lamps operating in dimming modes, a simple power-dependent lamp model is developed. Based on this model, circuit equations are derived to predict the dimming operation of the ballast-lamp circuit. Study shows that switching-frequency-controlled boost-derived single-stage PFC electronic ballasts are not suitable for wide-range dimming applications due to the high bus voltage stress.

To achieve a wide range of dimming control, asymmetrical duty-ratio-controlled single-stage PFC electronic ballasts are developed. By adjusting the duty ratio, the lamp power can be effectively controlled over a wide range. ZVS can be retained on the MOSFETs by integrating the resonant converter with QSW DC/DC converter into one stage. Moreover, a small amount of DC-biased current is naturally injected into the lamp, which effectively eliminates the striations from the lamp and expands the stable dimming range.

Based on the different control characteristics, the proposed circuits can be categorized into two types: type I with a parabolic control curve, and type II with an almost linear control curve. Experimental results show that the sepic-based single-stage PFC dimmable electronic ballast (type II circuit) performs satisfactorily with good PF, low harmonic distortion, low bus voltage stress and wide dimming range.

Untill now, the studied single-stage PFC electronic ballasts integrate the DCM boost converter with the inverter. The boost inductor is necessary. The next chapter will study another family of PFC circuits, the CPPFC electronic ballasts, in which the PFC inductor is eliminated.

Chapter 4 Single-Stage Charge-Pump Power-Factor-Correction Electronic Ballasts

4.1 Introduction

Boost-derived single-stage PFC electronic ballasts have been studied. In the boost-derived PFC circuits, an inductor is used in series with the line input terminal through the diode rectifier to shape the line-input current waveform to meet the harmonic regulations. Figure 4-1(a) shows the basic circuit diagram [B24]. Using the dither-rectifier concept introduced by I. Takahashi, et al. [B7], a conceptual boost-derived PFC circuit is obtained, as shown in Figure 4-1(b). Based on the study of J. Zhang, et al. [B37], the unity PF condition is given by

$$d_{Dither} = 1 - V_p \left|\sin \omega_l t\right| + \frac{2L_b P_{in}}{V_p} \frac{d}{dt}\left(\left|\sin \omega_l t\right|\right), \tag{4.1}$$

where d_{Dither} is the duty ratio of the dither voltage waveform.

The dual element of an inductor is a capacitor. There is another family of single-stage PFC electronic ballasts called CPPFC electronic ballasts, which utilize a capacitor to shape the line-input current waveform. Figure 4-2(a) shows the basic circuit diagram [D2]. From it, a conceptual circuit can be obtained, as shown in Figure 4-2(b). As derived next, the unity PF condition is given by

$$I_s = \pi C_{in} f_s V_B, \tag{4.2}$$

where I_s is the magnitude of the charge-pump current waveform.

Since the CPPFC technique eliminates the use of boost inductor, this chapter will focus on the study and development of single-stage CPPFC electronic ballasts.

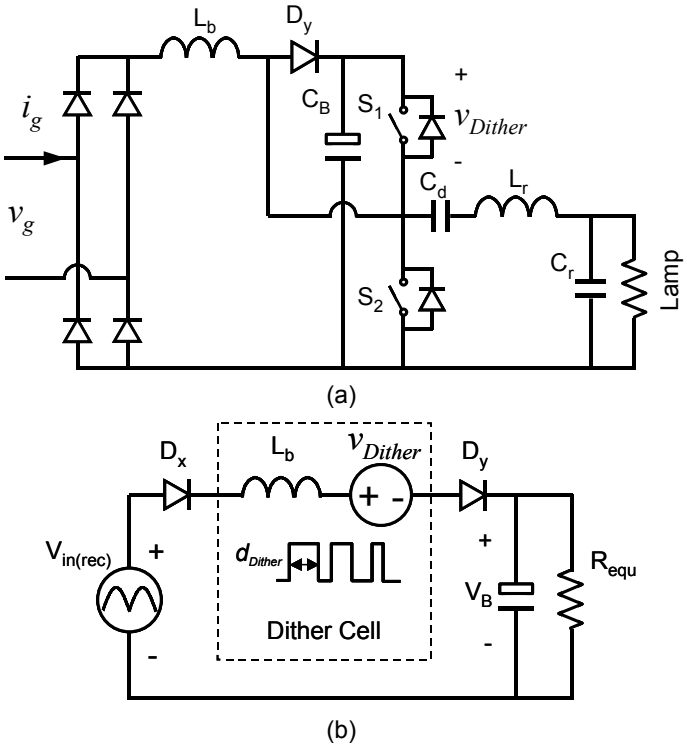


Figure 4-1. (a) Basic boost PFC electronic ballast [B24], and (b) conceptual circuit diagram.

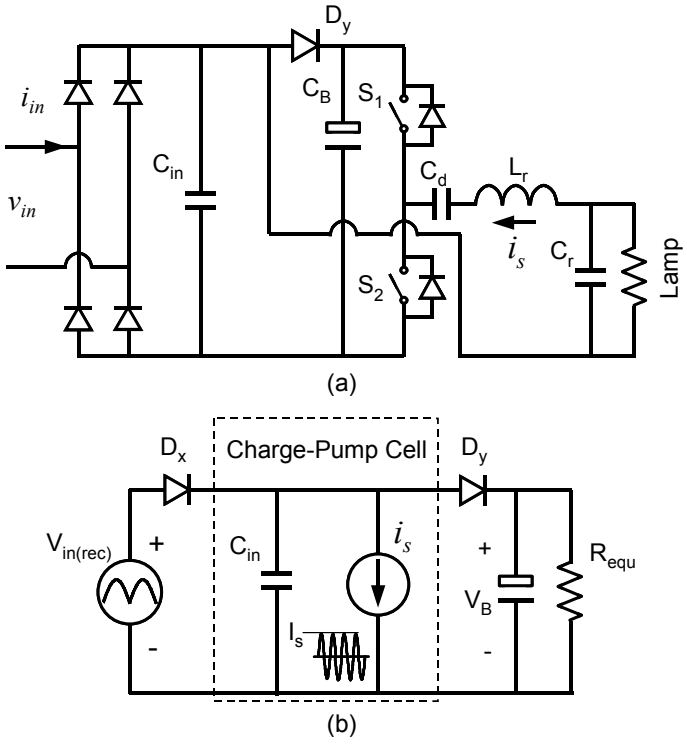


Figure 4-2. (a) Basic CPPFC electronic ballast [D2], and (b) conceptual circuit diagram.

4.2 Analysis of a Family of Single-Stage CPPFC Electronic Ballasts

A family of single-stage CPPFC electronic ballasts has been previously proposed [D1-D21]. However, the diversity of circuit topologies and interrelated operations of the charge-pump capacitor with the resonant components complicate the circuit evaluation. To better understand the CPPFC mechanism and evaluate the performance, three basic and two improved topologies are studied in this section. Based on the analysis, a new, improved topology is derived in the next section.

4.2.1 Analysis of CS-CPPFC Electronic Ballasts

The circuit shown in Figure 4-2 is called the basic current source (CS) CPPFC electronic ballast since a high-frequency CS i_s is used to charge C_{in} to absorb energy from the line input and discharge C_{in} to pump energy to the bus capacitor C_B.

A. Circuit Operation Principle

The series-resonant parallel-loaded tank in Figure 4-2(a) can be considered as a high-frequency current source. The circuit diagram can be redrawn, as shown in Figure 4-3(a). Using fundamental approximation, six topological stages exist over one switching cycle in steady state, as shown in Figure 4-3(b). Figure 4-3(c) shows key switching waveforms.

Stage 1 [t_0, t_1]: Before t_0, i_s has a negative value and flows through S_2 and D_y. The voltage at node m is clamped to the bus voltage V_B. At t_0, i_s becomes positive and starts to discharge C_{in}, resulting in the decrease of v_m. This stage ends when v_m decreases to the rectified line-input voltage, and D_x is turned on. The time interval τ and charge variation ΔQ of C_{in} are given by

$$\tau = \frac{1}{\omega_s}\arccos\left[1 - \frac{\omega_s C_{in}}{I_s}\left(V_B - v_{in(rec)}\right)\right], \tag{4.3}$$

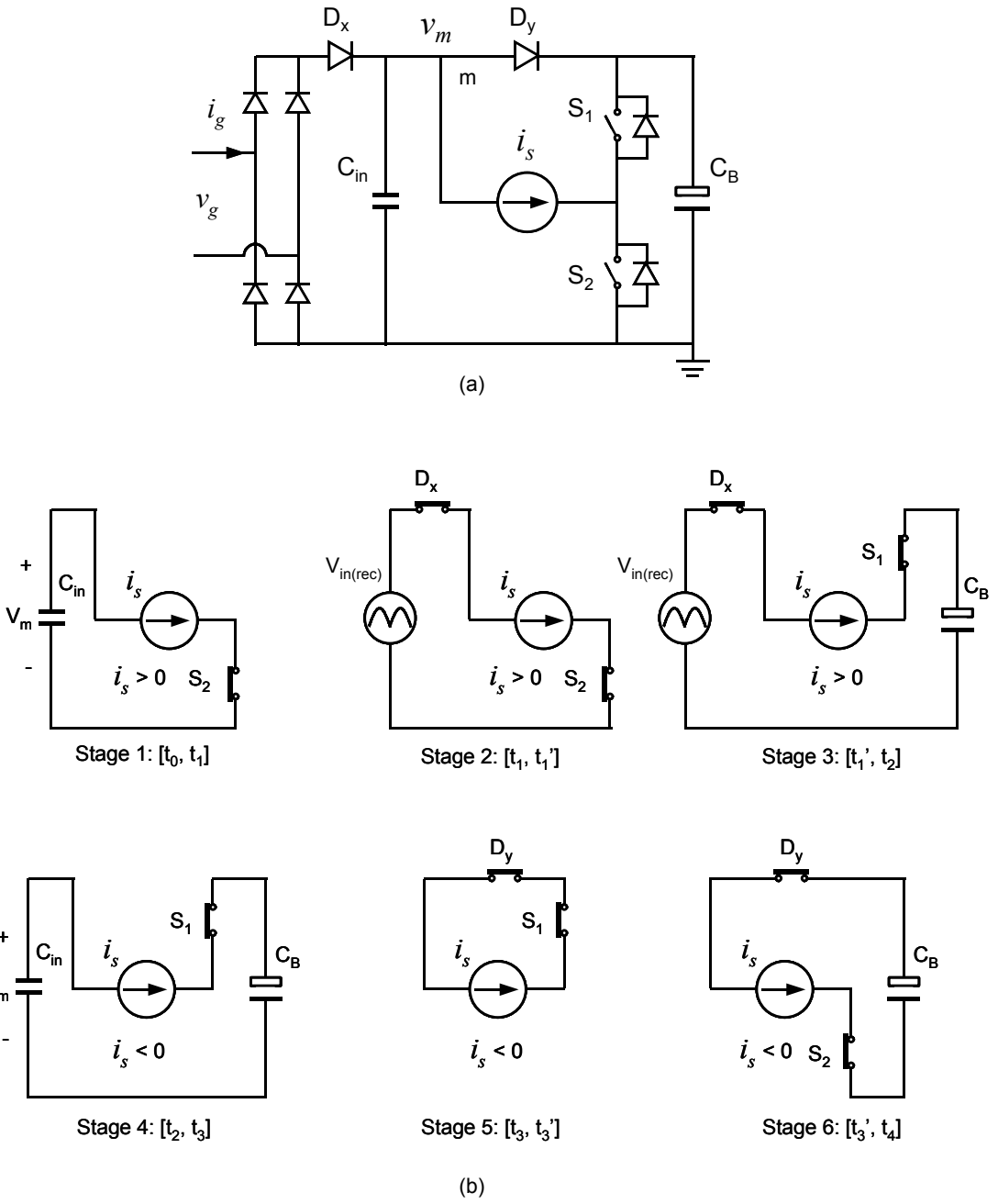
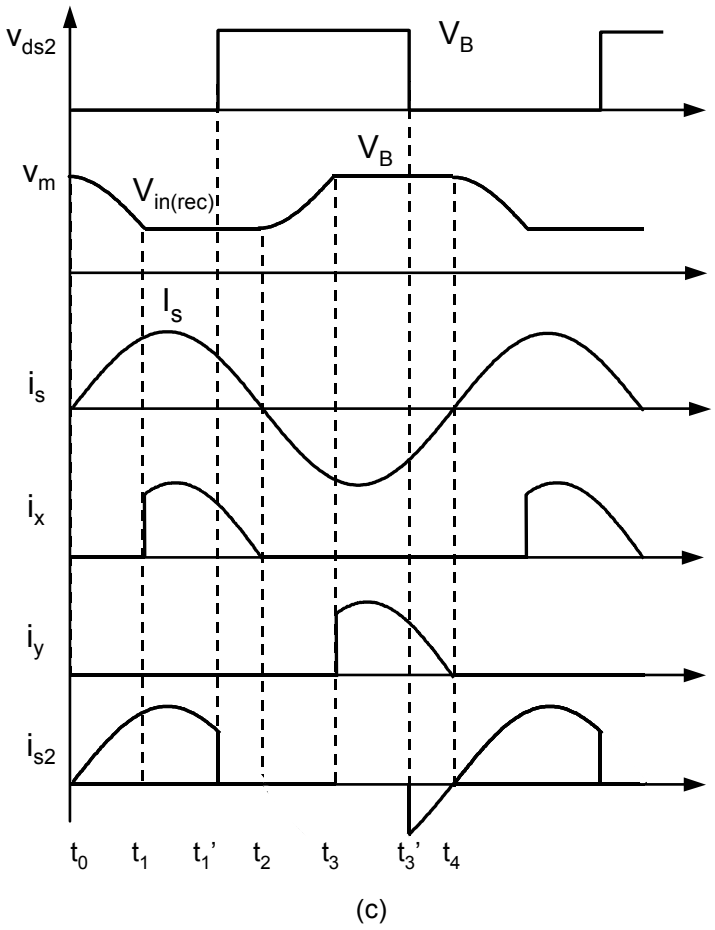


Figure 4-3. (a) Basic CS-CPPFC electronic ballast, (b) Six equivalent topological stages, (c) Key switching waveforms.



(c)

Figure 4-3. Continued.

$$\Delta Q = C_{in}\Delta V_c = C_{in}\left(V_B - v_{in(rec)}\right). \tag{4.4}$$

where ω_s is the switching frequency and V_B is the bus voltage.

Stage 2 [t_1, t_1']: At t_1, D_x starts to conduct current and v_m is clamped to the rectified line-input voltage. i_s flows through the line input, D_x and S_2. The load (in series with i_s) absorbs energy from the input line. This stage ends when S_2 is turned off and S_1 is turned on at t_1'. During this time interval, the rectified line current i_x is given by

$$i_x = i_s = I_S \sin \omega_s t \quad t \in \left(t_1, t_1'\right]. \tag{4.5}$$

Stage 3 [t_1', t_2]: Since i_s is still positive, it continues to flows through input line and D_x. It also charges C_B. This stage ends when i_s becomes negative at t_2 and D_x is naturally turned off. During this time interval, the rectified line current i_x is given by

$$i_x = i_s = I_S \sin \omega_s t \quad t \in (t_1', t_2]. \tag{4.6}$$

Stage 4 [t_2, t_3]: At t_2, i_s becomes negative and D_x is turned off. Since is still lower than V_B, D_y remains off. i_s starts to charge C_{in}, resulting in an increase of v_m. This charging period continues until v_m reaches V_B at t_3 and D_y is turned on. The time interval and charge variation ΔQ of C_{in} are given by (4.3) and (4.4), respectively.

Mode 5 [t_3, t_3']: At t_3, D_y is turned on and i_s flows through D_y and S_1. v_m is clamped to V_B. This stages lasts until t_3', when S_1 is turned off and S_2 is turned on.

Mode 6 [t_3', t_4]: S_2 is turned on when S_1 is turned off at t_3'. i_s is still negative and flows through S_2 and D_y. At t_4, i_s becomes positive and D_y is turned off naturally. A new switching cycle begins.

The average rectified input-line current equals the average i_x over one switching cycle, which is given by

$$i_{in(rec)} = i_{x(ave)} = \frac{1}{T_s}\int_{t_0}^{t_4} i_x dt = \frac{1}{T_s}\left(\int_{t_0}^{t_2} i_x dt - \int_{t_0}^{t_1} i_x dt\right) = \frac{I_s}{\pi} - \frac{\Delta Q}{T_s}. \tag{4.7}$$

Substituting (4.4) into (4.7) determines that

$$i_{in(rec)} = \left(\frac{I_s}{\pi} - C_{in} f_s V_B\right) + C_{in} f_s v_{in(rec)}. \tag{4.8}$$

The instantaneous input power is given by

$$p_{in}(t) = v_{in} i_{in} = v_{in(rec)} i_{in(rec)} = \left(\frac{I_s}{\pi} - C_{in} f_s V_B\right) v_{in(rec)} + C_{in} f_s v_{in(rec)}^2. \tag{4.9}$$

Averaging (4.9) over one line cycle yields

$$P_{in} = \frac{2V_p}{\pi}\left(\frac{I_s}{\pi} - C_{in} f_s V_B\right) + \frac{1}{2} C_{in} f_s V_p^2. \tag{4.10}$$

If the first two terms equal zero, the input current faithfully follows the line voltage without any distortion. The unity power factor condition is thus obtain as

$$I_s = \pi C_{in} f_s V_B . \tag{4.11}$$

The current and input power under the unity power factor condition become

$$i_{in(rec)} = C_{in} f_s v_{in(rec)}, \tag{4.12}$$

$$P_{in} = \frac{1}{2} C_{in} f_s V_p^2 . \tag{4.13}$$

Under unity PF operation, balancing the power between the input and output yields

$$P_o = \eta P_{in} = \frac{1}{2} \eta C_{in} f_s V_p^2 , \tag{4.14}$$

where P_o and η are the output power and conversion efficiency, respectively.

From (4.14) the capacitor C_{in} can be calculated as

$$C_{in} = \frac{2P_o}{\eta f_s V_p^2} . \tag{4.15}$$

Substituting (4.15) into (4.11), the magnitude of the resonant current I_s is given by

$$I_s = \frac{2\pi P_o V_B}{\eta V_p^2} , \tag{4.16}$$

Equations (4.11) and (4.16) show that a constant magnitude of current source is required to achieve unity PF.

B. Lamp CF and Bus Voltage Stress

To maintain long lamp life and eliminate lamplight flicker, a small lamp CF is preferred. The lamp CF is usually affected by the operation of the inverter stage. In steady state, six topological stages exist over one switching cycle. These six topological stages can be grouped into three sub-topologies, as shown in Figure 4-4. From Figure 4-4, C_{in} takes part in the resonance in sub-topology A (stages 1 and 4), but is clamped (switched out) in sub-topologies B (stages 2 and 3) and C (stages 5 and 6). Therefore,

there are two resonant modes over one switching cycle: Mode 1 in which C_{in} is connected in the resonant tank and Mode 2 in which C_{in} does not affect the resonant tank, and each resonant mode has a different time interval, which is approximately given by

$$t_I = \frac{2}{\omega_s}\arccos\left[1-\frac{\omega_s C_{in}}{I_s}\left(V_B - v_{in(rec)}\right)\right], \text{ and} \tag{4.17}$$

$$t_{II} = T_s - \frac{2}{\omega_s}\arccos\left[1-\frac{\omega_s C_{in}}{I_s}\left(V_B - v_{in(rec)}\right)\right], \tag{4.18}$$

where t_I is the time interval of Mode 1 and t_{II} is the time interval of Mode 2. It can be seen that t_I reaches its maximum value near the input-line zero crossing and t_{II} reaches its maximum value near the input-line peak. The different time intervals can also be explained from the boundary condition between these two resonant modes. The equivalent circuit shows that the charge stored in C_{in} changes in Mode 1 and remains constant in Mode 2. The charge variation of C_{in} is given by

$$\Delta Q = C_{in}\left(V_B - v_{in(rec)}\right). \tag{4.19}$$

ΔQ reaches it maximum value when $v_{in(rec)}$ =0, where it takes the longest time to charge and discharge C_{in} during the resonant Mode 1.

From the voltage and current waveforms of C_{in} in Figure 4-3(c), the equivalence of the "switched" C_{in} can be approximated as a variable capacitance C_{equ} plus a DC voltage source V_{equ} with a value of $\frac{1}{2}(V_B+V_{in(rec)})$, as shown in Figure 4-5(a). Since over one switching cycle the voltage variation across C_{equ} equals $\frac{1}{2}(V_B-V_{in(rec)})$ and the current amplitude is I_s, C_{equ} can be estimated as

$$C_{equ} = \frac{2I_s}{\omega_s\left(V_B - V_{in(rec)}\right)}. \tag{4.20}$$

Usually, the variation of V_B and I_s is relatively small over the half-line cycle, as compared with $V_{in(rec)}$; therefore, C_{equ} is mainly affected by the rectified line voltage. With the proper design, $I_s \approx \pi C_{in} f_s V_B$ can be achieved. So (4.20) can be approximated as

$$C_{equ} \approx C_{in}\frac{1}{1-\alpha\left|\sin\omega_l t\right|}, \tag{4.21}$$

where $\alpha = V_p/V_B$.

The output characteristic in the V-I plane is given by

$$V_o = \frac{\sqrt{2}V_B}{\pi} \cdot \frac{1}{\left| f_n^2 - \left(1 + \frac{C_r}{C_{equ}}\right)\right|} \cdot \sqrt{1 - \frac{I_o^2}{\left[\frac{\sqrt{2}V_B}{\pi} \cdot \frac{1}{\omega_s L_r - \frac{1}{\omega_s C_{equ}}}\right]^2}}, \qquad (4.22)$$

where $f_n = f_s / f_o$ and $f_o = 1/(2\pi\sqrt{L_r C_r})$.

Equation (4.22) shows that the output characteristic of the resonant tank changes with each half-line cycle, which causes the lamp current waveform to have a low-frequency ripple and deteriorates the lamp CF. Figure 4-5(b) shows an example in which two operation points are illustrated by the intersections of lamp characteristics with the output characteristics near the line peak and line-zero crossing, respectively. The lamp has high current near the line-zero crossing and small lamp current near the line-peak voltage, as shown in Figure 4-5(c). In order to improve lamp CF, a suitable control scheme is needed.

The variable capacitance also causes the resonant inductor current to have a low-frequency ripple, and the unity PF condition of (4.11) cannot be satisfied, which deteriorates the line-input current.

There is another problem in that the bus voltage increases during light-load operation. Normally, the rapid-start electronic ballast consists of three operation modes: preheat, startup and steady state. The preheat and startup modes correspond to the light load because the lamps are not fully turned on. The preheat mode is needed to have a long lamp life when the lamp is frequently turned on and off. Also, with preheating the lamp is easy to ignite since the lamp ignition voltage is reduced. Usually, it takes 0.5 to 0.75 seconds to preheat the filament at a fixed switching frequency [A5], and then the switching frequency is reduced towards the resonant frequency so that a high lamp voltage is obtained to ignite the lamp, as shown in Figure 4-6(a). The amplitude of the resonant inductor current I_s also increases as the switching frequency is reduced, as shown in Figure 4-6(b). However, the power balance between the input and output should be maintained, as given by

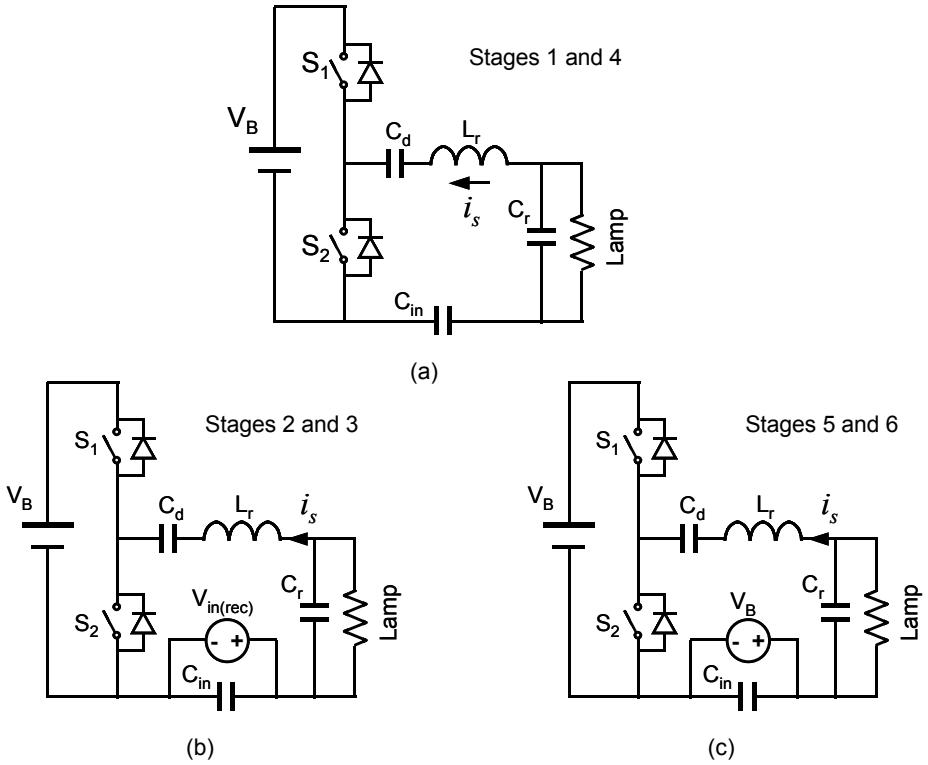


Figure 4-4. Three sub-topologies of the CS-CPPFC electronic ballast.

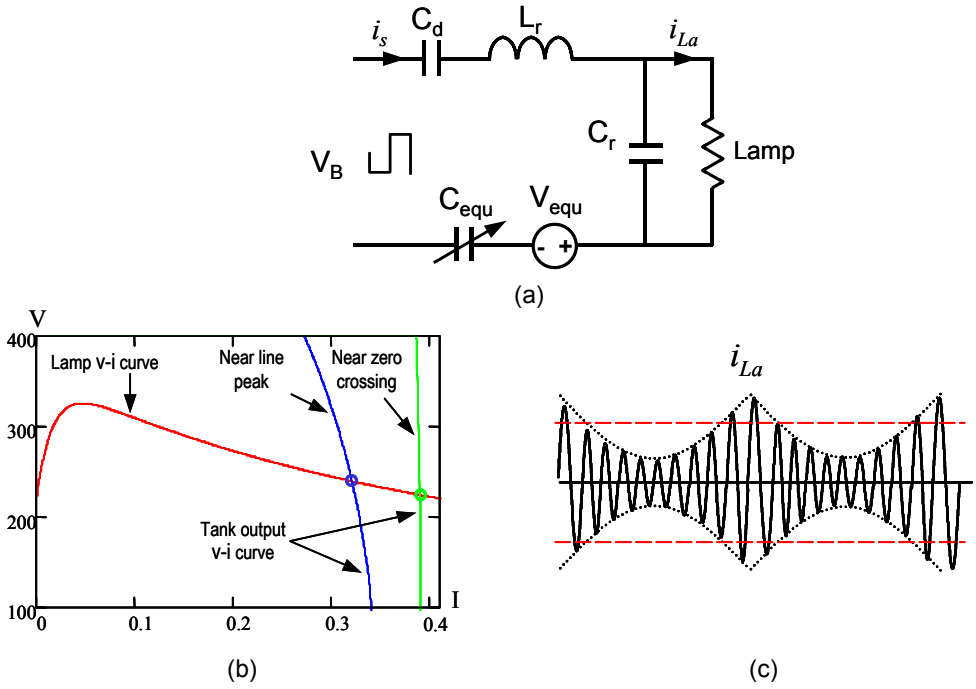


Figure 4-5. (a) Equivalent resonant tank, (b) operation points near line zero crossing and the line-peak voltage, and (c) lamp current waveforms.

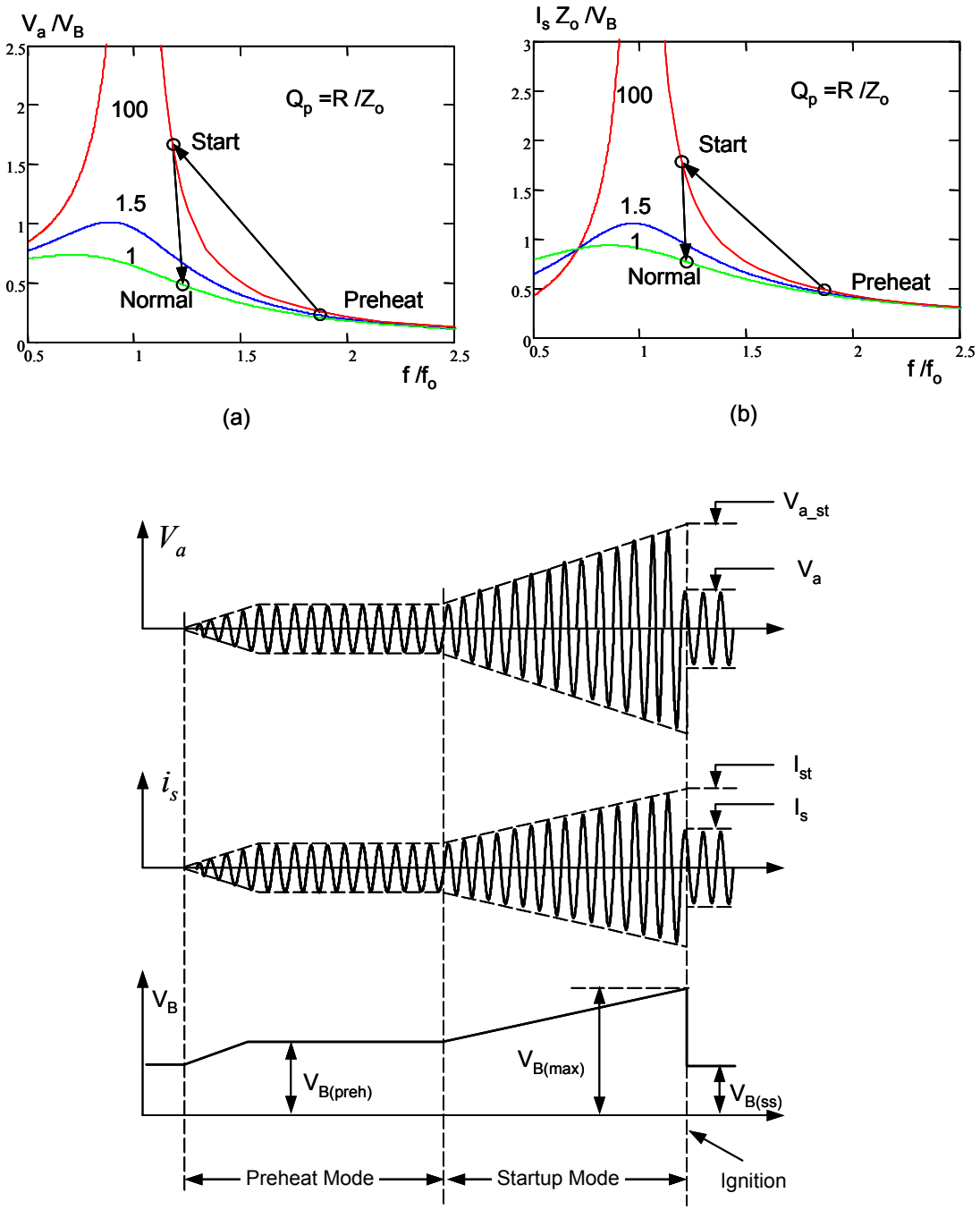


Figure 4-6. (a) Voltage conversion gain of series-resonant parallel-loaded circuit, (b) normalized resonant inductor current, and (c) waveforms of lamp voltage V_a, resonant inductor current i_s, and bus voltage V_B during preheat, startup and steady-state operations.

$$P_{in} = \frac{2V_p}{\pi}\left(\frac{I_s}{\pi} - C_{in} f_s V_B\right) + \frac{1}{2} C_{in} f_s V_p^2 = P_{out} . \quad (4.23)$$

Since in the preheat and startup modes, I_s and f_s are larger and P_{out} is smaller than those in the steady-state mode, V_B has to increase to maintain the equality of (4.23), as illustrated in Figure 4-6©. Therefore, three problems exist in the basic CS-CPPFC electronic ballast: high lamp CF, its inability to automatically meet the unity PF condition, and high bus voltage stress at light-load operations.

C. Design Considerations

The design objective is to find the values of charge pump capacitor C_{in} and resonant components L_r and C_r. To optimally design this CS-CPPFC electronic ballast, the following should be taken into account:

- Minimum bus voltage $V_B = V_p$, where V_p is the line peak voltage;
- Satisfying the unity PF condition $I_s = \pi C_{in} f_s V_B$; and
- Maintaining ZVS operation, that is

$$f_s > \frac{1}{2\pi\sqrt{\frac{C_{in}C_r}{C_{in}+C_r} L_r}} . \quad (4.24)$$

From (4.15), C_{in} is given by

$$C_{in} = \frac{2P_o}{\eta f_s V_p^2} , \quad (4.25)$$

where P_o and η are the output power and the conversion efficiency, respectively.

To simplify the resonant tank design, the tank is designed near line-peak voltage, where the modulation effect of C_{in} is minimized and the excitation voltage is close to a pure square waveform. Using fundamental approximation, the output voltage and the resonant inductor peak current are given by

$$V_{o(rms)} = \frac{\sqrt{2}V_B}{\pi} \frac{1}{\sqrt{\left(1-\frac{\omega_s^2}{\omega_o^2}\right)^2 + \left(\frac{\omega_s L_r}{R_{lamp}}\right)^2}}, \text{ and} \tag{4.26}$$

$$I_{Lr(peak)} = \frac{2V_B}{\pi} \frac{\sqrt{(\omega_s C_r)^2 + 1/R_{lamp}^2}}{\sqrt{\left(1-\frac{\omega_s^2}{\omega_o^2}\right)^2 + \left(\frac{\omega_s L_r}{R_{lamp}}\right)^2}} = I_s . \tag{4.27}$$

4.2.2 Analysis of VS-CPPFC Electronic Ballasts

A family of VS-CPPFC electronic ballasts has been patented or published previously [D8 – D15]. This family of circuits can be derived from the CS-CPPFC electronic ballast by using the Thevenin equivalent network. The basic CS-CPPFC electronic ballast and its simplified equivalent circuit are shown in Figures 4-7(a) and (b), respectively. In Figure 4-7(b), the charge pump capacitor C_{in} is in parallel with the current source as a Norton form. The corresponding Thevenin form is shown in Figure 4-7(d), in which C_{in} is in series with a voltage source. Since a voltage source is used to achieve PFC, this kind of circuit is called VS-CPPFC circuit. Figure 4-7(c) shows the basic VS-CPPFC electronic ballast, in which the lamp voltage is considered as a high-frequency voltage source [D11]. The relationship between the VS and CS is given by

$$V_s = \frac{I_s}{j\omega_s C_{in}}. \tag{4.28}$$

As expected, there is no characteristic change to the port terminal after this replacement. The line current and input power can be obtained directly from (4.8) and (4.10) as

$$i_{in(rec)} = C_{in} f_s \left(2V_a - V_B\right) + C_{in} f_s v_{in(rec)}, \text{ and} \tag{4.29}$$

$$P_{in} = \frac{2V_p}{\pi} f_s C_{in} \left(2V_a - V_B\right) + \frac{1}{2} C_{in} f_s V_p^2 . \tag{4.30}$$

Obviously, the unity PF condition is

$$2V_a = V_B . \tag{4.31}$$

Under unity PF condition, the line current and average power become

$$i_{in(rec)} = C_{in} f_s v_{in(rec)}, \text{ and} \tag{4.32}$$

$$P_{in} = \frac{1}{2} C_{in} f_s V_p^2 . \tag{4.33}$$

Under unity PF operation, balancing the power between the input and output yields

$$C_{in} = \frac{2P_o}{\eta f_s V_p^2}, \tag{4.34}$$

where P_o and η are the output power and conversion efficiency, respectively.

Like in the CS-CPPFC electronic ballast, there is C_{in} modulation effect on the resonant tank of the basic VS-CPPFC electronic ballast, as shown in Figure 4-8(a). The modulation effect of C_{in} can be approximated as a variable capacitance C_{equ}, which is given by previous work [D11], as follows:

$$C_{equ} \approx C_{in}\left(\alpha \left|\sin \omega_l t\right|\right), \tag{4.35}$$

where $\alpha = V_p/V_B$.

Therefore, the output characteristic of the resonant tank in the V-I plane is given by

$$V_o = \frac{\sqrt{2}V_B}{\pi} \cdot \frac{1}{\left|f_n^2 - 1\right|} \cdot \sqrt{1 - \frac{I_o^2}{\left[\frac{\sqrt{2}V_B}{\pi} \cdot \frac{1}{\omega_s L_r}\right]^2}}, \tag{4.36}$$

where $f_n = f_s / f_o$ and $f_o = 1/\left(2\pi\sqrt{L_r\left(C_r + C_{equ}\right)}\right)$.

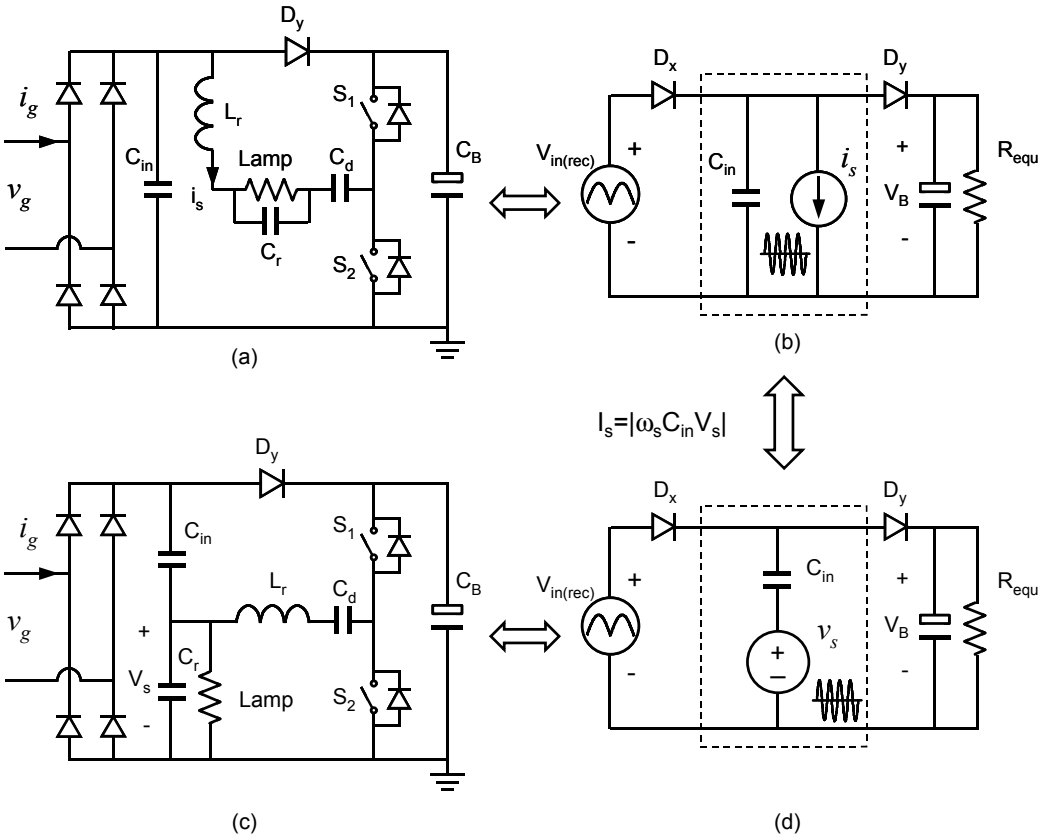


Figure 4-7. (a) Basic CS-CPPFC electronic ballast, (b) conceptual CS-CPPFC circuit, (c) basic VS-CPPFC electronic ballast, and (d) conceptual VS-CPPFC circuit.

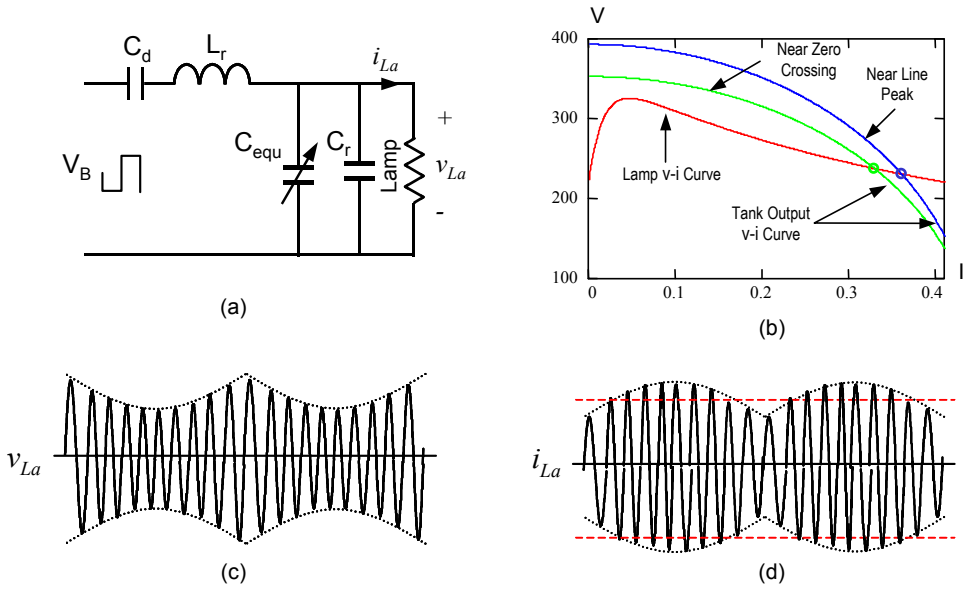


Figure 4-8. (a) Equivalent resonant tank, (b) operation points near line-zero crossing and line-peak voltage, (c) lamp voltage waveform, and (d) lamp current waveform.

From (4.37), the corner frequency f_o is modulated by the half-line cycle, which causes the envelope of V_a to have 120Hz ripple. Since the lamp impedance can be approximated as a resistance with a negative incremental impedance, the 120Hz ripple on the lamp voltage causes a strong 120Hz ripple on the lamp current, and the lamp CF is deteriorated. Figure 4-8 shows an example in which two operation points are shown to demonstrate the modulation effect of C_{in} on V_a and lamp current. It should be noted that since V_a is not constant, the unity PF condition of (4.31) could not be satisfied; therefore the line current is distorted.

Besides high lamp CF and inability to meet unity PF condition, this basic VS-CPPFC electronic ballast also suffers from high bus voltage stress during light-load operations. As shown in Figure 4-6, during preheat mode, the frequency is higher than normal operation and V_B has to increase to keep low input power. During startup mode, lamp voltage is much higher than that of normal operation in order to ignite the lamp. Therefore, V_B has to increase to maintain the power balance, which is given by

$$P_{in} = \frac{2V_p}{\pi} f_s C_{in} \left(2V_a - V_B\right) + \frac{1}{2} C_{in} f_s V_p^2 = P_{out} . \tag{4.37}$$

In summary, three problems exist in the basic VS-CPPFC electronic ballast: high lamp CF, its inability to automatically meet the unity PF condition, and high bus voltage stress at light-load operations.

To improve the lamp CF, one approach is to minimize the modulation effect of C_{in}. In order to achieve this goal, C_{in} is split into two capacitors, C_{in1} and C_{in2}, in which C_{in2} is in parallel with either D_x or D_y, as shown in Figure 4-9(a) [D15]. From the equivalent tank of Figure 4-9(b), C_{in1} is in series with C_{in2} so that the equivalent capacitance is reduced. Therefore, this circuit is called the VS-CPPFC electronic ballast with improved crest factor (ICF).

Using the Thevenin equivalent port, the functions of C_{in1}, C_{in2} and VS can be replaced by an equivalent capacitor C_T and voltage source V_T, as shown in Figure 4-9(d). C_T and V_T are given by

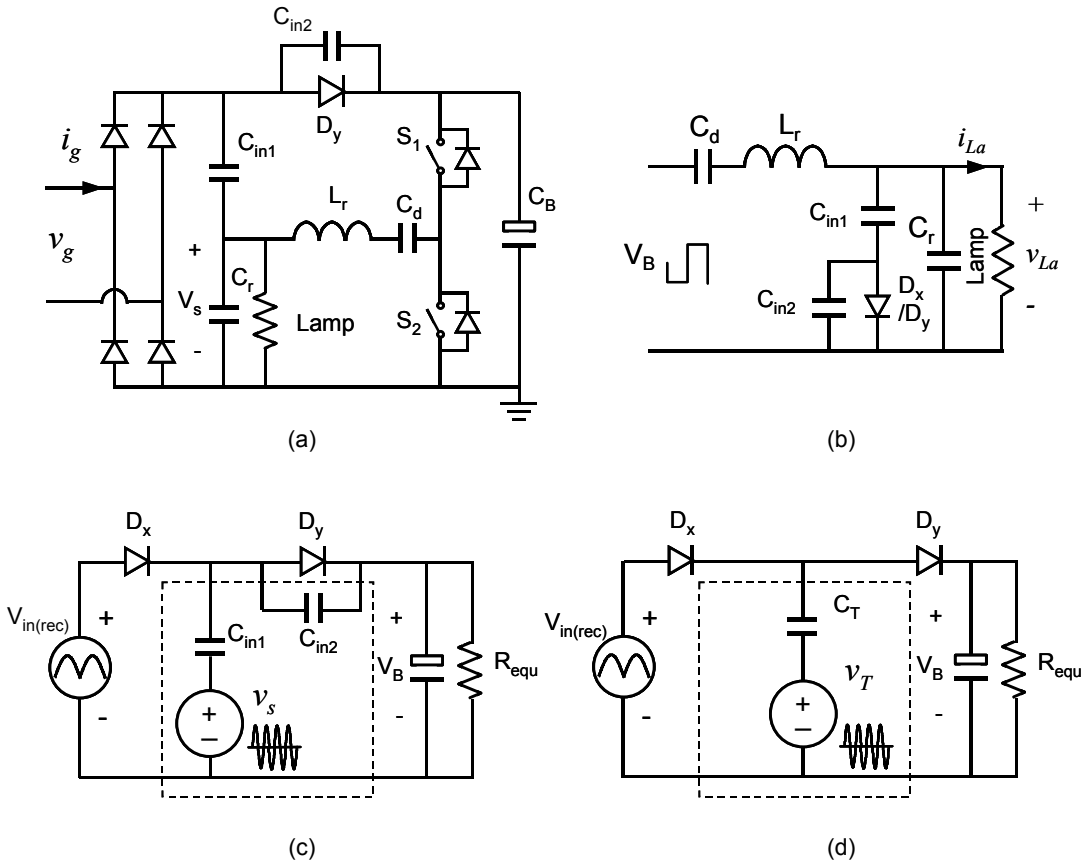


Figure 4-9. (a) Circuit diagram of VS-CPPFC electronic ballast with ICF, (b) equivalent resonant tank, (c) equivalent circuit, and (d) Thevenin equivalent circuit.

$$C_T = C_{in1} + C_{in2} = C_{in}\text{, and} \tag{4.38}$$

$$V_T = \frac{C_{in1}}{C_{in1} + C_{in2}} V_a = \frac{C_{in1}}{C_{in}} V_a \tag{4.39}$$

Substituting the above equations into (4.29) and (4.30), the line current and input power are obtained as

$$i_{in(rec)} = C_{in} f_s \left(2\frac{C_{in1}}{C_{in}} V_a - V_B \right) + C_{in} f_s v_{in(rec)}\text{, and} \tag{4.40}$$

$$P_{in} = \frac{2V_p}{\pi} f_s C_{in} \left(2\frac{C_{in1}}{C_{in}} V_a - V_B \right) + \frac{1}{2} C_{in} f_s V_p^2 . \tag{4.41}$$

The unity PF condition becomes

$$2\frac{C_{in1}}{C_{in}}V_a = V_B\,. \tag{4.42}$$

From (4.34), the charge pump capacitances are given by

$$C_{in1} + C_{in2} = C_T = \frac{2P_o}{\eta f_s V_p^2}\,. \tag{4.43}$$

The design of this VS-CPPFC electronic ballast with ICF is straightforward. From (4.39), it can be seen that the effect of the lamp voltage V_a on PFC can be adjusted by the scale of C_{in1} to (C_{in1}+C_{in2}). In the two lamps-in-series applications, the total lamp voltage is usually larger than the bus voltage. From (4.42) and (4.43), C_{in1} and C_{in2} are given by

$$C_{in1} = \frac{V_B}{2V_a}\frac{2P_o}{\eta f_s V_p^2}\,, \text{ and} \tag{4.44}$$

$$C_{in2} = \frac{2P_o}{\eta f_s V_p^2}\left(1 - \frac{V_B}{2V_a}\right). \tag{4.45}$$

4.2.3 Analysis of Voltage-Source Current-Source (VSCS) CPPFC Electronic Ballasts

There is another family of CPPFC electronic ballasts, called VSCS-CPPFC electronic ballasts, which employ both a current source and a voltage source to achieve PFC [D15-16]. Figure 4-10 shows the basic VSCS-CPPFC electronic ballast, which can be regarded as a combination of the basic CS-CPPFC electronic ballast with the basic VS-CPPFC electronic ballast. The CS-CPPFC circuit consists of C_{y2}, D_{y2}, C_r, L_r and lamp, while the VS-CPPFC circuit consists of C_{in}, D_{y1}, C_r, L_r and lamp. Both the VS-CPPFC circuit and the CS-CPPFC circuit share a common resonant tank composed of C_r and L_r. From the simplified equivalent circuit of Figure 4-10(d), it can be seen that D_{y1} is inserted into the voltage-current source loop. More topological stages exist over one switching cycle.

Assume $i_s = I_s \sin \omega_s t$ and $v_a = V_a \sin(\omega_s t + 90^0)$, two different operation regions exist over a half-line cycle, as shown in Figures 4-11(a)-(b). A critical value $V_{(crit)}$, defined by (4.48), exists to separate these regions. If the instantaneous line voltage is larger than $V_{(crit)}$, D_x is on at stage M_5; otherwise D_x remains off at stage M_5'. This is because when the instantaneous line voltage is larger than $V_{(crit)}$, V_{Cy2} can easily be charged to $V_B - V_{in(rec)}$ at the end of stage M_4 so that D_x carries current. Otherwise, V_{Cy2} cannot be charged to $V_B - V_{in(rec)}$ before the current source changes polarity. D_x remains off at mode M_5'. Because of this difference, the average line current over one switching cycle becomes

$$i_{in(rec)} = C_{in} f_s \left(\frac{2I_s}{\omega_s C_{y2}} + 2V_a - V_B \right) + C_{in} f_s v_{in(rec)} \qquad v_{in(rec)} \in [0, V_{crit}) \text{ and} \qquad (4.46)$$

$$i_{in(rec)} = C_{y2} f_s \left(\frac{2I_s}{\omega_s C_{y2}} - V_B \right) + C_{y2} f_s v_{in(rec)} \qquad v_{in(rec)} \in [V_{crit}, V_p], \qquad (4.47)$$

where $C_{in} = C_{in1} C_{y2} / (C_{in1} + C_{y2})$,

$$V_{(crit)} = V_B + \frac{2}{\omega_s C_{y2}} (C_{in1} \omega_s V_a - I_s) \text{ and} \qquad (4.48)$$

$$I_{(crit)} = \frac{1}{2} C_{y2} \omega_s V_B + C_{in1} \omega_s V_a . \qquad (4.49)$$

The unity PF condition is no longer applicable. However, there is sufficient room to meet the IEC 1000-3-2 Class C regulations.

Although the modulation of the charge pump capacitors on the resonant tank still exist, the effect is reduced, as shown in Figure 4-12. Since the envelopes of the lamp current of the CS-CPPFC and VS-CPPFC electronic ballasts are somewhat complementary, the lamp ripple is therefore lowered by their combination.

This basic VSCS-CPPFC electronic ballast still suffers from high bus voltage stress during light-load operation. However, it can be designed to be lower than that in the VS-CPPFC circuit and the CS-CPPFC circuit. As shown in (4.47), the circuit behaves like a basic CS-CPPFC circuit when the instantaneous line voltage is larger than the critical

voltage $V_{(crit)}$. If $V_{(crit)}$ is designed very low, the circuit will operate in CS-CPPFC mode most of the time. Therefore, the value of C_{y2} equals the C_{in} of the basic CS-CPPFC circuit. During the light-load operation, the critical voltage increases as V_B increases, and the circuit will operate in the combined mode given by (4.46). If C_{in1} is a small number, the input power will be lower than that in the CS-CPPFC or the VS-CPPFC circuit. As a result, the bus voltage will not increase as high as that in either the CS or the VS circuit. However, the lamp CF becomes large if a small C_{in1} is used. A trade-off exists between the bus voltage stress and lamp CF.

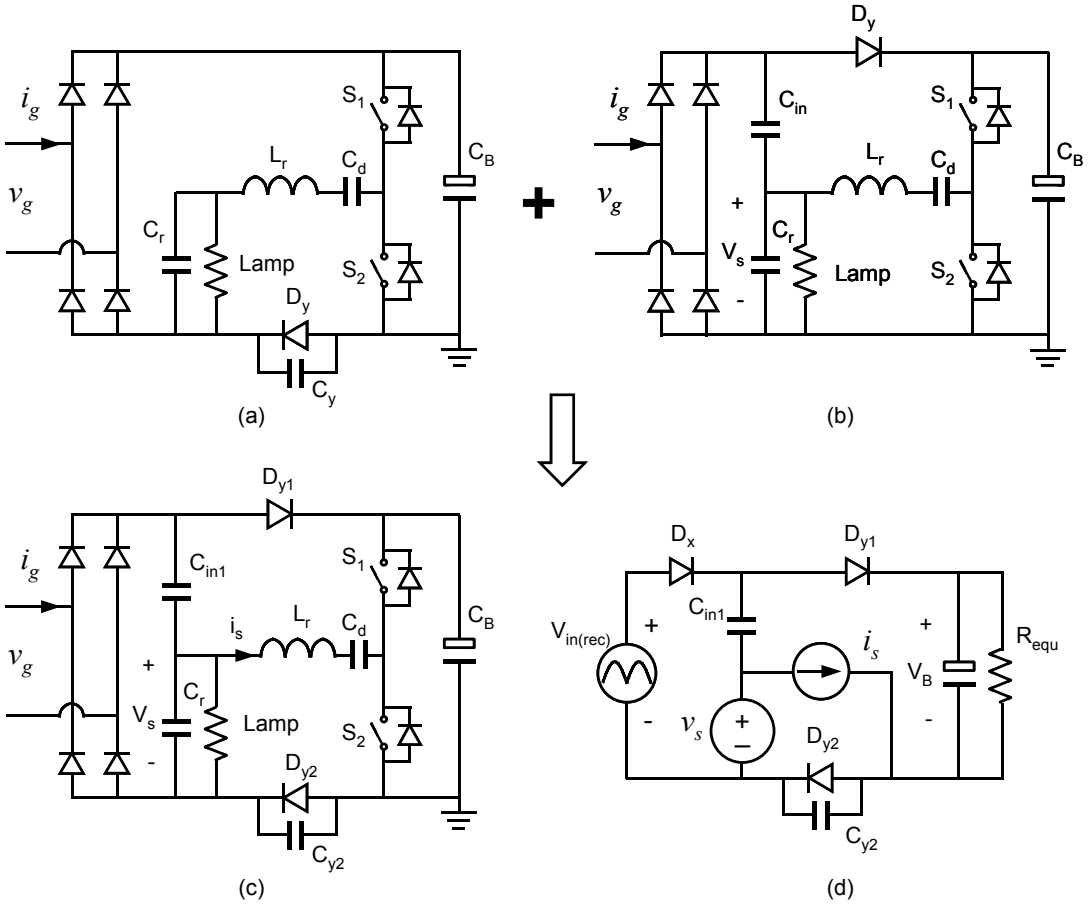
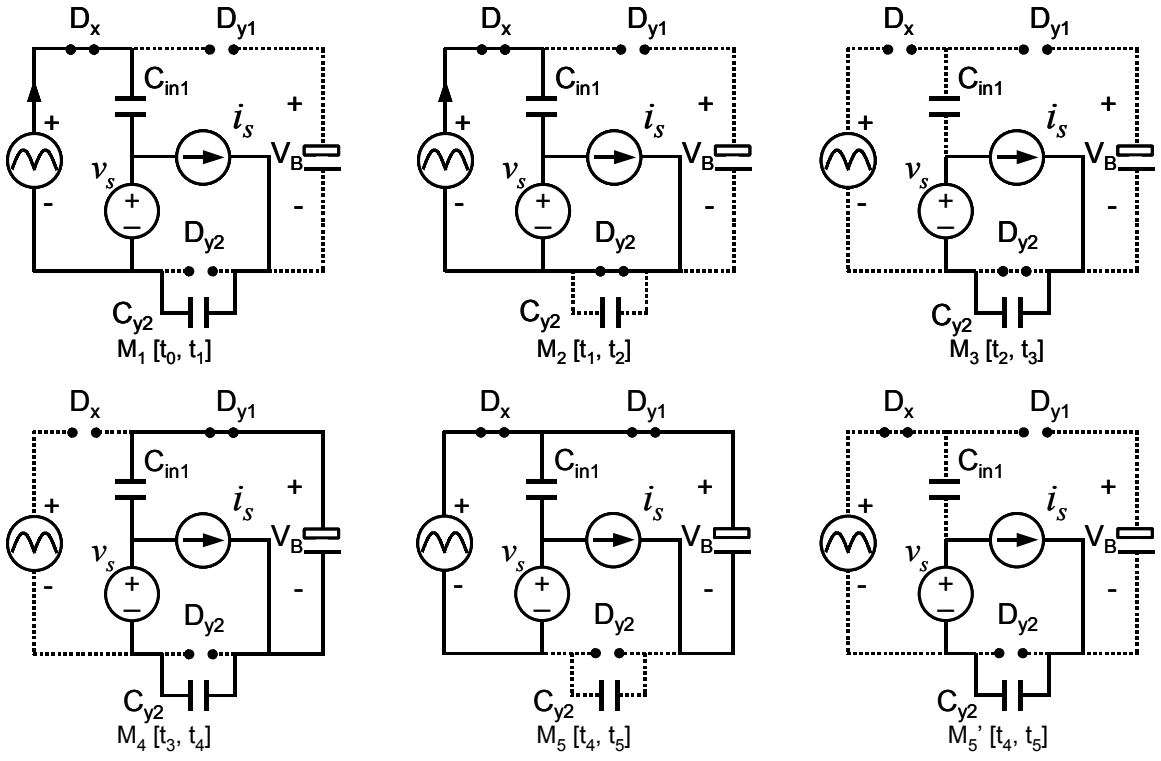
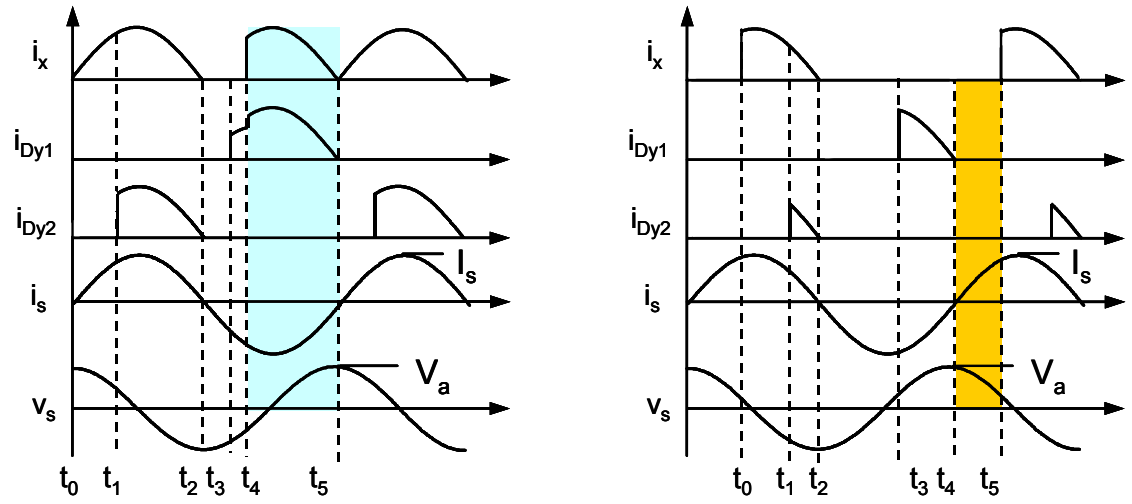


Figure 4-10. (a) Basic CS-CPPFC circuit, (b) Basic VS-CPPFC circuit, (c) Basic VSCS-CPPFC circuit, (d) Conceptual basic VSCS-CPPFC circuit.



(a)



(b)

Figure 4-11. (a) Two five-topology-stage series: If $V_{in(rec)} > V_{(crit)}$, then (M1) → (M2) → (M3) → (M4) → (M5) → (M1); otherwise, (M1) → (M2) → (M3) → (M4) → (M5') → (M1), and (b) Key waveforms.

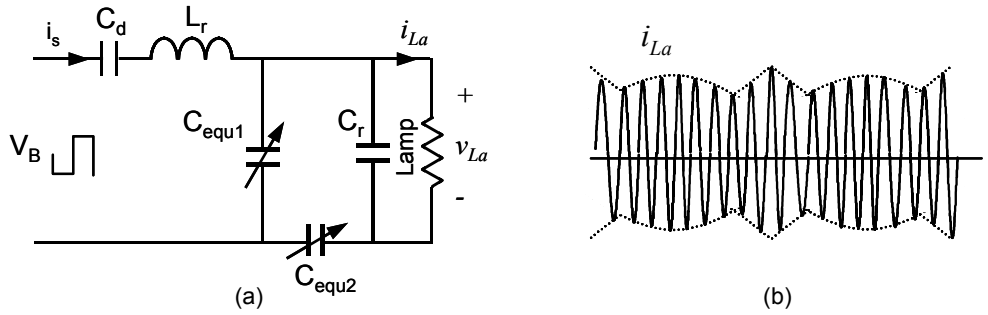


Figure 4-12. (a) Equivalent resonant tank, and (b) lamp current waveform.

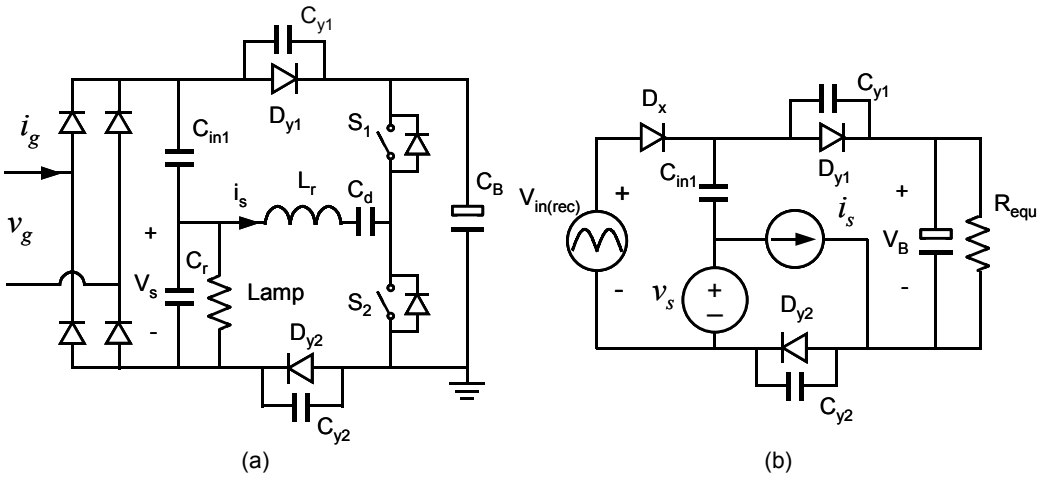


Figure 4-13. (a) Circuit diagram of VSCS-CPPFC electronic ballast with ICF, and (b) conceptual VSCS-CPPFC with ICF circuit.

To further improve CF, another high-frequency capacitor is added in parallel with D_{y1} so that the modulation effect of charge pump capacitors is further reduced. The resulting circuit is called the VSCS-CPPFC electronic ballast with ICF, as shown in Figure 4-13. It can be regarded as the combination of the basic CS-CPPFC circuit with the VS-CPPFC with ICF circuit.

Depending on the relative magnitude of the voltage source and current source, three operational modes exist, which can be classified as follows: Mode 1, in which the current source greatly dominates the voltage source; Mode 2, in which the current source dominates the voltage source; and Mode 3, in which the voltage source dominates the

current source. Identifying different operational modes is important not only for understanding the circuit operation principle, but also for circuit design.

For each operational mode, two different operation regions or topological stage series exist over a half-line cycle. Similar to the basic VSCS-CPPFC electronic ballast, for each operational mode there is a critical value $V_{(crit)}$, which separates them into two different regions. The topological stage series and critical voltage $V_{(crit)}$ are studied as follows.

I) Mode 1 (current source greatly dominates voltage source):

The circuit operates in Mode 1 if the condition given in (4.50) is satisfied. There are two five-topology-stage series over a half-line cycle, as shown in Figure 4-14. It can be seen that the input rectifier diode current waveforms are different in the two operation regions. In region A, the rectified input-line voltage is bigger than $V_{(crit)}$, and the conduction angle of the input rectifier is larger that that in region B where the rectified line voltage is lower than $V_{(crit)}$. Based on the waveforms and topological stages, the rectified average line current and the critical voltage $V_{(crit)}$ are obtained as

$$\frac{I_s}{\omega_s C_{in1}} \geq \frac{C_{y1}}{C_{y1}+C_{y2}} \frac{I_s}{\omega_s C_{in1}} \geq V_a , \tag{4.50}$$

$$i_{in(rec)} = C_{in} f_s \left(\frac{2I_s}{\omega_s C_{in}} + \frac{C_{in1} C_{y1} / (C_{in1}+C_{y1})}{C_{in}} 2V_a - V_B \right) + C_{in} f_s v_{in(rec)} \qquad v_{in(rec)} \in [0, V_{crit}), \text{ and} \tag{4.51}$$

$$i_{in(rec)} = (C_{y1}+C_{y2}) f_s \left(\frac{2I_s}{\omega_s (C_{y1}+C_{y2})} - V_B \right) + (C_{y1}+C_{y2}) f_s v_{in(rec)} \qquad v_{in(rec)} \in \lfloor V_{crit}, V_p \rfloor, \tag{4.52}$$

where $C_{in} = (C_{in1}C_{y1} + C_{in1}C_{y2} + C_{y1}C_{y2}) / (C_{in1}+C_{y1})$, and

$$V_{(crit)} = V_B - 2V_a C_{in1} / C_{y1} . \tag{4.53}$$

From (4.50) – (4.53), it can be seen that unity PF occurs only when $V_{(crit)}$ =0 and $\frac{C_{y1}}{C_{y1}+C_{y2}} \frac{I_s}{\omega_s C_{in1}} = V_a$.

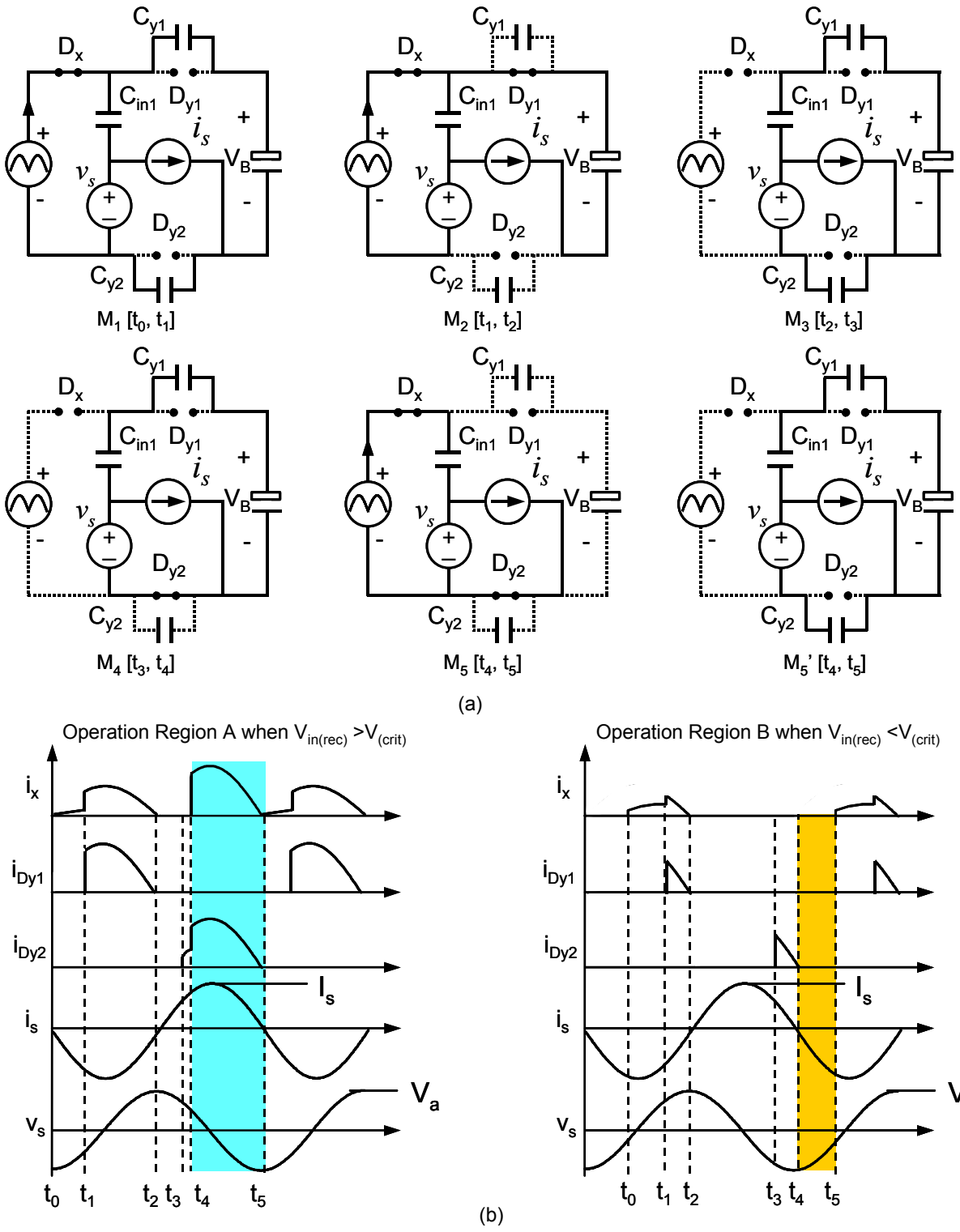


Figure 4-14. Mode 1 (CS greatly dominates VS). (a) Two five-topology-stage series: If $V_{in(rec)} > V_{(crit)}$, then $(M_1) \rightarrow (M_2) \rightarrow (M_3) \rightarrow (M_4) \rightarrow (M_5) \rightarrow (M_1)$; otherwise, $(M_1) \rightarrow (M_2) \rightarrow (M_3) \rightarrow (M_4) \rightarrow (M_5') \rightarrow (M_1)$, and (b) key waveforms.

II) Mode 2 (current source dominates voltage source):

The circuit operates in Mode 2 if the condition given in (4.54) is satisfied. In steady state, two five-topology-stage series exist over a half-line cycle, as shown in Figure 4-15(a). The key switching waveforms are shown in Figure 4-15(b). Similar to the circuit operating in Mode 1, two different operation regions exist over a half-line cycle. Compared with the waveforms in Mode 1, the waveform of D_{y1} changes with the waveform of D_{y2}. Based on the waveforms and topological stages, the rectified average line current and the critical voltage $V_{(crit)}$ are obtained as

$$\frac{I_s}{\omega_s C_{in1}} \geq V_a \geq \frac{C_{y1}}{C_{y1}+C_{y2}} \frac{I_s}{\omega_s C_{in1}}, \tag{4.54}$$

$$i_{in(rec)} = C_{in} f_s \left(\frac{C_{in1}}{C_{in1}+C_{y2}} \frac{2I_s}{\omega_s C_{in}} + \frac{C_{in1}C_{y2}/(C_{in1}+C_{y2})}{C_{in}} 2V_a - V_B \right), \text{ and} \tag{4.55}$$
$$+ C_{in} f_s v_{in(rec)} \qquad v_{in(rec)} \in [0, V_{crit})$$

$$i_{in(rec)} = (C_{y1}+C_{y2}) f_s \left(\frac{2I_s}{\omega_s (C_{y1}+C_{y2})} - V_B \right) \tag{4.56}$$
$$+ (C_{y1}+C_{y2}) f_s v_{in(rec)} \qquad v_{in(rec)} \in [V_{crit}, V_p]$$

where $C_{in} = (C_{in1}C_{y1} + C_{in1}C_{y2} + C_{y1}C_{y2})/(C_{in1}+C_{y2})$, and

$$V_{crit} = V_B - 2\frac{C_{in1}}{C_{y2}} \left(\frac{I_s}{\omega_s C_{in1}} - V_a \right). \tag{4.57}$$

From (4.54) – (4.57), it can be seen that unity PF occurs only when V_{crit} =0 and $\frac{C_{y1}}{C_{y1}+C_{y2}} \frac{I_s}{\omega_s C_{in1}} = V_a$. Experimental result shows that the higher the critical voltage, the higher the line current distortion.

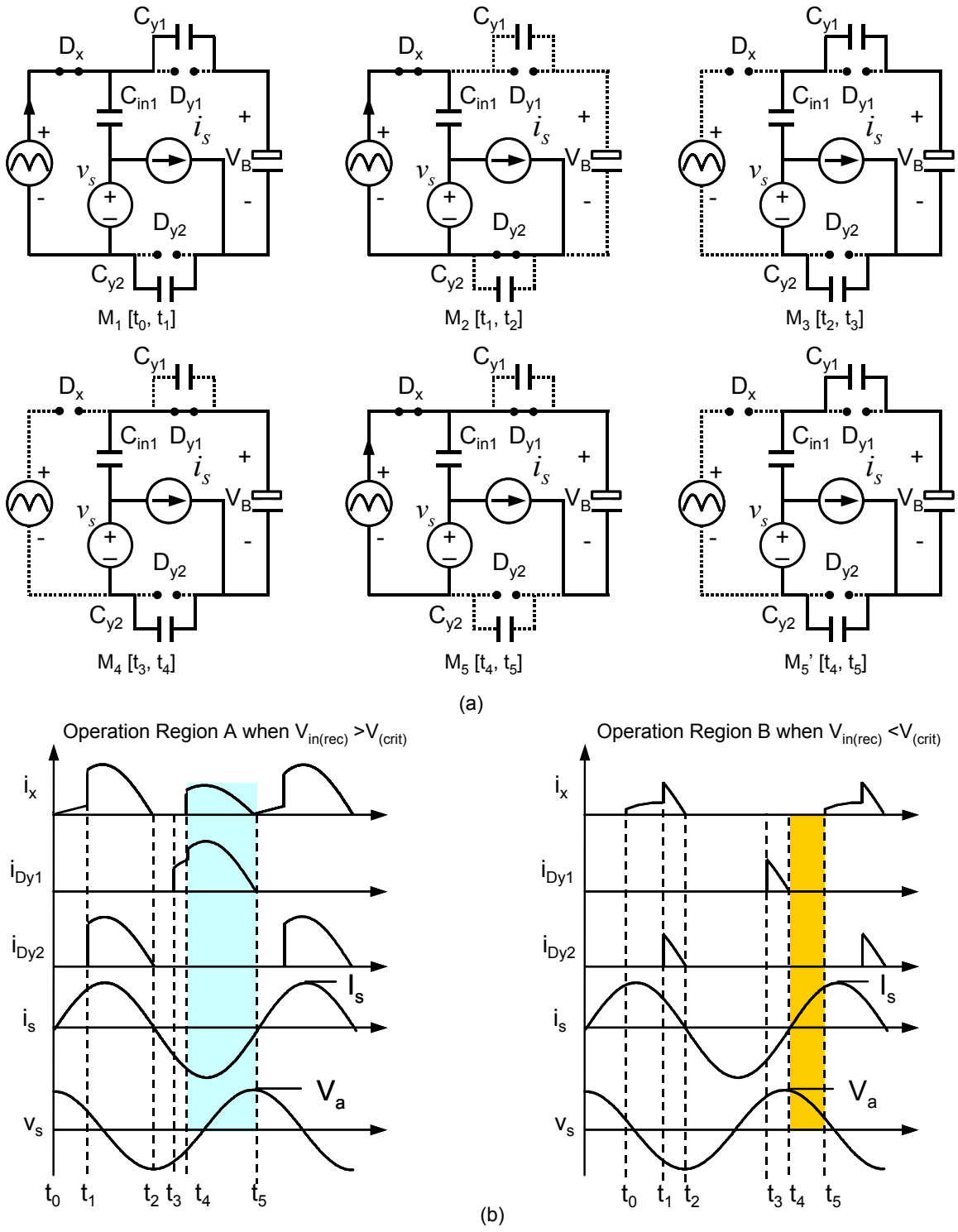


Figure 4-15. Mode 2 (CS dominates VS). (a) Two five-topology-stage series: If $V_{in(rec)} > V_{(crit)}$, then $(M_1) \rightarrow (M_2) \rightarrow (M_3) \rightarrow (M_4) \rightarrow (M_5) \rightarrow (M_1)$; otherwise, $(M_1) \rightarrow (M_2) \rightarrow (M_3) \rightarrow (M_4) \rightarrow (M_5') \rightarrow (M_1)$, and (b) key waveforms.

III) Mode 3 (voltage source dominates current source):

The circuit operates in Mode 3 if the condition given in (4.58) is satisfied. The topological stages and key switching waveforms are shown in Figures 3-16(a) and (b), respectively. Similar to the circuit operating in Mode 1 or 2, two five-topology-stage series exist over a half line cycle. It can be seen that the conduction angle of D_x is much smaller so that a larger EMI filter is needed. The conduction angle of D_{y2}, however, enlarges. Therefore, the ripple current of bus capacitor is reduced. The rectified average line current and the critical voltage $V_{(crit)}$ are given by

$$V_a \geq I_s / \omega_s C_{in1}, \tag{4.58}$$

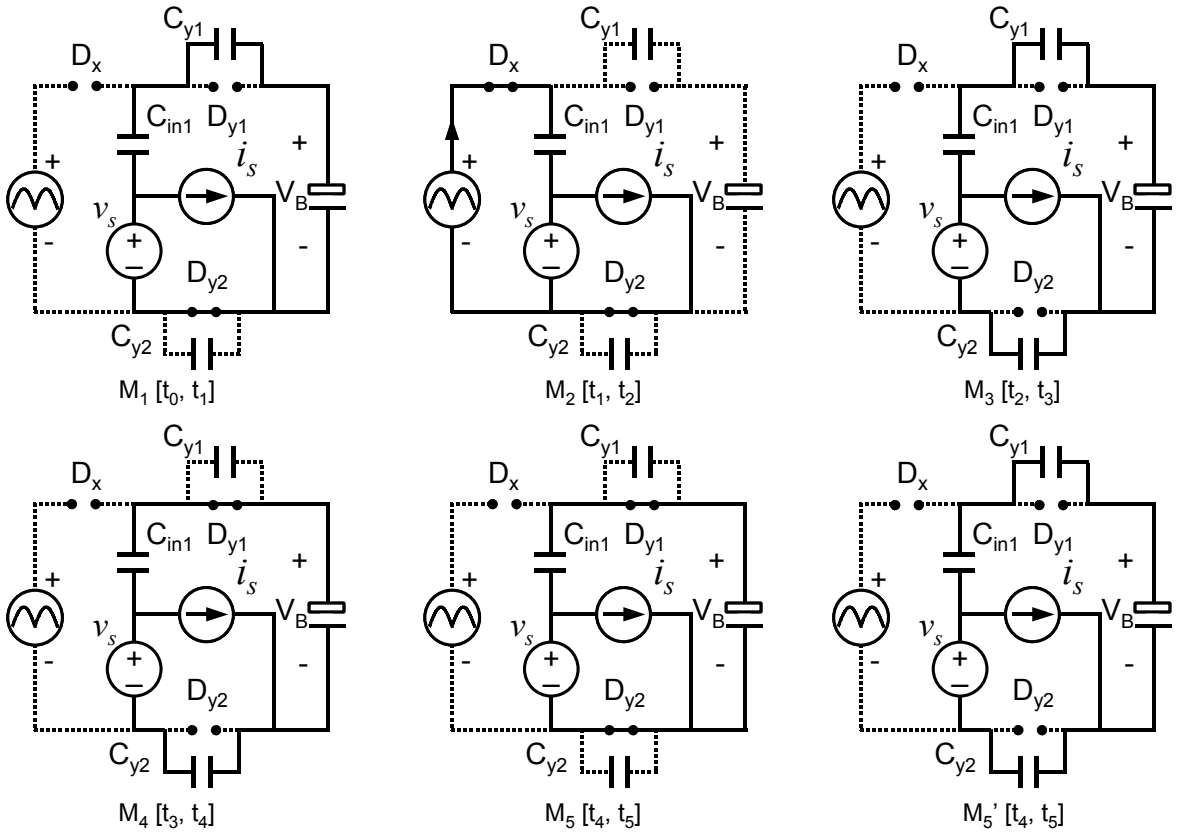
$$i_{in(rec)} = \begin{cases} C_{in} f_s \left(\dfrac{C_{in1}}{C_{in1} + C_{y2}} \dfrac{2I_s}{\omega_s C_{in}} + \dfrac{C_{in1} C_{y2} / C_{in1} + C_{y2}}{C_{in}} 2V_a - V_B \right), \text{ and} \\ + C_{in} f_s v_{in(rec)} \qquad\qquad v_{in(rec)} \in [0, V_{crit}) \end{cases} \tag{4.59}$$

$$i_{in(rec)} = \begin{cases} (C_{in1} + C_{y1}) f_s \left(\dfrac{C_{in1}}{C_{in1} + C_{y1}} 2V_a - V_B \right) \\ + (C_{in1} + C_{y1}) f_s v_{in(rec)} \qquad\qquad v_{in(rec)} \in [V_{crit}, V_p] \end{cases}, \tag{4.60}$$

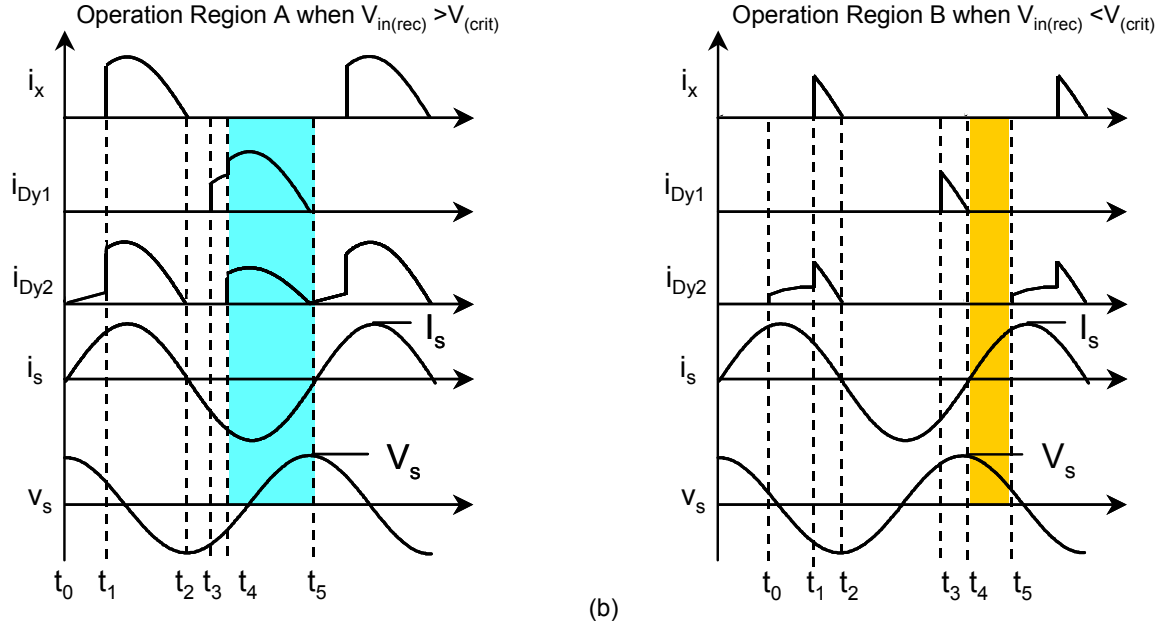
where $C_{in} = (C_{in1} C_{y1} + C_{in1} C_{y2} + C_{y1} C_{y2}) / (C_{in1} + C_{y2})$, and

$$V_{crit} = V_B - 2(V_a - I_s / \omega_s C_{in1}). \tag{4.61}$$

From (3.58) – (3.61), it can be seen that there is no unity PF condition. When the instantaneous rectified line voltage is higher than $V_{(crit)}$, the circuit operation is the same as that of the VS-CPPFC. When the line voltage becomes lower than $V_{(crit)}$, the circuit operation is the same as that of the VSCS-CPPFC. The voltage stress at light-load operations is high, the same as that in the VS-CPPFC electronic ballast.



(a)



(b)

Figure 4-16. Mode 3 (VS dominates CS). (a) Two five-topology-stage series: If $V_{in(rec)} > V_{(crit)}$, then $(M_1) \rightarrow (M_2) \rightarrow (M_3) \rightarrow (M_4) \rightarrow (M_5) \rightarrow (M_1)$; otherwise, $(M_1) \rightarrow (M_2) \rightarrow (M_3) \rightarrow (M_4) \rightarrow (M_5') \rightarrow (M_1)$, and (b) key waveforms.

The preceding analysis shows that this operation of the VSCS-CPPFC electronic ballast with ICF is very complicated. However, this gives design flexibility to optimize performance. The lamp CF is improved based on the concepts in the VS-CPPFC with ICF and basic VSCS-CPPFC circuits. However, the bus voltage at light-load operation still exists. Experimental results show that the bus voltage stress is somewhere in between those of the VS-CPPFC with ICF and the basic CS-CPPFC electronic ballast.

To verify the analysis, five studied circuits have been implemented. Table 4.1 shows the experimental results. It can be seen that the basic VS-CPPFC electronic ballast has the highest bus voltage stress, a moderate current stress, and the highest lamp current CF. The circuit component count is lowest. The VSCS-CPPFC with ICF electronic ballast dramatically improves the bus voltage stress and lamp CF over those of the basic VS-CPPFC circuit. However, the current stress becomes worse, and another high-frequency capacitor is needed. The basic CS-CPPFC electronic ballast has moderate bus voltage stress, moderate current stress and moderate lamp CF. The circuit component count is lowest. The basic VSCS-CPPFC electronic ballast has improved bus voltage stress, current stress and lamp CF over those of the basic VS-CPPFC and CS-CPPFC circuits. However, as additional high-frequency diode and capacitor are needed. The VSCS-CPPFC with ICF electronic ballast further improves the lamp CF and current stress. Without any feedback control, the circuit can satisfy the lamp CF regulation. The bus voltage stress, however, becomes worse.

Table 4-1. The performance of CPPFC electronic ballasts.

Type	THD	V_{Bmax} (V)	I_s (A)	CF	HF Diodes	HF Capacitors
Basic VS-CPPFC	12%	800	2.4	2.6	2	1
VS-CPPFC w/ICF	6.8%	496	2.6	2.1	2	2
Basic CS-CPPFC	11%	470	2.2	1.9	2	1
Basic VSCS-CPPFC	12.3%	455	1.95	1.8	3	2
VSCS-CPPFC w/ICF	13%	495	1.9	1.6	3	3

4.3 VSCS-CPPFC Electronic Ballast with Lamp Voltage Feedback

This analysis of a family of CPPFC electronic ballasts shows that the high bus voltage stress at light-load operation is a common problem since there is no particular means to reduce the input power at light load. As a result, the bus voltage increases to reduce the input power and maintain power balance, according to the derived line current and input power formulas. If the input power is inherently able to decrease when the load becomes light, then the bus voltage stress can be suppressed. Based on this idea, a new VSCS-CPPFC electronic ballast with lamp voltage feedback (LVFB) mechanism is derived.

As discussed in Section 4.2.3, the voltage source and current source work together to achieve PFC in the VSCS-CPPFC circuits. Due to the negative impedance characteristic of the lamp, the lamp voltage increases when the lamp current decreases, which means the magnitude of the voltage source increases when the load becomes light. In the previous two VSCS-CPPFC electronic ballast circuits, the increase of the magnitude in the voltage source will increase the input power, which will further worsen the bus voltage. If the diode D_{y1} is removed from the basic VSCS-CPPFC circuit, there is no impedance between the loop of the voltage source and the current source, so the current source and the voltage source can be combined as an equivalent current source, as shown in Figure 4-17. The equivalent current source is given by

$$I_{s\_equ} = I_s - \omega_s C_{in1} V_a . \tag{4.62}$$

Therefore, the magnitude of the equivalent current source decreases when the lamp voltage increases. The input power can be reduced through this negative feedback, so as to reduce the bus voltage stress.

The circuit operation is the same as that of the basic CS-CPPFC electronic ballast. The equivalent charge-pump capacitance C_{equ} is given by

$$C_{equ} = C_{in1} + C_y = C_{in} . \tag{4.63}$$

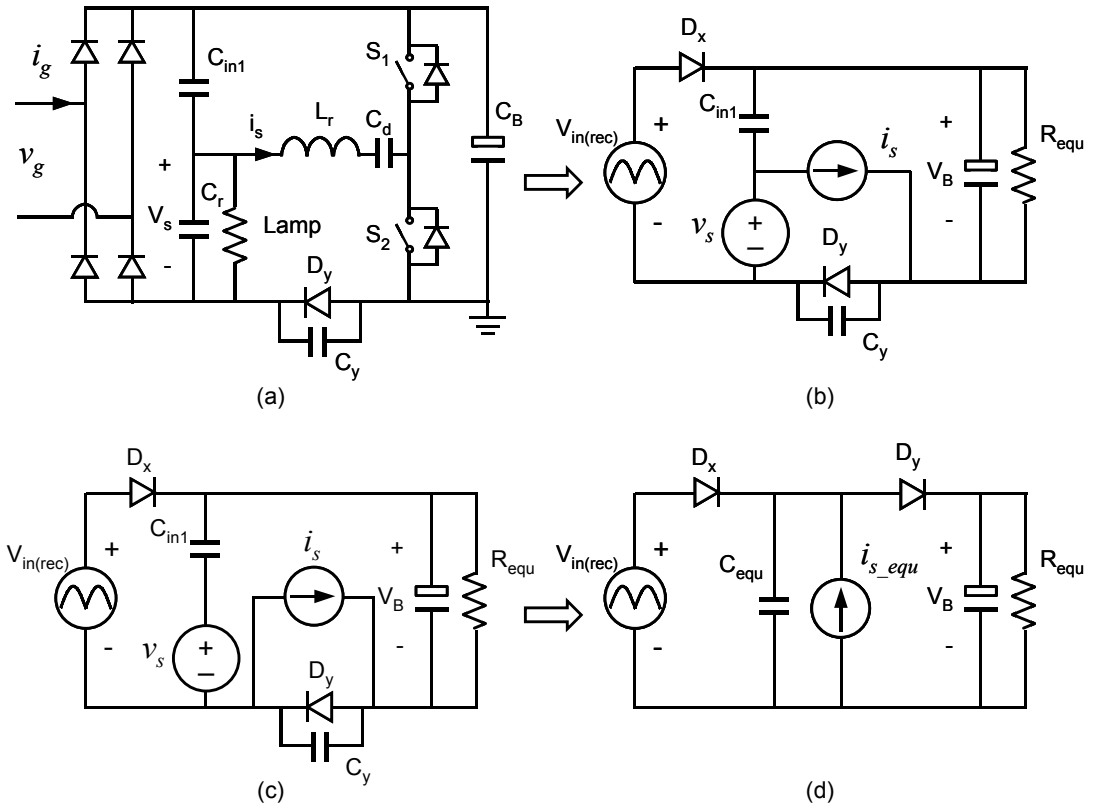


Figure 4-17. (a) VSCS-CPPFC electronic ballast with LVFB, (b) equivalent circuit, (c) CS shifts through VS, and (d) equivalent circuit at a Norton form.

Substituting (4.62) and (4.63) into (4.8) and (4.10) results in

$$i_{in(rec)} = C_{in} f_s \left(\frac{2I_s}{\omega_s C_{in}} - 2\frac{C_{in1}}{C_{in}} V_a - V_B \right) + C_{in} f_s v_{in(rec)}, \text{ and} \tag{4.64}$$

$$P_{in} = \frac{2V_p}{\pi} f_s C_{in} \left(\frac{2I_s}{\omega_s C_{in}} - 2\frac{C_{in1}}{C_{in}} V_a - V_B \right) + \frac{1}{2} C_{in} f_s V_p^2 . \tag{4.65}$$

The unity PF becomes

$$\frac{2I_s}{\omega_s C_{in}} = 2\frac{C_{in1}}{C_{in}} V_a + V_B . \tag{4.66}$$

Under the unity PF condition, the line current and real power become

$$i_{in(rec)} = C_{in} f_s v_{in(rec)}, \text{ and} \tag{4.67}$$

$$P_{in} = \frac{1}{2} C_{in} f_s V_p^2 . \tag{4.68}$$

From (4.66) and (4.68), tank current I_s can be represented under the unity PF condition as

$$I_s = \frac{2\pi P_o V_B}{\eta V_p^2} + \frac{\frac{4\pi C_{in1}}{C_{in}} P_o V_a}{\eta V_p^2} . \tag{3.69}$$

Obviously, (4.64) – (4.66) show that the current source and voltage source have a combined effect on the line current and power. During light-load operations, the output power is very low and the lamp voltage is higher than at normal lighting operation. According to (4.65), the increase of lamp voltage V_a will reduce the input power. Therefore, the bus voltage stress can be suppressed. However, a higher resonant tank current may be needed for a given line voltage and lamp power, according to (4.69).

Although the bus voltage is suppressed, the lamp CF is almost the same as that of the basic CS-CPPFC electronic ballast since their operations are almost the same. To verify the circuit, a prototype is built. The design condition is the same previous five circuits. The electronic ballasts operate with $200V_{rms}$ line input and two 45W lamps in series. The switching frequencies at normal operation and preheat mode are about 56 and 90 kHz, respectively, with 0.5 duty ratio. The circuit parameters are L_r =0.64 mH, C_r =3.9 nF, C_{in1} =20.6 nF, and C_y =39 nF.

Table 4.2 shows the experimental results. It can be seen that the basic VS-CPPFC electronic ballast has the highest bus voltage stress, a moderate current stress, and the highest lamp current CF. The circuit component count is lowest. The VSCS-CPPFC with ICF electronic ballast dramatically improves the bus voltage stress and lamp CF from that of the basic VS-CPPFC circuit. However, the current stress becomes worse and another high-frequency capacitor is needed. The basic CS-CPPFC electronic ballast has moderate bus voltage stress, moderate current stress and moderate lamp CF. The circuit component count is lowest. The basic VSCS-CPPFC electronic ballast has improved bus voltage

stress, current stress and lamp CF are those of the basic VS-CPPFC and CS-CPPFC circuits. However, an additional high-frequency diode and capacitor are needed. The VSCS-CPPFC with ICF electronic ballast further improves the lamp CF and current stress. Without any feedback control, the circuit can satisfy the lamp CF regulation. The bus voltage stress, however, becomes worse. The VSCS-CPPFC with LVFB electronic ballast has the lowest bus voltage stress and a moderate lamp CF. However, the current stress is high.

From the analysis and experimental results, it can be seen that the VSCS-CPPFC with ICF electronic ballast is attractive in the open-loop control application; the proposed VSCS-CPPFC electronic ballast with LVFB is attractive in high-line operation; and the basic CS-CPPFC electronic ballast has potential low cost with good performance.

Table 4-2. The performance of CPPFC electronic ballasts:

Type	THD	V_{Bmax} (V)	I_s (A)	CF	HF Diodes	HF Capacitors
Basic VS-CPPFC	12%	800	2.4	2.6	2	1
VS-CPPFC w/ICF	6.8%	496	2.6	2.1	2	2
Basic CS-CPPFC	11%	470	2.2	1.9	2	1
Basic VSCS-CPPFC	12.3%	455	1.95	1.8	3	2
VSCS-CPPFC w/ICF	13%	495	1.9	1.6	3	3
VSCS-CPPFC w/LVFB	6.7%	450	2.6	2.0	2	2

4.4 Summary

A family of CPPFC electronic ballasts has been investigated, implemented and compared in this chapter. It has been shown that capacitors can be used to achieve PFC function so that the CPPFC techniques appear to be a good alternative approach in electronic ballast applications.

From the analysis and experimental results, the basic VS-CPPFC electronic ballast suffers from the high bus voltage stress and high lamp CF and is not practical in electronic ballast applications. The VS-CPPFC with ICF has improved performance due to the adjustment effect of C_y. However, this option suffers from high current stress. The basic CS-CPPFC electronic ballast has the simplest structure, a moderate bus voltage, moderate switching current and a moderate lamp CF, and is considered as a good topology in electronic ballast applications. The basic VSCS-CPPFC electronic ballast improves the lamp CF, bus voltage stress and current stress of the basic VS-CPPFC and the basic CS-CPPFC electronic ballasts. However, this option increases the complexity of the circuit and the lamp CF still cannot meet the regulation with open-loop control. The VSCS-CPPFC with ICF electronic ballast appears to be the most complicated circuit, but is able to meet the lamp CF regulation without any feedback control. There is a trade-off between the complexity of the power stage and control circuit. The VSCS-CPPFC with LVFB electronic ballast performs well in the high-line application since it has lowest bus voltage. However, this option suffers from high current stress. Therefore, the basic CS-CPPFC electronic ballast shows the most promise in single-stage PFC electronic ballast applications.

The performance of the basic CS-CPPFC electronic ballast will be further improved using the self-oscillating technique, which is the topic of the next chapter.

Chapter 5 High-Frequency Self-Oscillating Electronic Ballasts

5.1 Introduction

Single-stage PFC electronic ballasts have been studied in previous chapters. An assumption has been made that the power switches are driven by some means that has yet to be described. Generally speaking, there are two driving methods for power switches: an external driver and a self-oscillating driver. The external driver has the advantages of flexibility, ease of control, and good sourcing and sinking capability, while the self-oscillating driver has the advantages of simplicity, robustness and low cost.

Figure 5-1 shows an example of an external driver circuit, which includes average lamp-current control with switching frequency modulation, for driving the basic CS-CPPFC electronic ballast [D5]. The purpose of the frequency modulation is to improve the lamp CF and maintain constant lamp power for a certain line-voltage variation. Figure 5-2 shows the lamp current waveforms with and without frequency modulation. The measured CF is improved from 1.85 to 1.54.

However, such a scheme is usually costly to ballast circuits. For example, the oscillator is either synchronized to the resonant network or is swept through resonance to ignite the lamp. A high-voltage IC or a transformer is used to drive the high-side switch. To fulfill the frequency modulation scheme, a lamp-current sensor, error amplifier and timing resistor are used. An auxiliary power supply is also necessary to supply current to the ICs.

In this chapter, a self-oscillating drive is proposed to reduce the complexity and cost of the drive circuit. The proposed self-oscillating drive includes switching frequency modulation to improve the lamp CF and power variation. Experimental results are provided to verify the proposed technique.

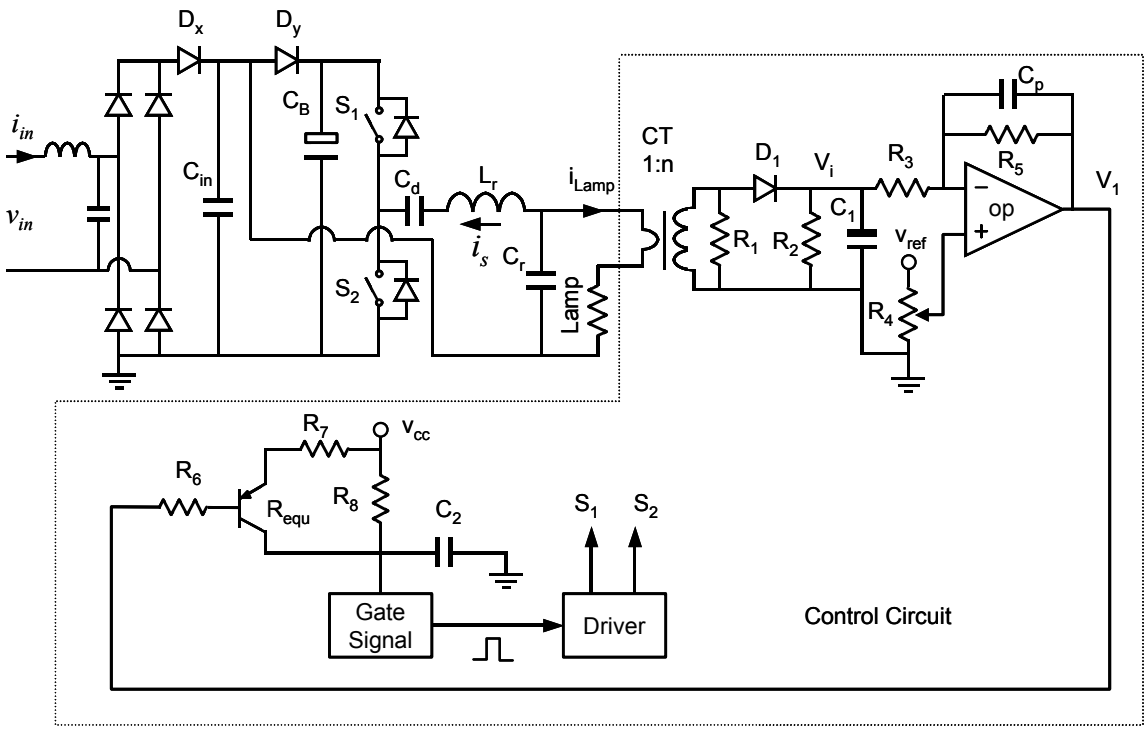


Figure 5-1. Average lamp current control with switching frequency modulation to improve crest factor [D5].

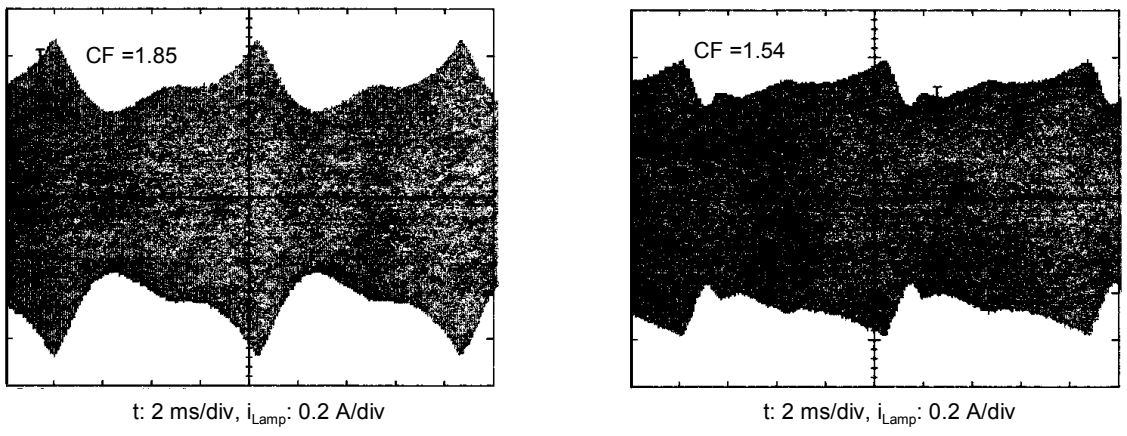


Figure 5-2. (a) Measured lamp current waveform with constant frequency control, and (b) Measured lamp current waveform with switching frequency modulation [D5].

5.2 Single-Stage CS-CPPFC Electronic Ballast with Self-Oscillating Drive

Figure 5-3 shows a conventional MOSFET-based self-oscillating electronic ballast (DC/AC stage), in which two MOSFETs are activated by a driver circuit consisting of a three-winding current transformer (CT) with its primary winding in series with the resonant path and two identical secondary windings to the gates of the transistors for a symmetrical operation. The load resonant circuit of the inverter stage is a series-resonant parallel-loaded tank. The resonant capacitor C_r provides a high striking voltage to the lamp for startup operation and a current path for filament-heating for normal lighting operation.

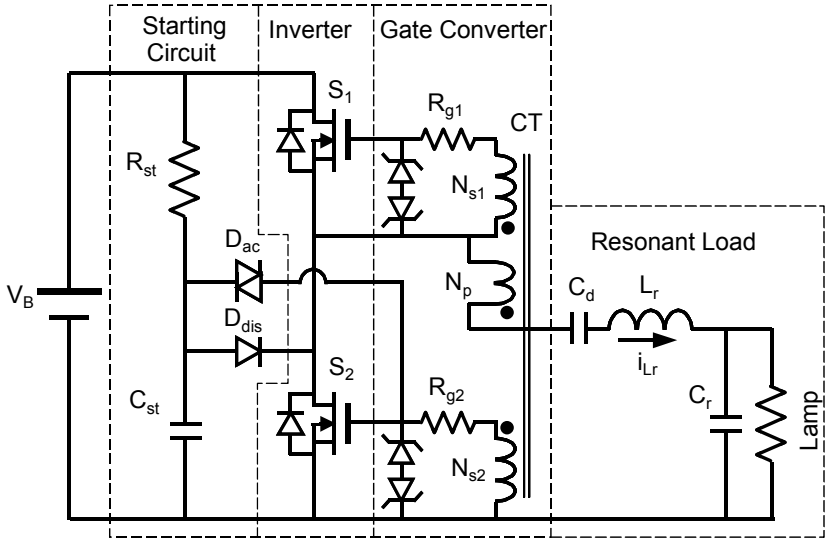


Figure 5-3. Conventional MOSFET-based self-oscillating electronic ballast (DC/AC stage) [E7].

The self-oscillating process is initiated by the starting network, which consists of an RC charging circuit (R_{st} and C_{st}), a diode-AC switch (DIAC) D_{ac}, and a discharging diode D_{dis}. Within approximately one second after power is applied, the voltage across C_{st} will reach about 30V break-over voltage of D_{ac}. With the D_{ac} conducting, a positive turn-on voltage pulse is applied to the gate of S_2. When S_2 is turned on by this pulse, the drain voltage of S_2 is rapidly switched to ground, and thus initiates the resonant circuit oscillation. Once the circuit is started, proper design of the circuit parameters will lead to

the self-oscillating mode. With S_2 switching each half cycle, any charge developed across C_{st} is discharged through D_{st}, preventing a build-up voltage of further startup pulses.

If the starting network is not considered, the operation of the self-oscillating electronic ballast can be represented by a system block diagram, as shown in Figure 5-4. In the block diagram, the transfer function G(s) is associated with the load resonant circuit. The input of G(S) is the inverter output voltage and the output is the feedback variable, i_{Lr}. The feedback variable is sensed by CT and fed into the gate converter, which is represented by a transfer function H(S). H(S) provides the gate voltages to the switches. Finally, a hard-limit block is used to represent the inverter. From the block diagram, it can be seen that the operation of the circuit is self-sustained. The switching frequency is no longer externally imposed, but is determined by the circuit parameters.

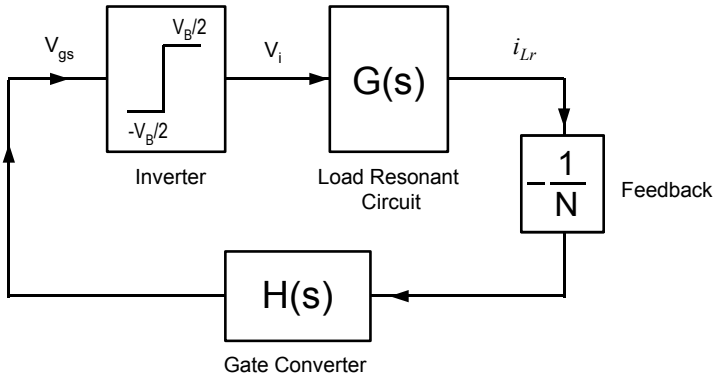
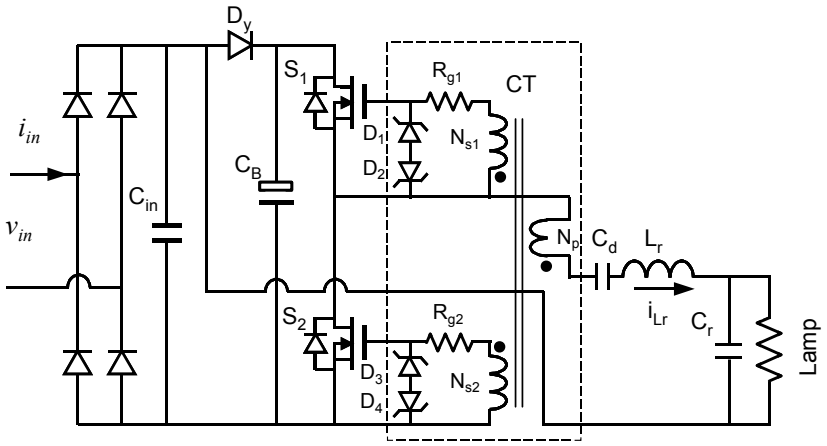


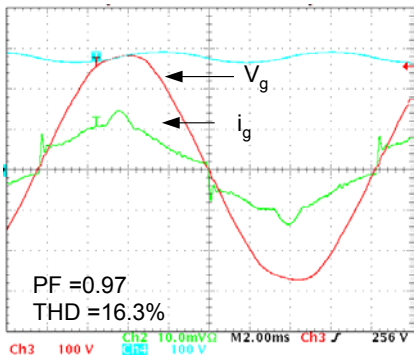
Figure 5-4. System diagram of the self-oscillating electronic ballast.

While this self-oscillating circuit is elegantly simple, the performance is not satisfactory if it is directly applied to the single-stage CS-CPPFC electronic ballast circuit. Figure 5-5 shows the circuit implementation and experimental results. It can be seen that the line current shows great distortions near the line peak and the zero crossing. The lamp envelope appears as a high ripple current with a measured CF as high as 1.88. Moreover, the lamp power is very sensitive to the line voltage variations. The measured lamp power variation is around ±14.5% with respect to the ±10% line voltage variation.

Large lamp CF and power variation deteriorate lamp life. To maintain lamp life, lamp CF should be lower than 1.7 and lamp power variation should be limited within ±10%.



(a)



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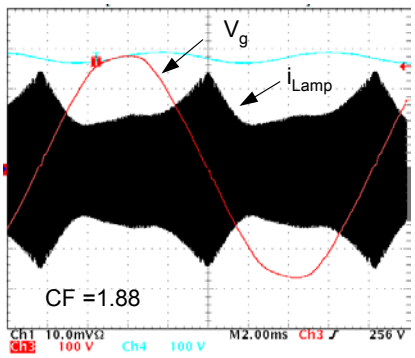


(c)

Figure 5-5. Single-stage self-oscillating CPPFC electronic ballast: (a) circuit diagram, (b) measured line current waveform, and (c) measured lamp current waveform.

In order to improve lamp CF and power variations, a proper control signal should be introduced into the self-oscillating system. Figure 5-6 shows the system block diagram, in which a control signal is applied to the gate converter. However, due to the self-sustained operation of the circuit, the control of circuit operation is usually not easy. In order to find a way to change the circuit operation, the operation principle is first studied.

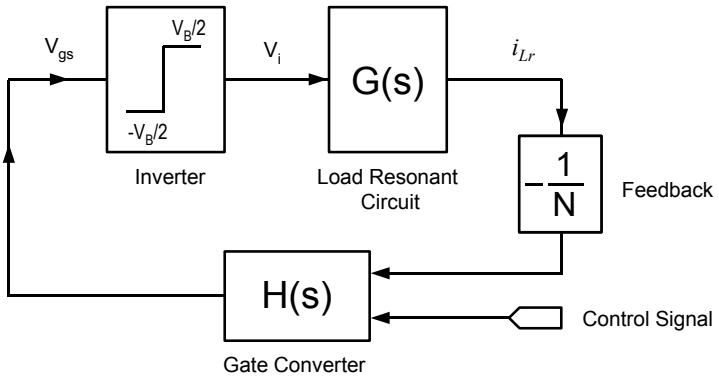


Figure 5-6. System diagram of self-oscillating electronic ballast with control signal.

5.3 Operation Principle and Control Aspect of the Self-Oscillating Electronic Ballast

5.3.1. Operation Principle of the Self-Oscillating Electronic Ballast

Circuit models should first be established in order to approximate the actual component behavior.

The MOSFET is used as a switch to control the power flow to the load. The MOSFET moves the i_D-v_{DS} characteristics from the cutoff region through the saturation region to the linear region as it turns on, and reverses its path when it turns off. Figure 5-7(a) shows the output characteristics of an n-channel MOSFET [F22, p575]. When the gate-source voltage V_{GS} is less than the threshold voltage $V_{GS(th)}$, the MOSFET is in the cutoff region. Power MOSFETs have a $V_{GS(th)}$ that is typically between 3 V and 6 V. When the gate-source voltage is sufficiently large, namely V_{GS}-$V_{GS(th)}$ >V_{DS} >0, the MOSFET operates in the linear region (on-state). The drain-to-source voltage V_{DS} is roughly proportional to the drain current I_D. Between the cutoff and linear regions is a saturation region. In the saturation region, the current flowing through the channel no longer depends on the drain-source voltage, and is given approximately by the equation $i_D = k\left(v_{GS} - V_{GS(th)}\right)^2$, as shown in Figure 5-7(b). Two circuit models therefore exist

corresponding to the different operation of the MOSFET. When the MOSFET is in the cutoff or saturation region, the equivalent circuit in Figure 5-7(c) is valid. When the MOSFET is in the linear region, the equivalent circuit in Figure 5-7d is valid. An appropriate circuit model is used in the analysis of circuit operation.

In order to simplify the analysis, an ideal Zener diode is assumed. The *i-v* characteristic of the back-to-back Zener diode pairs is given by

$$v_z = \begin{cases} V_z & i_z > 0 \\ (-V_z, V_z) & i_z = 0 \\ -V_z & i_z < 0 \end{cases}, \tag{5.1}$$

where V_z equals the sum of the Zener clamping voltage and forward drop voltage.

The current transformer can be modeled as a current-controlled current source shunted by a magnetizing inductor L_m referred to the transformer secondary. Two gates are connected via an ideal 1:1 transformer. The ideal transformer obeys the relationships of v_{s1}=-v_{s2} and i_{s1}=i_{s2}.

Using the preceding circuit models, the self-oscillating circuit of Figure 5-3 can be simplified, as shown in Figure 5-8. In steady state, eight topological stages exist over one switching cycle. Due to the symmetrical operation, half switching cycle operation is discussed, as shown in Figure 5-9. Figure 5-10 shows the key switching waveforms.

Stage 1 [t_0, t_1]: Assume at t_0 the feedback current i_s is bigger than the magnetizing current i_m, and V_{gs2} is clamped by the Zener diodes. Due to the positive volt-second applied, i_m linearly increases. The i_s changes in a resonant waveform. This stage ends when i_m reaches i_s at t_1. During this stage i_m is given by

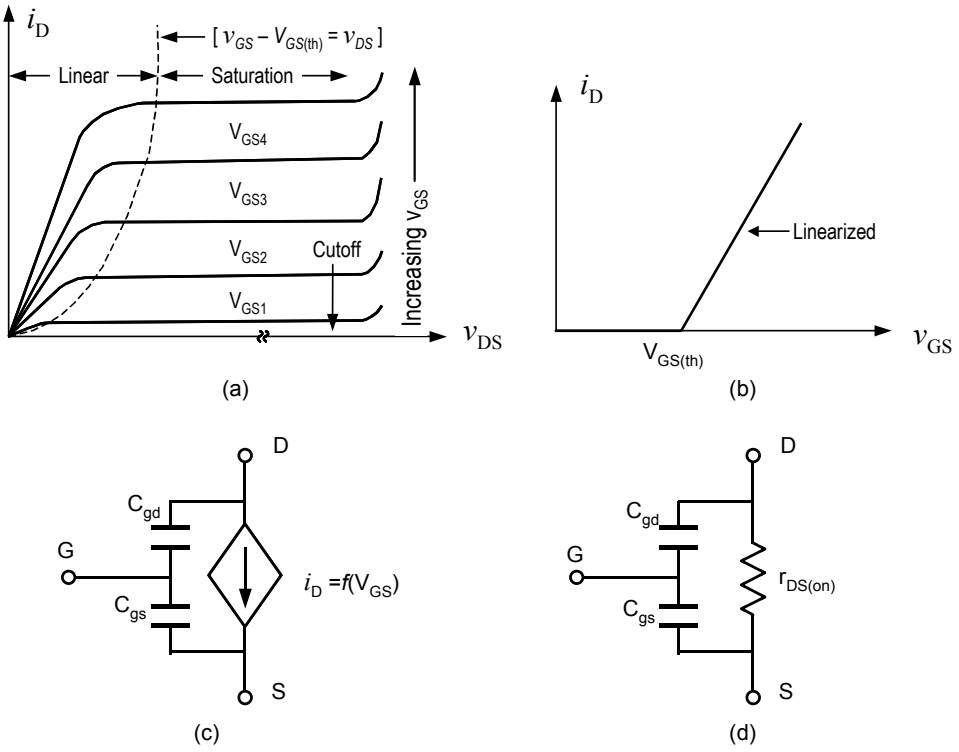


Figure 5-7. Characteristics and equivalent circuit models of an n-channel MOSFET: (a) output characteristics, (b) transfer curve, (c) equivalent circuit in cutoff or saturation region, and (d) equivalent circuit in the linear region [F22].

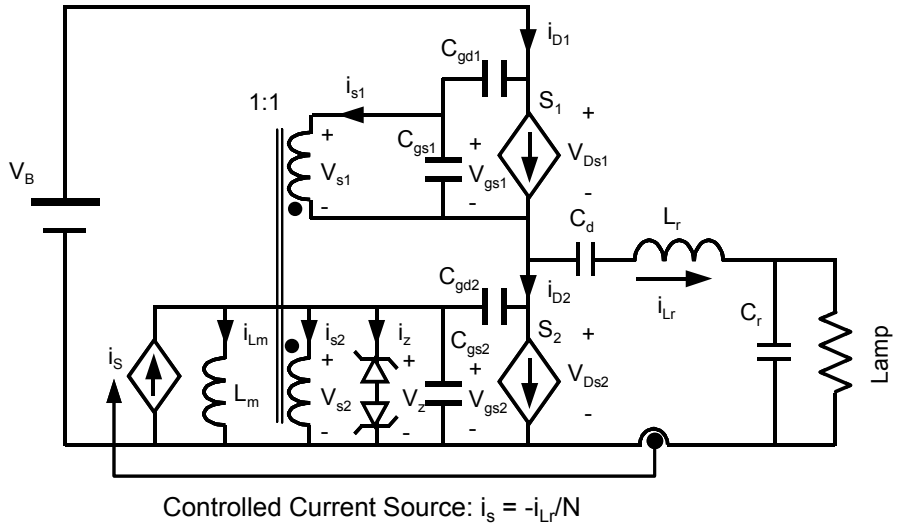


Figure 5-8. Simplified circuit model of self-oscillating electronic ballast.

$$i_m(t) = \frac{1}{L_m}\int_{t_0}^{t_1} V_z dt + I_{m0} = \frac{V_z}{L_m}(t_1 - t_0) + I_{m0}, \tag{5.2}$$

where I_{m0} is the initial magnetizing current at t_0.

Stage 2 [t_1, t_2]: Since i_m reaches i_s at t_1, the Zener diodes becomes unclamped and the gate capacitors appear, causing resonance with the magnetizing inductor. The energy stored in the gate capacitors starts transferring to the magnetizing inductor. V_{gs2} decreases and V_{gs1} increases. S_1 still carries the full resonant current until the gate voltage drops to a level of $V_{gs(I\_o)}$, which is the gate-source voltage from the transfer curve of Figure 5-7(b) needed to maintain $i_D = i_{Lr}$.

Stage 3 [t_2, t_3]: V_{gs2} becomes temporarily clamped at $V_{gs(I\_o)}$ at time t_2. Part of the resonant current flows through the Miller capacitors C_{gd2} and C_{gd1} so that V_{DS2} increases and V_{DS1} decreases, as shown in Figure 5-10(c). This mode ends when V_{DS2} reaches the bus voltage at t_3 and the body diode of S_1 is turned on.

Stage 4 [t_3, t_4]: Once the drain-to-source voltage of S_2 reaches the bus voltage, V_{gs2} becomes unclamped and continues its drop. Meanwhile, the drain current of S_2, i_{DS2}, decreases according to the transfer curve of Figure 5-7(b). The difference between i_{Lr} and i_{DS2} is carried by the body diode of S_1. This commutation ends when V_{gs2} drops below the threshold voltage and S_2 is turned off. V_{gs2} continues its drop until it is reverse-clamped by the Zener diode at t_4, and the next half switching cycle begins.

The preceding analysis shows that the switching period is mainly determined by the interval of Stage 1 (Stage 5), during which the magnetizing inductor is linearly charged (discharged) by the Zener clamping voltage. The interval of Stage 2 (Stage 6) causes a considerable amount of delay due to the effects of the gate charge. The instantaneous power loss occurs, however, primarily during the crossover time in Stage 3 (Stage 7) where $p(t) = v_{DS}i_D$ is high. When subjected to extreme fluctuations, circuit reliability and overall efficiency are impaired.

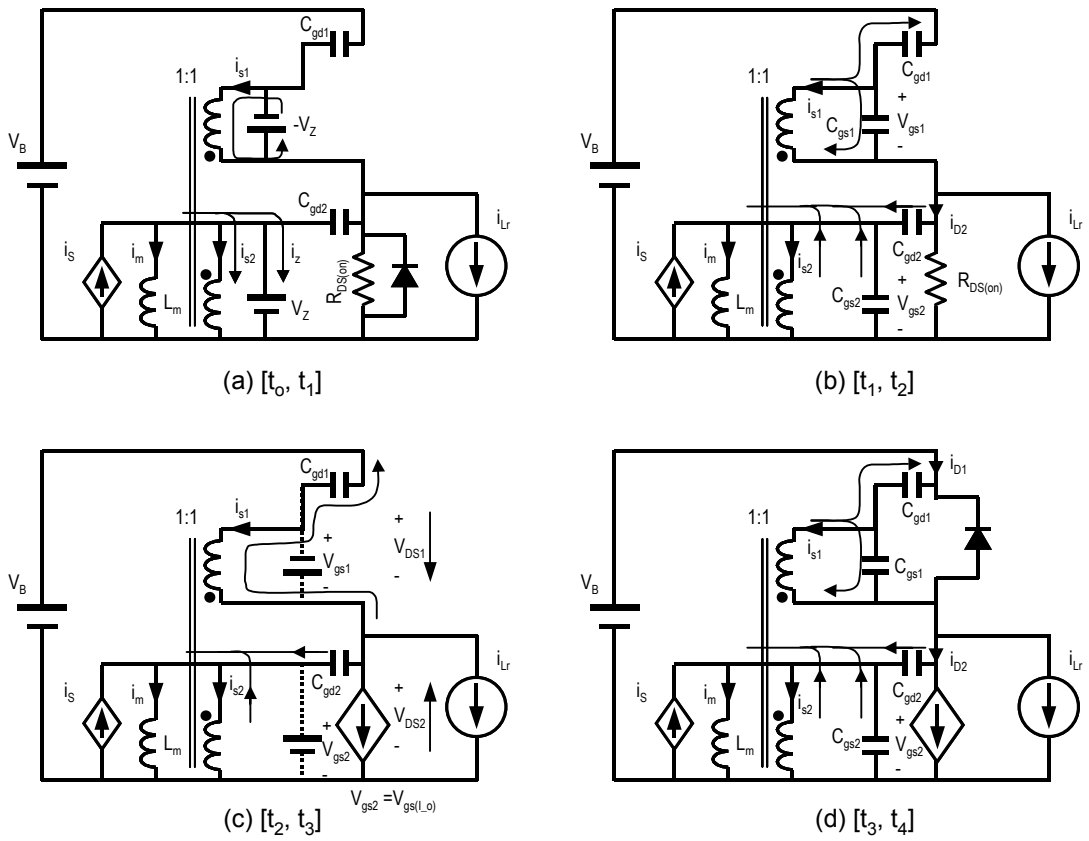


Figure 5-9. Topological stages over a half-switching cycle.

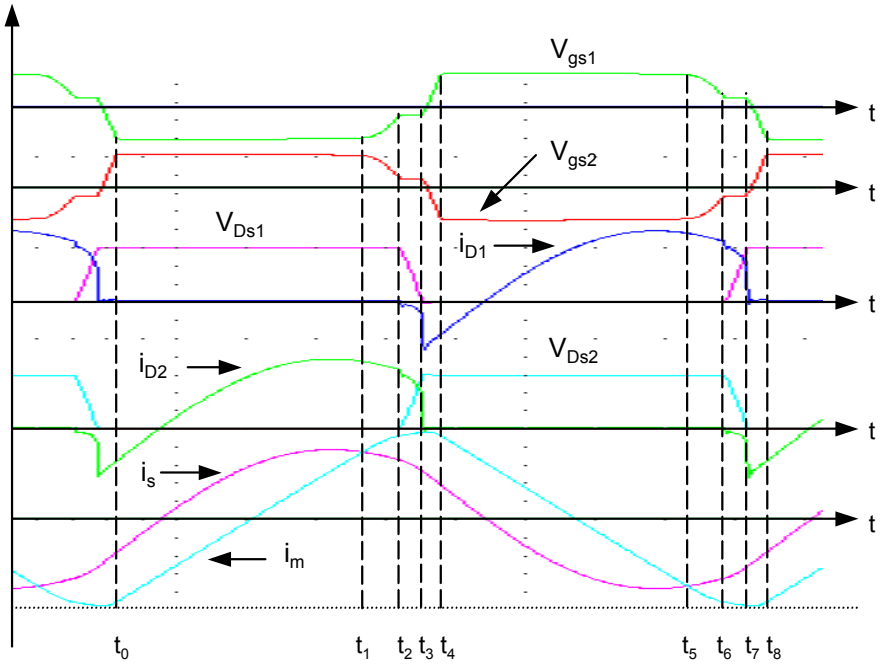


Figure 5-10. Key waveforms.

To reduce the turn-off losses, a speed-up winding and current amplifier circuit could be added as shown in Figure 5-11(a). The square wave output voltage of the inverter is coupled through C_{sp} to the winding N_{sp}. A regenerative switching action is generated, which speeds up the charge and discharge of the MOSFET gate capacitances, as shown in Figure 5-11(b). It can be seen that the intervals of Stage 2 to Stage 4 are reduced. With the reduction of overlapping interval of voltage and current, the turn-off losses are reduced dramatically. Experimental results show that efficiency is improved by about 4.4%.

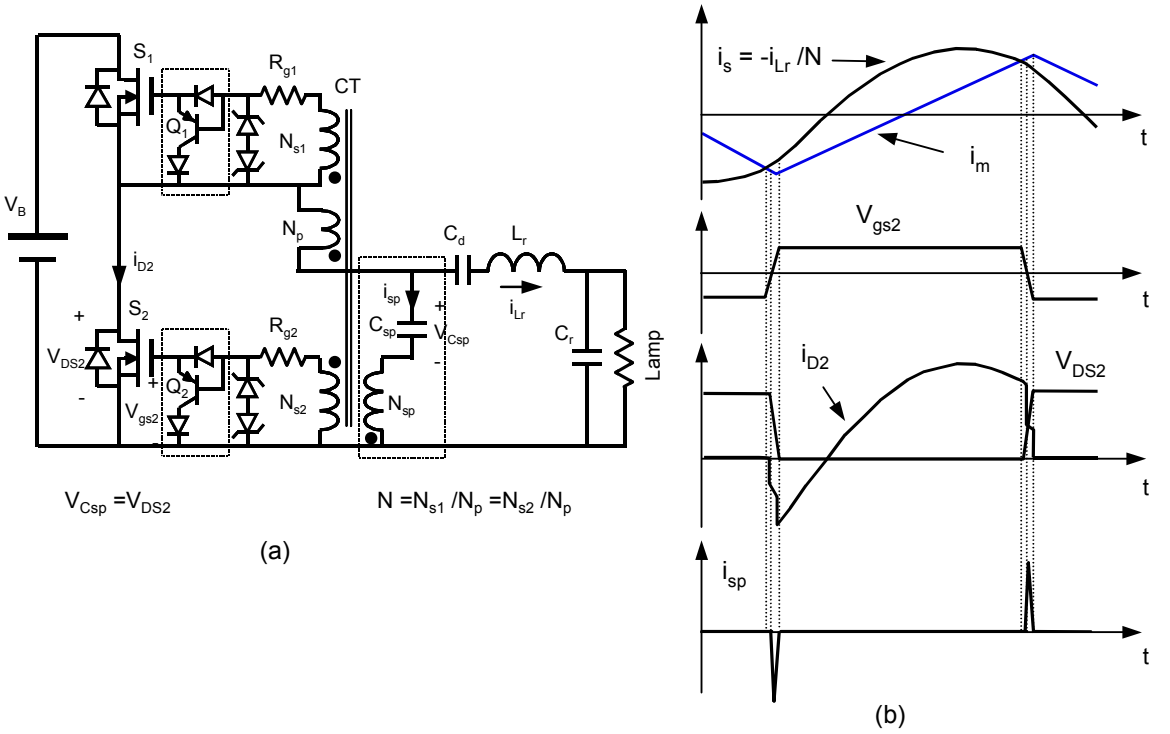


Figure 5-11. Self-oscillating electronic ballast with speed-up winding and current amplifier circuit to reduce turn-off losses: (a) circuit diagram, and (b) key waveforms.

5.3.2 Prediction of the Operation Frequency of the Self-Oscillating Electronic Ballasts

Generally, the condition of stable self-oscillation is governed by the Barkhausen criterion, which states that a unity loop gain is required to sustain stable oscillations in the system [E15]. The Barkhausen criterion implies both unity magnitude and a phase angle of 2kπ, which can be expressed in symbolic form as follows [E8]:

$$G(s)\cdot H(s)\cdot I(s) \rightarrow G(j\omega)\cdot H(j\omega)\cdot I(j\omega) = 1\angle 2k\pi\,, \tag{5.3}$$

where G(s), H(s) and I(s) are the transfer functions of the load resonant circuit, gate converter and the inverter plus feedback network, respectively.

The Barkhausen criterion is used to predict the self-oscillating frequency. To simplify the analysis, the following assumptions are made:

- Ideal MOSFETs with zero conduction losses, zero gate capacitances, and zero drain-to-source transition time are used;
- Ideal Zener diodes are used; and
- Only fundamental components are considered.

Under these assumptions, a simplified equivalent circuit and its switching waveforms are obtained, as shown in Figure 5-12. The switching waveforms are very close to those in Figure 5-11. Using fundamental approximation, the fundamental voltage $v_{i(fund)}$ applied to the resonant tank, the resonant inductor current i_{Lr} and lamp RMS voltage V_{la} are given by

$$v_{i(\,fund\,)} = -\frac{2V_B}{\pi}\sin(\omega t + \phi)\,, \tag{5.4}$$

$$i_{Lr}(t) = -I_p \sin\omega t\,, \text{ and} \tag{5.5}$$

$$V_{la} = \frac{\sqrt{2}V_B}{\pi}\frac{1}{\sqrt{\left(1-f_n^2\right)^2 + \left(\frac{f_n Z_o}{R_{la}}\right)^2}}\,, \tag{5.6}$$

where V_B, ω, ϕ, I_p, Z_o, f_n and R_{la} are the bus voltage, switching frequency, phase lag of i_{Lr} with respect to $v_{i(fund)}$, resonant inductor peak current, tank characteristic impedance, normalized switching frequency and lamp resistance, respectively. $Z_o = \sqrt{L_r / C_r}$, $f_n = f / f_o = \omega / \omega_o$, and $f_o = 1/\left(2\pi\sqrt{L_r C_r}\right)$. The lamp is assumed to be a pure power-dependent resistor in steady state, which is given by

$$R_{la} = \frac{V_{la}^2(P)}{P}, \text{ and} \tag{5.7}$$

$$V_{la}(P) = a_0 + a_1 \cdot P + a_2 \cdot \exp(a_3 \cdot P), \tag{5.8}$$

where V_{la}(P) is lamp RMS voltage, P is the lamp power, and a_0-a_4 are parameters determined from the measured lamp data.

The phase lag ϕ is given by

$$\phi = \arctan\left\{\frac{R_{la}}{Z_o} f_n \left[f_n^2 + \left(\frac{Z_o}{R_{la}}\right)^2 - 1 \right]\right\}. \tag{5.9}$$

The resonant inductor peak current I_p is given by

$$I_p = \frac{2V_B}{\pi \cdot Z_o} \sqrt{\frac{1 + \left(\frac{R_{la}}{Z_o}\right)^2 f_n^2}{\left(\frac{R_{la}}{Z_o}\right)^2 \left[1 - f_n^2\right]^2 + f_n^2}}. \tag{5.10}$$

Therefore, the feedback current i_s is given by

$$i_s(t) = -\frac{i_{Lr}(t)}{N} = \frac{I_p}{N} \sin \omega t, \tag{5.11}$$

where N (=N_{s1}/N_p =N_{s2}/N_p) is the turns ratio of the current transformer *CT*.

Assume θ is the phase angle between the current applied to the CT and the winding voltage induced. Therefore, the magnetizing current i_m is given by

$$i_m(t) = \frac{V_z}{L_m}\left(t + \frac{\theta}{\omega} - \frac{\frac{\pi}{2}}{\omega}\right) = \frac{V_z}{L_m}\left(t - \frac{\frac{\pi}{2} - \theta}{\omega}\right), \tag{5.12}$$

where L_m is the magnetizing inductance seen from the secondary winding and V_z is the Zener clamping voltage.

At $t_1 = \dfrac{\pi - \phi}{\omega}$, i_m reaches i_s and i_z changes polarity, resulting in the change of gate-voltage polarity. Therefore, S_2 is turned off at t_1. The values of i_s and i_m are given by

$$i_s(t_1) = \frac{I_p}{N}\sin(\pi - \phi) = i_m(t_1) = \frac{\pi V_z + 2(\theta - \phi)V_z}{2\omega L_m}. \tag{5.13}$$

Based on the Barkhausen criterion, θ equals ϕ in order to sustain oscillations, which results in

$$\frac{I_p}{N}\sin\phi = \frac{\pi V_z}{2\omega L_m},$$

or

$$\frac{2V_B}{N\pi Z_o}\sqrt{\frac{1+\left(\frac{R_{la}}{Z_o}\right)^2 f_n^2}{\left(\frac{R_{la}}{Z_o}\right)^2\left[1-f_n^2\right]^2 + f_n^2}}\sin\left(\arctan\left\{\frac{R_{la}}{Z_o}f_n\left[f_n^2 + \left(\frac{Z_o}{R_{la}}\right)^2 - 1\right]\right\}\right)$$

$$= \frac{\pi V_z}{2 f_n \omega_o L_m}. \tag{5.14}$$

Equation (5.14) is complicated and it is hard to get a closed-form solution of the self-oscillating f_s ($=f_n \bullet f_o$). Theoretically, given bus voltage V_B, lamp impedance R_{la}, resonant components L_r, C_r, Zener clamping voltage V_z and current transformer parameters N and L_m, the numerical solution of f_s can be obtained from (5.14). However, there is an easy way to find the relationship between f_n and V_z. Given lamp power P, the lamp impedance R_{la} and lamp voltage V_{la} are obtained from (5.7) and (5.8), respectively. Substituting obtained R_{la} and V_{la} into (5.6), f_n is obtained for the given lamp power P. Substituting calculated R_{la} and f_n into (5.14), V_z is obtained. Figure 5-13 shows the calculated curve.

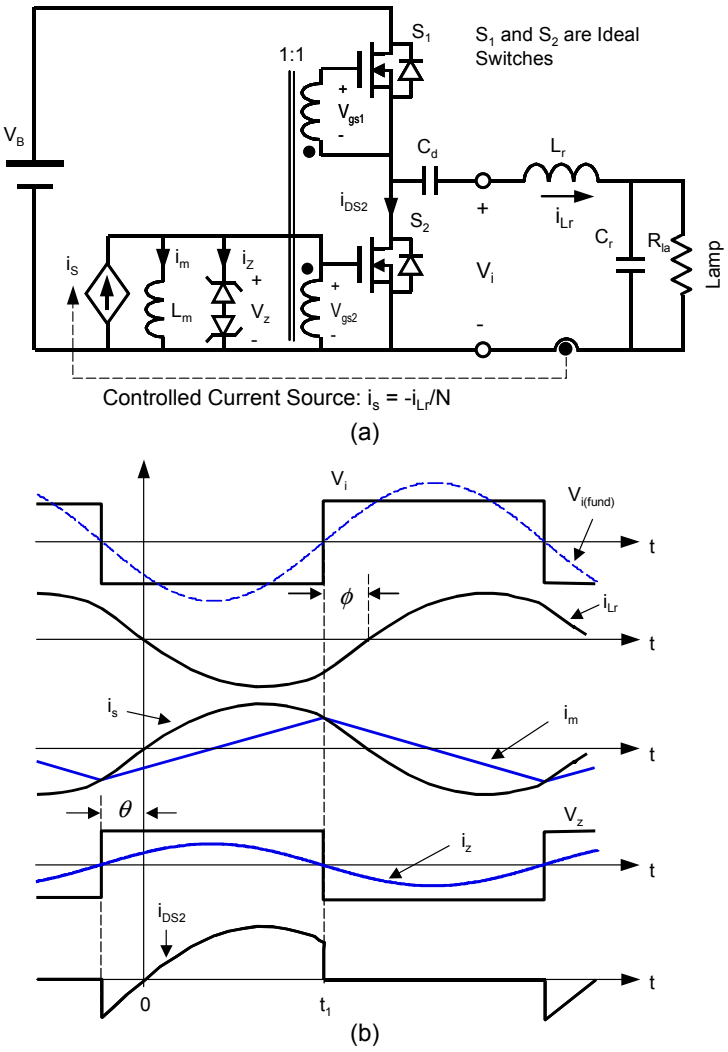


Figure 5-12. (a) Simplified equivalent circuit of self-oscillating electronic ballast showing reference directions of currents and voltages, and (b) key waveforms.

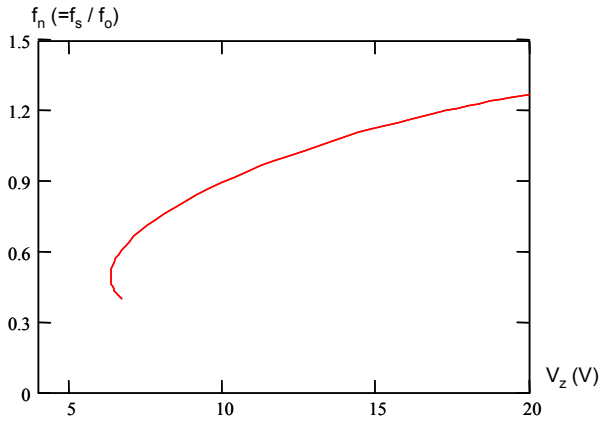


Figure 5-13. Calculated self-oscillating frequency as a function of winding voltage.

5.3.2 Control of the Self-Oscillating Electronic Ballasts

Equation (5.14) gives the relationship between the self-oscillating frequency and Zener diode voltage V_z. From Figure 5-13, it can be seen that f_s increases with V_z. Therefore, one way to change switching frequency is to make the Zener clamping voltage controllable. However, this is usually not easy. An equivalent circuit should be used. Figure 5-14 shows a conceptual circuit diagram and key waveforms, in which the switching frequency is controlled by a variable voltage source V_{ctrl}. As seen from the graphic illustrations, the higher the V_{ctrl}, the higher the switching frequency. Therefore, this method is called self-oscillating control with winding voltage modulation.

To verify the proposed control concept, a prototype is built, which has circuit parameters of: L_r =1.56mH, C_r =5.6nF, V_B =300V, and CT components of n_p =1 turn ($L_{m(p)}$ =2.157μH) and n_s =71 turns on a TDK PC 40 EI16 core [E16]. The circuit diagram is shown in Figure 5-15; the winding voltage is controlled by a voltage source V_{ctrl} and the polarity is controlled by the sign of secondary winding current i_z. Figure 5-16 shows the experimental results. The measured self-oscillating frequency increases from 25.6 kHz to 59.2 kHz when the control voltage V_{ctrl} changes from 5.5 V to 13.8 V. The corresponding lamp power decreases from 45 W to 27 W.

The proposed control concept can be applied to the single-stage CS-CPPFC electronic ballast, as shown in Figure 5.17, in which the lamp current is sensed via a current transformer. The sensed current is converted into a voltage, which functions as V_{ctrl} in Figure 5-15. When the lamp current increases, V_{ctrl} increases, so switching frequency also increases. The lamp current then decreases. Lamp current negative feedback is thus introduced via the proposed concept. Figure 5-17(b) shows the experimental waveforms. It can be seen that THD and PF improve. The lamp CF reduces from 1.88 to 1.6. The lamp power variation reduces from ±14.5% to ±12%. However, high ripple current still exists in the lamp current envelope, and this may shorten lamp life. To further improve the lamp CF and power variation, another switching frequency modulation method is proposed next.

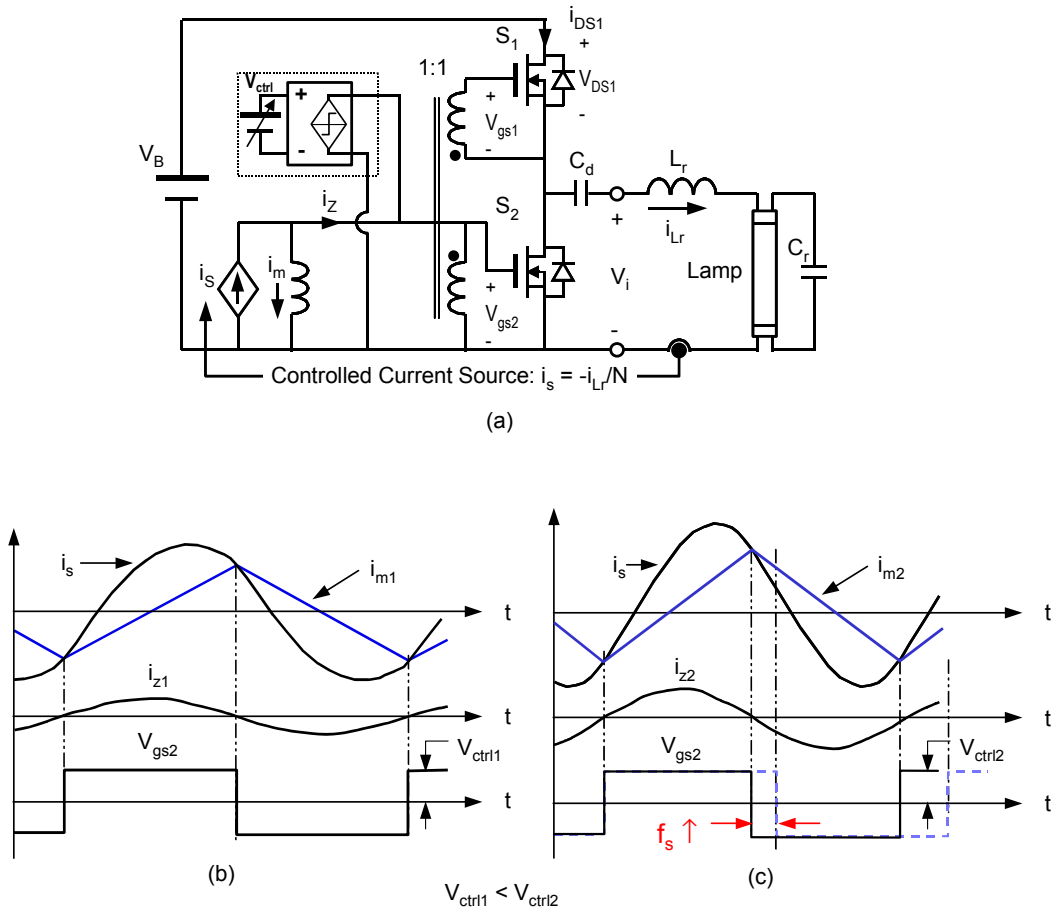


Figure 5-14. Conceptual self-oscillating electronic ballast with winding voltage modulation: (a) circuit diagram, (b) key waveforms with V_{ctrl1}, and (c) key waveforms with V_{ctrl2}, where $V_{ctrl2} > V_{ctrl1}$.

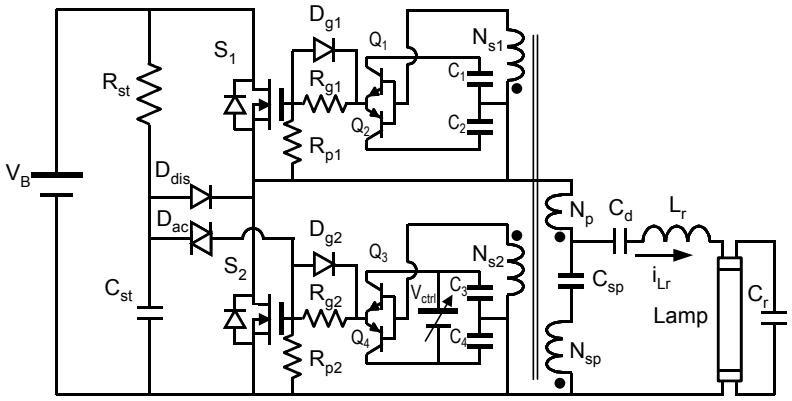
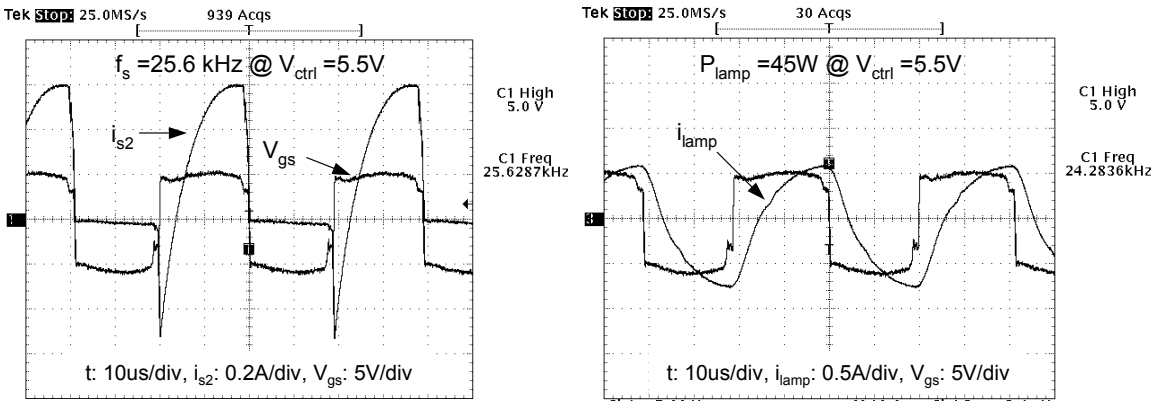
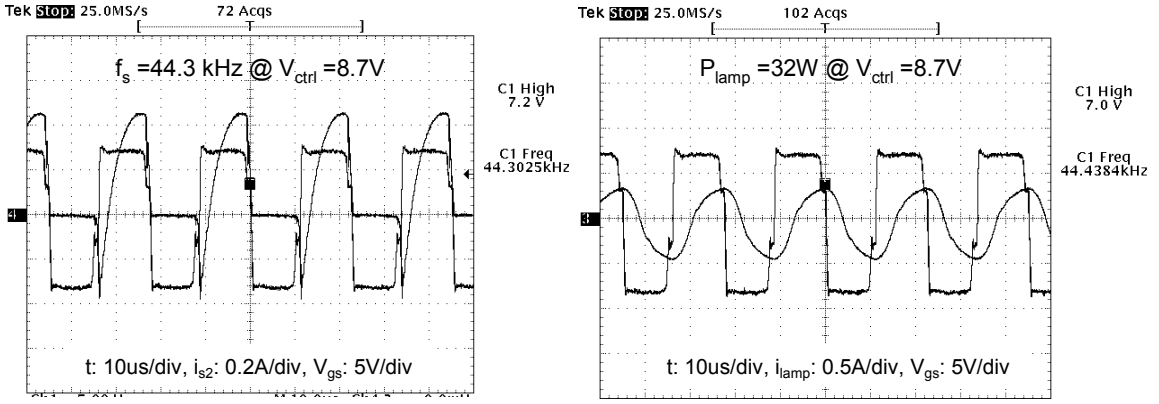


Figure 5-15. Implementation of self-oscillating electronic ballast with winding voltage control.



(a)



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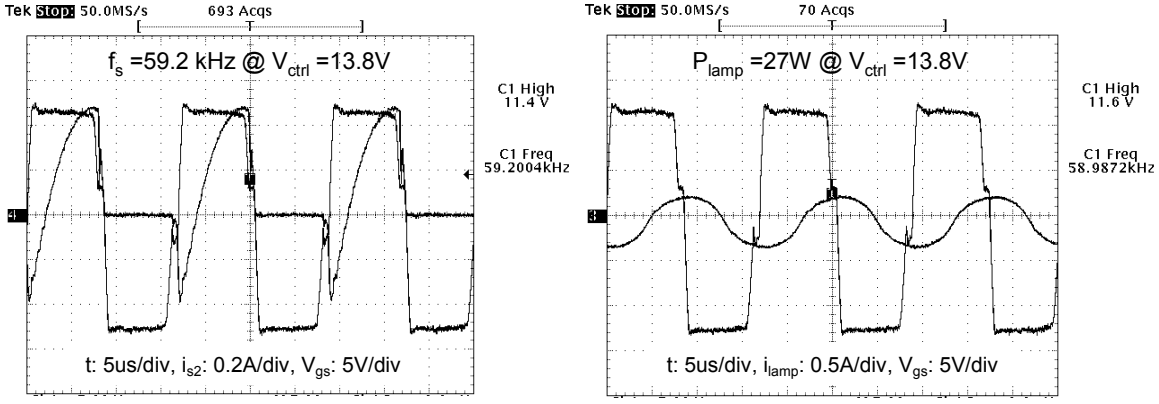
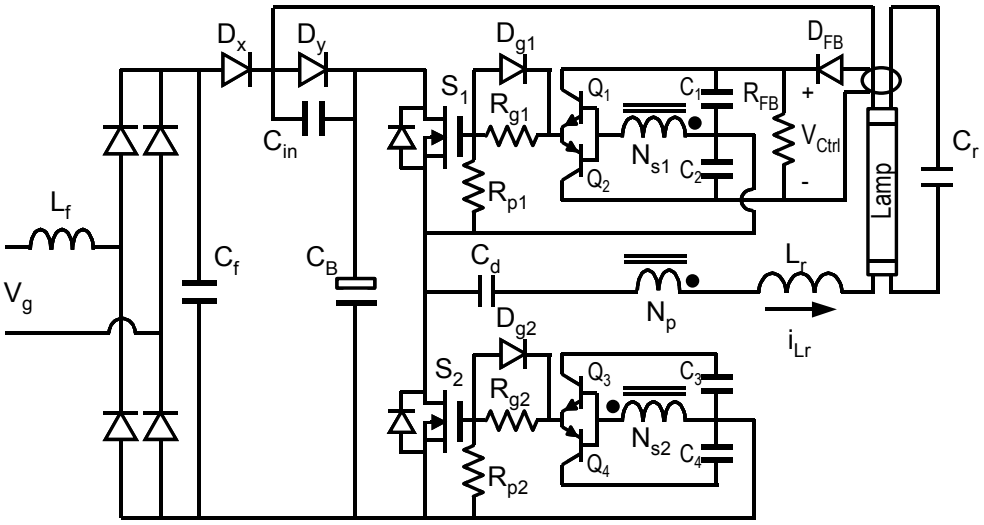
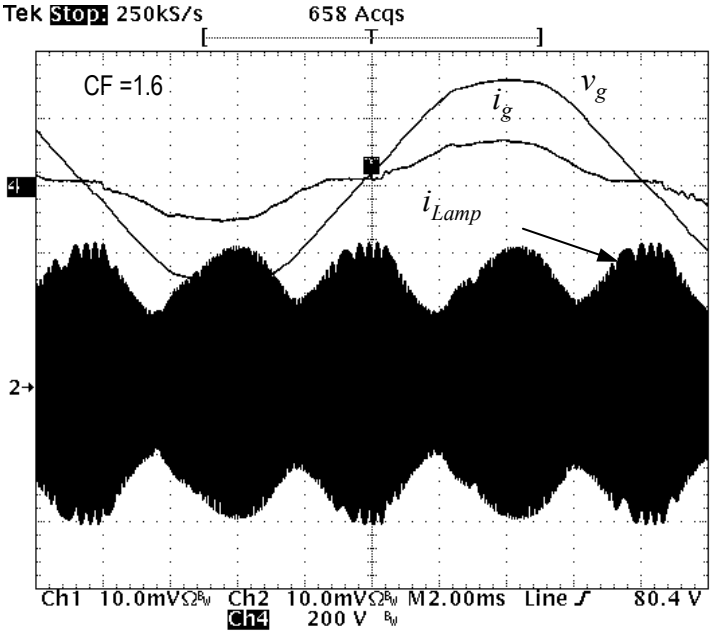


(c)

Figure 5-16. Measured switch current, lamp current and gate voltage at different control voltages: (a) V_{ctrl} =5.5 V, f_s =25.6 kHz and P_{lamp} =45 W, (b) V_{ctrl} =8.7 V, f_s =44.3 kHz and P_{lamp} =32 W, and (c) V_{ctrl} =13.8 V, f_s =59.2 kHz and P_{lamp} =27 W.



(a)



(b)

Figure 5-17. Circuit implementation of single-stage self-oscillating CS-CPPFC electronic ballast with winding voltage modulation: (a) circuit diagram, and (b) measured lamp current waveform and input current waveform.

Another way to control the operation frequency is to introduce a controllable current signal i_{inj} so that the turn-off instant of switch changes with i_{inj}. A conceptual circuit diagram and key waveforms with and without current injection are shown in Figure 5-18. Accordingly, the current relationship at $t_1 = \dfrac{\pi - \phi}{\omega}$ becomes

$$\frac{2V_B}{N\pi Z_o}\sqrt{\frac{1+\left(\frac{R}{Z_o}\right)^2 f_n^2}{\left(\frac{R}{Z_o}\right)^2\left[1-f_n^2\right]^2+f_n^2}}\sin\left(\arctan\left\{\frac{R}{Z_o}f_n\left[f_n^2+\left(\frac{Z_o}{R}\right)^2-1\right]\right\}\right)$$

$$=\frac{\pi V_m}{2f_n\omega_o L_m}+I_{inj\_m}, \tag{5.15}$$

where I_{inj_m} is the injected current magnitude at time t_1. Therefore, switching frequency is a function of I_{inj_m}. Figure 5-19 is a numerical curve obtained from (5.15), which shows that switching frequency increases as I_{inj_m} increases.

The current injection concept can be implemented by current transformer through additional winding since the current transformer can be regarded as a current-mixing network defined by

$$n_{s2}i_m = n_p i_p + n_{s1}i_{s1} + n_{s2}i_{s2} + n_{inj}i_{inj} + \ldots, \tag{5.16}$$

where n_p, n_{s1}, n_{s2}, n_{inj}, … are transformer winding turns, and I_p, i_{s1}, i_{s2}, i_{inj}, … are the corresponding winding currents. The i_m is the magnetizing current, referred to the n_{s2} winding.

The next step is to find a suitable current signal, which helps to reduce the lamp CF and lamp power variation. From the measured lamp current waveform in Figure 5-2(a), the lamp current is large near the line-zero crossing and small near the line-peak voltage. It is required that the switching frequency is high near line-zero crossing and low near line-peak voltage; therefore, the magnitude of the injected current is large near-line zero crossing and low near line-peak voltage. The current through the charge-pump capacitor C_{in} fits the requirement, and can be injected into the gate converter via winding n_{inj}, as shown in Figure 5-20. A small capacitor C_{inj} (=390 pF) is used to adjust the magnitude.

The turns of the current transformer are: n_p =2 turns, and n_{s1} =n_{s2} =n_{sp} =n_{inj} =33 turns on a TDK PC40 EI-16 core. The measured line current waveforms with ±10% line voltage variations are also shown in Figure 5-20. Good PF and THD are achieved. Figure 5-21 shows the measured switching waveforms near the line-zero crossing, line-half voltage, and line-peak voltage. The corresponding frequencies are 50 kHz, 44.5 kHz and 37.3 kHz. A good frequency modulation is achieved. Figure 5-21 also shows the measured lamp current waveforms with ±10% line voltage variations. The corresponding lamp CFs are 1.48, 1.49 and 1.46. From the lamp current waveforms, it can be seen that the proposed current injection approach has a better control effect than either the proposed winding voltage modulation or the average lamp current feedback control proposed in other research [D5] because it modulates the switching frequency cycle by cycle. The measured lamp power variations are (-8.7%, 9.5%), within the ±10% requirement.

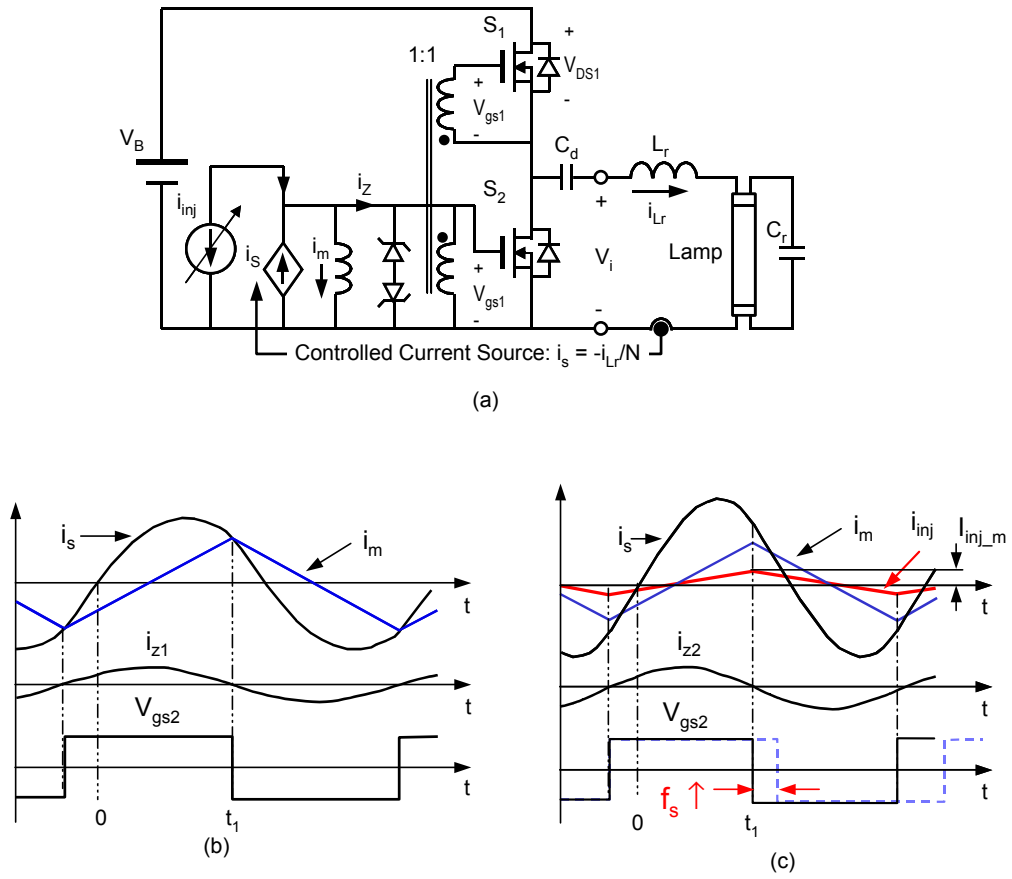


Figure 5-18. Conceptual self-oscillating electronic ballast with current injection: (a) circuit diagram, (b) key waveforms without current injection, and (c) key waveforms with current injection.

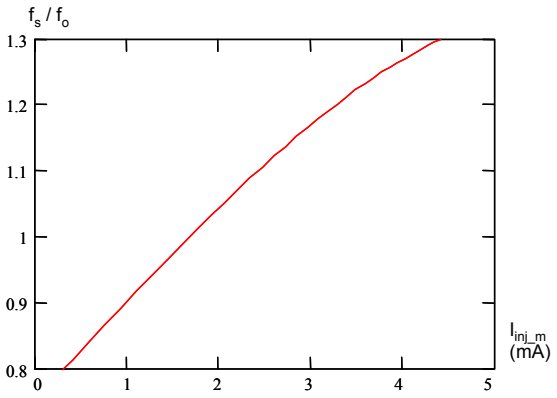


Figure 5-19. Calculated self-oscillating frequency as a function of injected current.

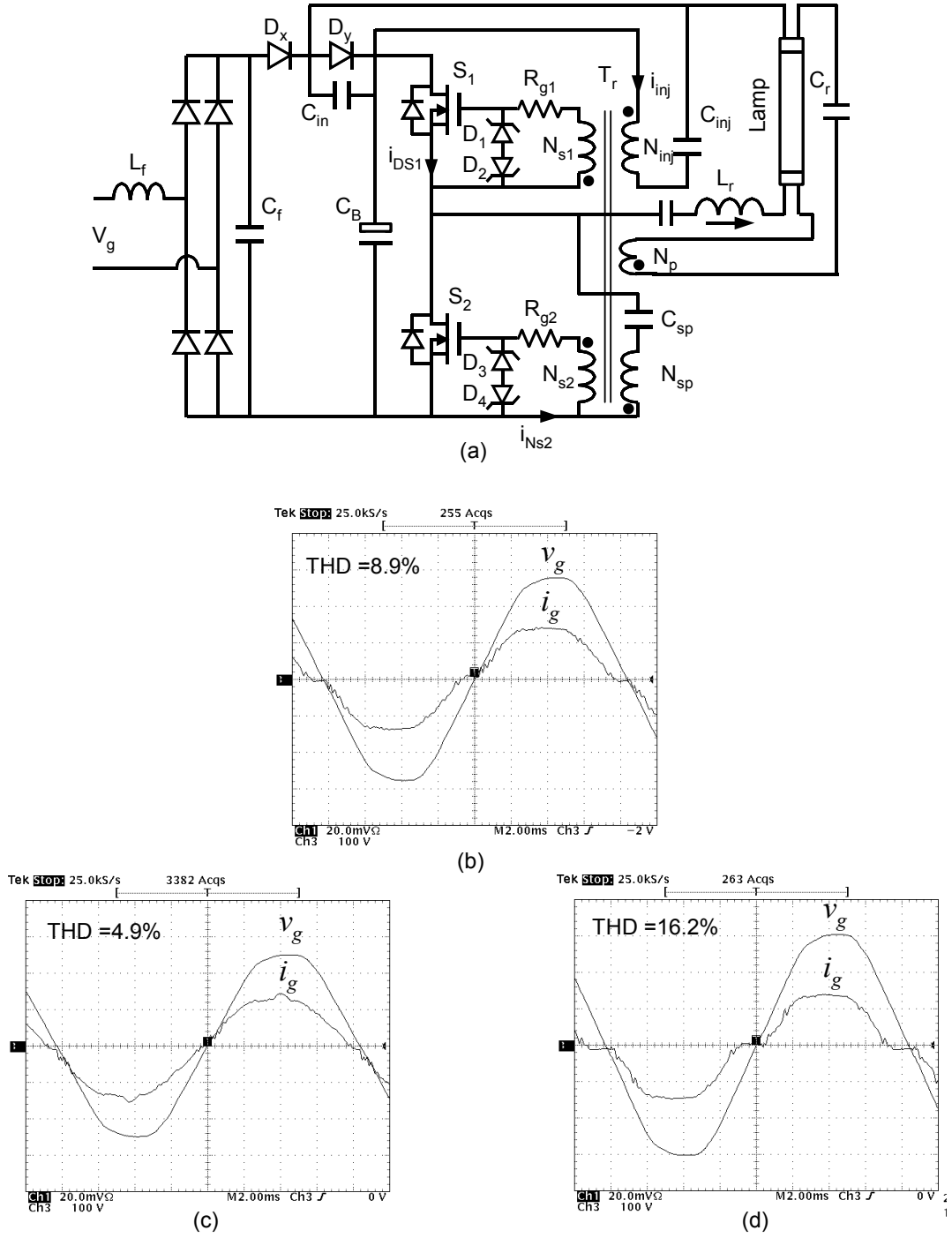


Figure 5-20. Self-oscillating CS-CPPFC electronic ballast with current injection: (a) circuit diagram, (b) line current waveform at the rated line voltage (V_g =200 V), (c) line current waveform at –10% line variation (V_g =180 V), and (d) line current waveform at 10% line variation (V_g =220 V). v_g: 100 V/div, i_g: 0.5 A/div, time: 2 ms/div.

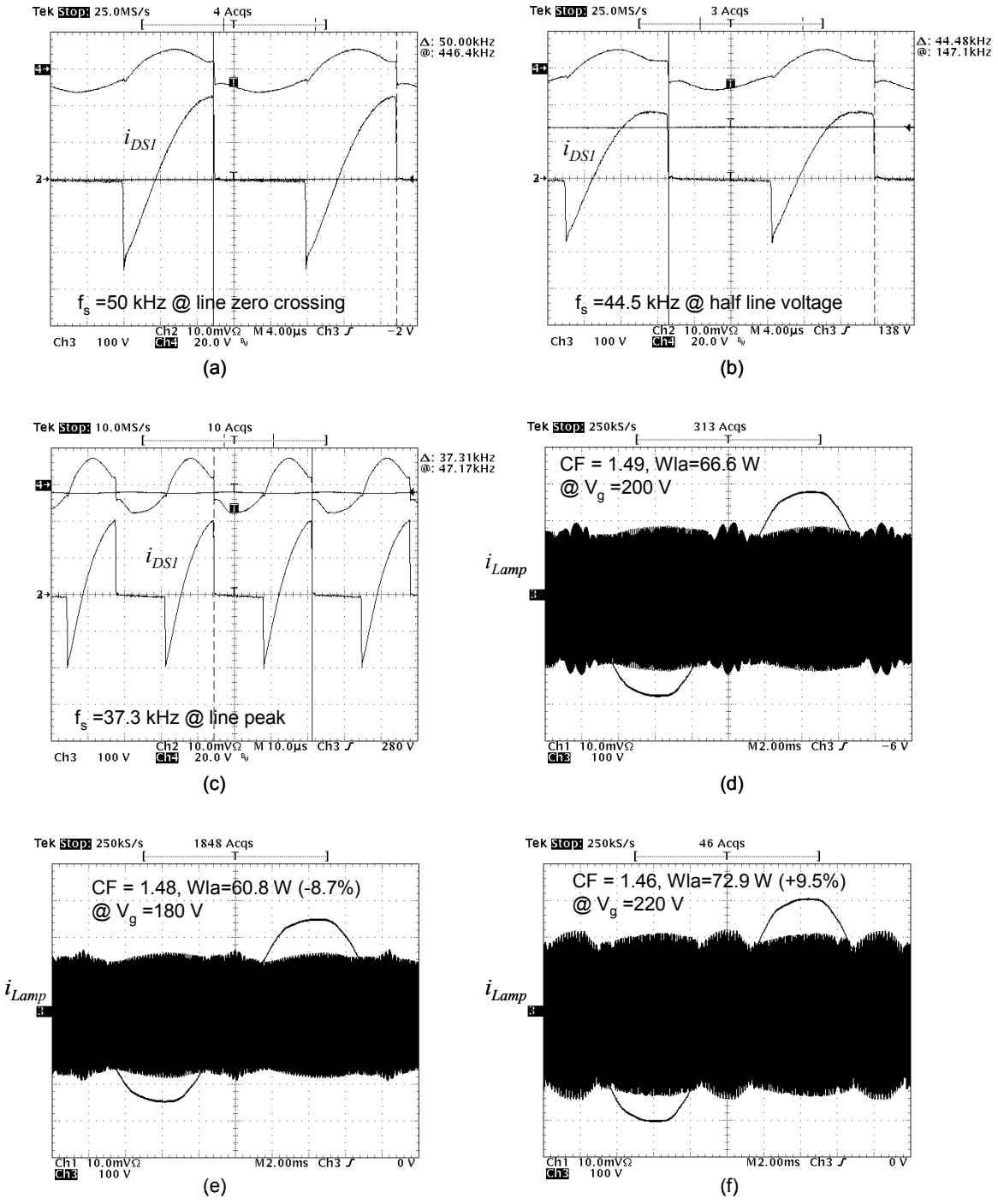


Figure 5-21. Experimental results: (a) measured switching waveforms near line zero crossing, (b) switching waveforms near half-line voltage, (c) switching waveforms near line peak, (d) lamp current waveform at the rated line voltage (V_g =200 V), (e) lamp current waveform at –10% line variation (V_g =180 V), and (f) lamp current waveform at 10% line variation (V_g =220 V).

5.4. Summary

The cost of the CS-CPPFC electronic ballast can be reduced and the performance can be improved by using the self-oscillating technique. However, the conventional self-oscillating driver cannot be directly applied to the CPPFC electronic ballast because of poor lamp CF, high line current distortion, and large sensitivity of lamp power to the line voltage variation.

Novel winding voltage modulation concept and current injection concept have been proposed, implemented and tested in this chapter. With the proposed concepts, the switching frequency of the self-oscillating circuit can be effectively modulated by a control signal so that the performance of the circuit is improved. Circuit topology and experimental results show that the self-oscillating CS-CPPFC electronic ballast with current injection circuit provides a good alternative for cost-effective non-dimming electronic ballasts.

Chapter 6 Conclusions

Electronic ballasts for gas discharge lamps received great attention in recent years due to their merits of small size, light weight, high efficacy, and long lamp life. However, poor input PF and rich harmonic current will be produced if the electronic ballasts are powered directly by a simple peak rectifying circuit from the utility AC lines, which deteriorates the power line quality and interferes with other electronic equipment. To maintain high PF and low harmonic current, stringent regulations such as the IEC 1000-3-2 have recently been established and enforced. These regulations have stimulated considerable interest in developing cost-effective solutions in designing and manufacturing high-power-factor electronic ballasts. A two-stage approach with a current-shaping stage (PFC stage) followed by an inverter stage is used in practical applications. To reduce the cost and component count, it is attractive to integrate the PFC stage with the inverter stage so that power switch and its controller can be eliminated.

The use of controllable output electronic ballasts or dimming electronic ballasts can significantly reduce energy consumption and make intelligent lighting feasible. Recently, the development of cost-effective single-stage PFC electronic ballasts with wide-range dimming control has become a dynamic research area.

To further reduce the cost, self-oscillating techniques are used in single-stage PFC electronic ballasts. However, to achieve satisfactory performance, it is important to add a control aspect to the self-oscillating electronic ballast when it is to be used in the single-stage CPPFC circuits.

This dissertation presents several single-stage PF correction techniques, wide-range dimming control techniques, and self-oscillating techniques. The following issues are addressed: bus voltage stress in the boost-derived single-stage PFC electronic ballasts, dimming control in the boost-derived single-stage PFC electronic ballasts, study and

comparison of charge-pump PFC electronic ballasts, and self-oscillating technique with control capability.

The most commonly used PFC topology in low-power applications is the DCM boost converter, due to its inherent PFC function. However, when applied in the half-bridge electronic ballast applications, the bus voltage is required to be higher than two times the line peak voltage to ensure DCM operation, which may severely penalize the power stage design. A novel voltage-divider concept is proposed and implemented by two new circuits: the critical-conduction-mode electronic ballast and the interleaved electronic ballast. The circuit analysis and experimental results show that the bus voltage can be reduced to half that of the conventional DCM boost circuit.

To achieve a wide range of dimming control, asymmetrical duty-ratio controlled single-stage PFC electronic ballasts are developed. By adjusting the duty ratio, the lamp power can be effectively controlled over a wide range. ZVS can be retained on the MOSFETs by integrating the resonant converter with QSW DC/DC converter into one stage. Moreover, a small amount of DC biased current is naturally injected into the lamp, which effectively eliminates the striations from the lamp and expands the stable dimming range. Experimental results show that the proposed sepic-based single-stage PFC dimmable electronic ballast performs satisfactorily with good PF, low harmonic distortion, low bus voltage stress and wide dimming range.

A family of CPPFC electronic ballasts has been investigated, implemented, and compared. It has been shown that capacitors can be used to achieve PFC function so that the CPPFC techniques appear to be a good alternative approach in electronic ballast applications.

From the analysis and experimental results, the basic VS-CPPFC electronic ballast suffers from the high bus voltage stress and high lamp CF and is not practical in electronic ballast applications. The VS-CPPFC with ICF has improved performance due to the adjustment effect of C_y. However, this option suffers from high current stress. The basic CS-CPPFC electronic ballast has the simplest structure, a moderate bus voltage, moderate switching current and moderate lamp CF, and is considered to be a good topology for electronic ballast applications. The basic VSCS-CPPFC electronic ballast

improves the lamp CF, bus voltage stress and current stress of basic VS-CPPFC and basic CS-CPPFC electronic ballasts. However, this option increases the complexity of the circuit, and the lamp CF still cannot meet the regulation with open-loop control. The VSCS-CPPFC with ICF electronic ballast appears to be the most complicated circuit, but can meet the lamp CF regulation without any feedback control. There is a trade-off between the complexity of the power stage and control circuit. The VSCS-CPPFC with LVFB electronic ballast performs well in the high-line applications since it has the lowest bus voltage. However, this option suffers from high current stress. Therefore, the basic CS-CPPFC electronic ballast shows the most promise for single-stage PFC electronic ballast applications.

The performance and cost of CS-CPPFC electronic ballasts can be further improved by using the self-oscillating technique. However, the conventional self-oscillating driver cannot be directly applied to the CPPFC electronic ballast because of poor lamp CF, high line current distortion, and large sensitivity of lamp power to the line voltage variation.

Novel winding voltage modulation and current injection concepts have been proposed, implemented and tested. With the proposed concepts, the switching frequency of the self-oscillating circuit can be effectively modulated by a control signal so that the performance of the circuit is improved. The circuit topology and experimental results show that the self-oscillating CS-CPPFC electronic ballast with current injection circuit is one of the best electronic ballasts.

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