Electrochemical Capacitor Characterization for Electric Utility Applications

By

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ABSTRACT

Electrochemical capacitors (ECs) have received a significant level of interest for use in the electric utility industry for a variety of potential applications. For example, ECs integrated with a power conversion system can be used to assist the electric utility by providing voltage support, power factor correction, active filtering, and reactive and active power support. A number of electric utility applications have been proposed but, to date, ECs have not been very well characterized for use in these applications. Consequently, there is a need to gain a better understanding of ECs when used in electric utility applications. ECs are attractive for utility applications because they have higher energy density than conventional capacitors and higher power density than batteries. ECs also have higher cycle life than batteries, which results in longer life spans. To better understand the system dynamics when ECs are used for utility applications requires suitable models that can be incorporated into the variety of software programs currently used to create dynamic simulations for the applications, programs such as PSPICE™, MATLAB Simulink™, and PSCAD™. To obtain a relevant simulation with predictive capability, the behavior of the EC on which the model is based must be well defined; this necessitates a thorough understanding of the electrical characteristics of these devices.

This paper and the associated research focus on the use of the electrochemical impedance spectroscopy (EIS) to develop nonlinear equivalent circuit models to better understand and characterize symmetric ECs (SECs) for electric utility applications. It also focuses on the development of analytical solutions to better understand SEC efficiency and energy utilization.

Representative static synchronous compensator (StatCom) systems, with and with out SECs, were simulated and discussed. The temperature effects on device ionic resistance and capacitance are covered as is the effect of temperature on maximum power transfer to

a resistive load. Experimental data showed that the SEC's double-layer capacitance and ionic resistance are voltage dependent. Therefore a voltage-dependent RC network model was developed and validated and the results showed that this type of model mimicked the experimental SEC better than traditional electrical models. Analytical solutions were developed for the efficiency and energy utilization of an SEC. The analytical solutions are a function of operating voltages, constant current, and ionic resistance. The operating voltage method is an important factor in system design because the power conversion interface is typically limited by a voltage window and thus can determine the performance of SECs during charge and discharge. If the operating voltage window is not properly selected the current rating of the system can be reduced thus limiting the SECs performance.

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CONTENTS

FIGURES

TABLES

1. Introduction

Electrochemical capacitors (ECs) have received a significant level of interest for use in the electric utility industry for a variety of potential applications. For example, ECs integrated with a power conversion system can be used to assist the electric utility by providing voltage support, power factor correction, active filtering, and reactive and active power support. To better understand the system dynamics when ECs are used for utility applications, such as voltage sags, requires suitable EC models that can be incorporated into the various software programs currently used to create dynamic simulations of power systems, programs such as PSPICE™, MATLAB Simulink™, and PSCAD™. The need for accurate models necessitates a thorough understanding of the electrical characteristics of these devices. This paper and the associated research focus on the use of electrochemical impedance spectroscopy (EIS) to develop nonlinear equivalent circuit models to characterize ECs for utility applications.

2. EC History

The double-layer capacitance concept was first described by Hermann von Helmholtz, a German physicist, in 1853 [1]. The first patented EC based on the double-layer capacitance structure was developed by General Electric Company in 1957 (Becker, H.I., "Low voltage electrolytic capacitor", U.S. Patent 20800616, 23 July 1957). This capacitor consisted of porous carbon electrodes using the double-layer capacitance mechanism for charge [2]. Standard Oil Company of Ohio (or Sohio) patented the EC for practical applications in November 1966 (Rightmire, R.A., "Electrical energy storage apparatus", U.S. Patent 3288641, 29 Nov 1966). In August 1979, Nippon Electric Company (or NEC) of Japan licensed the technology from Sohio and introduced the first

EC products to the marketplace as memory back-up devices in computers [3]. More recent applications for the devices include advanced transportation and electric utility applications. For example, ECs integrated with a power conversion system can be used to provide voltage support, power factor correction, active filtering, and reactive and active power support for electric utilities. The technology has become attractive to electric utilities because of its high energy density compared to conventional capacitors and its fast recharge times, high power density, and long cycle life compared to batteries. Since NEC first introduced the technology to the market, a number of manufacturers have begun to market various types and sizes of ECs. A current list of manufacturers of utility-scale ECs is shown in Table 1 [4]. As can be seen, only one American company, Maxwell Technologies, is currently producing ECs large enough for utility applications; the rest are from abroad.

Table 1. Current Manufacturers of ECs for Utility-scale Applications*

Manufacturer	Country	State of the Technology	Typical Energy Storage and DC Voltage Ratings	Technology VDC/Cell
ECOND	Russia	Commercial products	40 kJ, 14-200V modules	Type I, .9
Elit Stock Company	Russia	Commercial products	50 kJ, 14-400V	Type I, 9
EPCOS AG	Germany	Commercial products	15 kJ, 2.5 V 40 kJ, 14 V	Type II, 2.5 -- 2.7
ESMA Joint Stock Company	Russia	Commercial products	20 kJ – 1.2 MJ, 14V 30 MJ, 180 V modules	Type III, 1.4 – 1.6
Maxwell Technologies Inc.	USA	Commercial products	8 kJ, 2.5 V	Type II, 2.3 – 2.5

* The distinctions between Type I, II, and III ECs are defined later in the report.

Table 1. Current Manufacturers of ECs for Utility-scale Applications (continued).

Manufacturer	Country	State of the Technology	Typical Energy Storage and DC Voltage Ratings	Technology V_{DC}/Cell
NESS Capacitor Company	Korea	Commercial products	18 kJ, 2.7 V	Type II, 2.5 -- 2.7
NEC Tokin	Japan	Development	8 kJ, 14 V	Type I, .9
Okamura Laboratory Inc. with license from ECaSS to Shizuki Nissan, etc.	Japan	Commercial products	1350 – 1500 F, 2.7 V 35 F, 346 V, 75 F, 54 V	Type II, 2.5 – 2.7
Panasonic	Japan	Commercial products	6 kJ, 2.5 V	Type II, 2.5 – 2.7
Saft	France	Advanced prototype	10 kJ, 2.5 V	Type II, 2.5 -- 2.7

3. Classification of ECs

There are three general classifications of capacitors—electrostatic, electrolytic, and electrochemical. Electrostatic capacitors are typically made of two metal electrodes (parallel plates) separated by a dielectric as shown in Figure 1.

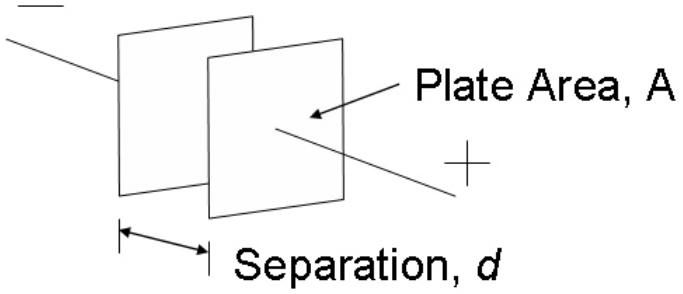


Figure 1. Simplified parallel-plate capacitor.

The dielectric is a non-conducting material (*e.g.,* air, plastic, paper, Mylar, etc.) that is inserted between the parallel plates of the metal electrode material [5]. The strength of the dielectric material measured in volts per meter determines the operating voltage of the capacitor. The dielectric strength equals the maximum electric field that can exist in a dielectric without electrical breakdown [6]. For example, air has a dielectric strength of

3×10^6 V/m, whereas, paper has a dielectric strength of 16×10^6 V/m. The dielectric increases the overall capacitance and the maximum operating voltage of the capacitor. The capacitance, measured in Farads (F), is defined as the ratio of total charge in coulombs (Q) in each electrode to the potential difference (V) between the plates:

$$C = \frac{Q}{V} \tag{1}$$

The capacitance is also proportional to the surface area (A) of the plates and inversely proportional to the distance (d) between the plates multiplied by a permittivity constant ε_0 (8.8542×10^{-12} C^2/Nm^2) [7]:

$$C = \frac{\varepsilon_0 A}{d} \tag{2}$$

The stored energy of the capacitor in joules (J) is proportional to the capacitance (C) and voltage (V) square across the plates [8]:

$$E = \frac{1}{2} C V^2 \tag{3}$$

It should be noted that the energy equation assumes that the initial voltage of the capacitor is zero. If the voltage is not zero, then the energy equation becomes

$$E_1 - E_2 = \frac{1}{2} C (V_2^2 - V_1^2) \tag{4}$$

where V_2 is the final voltage and V_1 is the initial voltage.

An electrolytic capacitor is similar in construction to an electrostatic capacitor but has a conductive electrolyte salt in direct contact with the metal electrodes. Aluminum electrolytic capacitors, for example, are made up of two aluminum conducting foils (one coated with an insulating oxide layer) and a paper spacer soaked in electrolyte [9]. The oxide layer serves as the dielectric and is very thin, which results in higher capacitance per unit volume than electrostatic capacitors. Electrolytic capacitors have plus and minus polarity due to the oxide layer, which is held in place by the electric field established during charge. If the polarity is reverse-biased, the oxide layer dissolves in the electrolyte and can become shorted and, in extreme cases, the electrolyte can heat up and explode.

In general, ECs also use electrolyte solutions but have even greater capacitance per unit volume due to their porous electrode structure compared to electrostatic and electrolytic capacitors. At the macroscopic level, the EC takes the equation $C = \varepsilon_0 A/d$ to the extreme by having a very high electrode surface area (A) due to the porous electrodes and very small separation d between the electronic and ionic charge at the electrode surface. Indeed, the surface area of the porous electrodes has been recorded to be as large as 1000 to 2000 m^2/cm^3 [10]. The high energy density of ECs is due to their greater capacitance per unit volume compared to conventional capacitors.

ECs themselves are grouped into two major categories—symmetric and asymmetric. Symmetric ECs (or SECs) use the same electrode material (usually carbon) for both the positive and negative electrodes. Asymmetric ECs (or AECs) use two different materials for the positive and negative electrodes. SECs get their electrostatic charge from the accumulation and separation of ions at the interface between the electrolyte and

electrodes. AECs, in contrast, get their charge from the reduction and oxidation (redox) reaction; redox is the charge transfer of electrons that takes place at the electrode and electrolyte interface due to change in oxidation state [11].

As mentioned above, the electric double-layer concept was first described by Hermann von Helmholtz. By assuming that there is no oxidation and/or reduction reaction at the electrode and that the interaction between the ions in solution and the electrode surface is purely electrostatic, he concluded that the ions hold electric charge at the electrode surface. When an electric potential is applied to the current collectors, electrons accumulate on the negative electrode thus attracting the positively charged cations to accumulate on the electrode surface to balance the charge locally. Similarly, on the positive electrodes, the electron vacancies attract the negatively charged anions to settle on the electrode surface to balance the charge. This separation of ionic and electronic charge gave rise to the name ‘double-layer’ capacitors. Double-layer capacitance forms on each electrode in the presence of electric potential. The double-layer capacitance at the positive and negative electrodes adds in series to the total capacitance of the device. The amount of ion accumulation depends on the electric potential—the higher the electric potential the higher the concentration of ions at the surface. A simplified cation accumulation on a negatively charged particle is shown in Figure 2.

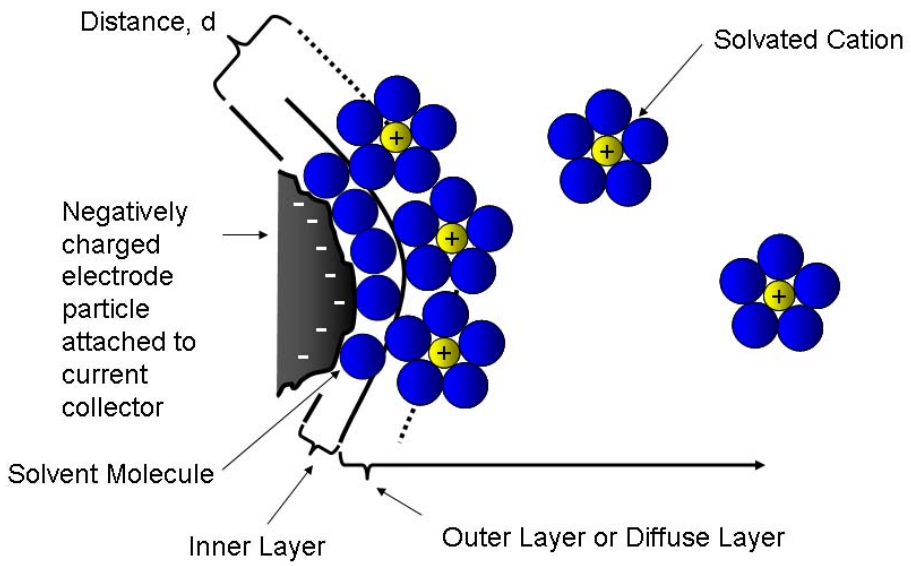


Figure 2. Simplified cation accumulation on a negatively charged particle.

Furthermore, with the presence of the electric potential, two layers are formed in the electrolyte near the electrode surface; the inner layer (also known as the Helmholtz layer) and the outer (or diffused) layer [12]. The inner layer primarily consists of non-conducting solvent molecules; the outer layer mainly consists of solvated ions (ions surrounded by solvent molecules) that are attracted to and held near the electrode through long-range electrostatic forces. The distance (*d*) between the ions and the electrode particle as shown in Figure 2 is analogous to the parallel plate dielectric separation in conventional capacitor. This distance can be very small. For example, assuming spherical geometry the average radii of acetonitrile, a common electrolyte used in ECs, is about .37 nm or 3.7 angstroms [13]; therefore the distance (*d*) can be only a few angstroms wide. The high surface area of the porous electrodes combined with a very small dielectric width or distance (*d*) at the double-layer is the key to establishing high capacitance. The double-layer capacitance can range from 10 to 40 μF per cm^2 [14]. Thus, double-layer capacitors can range from a single Farad to thousands of Farads, unlike conventional capacitors which are rated in the nano- to micro-Farad range. The

electrolyte remains conductive, with solvated ions held away from the electrode surface to allow for conduction between the double-layer capacitances at the positive and negative electrodes during charge and discharge.

Over the years, ECs have acquired many names coined by manufacturers including 'supercapacitors', 'ultracapacitors', 'pseudocapacitors', and 'double-layer capacitors'. The most common ones are 'supercapacitors' and 'ultracapacitors'. Supercapacitor is a trade name developed by NEC and Ultracapacitor is a trade name developed by Pinnacle Research Institute. There is confusion in industry with respect to terminology for the various types of ECs. Despite B. E. Conway's best efforts people still use all this nomenclature inconsistently. Throughout this report a more scientific and generic name 'electrochemical capacitors' (abbreviated 'ECs') will be used.

Figure 3 shows the taxonomy of different capacitor classifications and types. SECs can use aqueous or organic electrolyte solutions. The electrolyte solution comprises aqueous substances (such as potassium hydroxide or sulfuric acid) or organic substances (such as acetonitrile or propylene carbonate). An SEC using aqueous electrolyte is also known as a Type I SEC and an SEC using organic electrolyte is known as a Type II SEC. Similarly, an AEC using an aqueous electrolyte is known as a Type III AEC and one using organic electrolyte is known as a Type IV AEC. At the time of writing, there were no commercially available Type IV AEC devices. This report focuses on SECs. The abbreviation SEC will be used throughout the report.

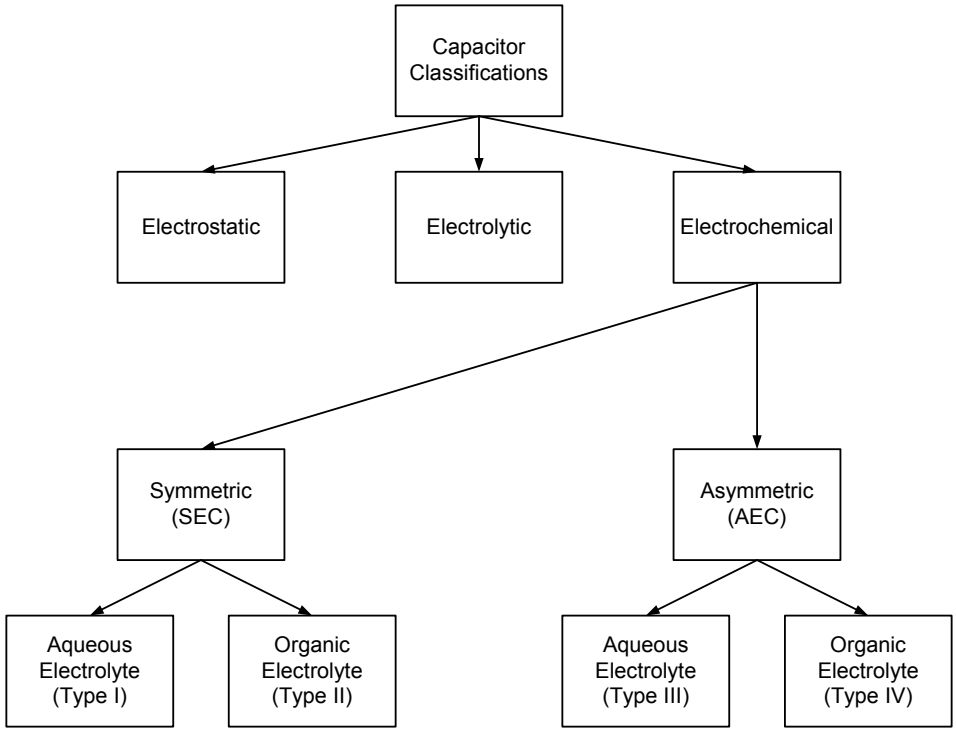


Figure 3. Taxonomy of capacitor classification and types.

4. SEC Construction

In its basic construction, the SEC consists of two porous electrodes, electrolyte, and two current collectors. The porous electrodes are bonded to the current collectors, which are then connected to external metal leads that are the positive and negative terminals of the device. Figure 4 shows the basic structure of an SEC in an uncharged and charged state.

During the uncharged state the electrolyte solution comprises positively charged cations and negatively charged anions. Once the device is charged, the cations are attracted to the surface of the negative electrode and the anions are attracted to the positive electrode. A double-layer capacitance is formed between the anions and the positively charged particles in the positive electrode and between the cations and the negatively charged particles in the negative electrode. These two double-layer capacitances contribute to the overall capacitance of the SEC.

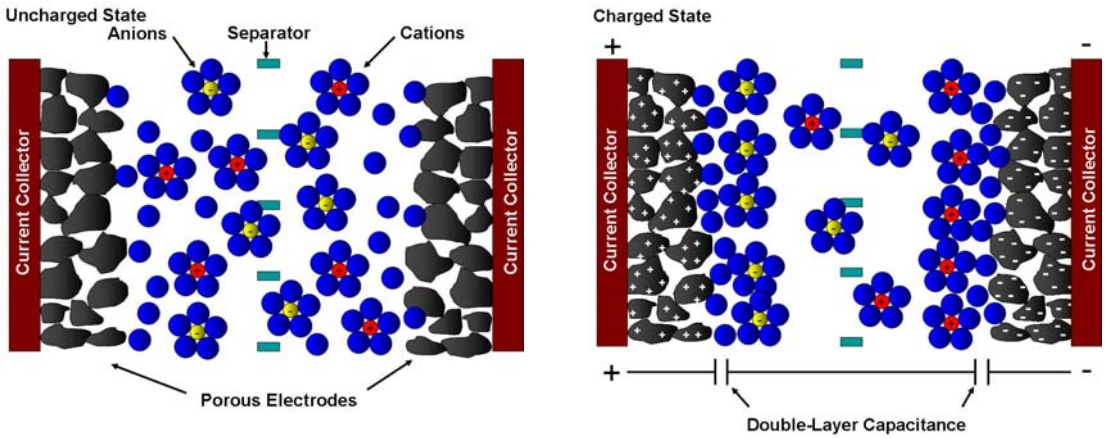


Figure 4. Basic structure of an SEC.

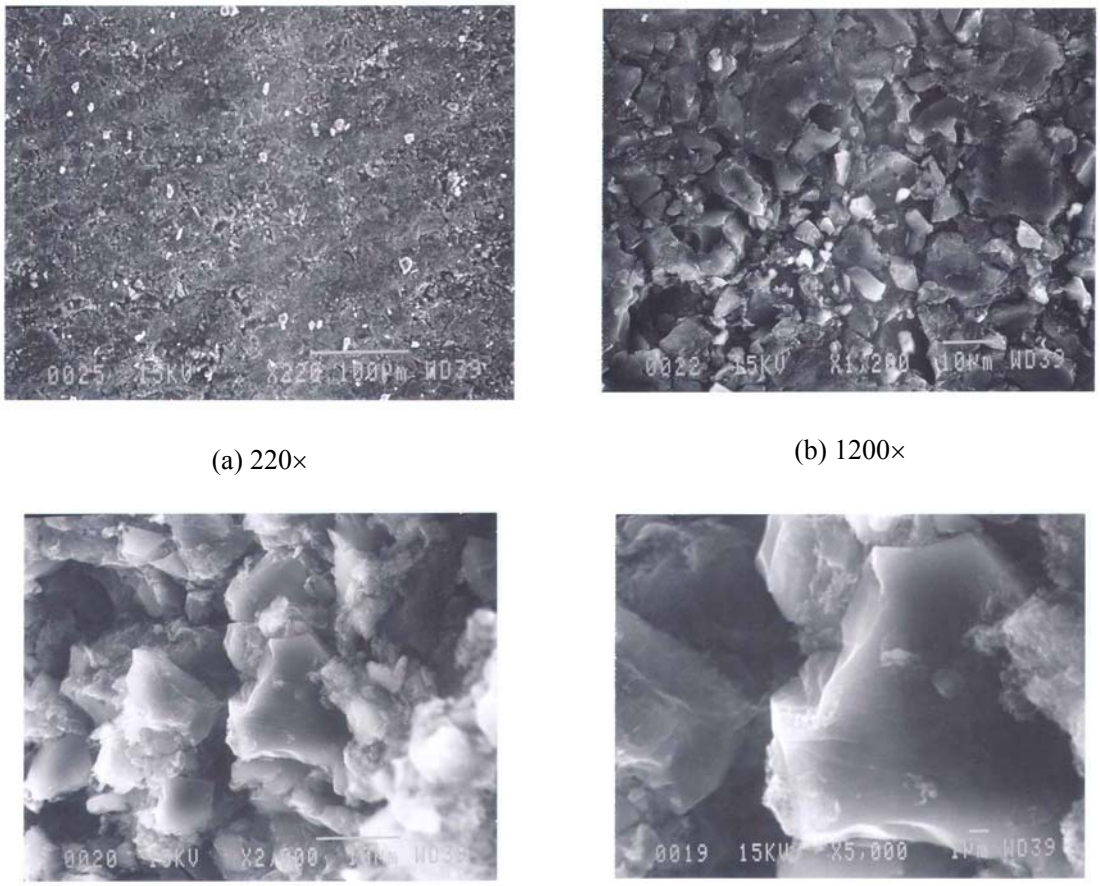
4.1. Electrolyte Characteristics

The rated voltage, or oxidation potential, of the SEC is determined by the electrochemical stability limits of the electrolyte or ionic solution. Water has an oxidation potential of 1.2 V, therefore ECs based on aqueous chemistries are limited to this voltage. Certain organic solvents are known to have oxidation potentials from 2.3 to 2.7 V/cell [15]. Additionally, more research in organic solutions could result in oxidation potentials up to 3.0 V/cell. The organic solvent must be able to solubilize salts, which are the source of ions for conduction. It is also important for the electrolyte solution to have high ionic mobility (*i.e.,* low ionic resistance). The ionic resistance and capacitance determines the overall time constant or charge/discharge characteristics of the SEC and, therefore, affects the overall performance of the device.

4.2. Electrode Characteristics

Carbon is typically the material of choice for the electrode material due to its high surface area, good electrochemical stability, low cost, and commercial availability. The SEC's electrodes are typically made of high-surface-area carbon in various forms such as powder, fiber, glass, and exotic materials such as carbon aerogels [16]. The surface area

of the carbon-based porous electrode can be significantly large at 1000 to 2000 m^2/cm^3 [17]. A scanning electron micrograph (SEM) picture of a sample of activated carbon used in SECs is shown in Figure 5 (a through d). As can be seen from the micrographs, the carbon particle size is on the average 10 μm in diameter.



(a) 220×

(b) 1200×

(c) 2000×

(d) 5000×

Figure 5. SEM micrograph of representative porous carbon electrode.

4.3. SEC Packaging

In general, SECs can be constructed in two types—cylindrical or stacked (prismatic) form factor. A generalized diagram of the external and internal structure of a cylindrical SEC is shown in Figure 6. In cylindrical SECs, the carbon is deposited on both sides of

the current collectors. This type of capacitor is easier to build than the stacked type and thus is amenable to high-volume manufacturing processes; building a stacked SEC is relatively labor intensive.

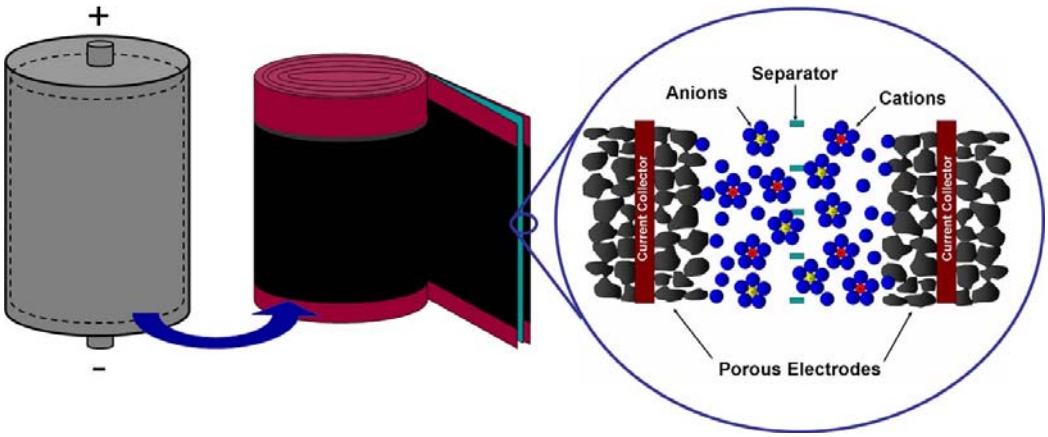


Figure 6. Simplified external and internal structure of a cylindrical SEC.

The internal structure of a simplified stacked SEC is shown in Figure 7. Like the cylindrical SEC, the stacked unit may have a cylindrical form factor, however, the stacked method results in higher packaging density. Each cell in the stack can be connected in series or parallel to achieve a variety of capacitance and voltage ratings.

Both the cylindrical and stacked structures are typically hermetically sealed packages with external connectors. The cylindrical and stacked packages also generally have a safety vent located near the external connectors or on the side of the capacitor to allow the gas to vent if it experiences a large pressure increase. In extreme cases the capacitor can rupture due to over pressure or over temperature conditions.

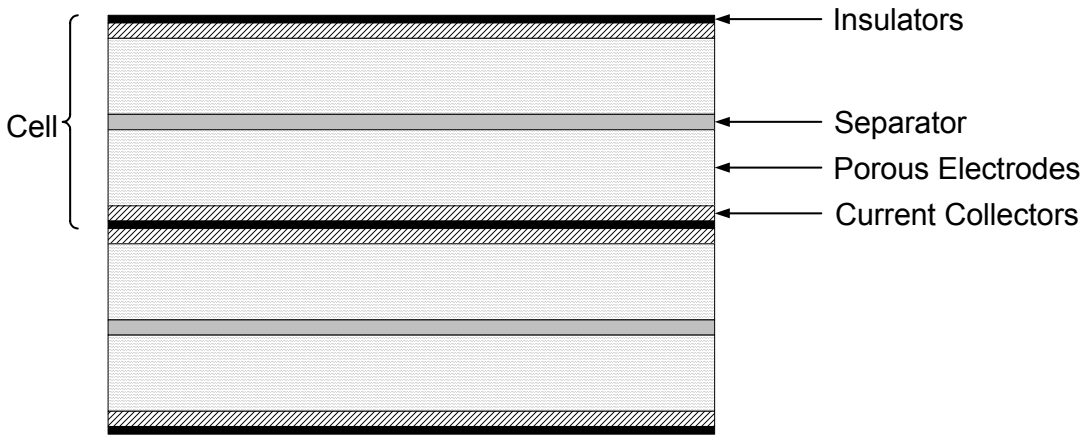


Figure 7. Simplified internal structure of a stacked (prismatic) SEC.

5. EC Power, Energy, and Cycle-life Tradeoffs

One way to compare various energy storage technologies is to plot their specific energy densities against their specific power densities in a plot known as a Ragone plot. Figure 8 shows a Ragone plot that compares batteries, ECs (labeled DLC), and conventional capacitors in terms of specific power and energy density. This comparison shows that conventional capacitors have high power densities but low energy densities. In contrast, batteries have high energy densities and low power densities. The energy and power densities for ECs are somewhere in between.

Also shown on the plot is the total time in seconds to completely discharge the energy storage device. This time is also referred to as the discharge duration. The plot shows that energy density decreases with shorter discharge duration and vice versa. The power density, on the other hand, decreases with longer discharge duration. The discharge duration for battery energy storage ranges from 1 to greater than 1000 seconds. The pulse duration for conventional capacitors ranges from hundreds of microseconds to less than 0.1 microseconds. EC pulse durations range from 1 microsecond to less than 1 second.

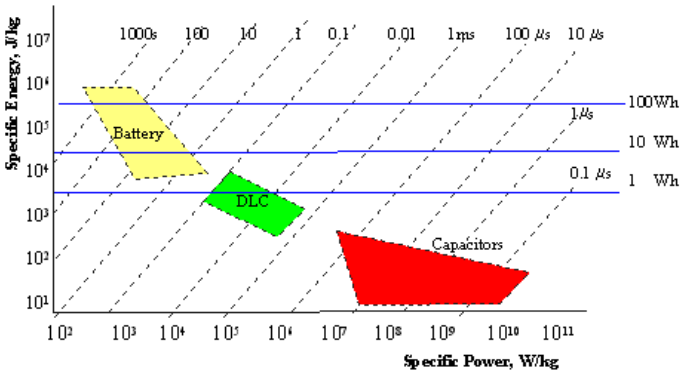


Figure 8. Energy storage technology comparison [18].

Along with high energy densities, another attractive feature of ECs is their long cycle life compared to batteries. Battery lifetimes are often measure by cycle life (*i.e.,* the total number of charge/discharge cycles before failure). Cycle life typically decreases as the state-of-charge (SOC) swing (or the SOC delta) increases. For example, if the SOC swing is 80% the battery or SEC could be cycled from 90% SOC to 10% SOC or any other SOC swing as long as there is an 80% delta, but cycle life at such a swing is relatively low. Likewise, as the SOC swing is reduced to, say, 5% (*e.g.,* 60% to 55%) the cycle life increases. Figure 9 compares the cycle-life performance of different battery chemistries. At present 500,000 to 1,000,000 cycles have been recorded at 80% SOC swing for SECs [19].

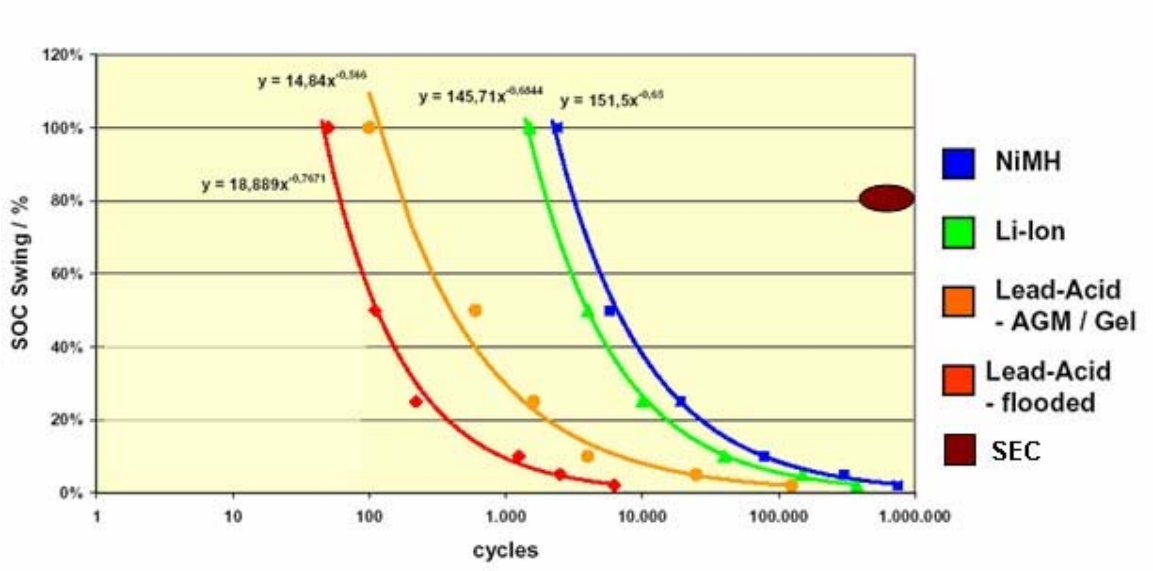


Figure 9. Cycle-life capabilities of different battery chemistries compared to an SEC [20].

6. EC Use in Electric Utility Applications

ECs have been used for electric vehicles and transportation systems in high-power, short-pulse applications in the past. Nevertheless, most ECs currently in use for electric utility applications are prototype demonstrations that use commercially available ECs. At the time of this writing, three demonstration systems using ECs in utility applications were being constructed and prepared for installation in the United States (U.S.). These systems show how ECs can potentially be used in a variety of utility applications. To be complete, more information is needed regarding non-domestic EC-based energy storage systems for electric utility demonstrations. The three U.S.-based demonstration projects are described below.

6.1. TUCAP Demonstration Project

This project focuses on the next-generation flexible AC transmission systems (FACTS) that incorporate a recently developed semiconductor switch (the emitter turn-off thyristor,

or ETO) and advanced controls with commercial ECs. This next generation FACTS is given the name Transmission Ultra CAPacitor, or TUCAP. The TUCAP is intended to provide active and reactive power support to electric utilities for power system stability and power quality improvement. The U.S. Department of Energy (DOE) Energy Storage Systems (ESS) Program at Sandia National Laboratories (SNL) and North Carolina State University (NCSU) initiated ETO development early in the project and are now focused on developing ETO-based power conversion systems. The Tennessee Valley Authority (TVA) is the current customer for this project and is providing the electric utility infrastructure for the demonstration. The overall objective of the project is to build and demonstrate a mobile, transformerless, 13.8-kV_{AC}, 60-MVA, 2-second discharge, TUCAP system on a TVA electric utility grid. Currently an asymmetric Type III EC manufactured by ESMA (a Russian capacitor manufacturer) is being used for the project, but the demonstration remains open to other EC technologies. The TUCAP concept is shown in Figure 10. Other contributors to the project include the Electric Power Research Institute (EPRI) and EPRI Solutions. Plans are in place to install the TUCAP system on a TVA demonstration site in 2007.

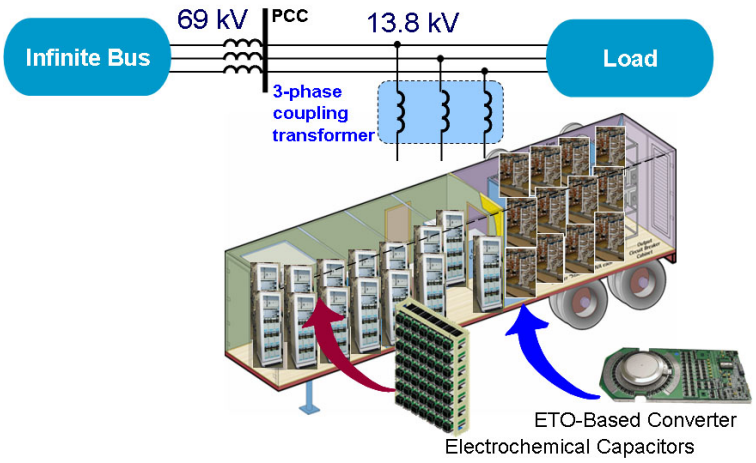


Figure 10. TUCAP conceptual drawing.

6.2. Palmdale Water District Demonstration Project

This goal of this demonstration project is to design, develop, and install a 450-kW EC-based electric energy storage system with an advanced power conversion system and static isolation at the Palmdale Water District water treatment facility in Palmdale, California. The EC-based system will supply energy to critical loads in the event of a utility outage or power quality event until back-up generation can be brought on-line. The system will be rated at 480 V_{AC}, 3-phase, and provide up to 450 kW over a discharge duration of 30 seconds. The energy storage technology will comprise three strings of 360 series-connected symmetric Type II ECs (each EC is rated at 2.5 V nominal) for a nominal voltage rating of 900 V_{DC}. The intent is to demonstrate that the EC has a cycle life greater than 500,000 cycles and a power density 10 times greater than batteries for the specified application. Northern Power Systems is the company responsible for integrating the electric utility, power conversion system, and energy storage device. Northern Power coined the term EnergyBridge^{TM} to describe this energy storage system. The symmetric Type II EC will be provided by Maxwell Technologies, Inc. The one-line diagram of the Palmdale project is shown in Figure 11. The California Energy Commission, Black & Veatch, the DOE ESS Program, and SNL are also involved in this project. Plans are in place to install the unit in early 2007.

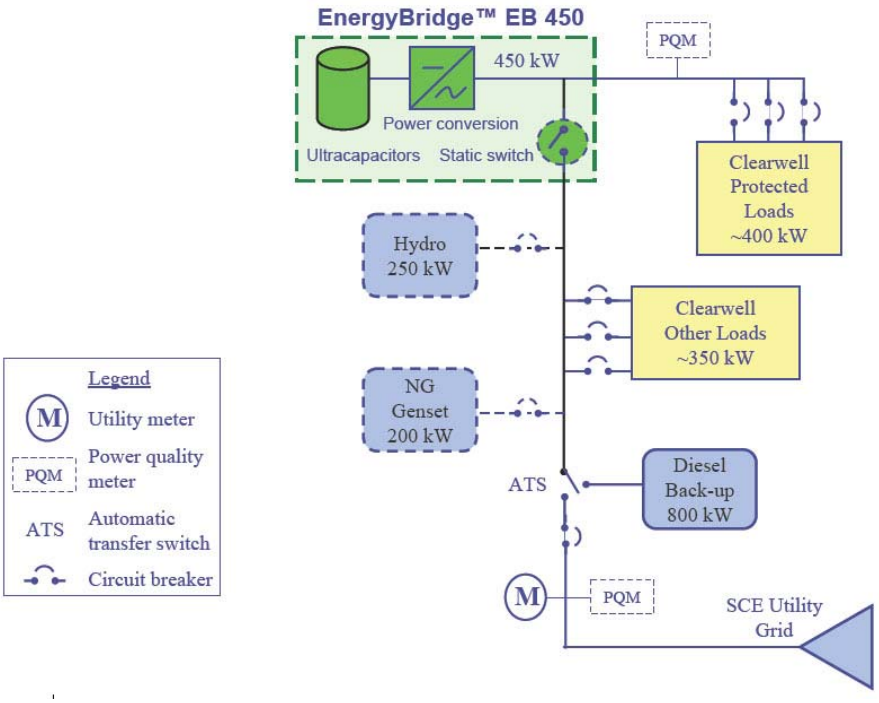


Figure 11. Northern Power Systems, Inc. Palmdale Water District EC demonstration project one-line.*

6.3. S&C Electric PureWave™ Electronic Shock Absorber Demonstration Project

The Hawaiian Electric Light Company (HELCO) is an electric utility company that serves the electricity needs on the big island of Hawaii. The HELCO system has 270 MW of capacity and about 25 MW of renewable energy available in the form of wind and hydroelectric power. HELCO currently has two wind farms rated at 2 MW and 7 MW and plans to install 21 MW of additional wind energy. Wind power can be highly unpredictable in terms of power generation and could cause perturbations, such as frequency instabilities, on a weak electric grid. The HELCO system has enough wind penetration to be known for wind-related frequency deviations on the system. To address this problem, HELCO teamed with S&C Electric Company to install a symmetric Type II

* Used with permission.

EC-based energy storage system integrated with a power conversion system to provide active and reactive power support to keep the frequency deviations within well-defined limits. This system is known as the PureWave™ Electronic Shock Absorber. A conceptual block diagram of the demonstration system is shown in Figure 12. The demonstration project will be located near the Lalamilo Wind Farm near Waikoloa, Hawaii. Like the TUCAP demonstration project, the PureWave™ system will be housed in a mobile trailer tied to a 12.47-kV_{AC} distribution substation near the wind farm. The ECs will be rated at 400 V_{DC} and will be stepped up with a boost converter to 800 V_{DC}. The power conversion system will have a 3-phase, 480-V_{AC} output and be stepped up through a transformer to 12.47 kV_{AC}. S&C Electric and HELCO plan to demonstrate two EC modules, each rated at 250 kW and 3 MJ for 15 seconds, from two different EC manufacturers: Maxwell Technologies, Inc. and EPCOS. This demonstration will compare the performance of the two technologies. The Maui Electric Company, Ltd., is also involved in the project. S&C Electric installed the unit in April 2006. [21]

As can be seen from the three demonstration project examples, SEC technology is expected to be useful for short-duration, high-power applications at utility-scale voltages (output levels). Because ECs are typically rated between .9 and 2.7 V/cell depending on the technology, to use this technology for utility-scale applications will require multiple cells to be connected in series/parallel to achieve the voltage/power needed by the power conversion system. In some cases, the EC can be integrated with electrolytic capacitors to handle the high-frequency filtering required at the DC-link of the power conversion system.

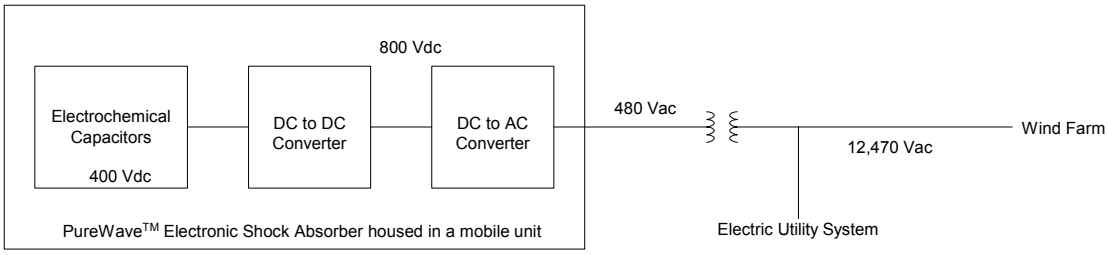


Figure 12. Conceptual block diagram of the S&C Electric PureWave™ demonstration project.

7. Description of the Equivalent Circuit Model for ECs

SECs can be modeled using the Porous Electrode Theory developed by de Levie in 1963 [22]. Figure 13 shows a microscopic view of a porous electrode from de Levie's paper. The theory assumes that the pores in the electrodes are cylindrical and are filled with homogeneous electrolyte solution. Each single cylindrical pore can be modeled by a uniformly distributed electrolyte solution resistance (R) and double-layer capacitance (C). This distribution of Rs and Cs is commonly referred to as the equivalent resistor-capacitor (RC) ladder network. A small section of the pore along with its RC ladder network is shown in Figure 14.

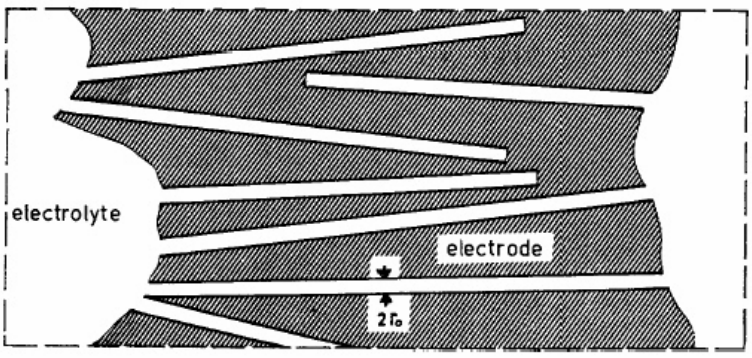


Figure 13. R. de Levie porous electrode model.

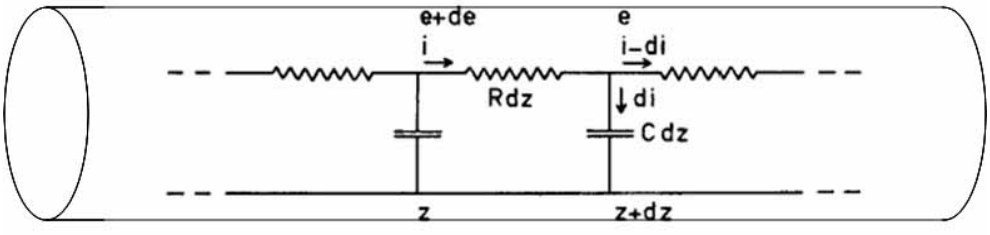


Figure 14. Small section of a cylindrical pore and the equivalent RC ladder network.

The porous electrode theory reveals how the electrical operating characteristics of ECs are affected by the charge transport process for a given electrode material and structure. Figure 15 shows a basic illustration of the equivalent RC ladder network based on porous electrode theory. Network (A) is the equivalent impedance of the SEC from one current collector to the other. It takes into account the pore electrolyte resistance, separator electrolyte resistance, and the interfacial double-layer capacitance. The number of cylindrical pores (n) on each electrode is assumed to be identical and, consequently, is grouped together and represented by an equivalent pore electrolyte resistance and interfacial double-layer capacitances. Network (A) can be further simplified by assuming both porous-electrode impedances are exactly the same; therefore, a circuit such as Network (B) can be obtained.

In this report, a five-stage Network (B) is used to model the SECs. The multistage ladder network is used because 1) it physically mimics the distributed nature of the EC within its pores and separator; 2) the performance in both the time and frequency domain fits the experimental data well over a wide range of frequencies; and 3) it can be combined easily with other system simulation software tools to find analytical solutions [23].

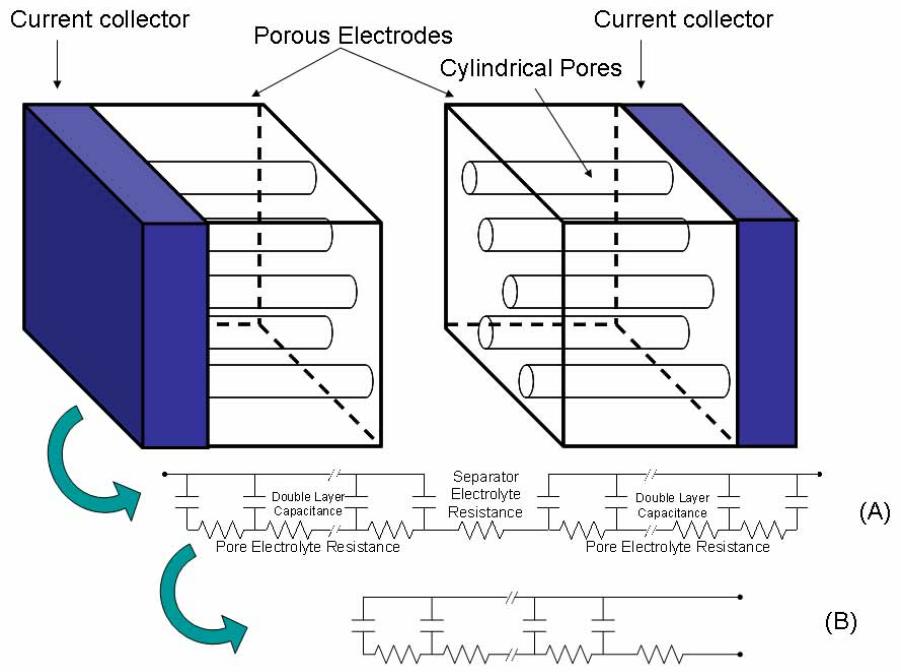


Figure 15. Porous electrode and RC ladder network.

Several papers, including Buller, *et. al.* [24], describe how EIS data is used to fit an equivalent circuit model for SECs. (EIS measurement techniques, equipment, and accuracy are described in more detail in Appendix A.) These equivalent circuit models mimic the SECs' electrical behavior in the time domain over a wide range of frequencies. EIS is typically performed potentiostatically by applying an AC excitation potential

$$E(t) = E_0 \sin(\varpi t) \tag{5}$$

to an electrochemical cell, such as a battery or an EC, and measuring the resulting current through the cell. The excitation potential is typically very small, generally in the millivolt range. The measured current is typically shifted in phase from the excitation signal:

$$I(t) = I_0 \sin(\varpi t - \phi) \tag{6}$$

The impedance is, therefore, calculated as follows:

$$Z(t) = \frac{E(t)}{I(t)} = \frac{E_0 \sin(\varpi t)}{I_0 \sin(\varpi t - \phi)} \tag{7}$$

The expression for $Z(t)$ is composed of both a real and an imaginary part and when these are plotted against one another a Nyquist plot is obtained (see Figure 16). Note that in the plot shown below, the y-axis is plotted in units of –Zi. Additionally, the term 'SEC system' is used because the contributions of the electrical leads are also included in the data, and this can be an important consideration in utility applications.

In the Nyquist plot negative reactance corresponds to the capacitive portion of the SEC system and positive reactance corresponds to the inductive portion of the system. At very low frequencies the EC behaves more like an ideal capacitor. The zero crossing is the self-resonant point where the capacitance and inductance cancel out and is labeled *Re* in the figure (which corresponds to the electrolyte resistance between the electrodes); Ω is the total electrolyte resistance within the pore structure of the electrode. Figure 16 shows ϖ increasing.

The real and imaginary components of the impedance can also be plotted against frequency on a log-log scale; this type of plot is known as a Bode plot. Figure 17 shows a typical Bode plot of an SEC. In the figure, $Z_{imaginary}$ (or reactance) decreases as the frequency increases until it reaches the resonant point where capacitive reactance cancels out the inductive reactance. Beyond the resonant point the inductive reactance is derived primarily from the current collectors and external test equipment leads. Z_{real} (or resistance) decreases slightly with increases in frequency.

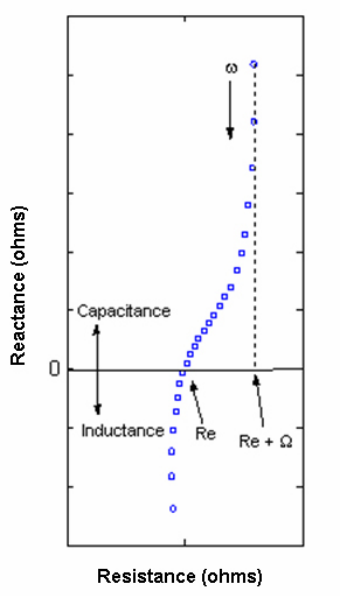


Figure 16. Typical Nyquist plot of an SEC system.

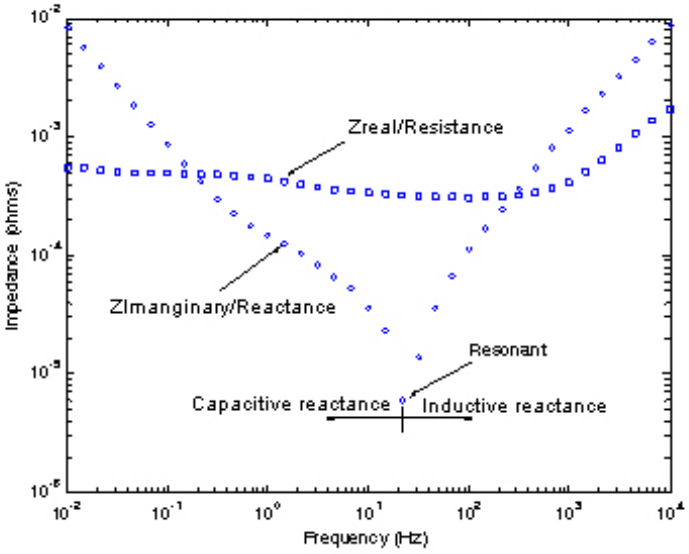


Figure 17. Typical Bode plot of an SEC.

The model parameters can be obtained from the EIS data using a nonlinear, least-squares fitting routine applied to measured data. To fit the EIS data in the frequency domain, a mathematical formula that represents the distributed network is needed. This mathematical formula is known as the RC ladder continued fraction equation [25]. The five-stage RC ladder continued fraction equation is shown below:

$$Z(\varpi) = L\varpi i + R1 + \cfrac{1}{C1\varpi i + \cfrac{1}{R2 + \cfrac{1}{C2\varpi i + \cfrac{1}{R3 + \cfrac{1}{C3\varpi i + \cfrac{1}{R4 + \cfrac{1}{C4\varpi i + \cfrac{1}{R5 + \cfrac{1}{C5\varpi i}}}}}}}}} \quad (8)$$

where $\varpi = 2\pi f$ in radians/sec and f is in Hz (or cycles/sec).

The generic five-stage RC network is shown in Figure 18. The inductor (L) is included to represent the inductance due to current collectors and test equipment leads. The continued fraction equation can be used in a nonlinear, least-squares fitting routine to fit experimental data to solve the RC network coefficients (L, R1, C1, R2, C2, R3, C3, R4, C4, R5, C5).

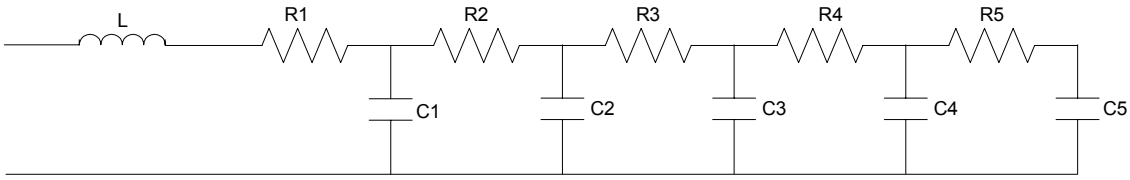
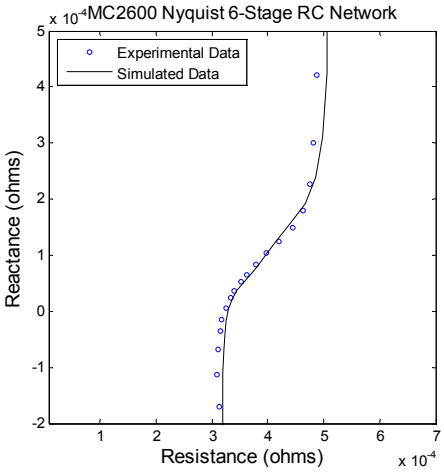
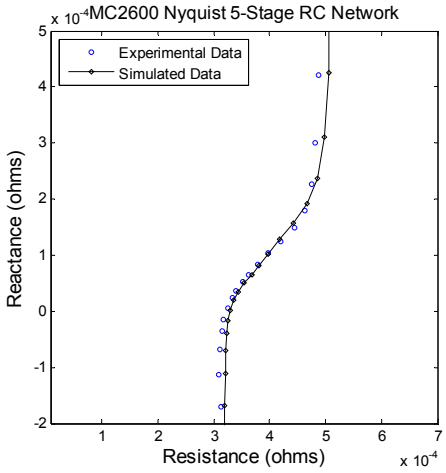


Figure 18. Generic five-stage RC network.

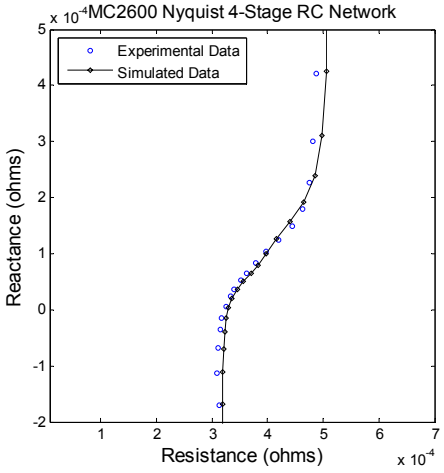
The five-stage RC network is used in the example above but the optimal number of RC network stages needs to be determined statistically. The plots in Figure 19 (a through f) show the experimental data fitted to six-, five-, four-, three-, two- and one-stage RC networks.



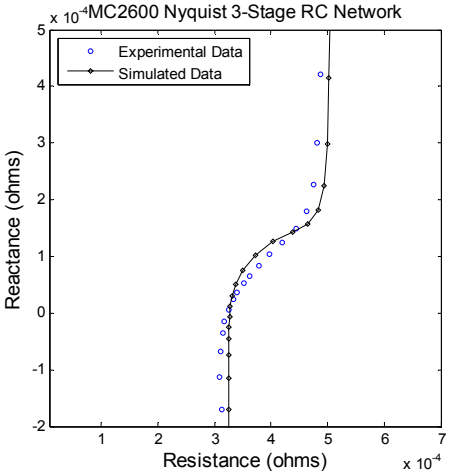
(a) Six-stage RC Network



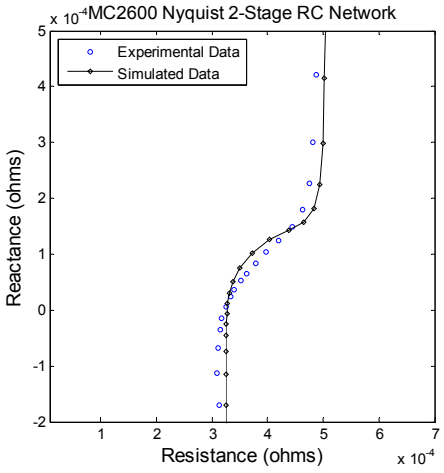
(b) Five-stage RC Network



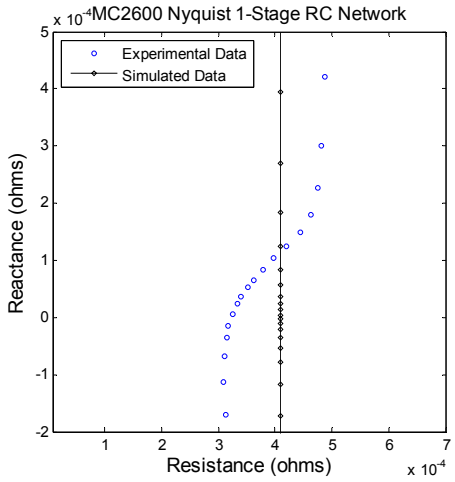
(c) Four-stage RC Network



(d) Three-stage RC Network



(e) Two-stage RC Network



(f) One-stage RC Network

Figure 19. Experimental data fitted to six- to one-stage RC networks.

To get a good fit between the experimental data and simulated data it is necessary to determine the root-mean-square-error (RMSE). The error between a single experimental data point represented by R_{exp} and X_{exp} and a simulated data point represented by R_{sim} and X_{sim} in a Nyquist plot (shown in Figure 20) is calculated as follows:

$$Error_n = \sqrt{(R_{\exp} - R_{sim})^2 + (X_{\exp} - X_{sim})^2} \qquad (9)$$

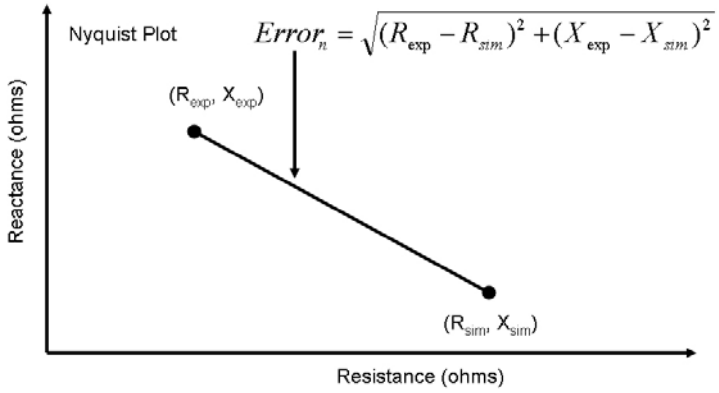


Figure 20. Graphical representation of Error$_n$.

The RMSE then calculated as

$$RMSE = \sqrt{\frac{Error_1^2 + Error_2^2 + ... + Error_n^2}{n - p}} \tag{10}$$

where n is the number of data points and p is the number of fitted parameters [26]. As can be been seen from Figure 19, the experimental impedance data is on the order of 10^{-4} Ω, therefore, the RMSE calculation was divided by the average impedance ($Z_{AVERAGE}$) of the experimental data over n-number of data points to make it relative (or normalized) to $Z_{AVERAGE}$. The relative-RMSE (RRMSE) is defined as

$$RRMSE = \frac{\sqrt{\frac{Error_1^2 + Error_2^2 + ... + Error_n^2}{n - p}}}{Z_{AVERAGE}} \tag{11}$$

The RRMSE was calculated for one-, two-, three-, four-, five-, and six-stage RC networks fit to the experimental data. The results of the RRMSE calculations for each stage are shown in Figure 21.

As can be seen from Figure 21, the one-stage RC network has the highest RRMSE (23.5%) whereas the four-stage RC network has the lowest RRMSE (3.61%) compared to the other stages. The increasing errors seen from two- to three-stage and also from four- to five- to six-stage result from overfitting. Based on the desire to avoid overfitting and to obtain the lowest RRMSE, the four-stage RC network appears to be the best model. Other experimental data may reveal a different *n*-stage RC network that optimizes the number of RC network parameters without overfitting.

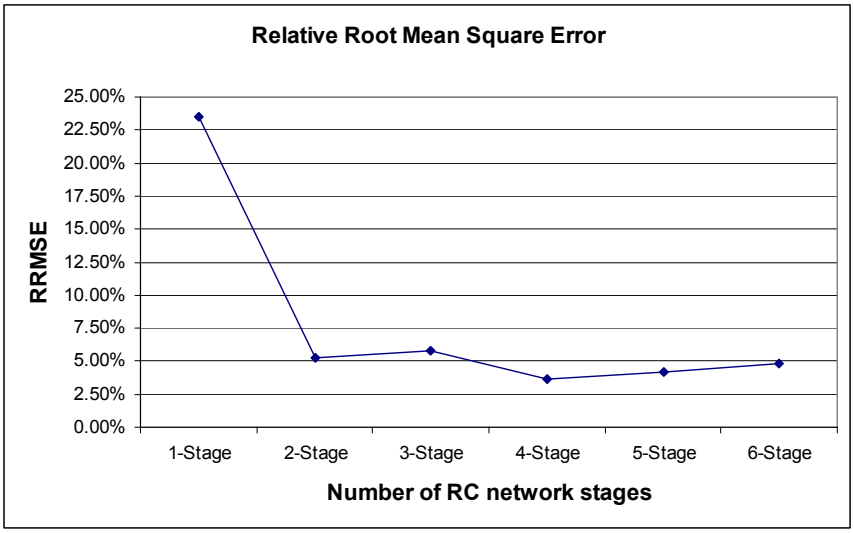


Figure 21. Summary of RRMSE of one- to six-stage RC networks.

To obtain the RC network coefficients, software was developed using MATLAB™. A built-in MATLAB algorithm fits the nonlinear continued fraction equation to EIS frequency domain data:

$$\min_x \frac{1}{2}\left\|F(x, xdata) - ydata\right\|_2^2 = \frac{1}{2}\sum_{i=1}^{m}(F(x, xdata_i) - ydata_i)^2 \quad (12)$$

This algorithm takes the experimental input data ($xdata_i$) and the calculated or observed output data ($ydata_i$) and finds coefficients (x) that best fit a user-defined equation.

8. Equivalent Circuit Model Implementation

The EIS data at various states of charge were measured on a representative SEC. The Bode and Nyquist plots of the device are shown in Figure 22 and Figure 23.

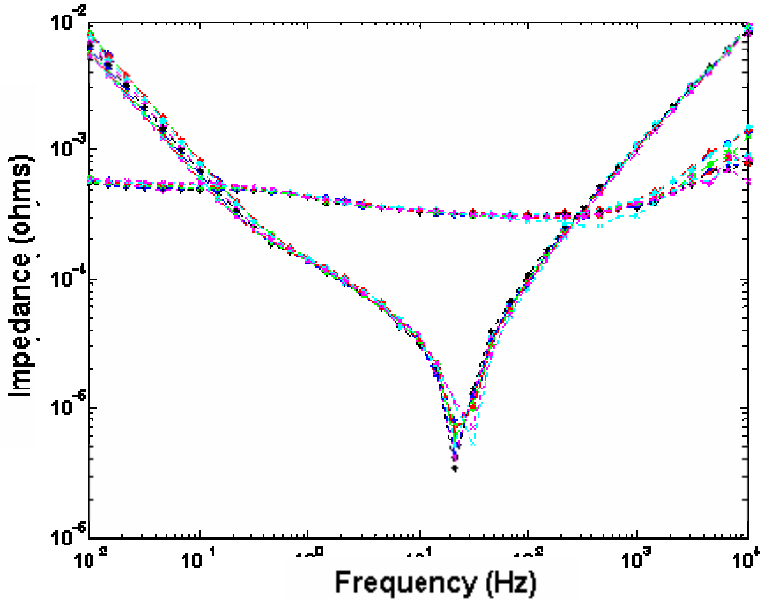


Figure 22. Bode plot of an SEC at various voltages.

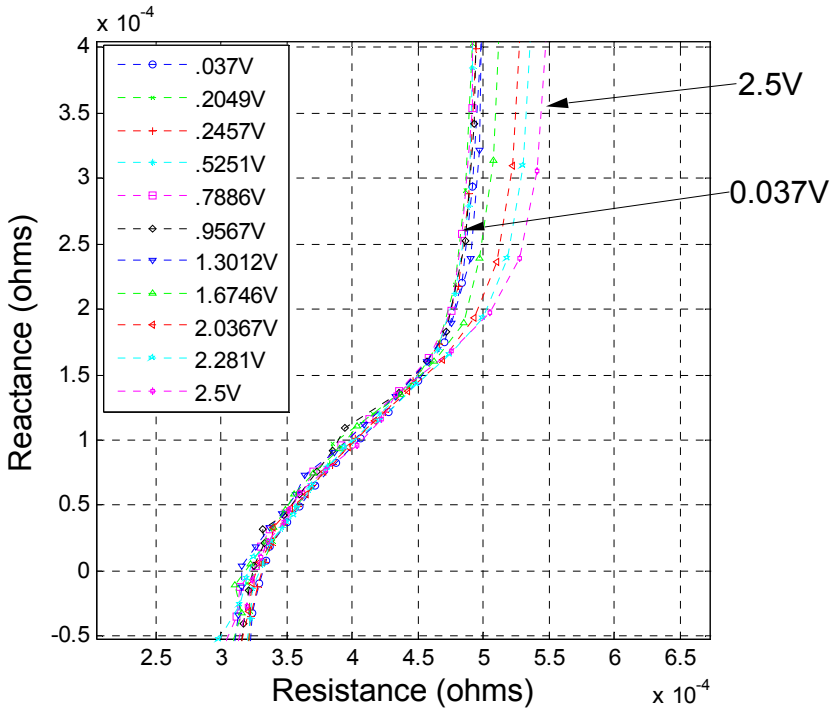


Figure 23. Nyquist plot of an SEC at various voltages.

A nonlinear curve-fitting program developed in MATLAB™ was used to obtain equivalent five-stage circuit models at the various SOC voltages.* The coefficients R1 to R5 and C1 to C5 of the RC ladder network were obtained at each SOC voltage. Thus plots of capacitance and resistance versus SOC voltage were generated. Graphs providing a summary of the capacitance and resistance at various voltages are shown in Figure 24 and Figure 25, respectively.

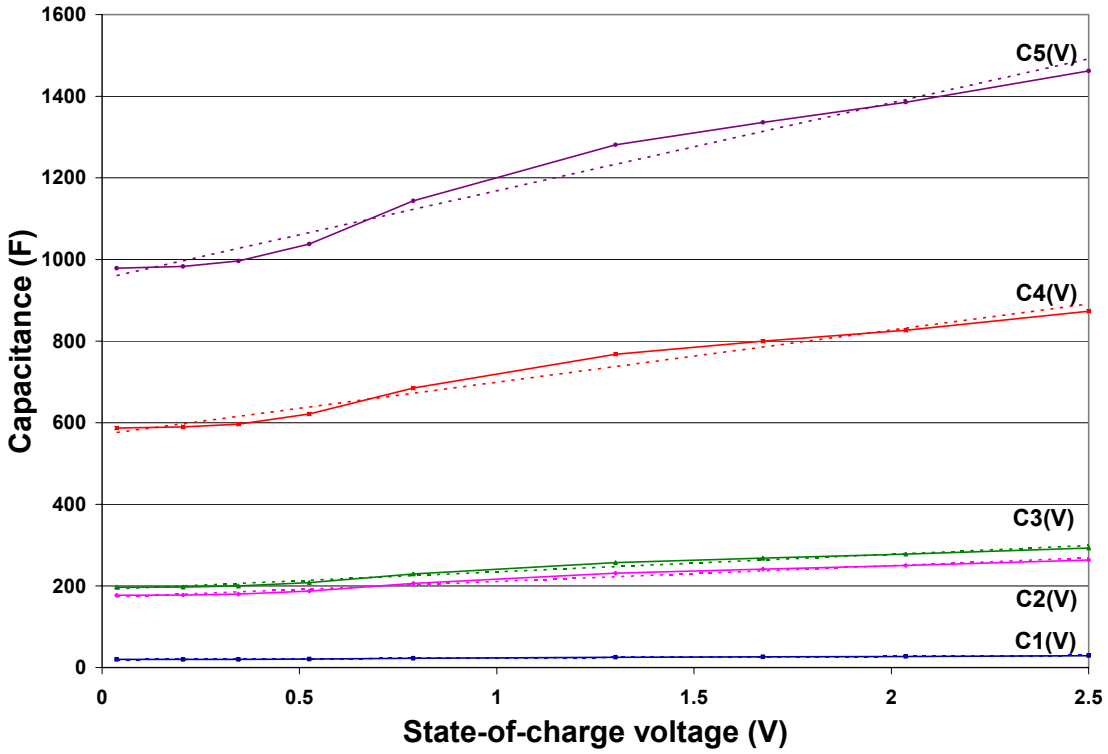


Figure 24. Capacitance versus SOC voltage.

* The five-stage model was selected for curve fitting in MATLAB™ based on the results of previous research. The statistical analysis that indicated that a four-stage network model would provide the least amount of overfitting had not yet been performed when the nonlinear curve-fitting program was developed. Nevertheless, the MATLAB™ results are basically the same for both four- and five-stage networks.

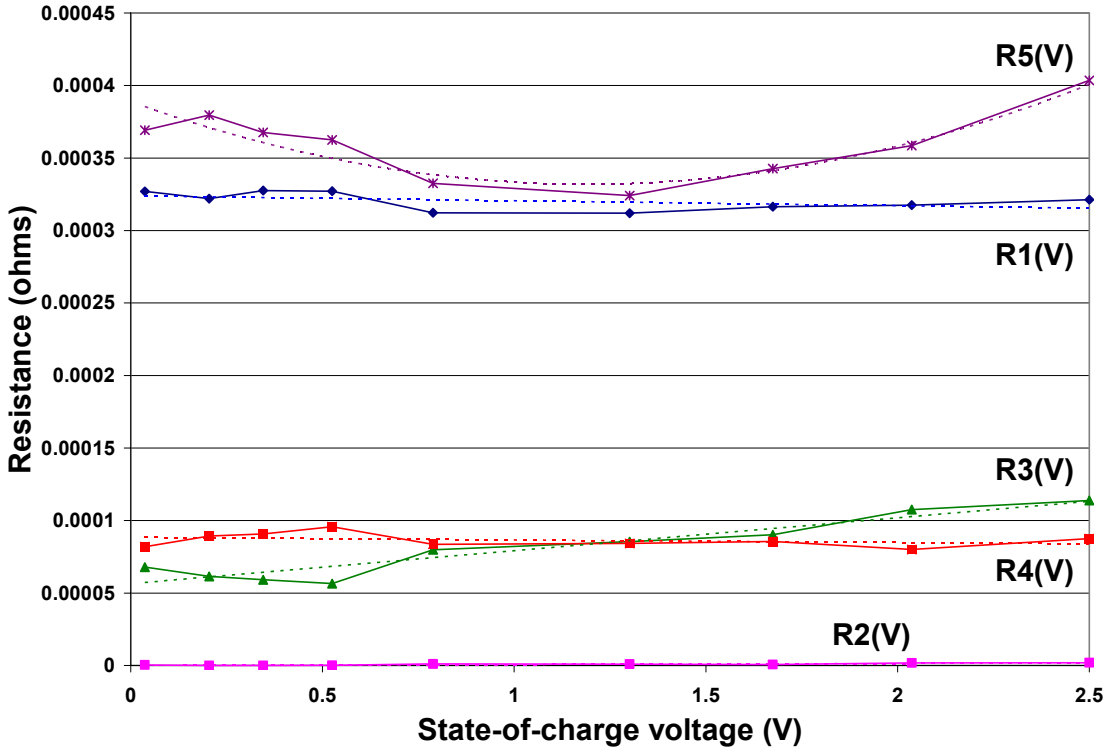


Figure 25. Resistance versus SOC voltage.

A simple curve-fitting function in Microsoft Excel was used to obtain the resistance and capacitance versus SOC voltage equations. The mathematical expressions for resistance as a function of voltage for R1 through R5 are as follows:

$$R1(V) = -3.38\times10^{-6}V + 3.24\times10^{-4} \quad (13)$$

$$R2(V) = 7.21\times10^{-7}V + 3.24\times10^{-8} \quad (14)$$

$$R3(V) = 2.28\times10^{-5}V + 5.64\times10^{-5} \quad (15)$$

$$R4(V) = -1.80\times10^{-6}V + 8.84\times10^{-5} \quad (16)$$

$$R5(V) = 4.01\times10^{-5}V^2 - 9.56\times10^{-5} + 3.89\times10^{-4} \quad (17)$$

Likewise the mathematical expressions for capacitance versus the SOC voltage are—

$$C1(V) = 4.20V + 18.98 \quad (18)$$

$$C2(V) = 38.78V + 172.09 \quad (19)$$

$$C3(V) = 43.18V + 191.19 \quad (20)$$

$$C4(V) = 127.90V + 571.39 \quad (21)$$

$$C5(V) = 215.77V + 952.51 \quad (22)$$

Figure 24 and Figure 25 clearly illustrate that the impedance and capacitance of the SEC depends on its SOC voltage.

With this in mind, an equivalent circuit model was specifically developed to account for the dependence of resistance and capacitance on the SEC's SOC voltage. The general circuit model as a function of SOC voltage is shown in Figure 26.

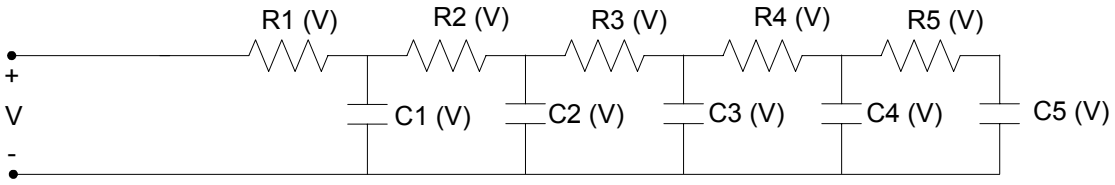


Figure 26. Generic voltage-dependent RC ladder network.

9. Equivalent Circuit Model Validation

To validate the SOC-dependent SEC model, one has to verify the model's response in the time domain. A constant-current (100-A) charge and discharge cycle with a 4-second rest period was applied to an experimental SEC cell and the potential was recorded. This type of test is also known as galvanostatic cycling. The same constant-current cycle profile was applied to the voltage-dependent RC ladder network and the simulated potential was

compared to the experimental results. The simulation and experimental results are shown in Figure 27.

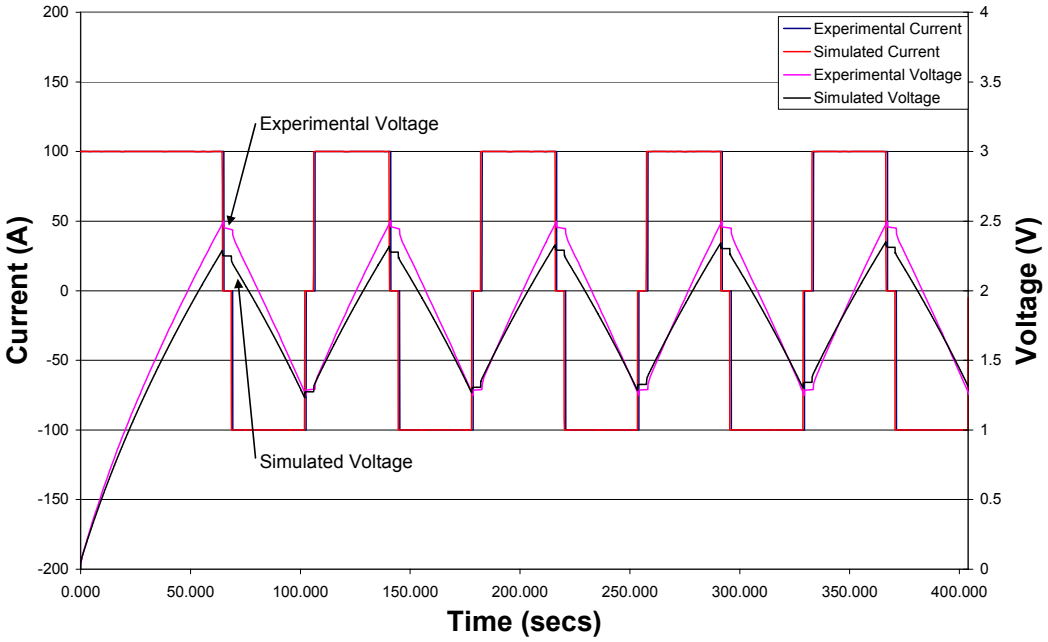


Figure 27. Galvanostatic cycling of the experimental SEC and voltage-dependent SEC model.

As can be seen from Figure 27, the experimental voltage of the SEC reaches 2.5 V in about 65.2 seconds during the first constant-current charge where the simulated voltage reaches 2.28 V in the same time. As in earlier experiments, the voltage-dependent network model was developed using EIS at various SOC voltages. The SEC was charged to a set voltage and allowed to rest open circuit (or equilibrate) for 24 hours before the impedance was measured. The equilibrated state suggests that the majority of the ions in the SEC have settled on the active carbon electrodes; thus the capacitance utilization of the carbon electrodes has been maximized. In a dynamic state such as galvanostatic cycling, however, the capacitance utilization of the carbon electrode is less compared to an equilibrated state because the ions are in motion while charging. The ions have a finite

time to settle in the porous electrode structure (*i.e.,* charge the electrode surface). Other phenomena that can contribute to the capacitance utilization are chemical faradic processes and absorption that occur at the electrode surface. Further explanation of these other factors is beyond the scope this report, but their effect on capacitance utilization is worth mentioning. Presently, this reduction in effective capacitance in a dynamic state is not well understood even by electrochemists.

Just how much does the capacitance utilization decrease in a dynamic state? is the key question. To determine this, several PSCAD™ simulations were run on the voltage-dependent RC network while adjusting the coefficients of the capacitance-versus-SOC voltage equations. PSCAD™ which stands for Power Systems Computer Aided Systems Design, is a dynamic simulation tool used to study electromagnetic transients in electric utility systems. It uses the EMTDC™ (Electromagnetic Transients including DC) software as its solution engine [27]. This software was developed by the Manitoba High Voltage DC Research Center in Canada. Basically, it is a multi-purpose simulation tool for power electronic design and simulation, power quality analysis, and electric utility system planning studies. After several PSCAD™ simulation runs, the capacitance-versus-SOC voltage equations were changed to the following equations:

$$C1(V) = 4.20(1-.45)V + 18.98(1+.1) \tag{23}$$

$$C2(V) = 38.78(1-.45)V + 172.09(1+.1) \tag{24}$$

$$C3(V) = 43.18(1-.45)V + 191.19(1+.1) \tag{25}$$

$$C4(V) = 127.90(1-.45)V + 571.39(1+.1) \tag{26}$$

$$C5(V) = 215.77(1-.45)V + 952.51(1+.1) \tag{27}$$

As can be seen from the above equations, the voltage multipliers were reduced by 45%, whereas the constant coefficients were increased by 10%. This represents a mathematical artifact based on simulation runs to fit the experimental data. Figure 28 shows the simulation-versus-experimental results based on the new capacitance-versus-SOC voltage equations.

As can be seen from Figure 28, better voltage results were seen after the adjustments were made. To evaluate robustness of the adjusted voltage-dependent RC network, galvanostatic cycling at 75 A, 50 A, and 25 A was performed. Figure 29, Figure 30, and Figure 31 show the galvanostatic cycling results at 75 A, 50 A, and 25 A, respectively. The figures illustrate that the effective capacitance adjustments on the voltage-dependent RC network work well for various current cycling profiles.

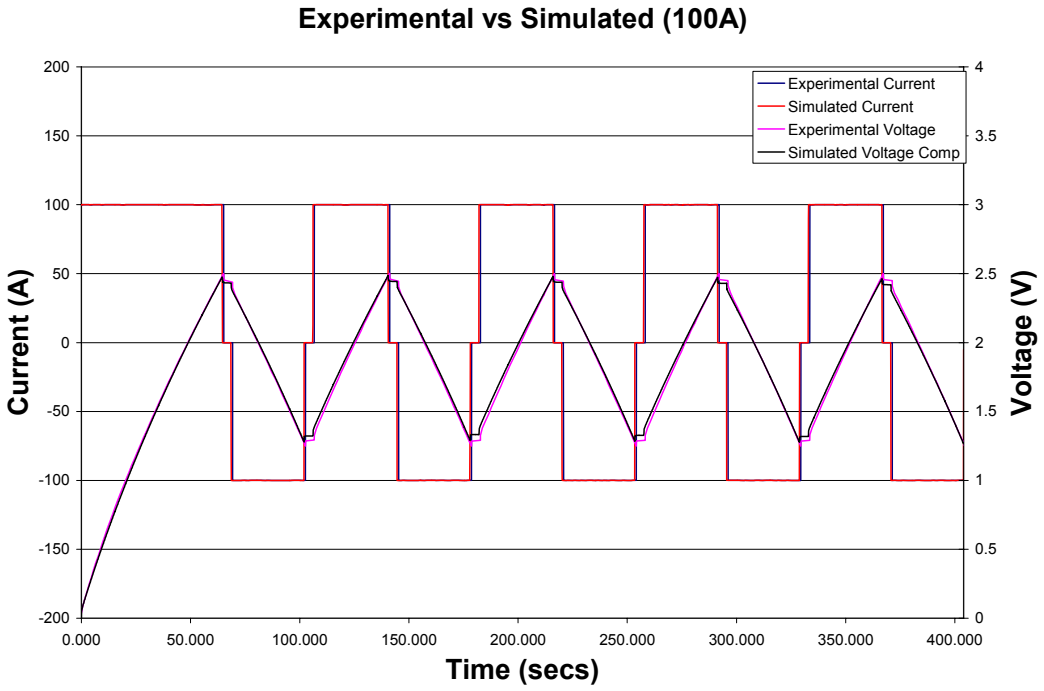


Figure 28. Galvanostatic cycling of the experimental SEC and voltage-dependent SEC model (with adjusted capacitance-versus-SOC voltage equations).

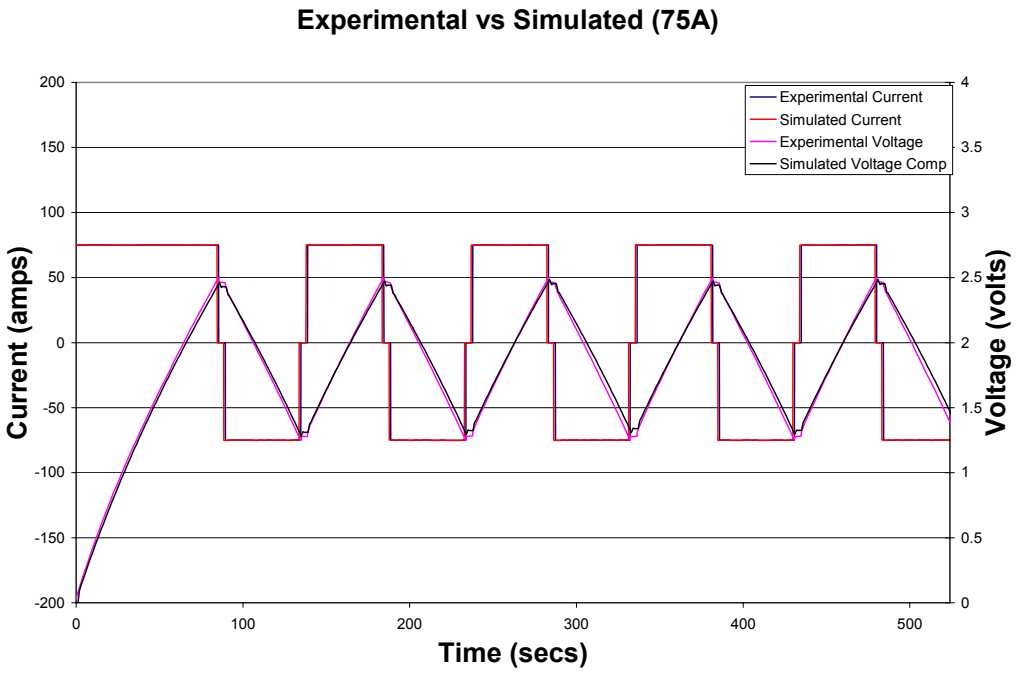


Figure 29. Galvanostatic cycling at 75 A.

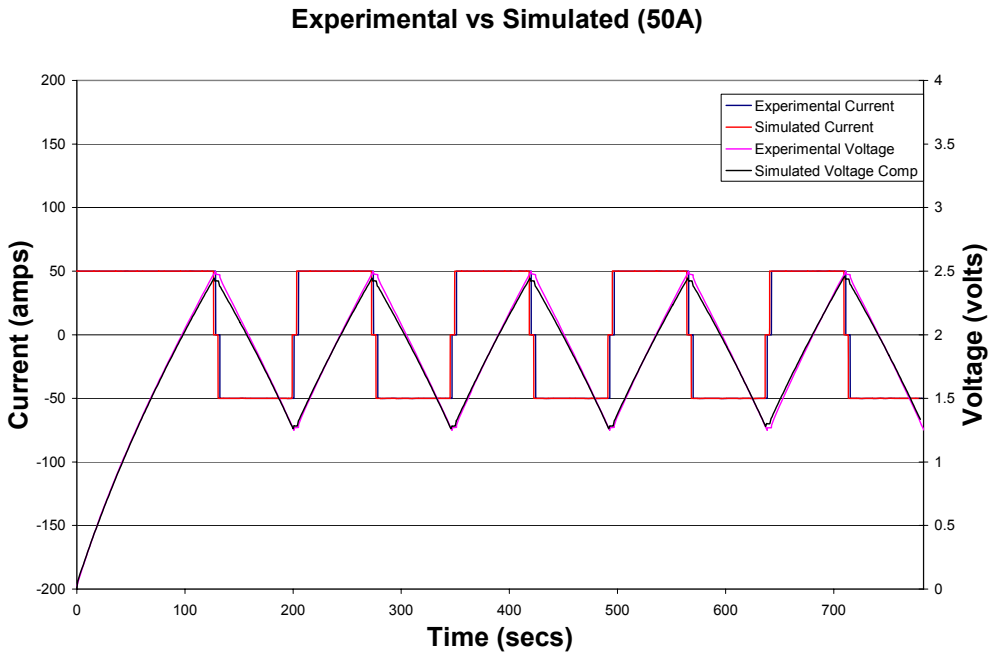


Figure 30. Galvanostatic cycling at 50 A.

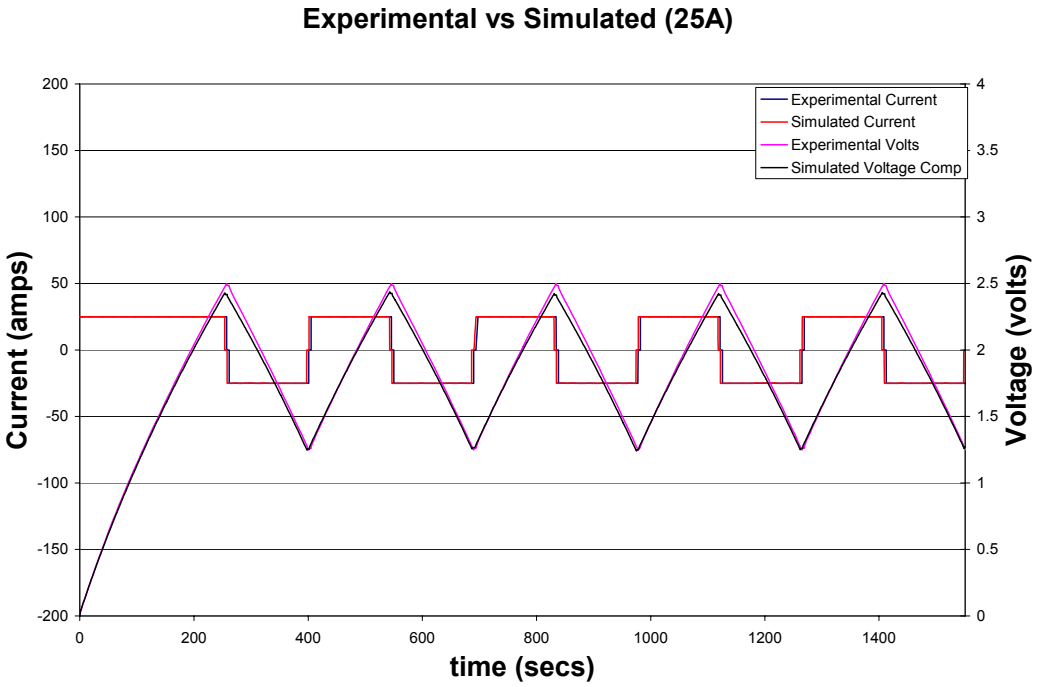


Figure 31. Galvanostatic cycling at 25 A.

As mentioned earlier, the total energy stored in a capacitor is proportional to one half the capacitance (C) times the square of the voltage across the capacitor as in equation (3). To compare the single RC network, the constant RC ladder network, and the voltage-dependent RC network with experimental SEC data, the three types of electrical models and the experimental data from the SEC were charged from 0 to 2.5 V using a 100-A constant current. The resulting data is shown in Figure 32. Note that the constant RC ladder network, where the network parameters L, R, and C are held constant, is labeled CRCN in the figure whereas the single RC circuit is labeled RC.

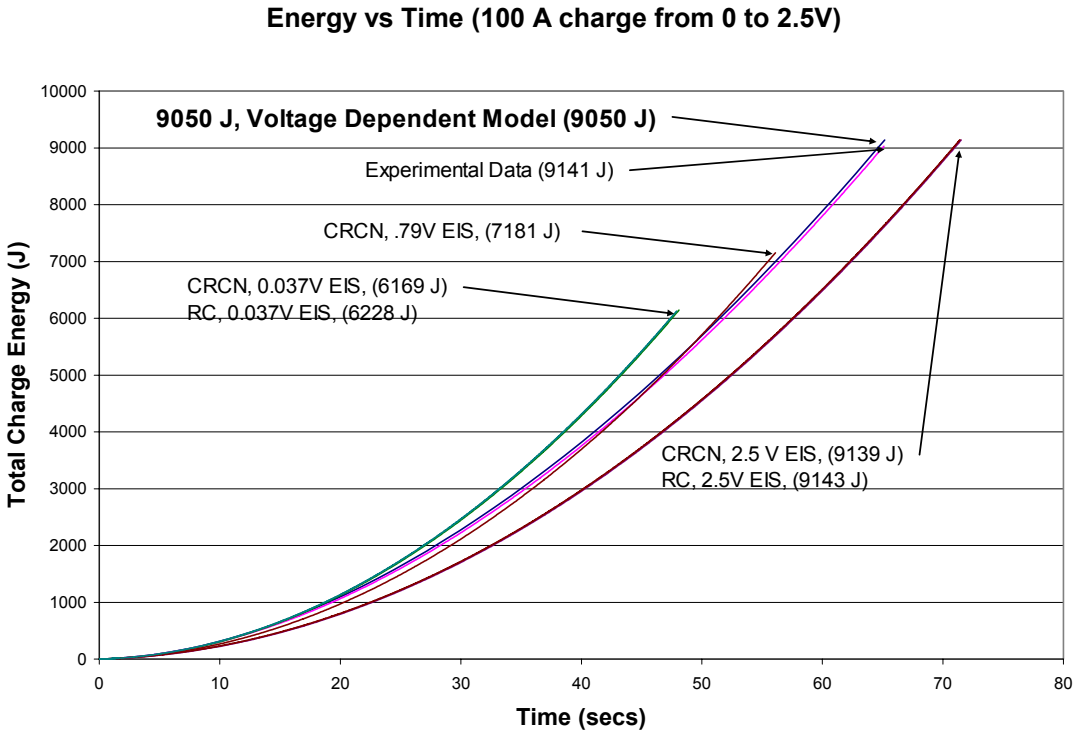


Figure 32. Total energy resulting from a 100-A charge from 0 to 2.5 V.

The CRCN models were developed based on the data from Figure 22. Three different voltages were selected from the EIS data (.037 V, .79 V, and 2.5 V) and CRCN models were developed using this data set. The single RC circuit model used only two of these voltages (.037 V and 2.5 V). As can be seen from the above figure, the experimental SEC data reached 9141 J in about 65.1 seconds. The voltage-dependent model reached 9050 J in the same amount of time (a difference of only 91 J). Both the CRCN and RC models (using the 2.5-V EIS data) charged to 2.5 V in about 71.41 seconds and reached 9139 J and 9143 J, respectively. The CRCN and RC (using the .037-V EIS data) both charged to 2.5 V in about 47.91 seconds with the total energy equaling 6169 J and 6228 J, respectively. The CRCN (using the .79-V EIS data) charged to 2.5 V in 56.1 seconds with a total energy of 7181 J. For comparative purposes and arbitrarily picking the time

to charge at 40 seconds, the experimental SEC data was compared to the models; the results and the deviation from the experimental data are given in Table 2.

Table 2. Total Energy Comparison at 40 Seconds

	Total Energy (J)	**Energy Difference (J)**
Experimental SEC data	3835	-
Voltage-dependent RC Network	3753	82
CRCN (.037-V EIS Data)	4314	479
RC (.037-V EIS Data)	4314	479
CRCN (.79-V EIS Data)	3694	141
CRCN (2.5-V EIS Data)	2979	856
RC (2.5-V EIS Data)	2979	856

At 40 seconds, and based on the above table, the voltage-dependent RC network model shows the least deviation from the experimental data. Additionally, the voltage-dependent model follows the experimental SEC energy curve throughout the charge time. The charge time and energy of the voltage-dependent RC network mimics the experimental SEC device very well.

10. SEC StatCom Application

In bulk power transmission systems, power-electronics-based controllers (FACTS controllers) are frequently used to improve the stability of the electric utility system both at transmission and distribution voltage levels. Some smaller rated FACTS controller concepts have been applied for end-use applications (*i.e.,* near the customer). These FACTS controllers can also help delay or minimize the need to build more transmission lines and power plants and enable neighboring utilities and regions to economically and

reliably exchange power. As the vertically integrated electric utility structure is phased out, centralized control of the bulk power system will no longer be possible. Transmission providers will be forced to seek means of local control to address a number of potential problems such as uneven power flow through the system (or loop flows); transient and dynamic instabilities; subsynchronous oscillations; and dynamic overvoltages and undervoltages. Several FACTS controller topologies have been proposed to mitigate these potential problems, but transmission service providers have been reluctant to use them, usually due to cost and a lack of systematic control. The integration of energy storage systems such as batteries, superconducting magnetic energy storage (SMES), and ECs into FACTS controllers, however, may lead to more economical and/or flexible controllers. In many applications, the energy storage device is small and is only required to supply power for a short time. It has been shown that energy storage integrated with FACTS controllers increases the performance compared to a FACTS controller without energy storage [28]. Energy storage integration and its benefits will be covered later in this report.

While the FACTS controller/energy storage combination has been proposed in theory [29], the development of a FACTS controller/energy storage combination has lagged far behind that of FACTS alone. Considerable attention has been given to developing control strategies for a variety of FACTS controllers, including static synchronous compensators (StatComs), the series StatCom (or SSSC), and the unified power flow controller (UPFC), to mitigate a wide range of potential electric utility issues. The comparable field of knowledge for FACTS with energy storage, however, is limited. This study focuses on using ECs integrated with a laboratory FACTS controller. Before moving on to the simulation results, a brief overview of the FACTS controller will be

provided. A simplified StatCom circuit is shown in Figure 33. This figure will be used to explain the real and reactive power equations for general StatCom operation.

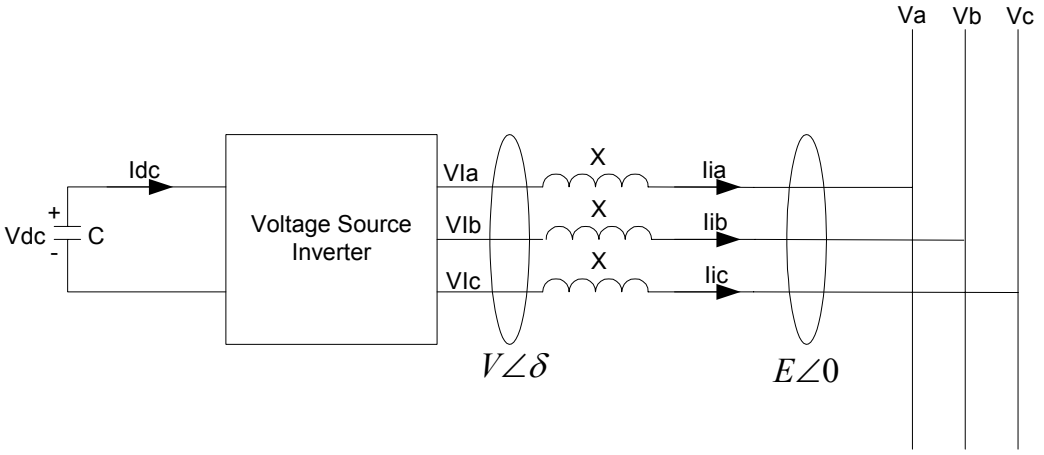


Figure 33. Simplified StatCom circuit.

The above figure includes a DC-link capacitor (C) that provides the voltage required by the voltage source inverter. Although the figure only shows a DC-link capacitor, energy storage technologies such as batteries and ECs, which are DC in nature, may be attached in parallel to the capacitor to provide additional power and voltage support. The power-electronics-based converter (in this case a voltage-source converter) converts DC power into AC power to be used by the utility at the load. The electric utility load is represented by a 3-phase voltage output (Vla, Vlb, and Vlc) and a 3-phase current output (Iia, Iib, and Iic). The leakage reactance is represented by *X*. Va, Vb, and Vc are the 3-phase voltages at the electric utility interface. The voltage-source inverter output voltage is also represented by voltage magnitude (V) and angle (δ). Similarly, the electric utility voltage at the interface is represented by voltage magnitude (E) with its reference angle set at zero. The real power (P) and reactive power (Q) delivered by the voltage-source inverter to the electric utility interface are represented by the following equations:

$$P(watts) = VE\sin\delta / X \tag{28}$$

$$Q(VAR) = (V^2 - VE\cos\delta) / X \tag{29}$$

Equation (28) indicates that real power (P) is a function of the AC voltage magnitudes (V) and (E) and the phase angle (δ) between the voltages. Given that the voltage magnitudes can only be allowed to vary within a rather narrow band (*e.g.,* ±5%), the real power is primarily a function of the phase angle. Therefore, the real power output of the inverter can be controlled by adjusting the phase angle of the inverter with respect to the grid voltage. Equation (29) shows that the reactive power (Q) is strongly dependent on the voltage magnitude, particularly for small values of δ. Thus ideally, increasing V causes the inverter to increase reactive power output. There are two methods for controlling reactive power: directly and indirectly. In direct control, the inverter output voltage magnitude (V) is adjusted, usually by keeping the phase angle (δ) close to zero to reduce real power flow into and out of the inverter. In indirect control, reactive power is absorbed from or injected into the electric utility by controlling the DC-link capacitor voltage (V_{DC}).

StatComs are best suited for voltage control because they can rapidly inject or absorb reactive power to stabilize any voltage excursions such as sags or swells [30]. Several prototype and commercial StatCom installations are currently operating and showing successful results [31]. The traditional StatCom can only provide reactive power. A StatCom with integrated energy storage, however, can provide better dynamic performance. The independent reactive and active control available from a StatCom with integrated energy storage can significantly enhance the flexibility and control of electric

utility system. The traditional StatCom has only two possible steady-state operating modes: inductive (lagging) and capacitive (leading). Although both the traditional StatCom output voltage magnitude and phase angle can be controlled, they cannot independently adjust the steady state because the StatCom has no significant active power capability. Thus, it is not possible to significantly affect both active and reactive power simultaneously. For a StatCom with energy storage, the number of steady-state operation modes is extended to all four quadrants: 1) inductive with DC charge; 2) inductive with DC discharge; 3) capacitive with DC charge; and 4) capacitive with DC discharge. Due to the nature of the energy storage technology, the StatCom will not be able to operate indefinitely in any one of the four modes (*i.e.,* the ECs cannot be continuously charged or discharged); therefore these modes only represent quasi-steady-state operation. However, depending on the energy storage technology, the discharge/charge profile is typically sufficient to provide enough energy to stabilize the power system and maintain operation until other long-term energy sources may be brought on-line.

An example of an SEC-based StatCom was evaluated using PSCAD™ with EMTDC™. A 2000-V DC link tied to a 13.8-kV (medium-voltage) AC system was used to simulate the representative SEC. As mentioned earlier, the representative SEC is rated at 2.5 V/cell. The typical operating voltage per cell is about 2.3 V/cell therefore, 1130 cells (in series) were used to achieve a voltage of 2600 V. The RC ladder network was used in the study because it can be connected in series to achieve higher voltage ratings and/or paralleled to achieve higher current ratings. The generic RC network shown in Figure 18, for example, can be scaled up using *m* cells in series and *n* cells in parallel to represent capacitor modules like those used in real applications. Assuming that all inductance (L),

resistance (*R*), and capacitance (*C*) values are identical in the RC ladder network, the number of cells in series (*m*) and of cells in parallel (*n*) can be represented by the equivalent RC circuit shown in Figure 34. Note that the voltage-dependent RC network could also be simplified using the method shown in Figure 34.

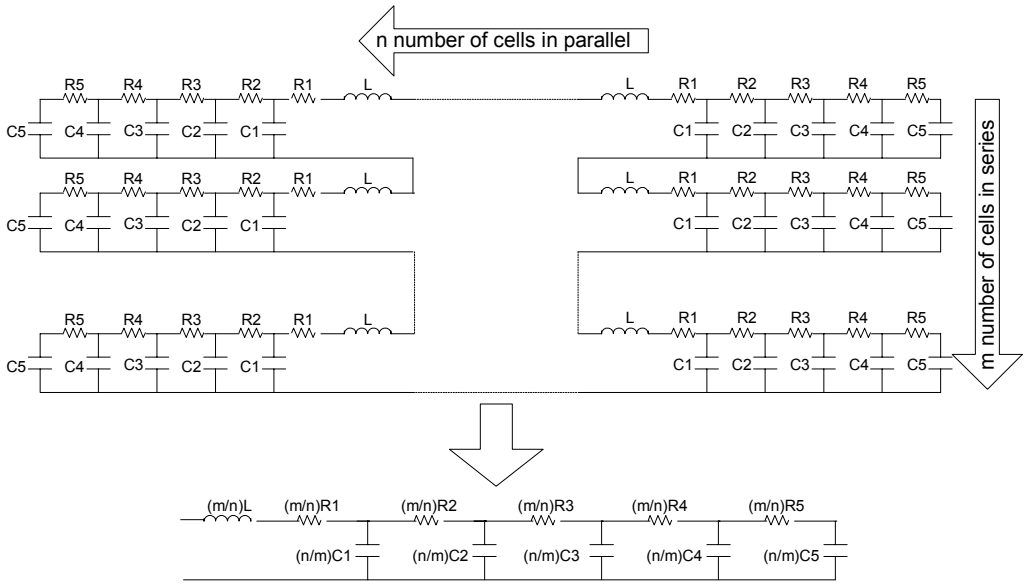


Figure 34. Equivalent RC network for series/parallel combinations.

Using the above method, a single string of 1130 cells in series was used in the dynamic simulation to create a 2600-V DC-link system rated at an operating voltage of 2000 V_{DC}. The system was subjected to a 50-ms, single-phase fault to study the transient behavior. The DC-link voltage and the AC output voltage at the grid interface were monitored and plotted during the simulation. A StatCom using electrolytic capacitors was compared with a StatCom using the representative SEC plus electrolytic capacitors. Figure 35 shows the circuit diagram of the StatCom with only electrolytic capacitors. Figure 36 shows the circuit diagram of the StatCom that uses the representative SEC plus

electrolytic capacitors. As shown in the figures, a single-phase fault occurs on Phase C of both systems.

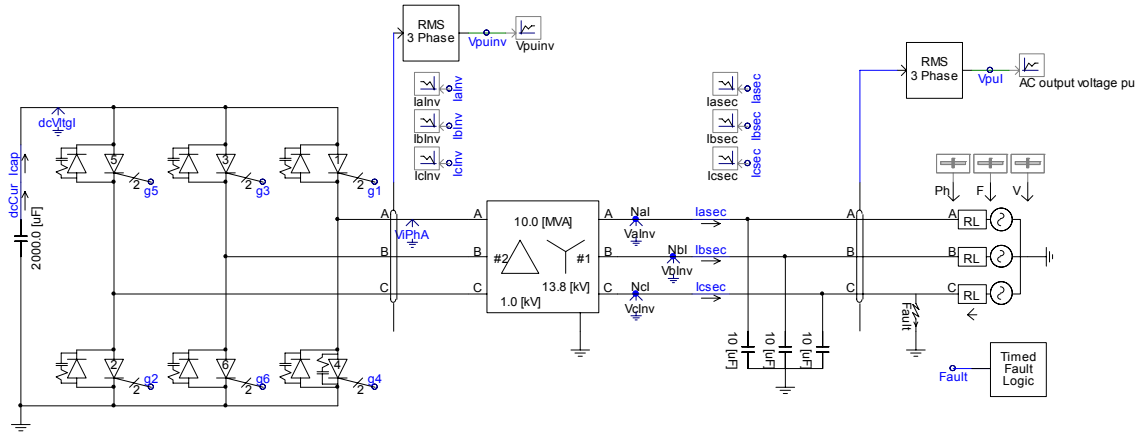


Figure 35. StatCom using typical DC-link electrolytic capacitor.

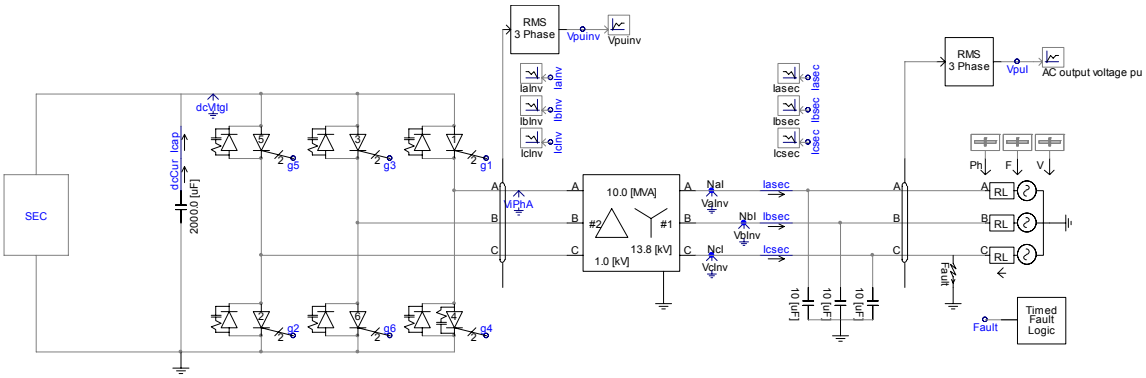


Figure 36. StatCom using representative SEC and a DC-link electrolytic capacitor.

The direct control method discussed earlier in the chapter was used in both systems. The 50-ms, single-phase fault was initiated 8 seconds into the simulation. Figure 37 shows the DC-link voltage (in kV) and the AC output voltage (per unit at the grid interface). As can be seen from the simulation results, at 8 seconds the AC output voltage starts to drop and reaches a minimum voltage of about 0.3 per unit at about 8.025 seconds. Soon after the fault goes away, the AC output voltage oscillates, and then settles back to 1.0 per unit voltage at about 8.6 seconds. The oscillation lasts about .575 seconds after the fault goes

away. In contrast, Figure 38 shows that the AC output voltage drops to about 0.8 per unit voltage at about 8.025 seconds then the voltage returns to 1.0 per unit voltage in about 5 ms. The DC-link voltage for the SEC plus electrolytic capacitor case drops to about 1.25 kV and quickly recovers to 2.0 kV.

Based on the simulation results and this system configuration, it can be seen that the addition of SECs does improve the dynamic performance of StatCom compared to a traditional StatCom solution.

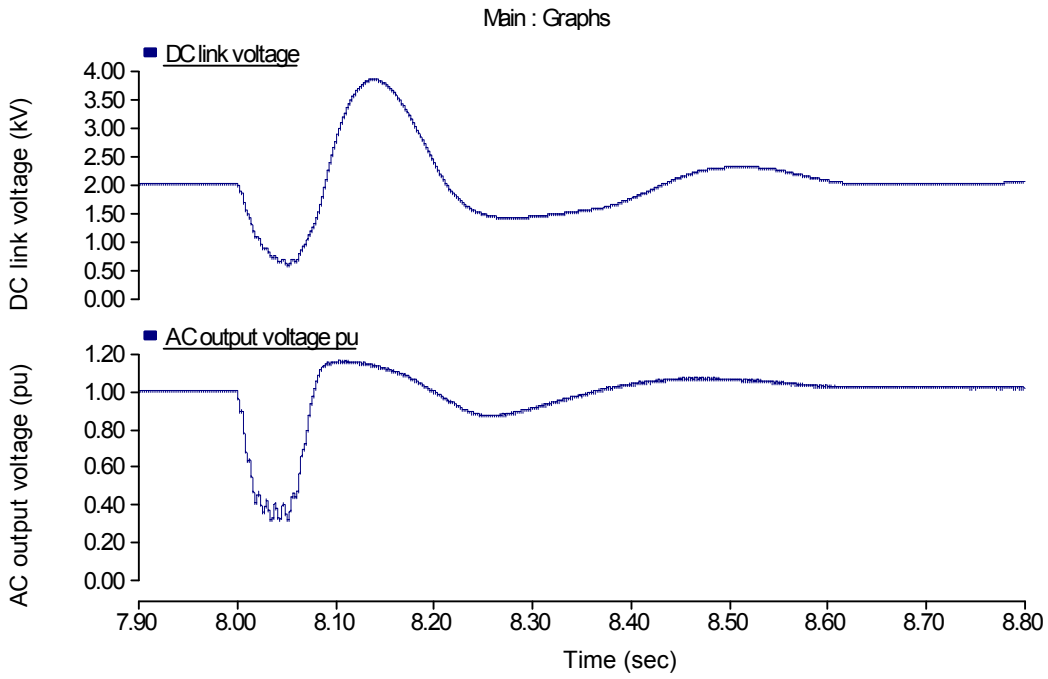


Figure 37. StatCom results (electrolytic capacitors only).

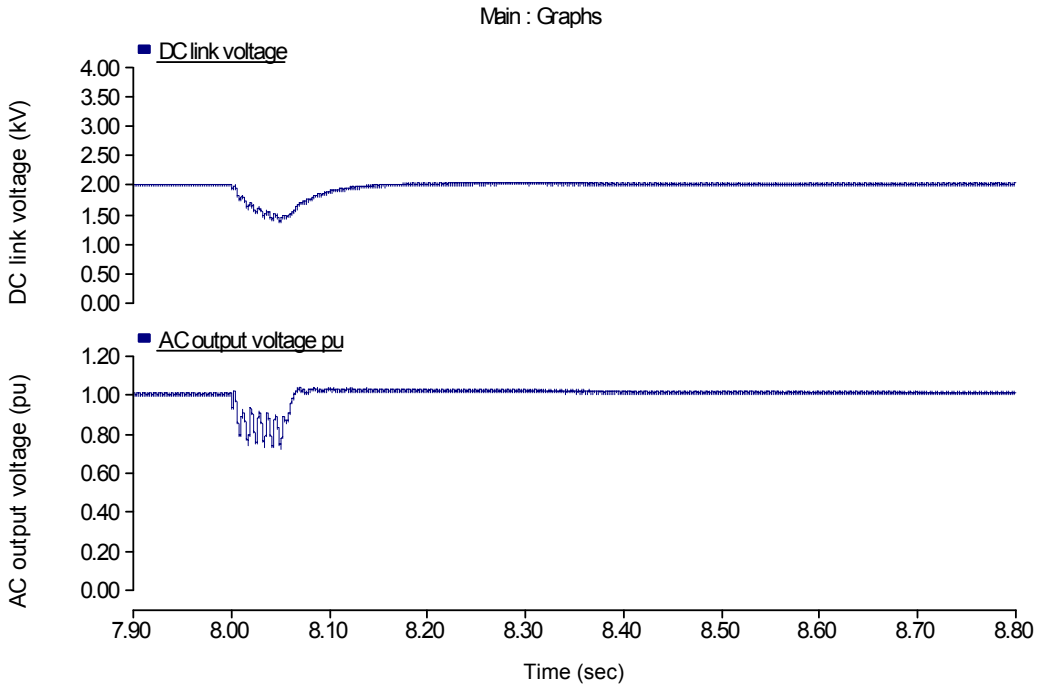


Figure 38. StatCom results (representative SEC plus electrolytic capacitors).

From a practical standpoint, connecting 1130 SEC cells in series to achieve the desired voltage may be challenging because the SECs themselves may not be perfectly voltage-matched. Most well-manufactured SECs start off well-matched in voltage but, after several cycles, they have a tendency to become unmatched; this voltage disparity among cells connected in series results in some of the cells being overcharged, which ultimately leads to cell failure or complete discharge [32]. It has been shown from abuse testing at SNL that some SECs have failed due to overcharge or over temperature [33]. Commercially available cell-balancing circuits have attempted to overcome this issue. It is beyond the scope of this paper, however, to evaluate the available cell-balancing technologies.

In an effort to reduce the number of strings in series, however, other converter topologies have been proposed, for example multilevel topologies comprising several lower rated

power converters that have a lower DC-link voltages (*e.g.,* 600 to 900 V). The lower rated converters can then be connected in series and strategically controlled to accommodate a higher voltage AC system (such as the medium-voltage AC system described above) [34]. Additionally, the direct control method may not be the best choice for SEC applications. The direct control method limits the active power and maximizes the reactive power injection into the utility. Other control methodologies have been proposed that maximize both active and reactive power, but these methodologies are still in the early stages of research and thus have not been fully tested.

Developing the optimal power converter topologies for SECs and control strategies for electric utility applications is a completely separate research topic and thus is beyond the scope of this report. Several future research opportunities exist in this area. The purpose of this study was to provide a background in StatCom technology and to compare dynamic simulations of a StatComs with and without SECs.

11. SEC Temperature Effects

The operating temperature of ECs can have a significant effect on the lifetime and performance of the device. Often ECs have to operate over a wide range of temperatures in enclosed environments, such as in electric vehicles, where the temperature under the hood can easily reach extreme high temperatures or, in colder climates in the north, where temperatures can easily fall to extreme lows. For example, the Maxwell MC2600 EC's operating temperature range is -40 to 65 ºC [35]. Additionally, ECs can have high internal heat production caused by high charge and discharge rates that cause internal current times resistance (or IR) drop. EC performance at various temperatures can have

practical significance in the overall design of the systems that use them. EIS data shows that the external temperatures affect the following two aspects of system design: 1) equivalent series resistance (ESR) and 2) capacitance. Self-discharge is another factor that can be affected by internal and external temperature changes but was not studied and reported here [36].

One way to see the temperature dependency of ECs is to analyze the EIS of the capacitor at various temperatures. A representative SEC was subjected to various temperatures (-39 ºC, -30 ºC, -20 ºC, -10 ºC, 0 ºC, 10 ºC, 17.5 ºC, 30 ºC, 40 ºC) and measured using EIS; the results are shown in Figure 39 and Figure 40. The Bode plot shows consistent real and imaginary complex impedance measurements in all frequencies and resonant frequencies within the 21.54 Hz and 31.62 Hz bands. As can be seen in the Nyquist plot, as the temperature decreases, the electrolyte resistance increases. In other words, the ESR increases as the temperature decreases (*i.e.,* it is inversely proportional). To see this clearly, the area of interest in Figure 40 was further magnified as shown in Figure 41.

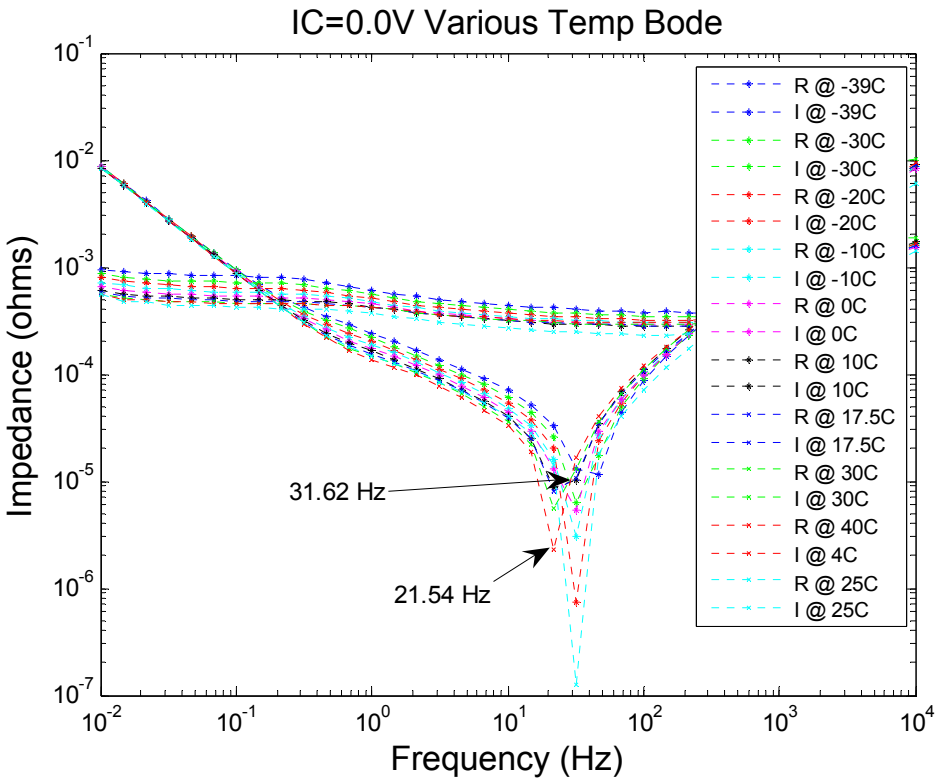


Figure 39. Bode plot of representative SEC at various temperatures.

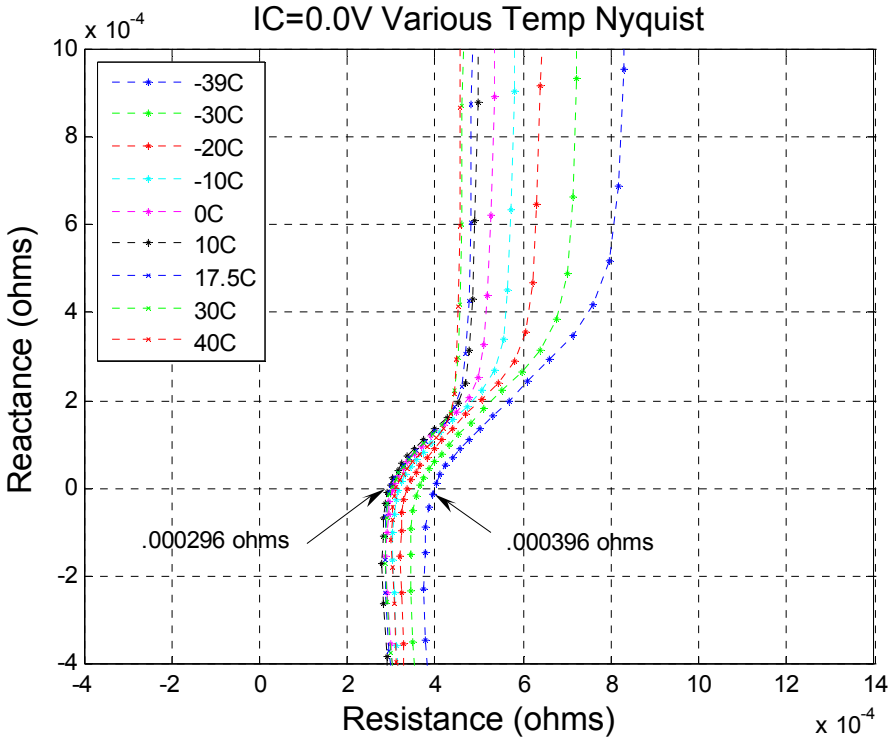


Figure 40. Nyquist plot of representative SEC at various temperatures.

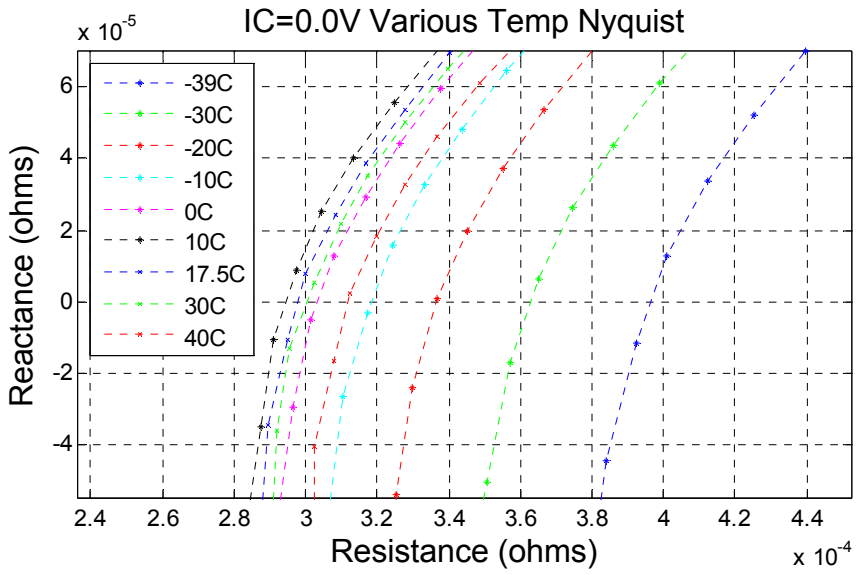


Figure 41. Magnified view of SEC EIS versus temperature.

The resistance at each temperature when it crosses the zero-reactance line was gathered and tabulated and the results are shown in Table 3. To further see the change in resistance as a function of temperature, the resultant data was plotted in Figure 42.

Table 3. Impedance at Zero-reactance Crossing

Temperature (ºC)	-39	-30	-20	-10	0	10	17.5	30	40
Resistance (Ω)	.000396	.000364	.000338	.000318	.000302	.000296	.000298	.0003	.000312

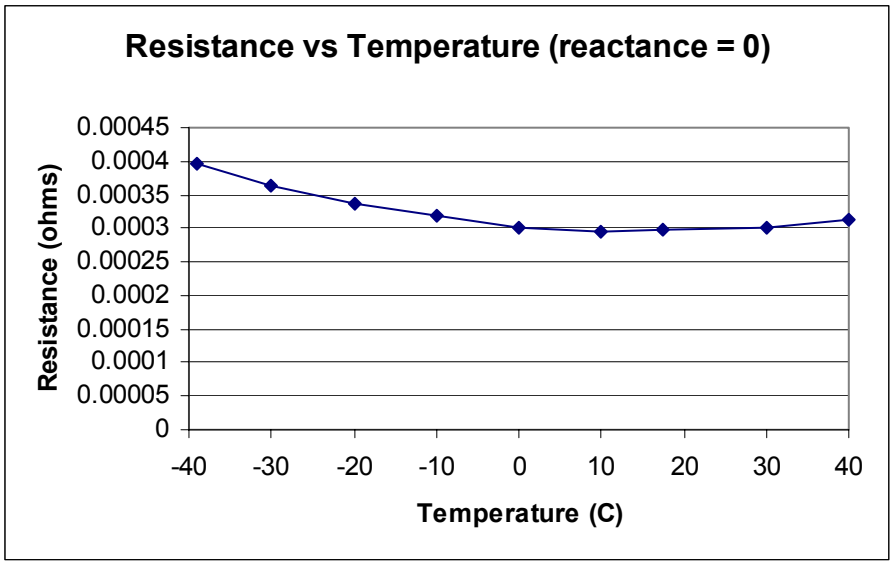


Figure 42. Resistance versus temperature at zero-reactance crossing.

As can be seen from Figure 42, the resistance decreases as the temperature increases up to about 10 ºC, after which the resistance increases slightly as the temperature continues to increase. The resistance decreases from 396 μΩ to 296 μΩ from -39 ºC to 10 ºC, which represents a 25.3% decrease. The resistance increases slightly thereafter from 296 μΩ at 10 ºC to 312 μΩ at 40 ºC (or a 5.4% increase). One possible explanation for this increase is that the resistance measurement comprises two primary resistances—ionic and electronic. These two resistances have different temperature coefficients (negative and positive, respectively). Depending on the temperature, one or the other type of resistance may be the 'dominant' type.

Ionic resistance has a negative temperature coefficient and the electrolyte conductivity of the ionic solution is temperature dependent (see Figure 43). The figure shows the conductivity measured in Siemens/cm of 1.4 molar of tetraethylammonium tetrafluoroborate (TEATFB) salt in 1.0 liter of methyl cyanide or acetonitrile [37]. Conductivity increases with temperature because the viscosity of the liquid is reduced as

the temperature increases, which reduces the drag on ions as they travel in solution. Thus, the ions become more conductive (conductivity increases) with increased temperatures. Likewise, as the temperature decreases the viscosity of the liquid is increased thus increasing the drag on the ions as they travel in solution. Consequently, the ions become less conductive (conductivity decreases) as temperature decreases.

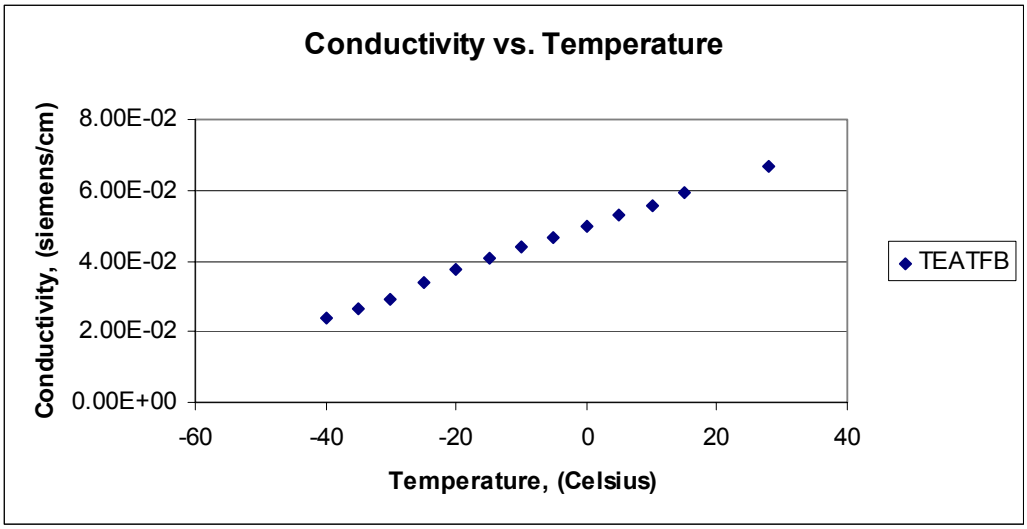


Figure 43. Conductivity of TEATFB versus temperature.

To view the conductivity plot as a resistivity plot, the experimental data was converted using the following equation:

$$R = \frac{1}{G} \tag{30}$$

where G is the conductance measured in Siemens/cm and R is the resistivity measured in Ω-cm [38]. The resistivity versus temperature is shown in Figure 44. As is evident from the figure, the resistivity of TEATFB has a negative temperature coefficient.

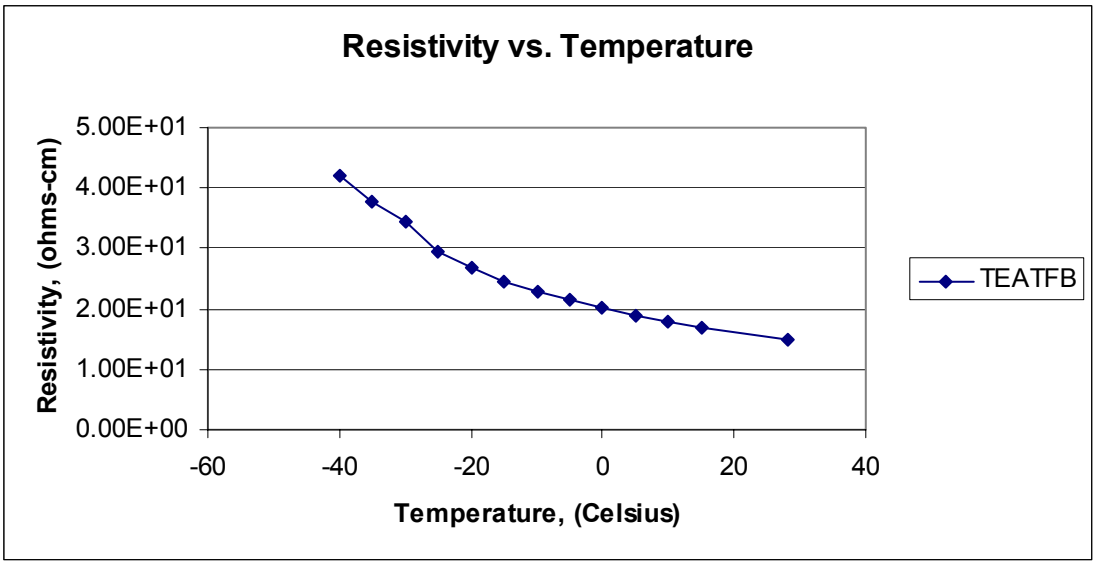


Figure 44. Resistivity of TEATFB versus temperature.

In contrast, the conductivity of most metals (*i.e.,* the electronic conductivity) decreases as temperature increases. In other words, the resistivity of most metals has a positive temperature coefficient; thus, when the temperature increases the resistance increases. The resistivity value of materials can be calculated using the following equation:

$$R = R_0[1 + \alpha(T - T_0)] \qquad (31)$$

where R equals the adjusted resistivity due to temperature (T); R_0 is the known resistivity at temperature (T_0) and α is the temperature coefficient of resistivity [39]. Figure 45, for example, shows the resistivity variation over a wide range of temperatures for copper, silver, aluminum, gold, and nickel.

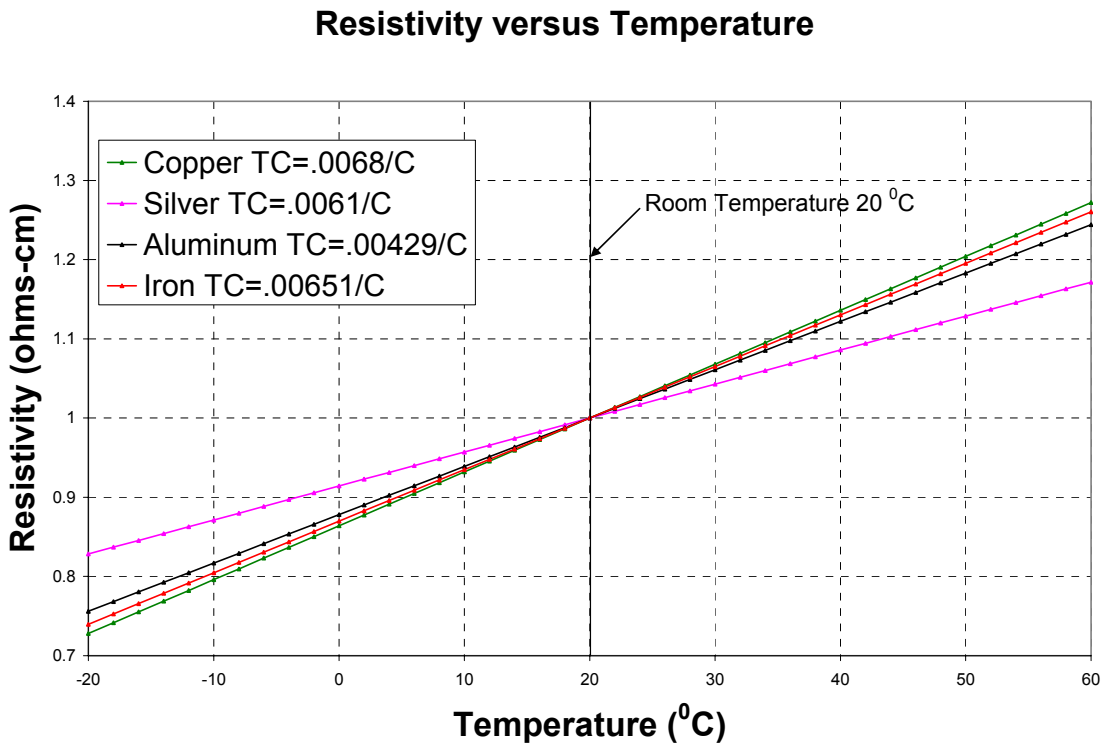


Figure 45. The resistivity of copper, silver, aluminum, gold, and nickel as a function of temperature [40].

Reviewing Figure 42, the resistance is decreasing to about 10 ºC then begins to rise. It is possible that the negative coefficient nature of the ionic resistance may dominate when the temperature is less than 10 ºC after which the electronic resistance could become dominant, therefore increasing the overall resistance. Additional research is required to better determine the exact mechanism responsible for resistance as a function of temperature.

EIS reveals that there is a slight variance in effective capacitance as the temperature increases. EIS is measured with an SOC voltage of zero. Figure 46 shows the results of the EIS measurement magnified at the lowest frequency.

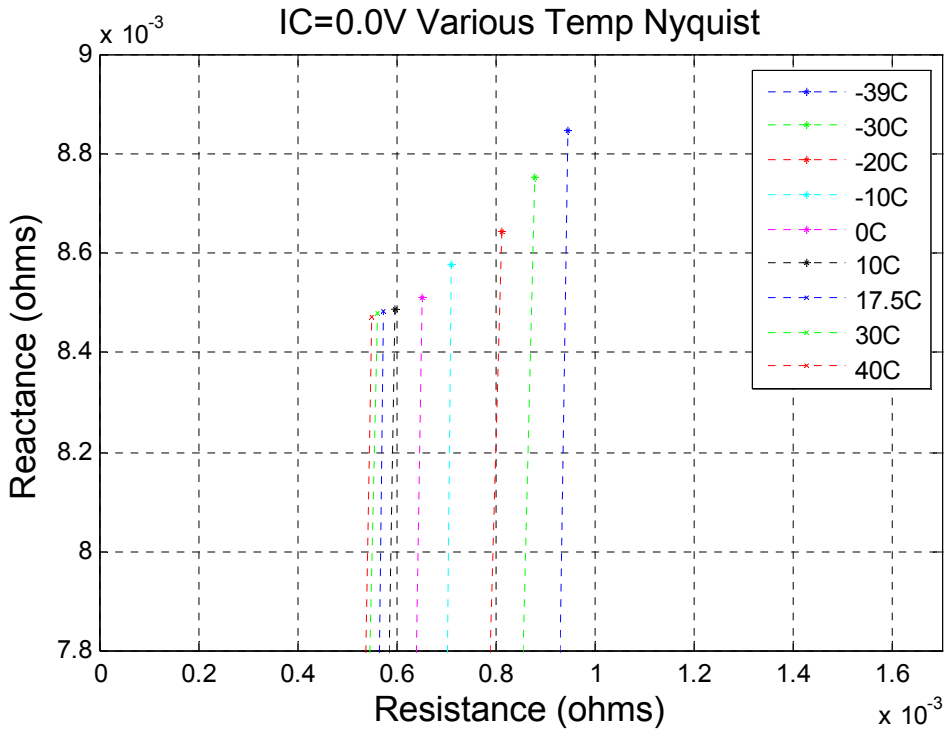


Figure 46. EIS measurement magnified at lowest frequency.

As can be seen from the figure, the reactance increases as the temperature decreases. The highest points on the plot represent a data point at .01 Hz. The capacitance reactance is defined as

$$Z_c = \frac{1}{2\pi f C} \tag{32}$$

where Z_c is the total capacitance reactance in Ω, f is the frequency in Hz, and C is the effective capacitance measured in Farads. Rearranging the above equation and solving for C yields

$$C = \frac{1}{2\pi f Z_c} \tag{33}$$

Because f at its lowest value is .01 Hz and each data point at this frequency is known, the effective capacitance using the EIS data can be calculated and evaluated as a function of temperature. The effective capacitance using EIS data at the lowest frequency (.01 Hz) as a function of temperature is shown in Table 4. This data is plotted in Figure 47.

Table 4. Effective capacitance using EIS data at various temperatures and .01 Hz.

Temperature (ºC)	-39	-30	-20	-10	0	10	17.5	30	40
Effective Capacitance (F)	1799	1818	1842	1856	1870	1875	1876	1877	1879

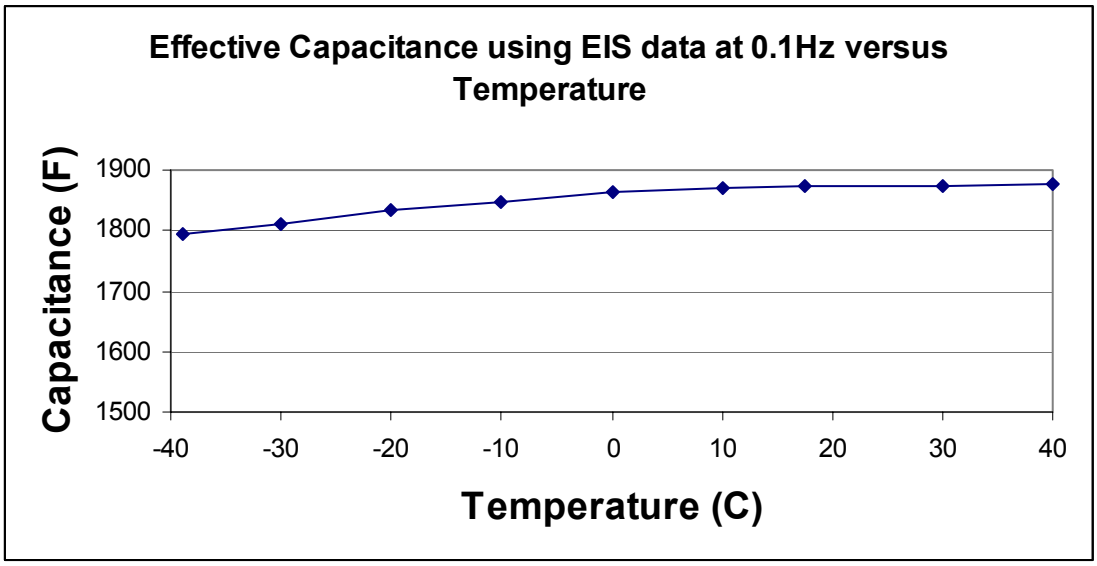


Figure 47. Effective capacitance at various temperatures and .01 Hz.

Figure 47 shows that the effective capacitance increases with temperature. According to this data, the effective capacitance increased from 1799 F to 1879 F when the temperature increased from -39 ºC to 40 ºC (a 4.45% increase). Effective capacitance increases sharply from -39 ºC to 0 ºC, and then slows down as it approaches 40 ºC. One possible explanation of this is that there might be some carbon particle separation at the

electrodes which would increase the active carbon area thus increasing the effective capacitance as the temperature rises.

The carbon particles are typically attached to the metal electrodes by some type of binder material (*e.g.,* polyvinylidene fluoride or PVDF). The coefficient of linear expansion is 25×10^{-6}/ºC for aluminum [41]; 42×10^{-6}/ºC for PVDF binder [42]; and 6×10^{-6}/ºC for carbon graphite [43]. Based on these numbers (the linear expansion of PVDF is about 1.68 times that of aluminum and 7 times that of carbon graphite) it is reasonable to expect that there will also be dimensional changes within the SEC due to the combination of aluminum/carbon/PVDF materials in the device.

In summary, the EIS data shows that the electrolyte resistance is more temperature dependent than effective capacitance. The data showed a 25.3% decrease in resistance, but only a 4.45% increase in effective capacitance over the same temperature range. The electrolyte resistance determines the ESR of the device. ESR is a significant factor in systems based on ECs because ESR determines the time constant response and power limitations of the device. The effects of temperature on time constant response and power limitations are covered in the next chapter.

12. EC Maximum Power Transfer via Resistive Load

As concluded in the previous chapter, the electrolyte resistance is temperature dependent. Temperature deviations on the EC can result from external factors and/or can be internally generated (especially in high-current and high-frequency applications). ECs used in electric vehicle applications, for example, can have extreme temperature

deviations during the summer and winter months. Likewise, high-current charges and discharges can occur in normal everyday driving.

To study the temperature effects on the maximum power transfer, a simplified case with a resistive load was used. Figure 48 is a schematic diagram showing the generic case used for this study.

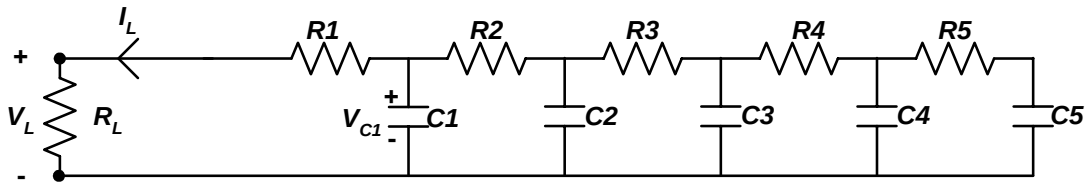


Figure 48. Generic SEC with a resistive load.

When an SEC is fully charged and equilibrated, the capacitors in the RC network (C1 through C5) will all be charged to the rated voltage. As soon as a resistive load is applied to a fully charged SEC, the voltage across the load resistor (R_L) becomes

$$V_L = \left(\frac{R_L}{R_L + R1} \right) V_{C1} \tag{34}$$

where V_{C1} is the rated charge voltage across C1. The power (P_L) dissipated by the load resistor (R_L) is

$$P_L = I_L^2 R_L \tag{35}$$

The current (I_L) through the load resistor (R_L) is defined as

$$I_L = \frac{V_{C1}}{R1 + R_L} \tag{36}$$

The power to resistive load then becomes

$$P_L = \left(\frac{V_{C1}}{R1 + R_L} \right)^2 R_L \tag{37}$$

Assuming V_{C1} and R1 are fixed, the power dissipation will be a function of R_L. To find R_L that maximizes the power dissipated, one needs to solve for R_L, where the derivative, of power (dP_L / dR_L) is equal to zero. To determine the derivative of power with respect to R_L, elementary calculus using the quotient rule was used [44]. The derivative of power with respect to R_L is

$$\frac{dP_L}{dR_L} = V_{C1}^2 \left(\frac{(R1 + R_L)^2 - 2R_L(R1 + R_L)}{(R1 + R_L)^4} \right) \tag{38}$$

For dP_L / dR_L to be zero, the equation in the numerator needs to be zero, thus,

$$(R1 + R_L)^2 = 2R_L(R1 + R_L) \tag{39}$$

Solving for R1 reveals

$$R1 = R_L \tag{40}$$

Substituting R1 in equation (38) gives the maximum power transfer to a resistive load from a fully charged EC. The maximum power transfer to a resistive load is, therefore [45],

$$P_{L(Max)} = \frac{V_{C1}^2}{4R_L} \tag{41}$$

The RC ladder network parameters for R1 were obtained using the nonlinear curve fitting routine as discussed in previous chapters. The resistor (R1) as a function of temperature is shown in Figure 49.

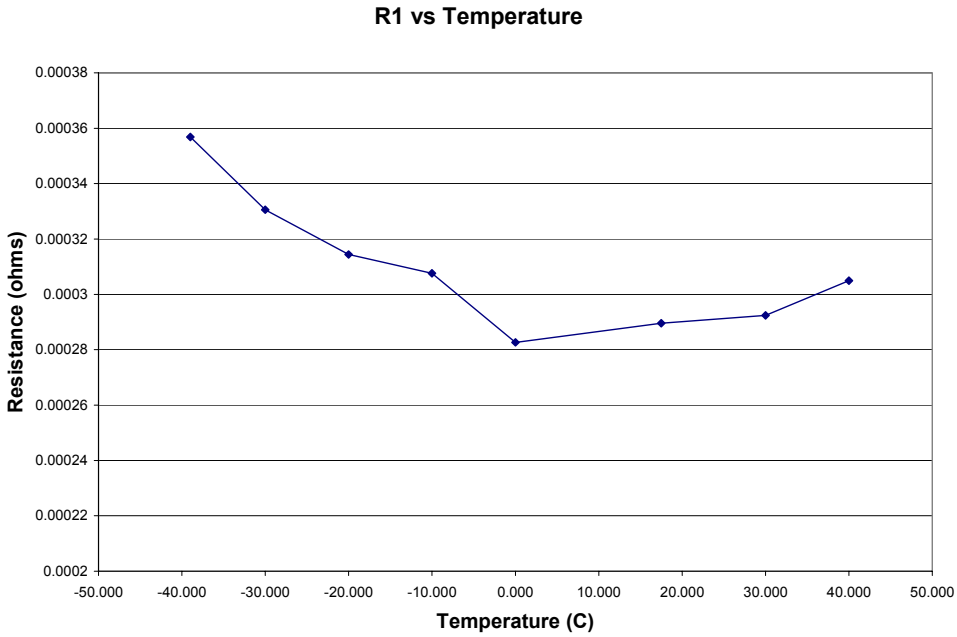


Figure 49. R1 as a function of temperature.

Equation (41) was used to generate the power transfer curves using fixed R1 values at different temperatures. Figure 50 shows power curves as a function of R_L that correspond to temperature changes from -39 ºC to 0 ºC. The maximum power increased from 4379 W to 5335 W as the temperature increased from -39 ºC to 0 ºC, respectively. In contrast, as the temperature increased from 10 ºC to 40 ºC, the maximum power decreased from 5527 W to 5124 W as shown in Figure 51. These results are consistent with Figure 49, where R1 decreases as temperature increases to 0 ºC, then increases as temperature increases. Figure 52 summarizes the maximum power transfer to a resistive load at different temperatures. As can be seen from the figures, temperatures due to internal and external factors can affect the device's maximum power delivery to a

resistive load. The results indicate that the maximum power delivered to a resistive load increases with increasing temperature.

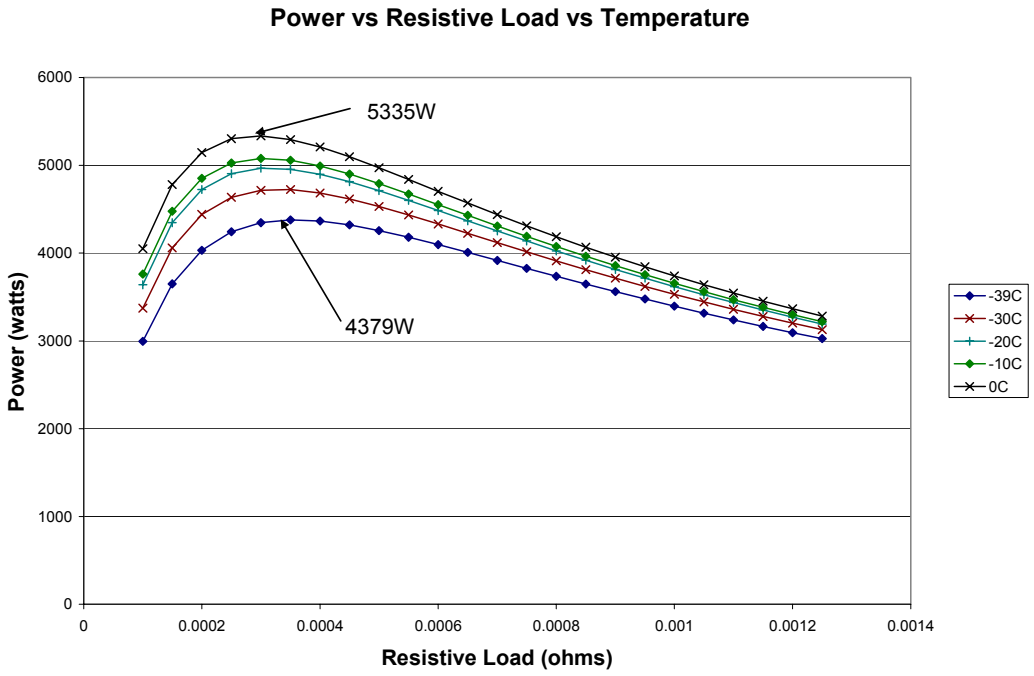


Figure 50. Power versus resistive load at temperatures from -39 ºC to 0 ºC.

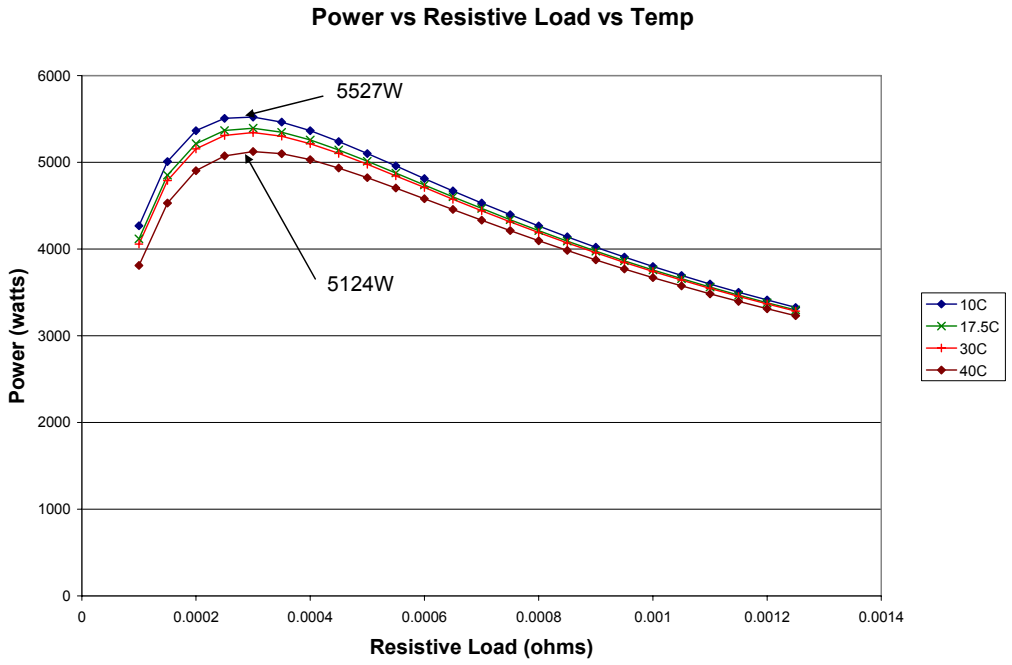


Figure 51. Power versus resistive load at temperatures from 10 ºC to 40 ºC.

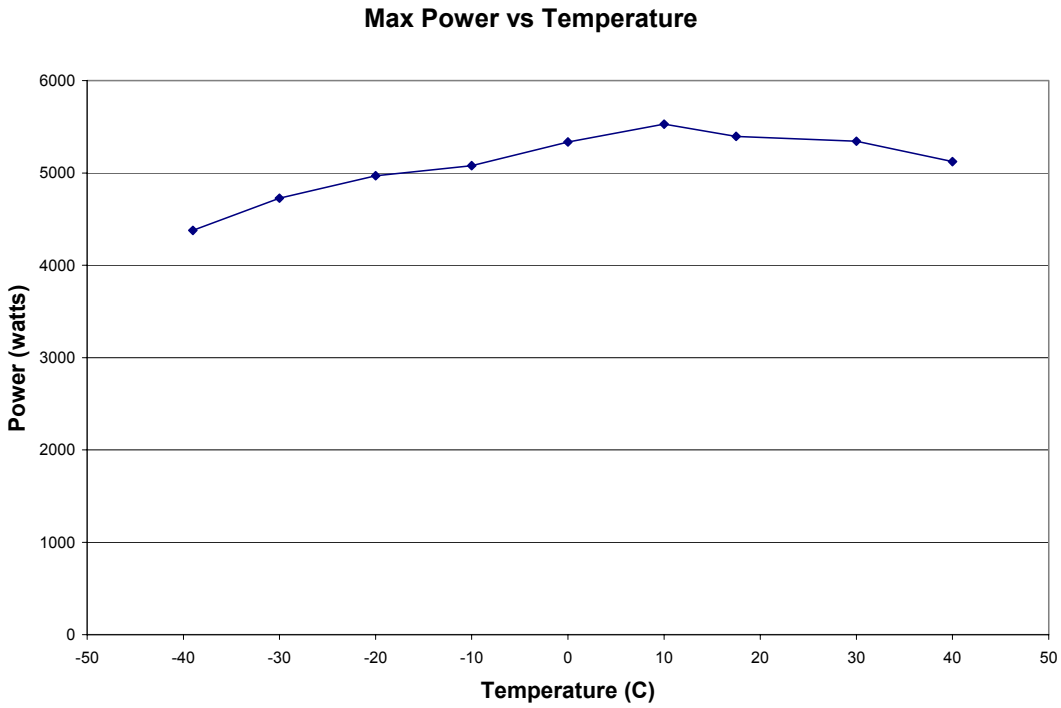
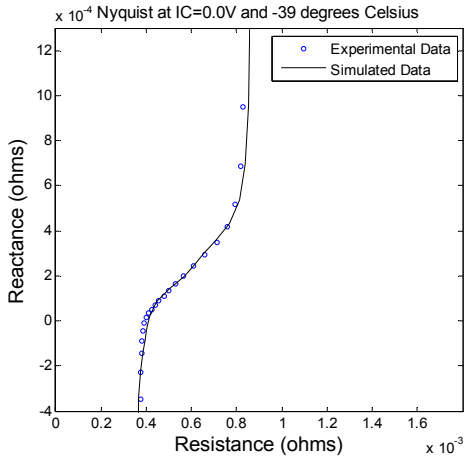
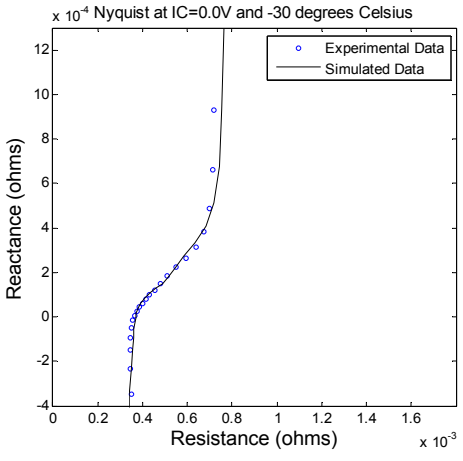


Figure 52. Maximum power transfer versus temperature.

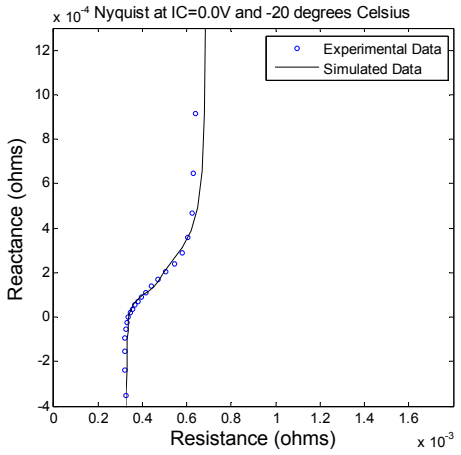
To further the understanding of temperature effects on energy, simulated constant-current discharges at 100 A and 300 A were studied. Using the same EIS data used in Figure 40, RC ladder network models were developed for the following temperatures: 40 ºC, 0 ºC, -20 ºC, -30 ºC, and -39 ºC. The Nyquist and Bode plots showing the simulated and experimental data are provided in Figure 53 (a through e) and Figure 54 (a through e).



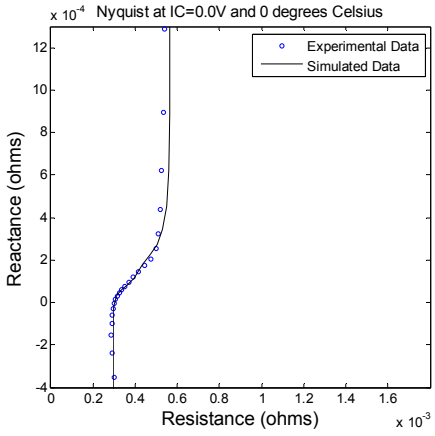
(a) -39 ºC



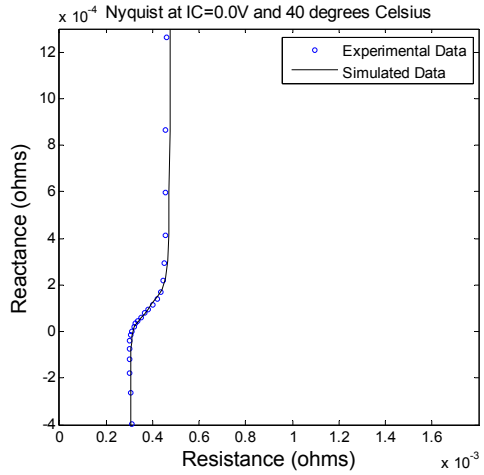
(b) -30 ºC



(c) -20 ºC

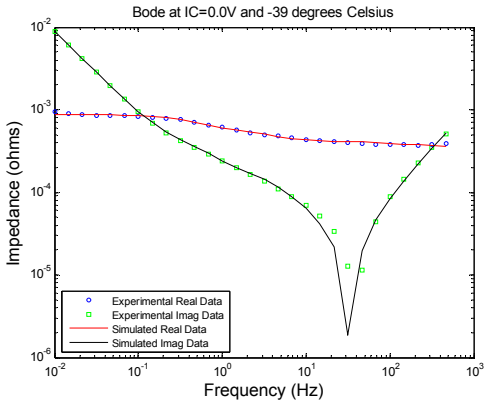


(d) 0 ºC

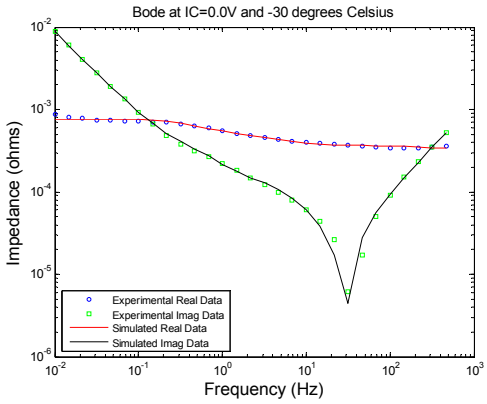


(e) 40 ºC

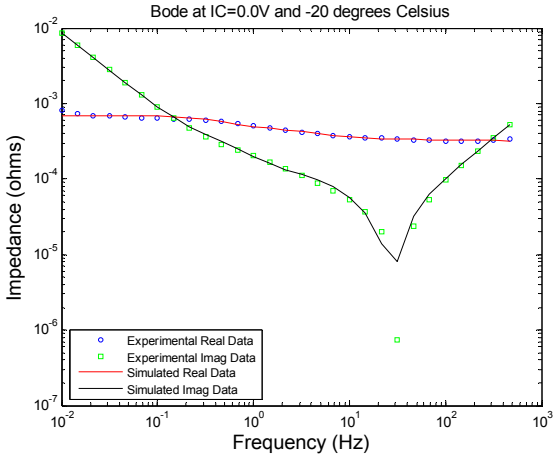
Figure 53. Nyquist plots of simulated *vs.* experimental data at various temperatures.



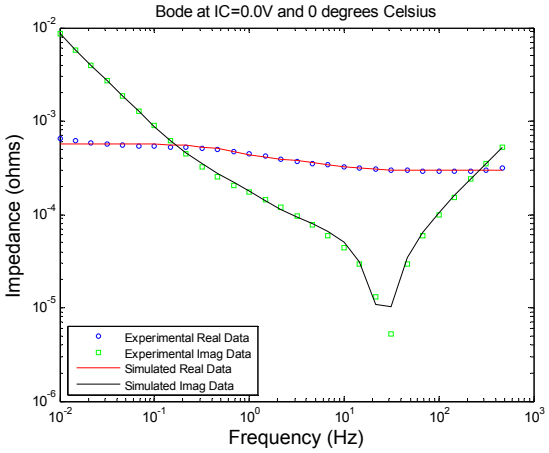
(a) -39 ºC



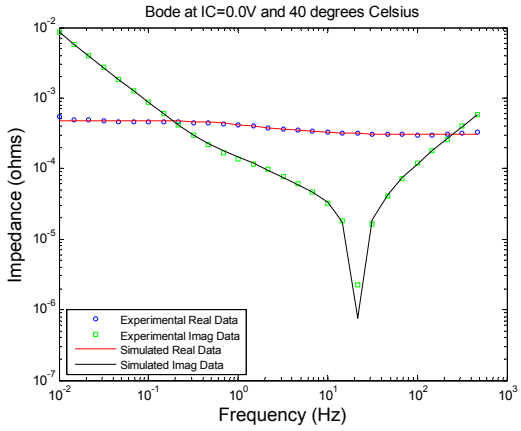
(b) -30 ºC



(c) -20 ºC



(d) 0 ºC



(e) 40 ºC

Figure 54. Bode plots of simulated *vs.* experimental data at various temperatures.

As can be seen from the above graphs, the RC ladder network models developed by nonlinear curve fitting the EIS data show good fits at all temperatures. The RC network model parameters at different temperatures are provided in Table 5.

Table 5. RC Network Model Parameters at Different Temperatures

Temp/RC Parameters	40 ºC	0 ºC	-20 ºC	-30 ºC	-39 ºC
R1	.00030	000028	.00031	.00033	.00036
R2	.000001	.000001	.00002	.00004	.00006
R3	.00005	.00009	.00015	.00016	.00017
R4	.00008	.00008	.00009	.00013	.00019
R5	.00030	.00044	.00068	.00072	.00075
C1	19	19	19	18	18
C2	169	169	166	164	162
C3	188	188	185	182	180
C4	562	560	547	542	536
C5	937	935	917	907	900
L	.20 µH	.19 µH	.18 µH	.18 µH	.18 µH

The above RC network models were subjected to 100-A and 300-A constant-current discharges; the results are shown in Figure 55.

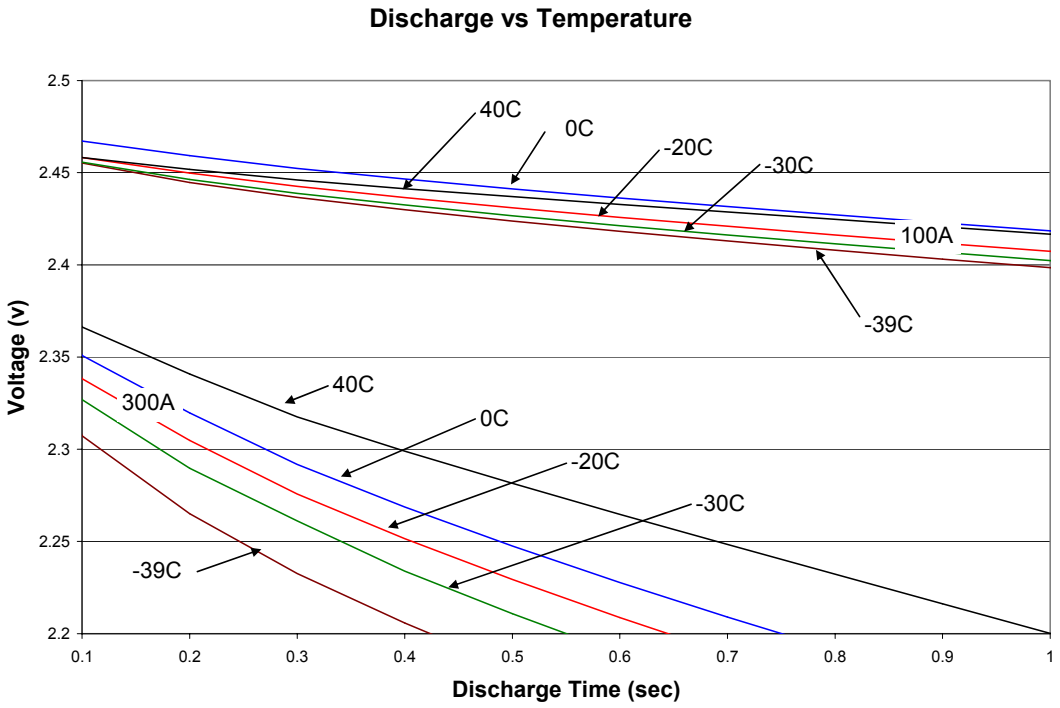


Figure 55. 100-A and 300-A simulated constant-current discharges at various temperatures.

The models were all charged to 2.5 V before a constant-current discharge was initiated. At 100 A the voltages diminished at lower temperatures due to the higher ionic resistance drop. An even higher voltage drop was seen with the 300-A constant-current discharge as the temperature decreased. The above simulation is, in general, consistent with experimental data collected by Idaho National Engineering Laboratories and shown in Figure 56 [46].

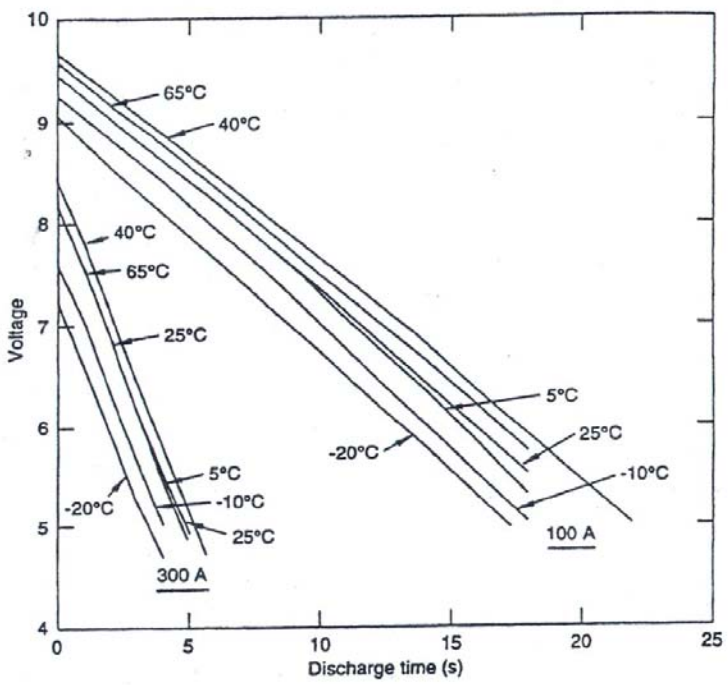


Figure 56. Effects of temperature on discharge curves for a Panasonic 3-V, 1500-F cell.

In the experiment described by Figure 56, a 4-cell string of 1500-F Panasonic devices were used to collect the data. The 4-cell string was tested at temperatures between -20 ºC and 65 ºC in an environmental chamber. The cells were initially charged to 10.25 V and discharged at a constant current of 100 and 300 A at various temperatures. The results of the experiment were similar to the modeled results; resistance increased with decreasing temperature due to the decreasing conductivity of the electrolyte. The experiment also showed a slight capacitance change as the temperature changed.

13. SEC Round-trip Efficiency

Round-trip efficiency and energy utilization are important parameters considered in system design of SEC applications. Energy utilization is defined as how much energy is stored in the capacitor during charge and how much is used during discharge. In general,

a good system design would have the highest round-trip efficiency and energy utilization. In systems that require high-power charge and discharge, for example an electric utility oscillation damping application where charge and discharge duration can be in the sub-cycles or tens of milliseconds to seconds at high current, obtaining the highest efficiency and energy utilization may be a challenge. High- and low-current charge and discharge and their effects on efficiency and energy utilization need to be better understood.

To gain a better understanding of the effects of charge and discharge currents on efficiency and energy utilization, consider a simple RC circuit with an operating voltage (V_{ov}) and a constant current source (I) shown in Figure 57.

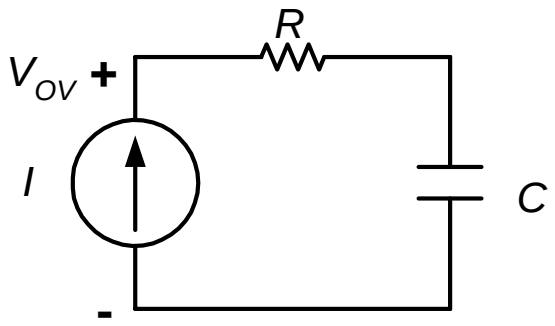


Figure 57. Simple RC circuit with a constant current source.

A typical voltage profile for a constant-current charge and discharge is shown in Figure 58. The currents (I_1 and I_2) may or may not be the same.

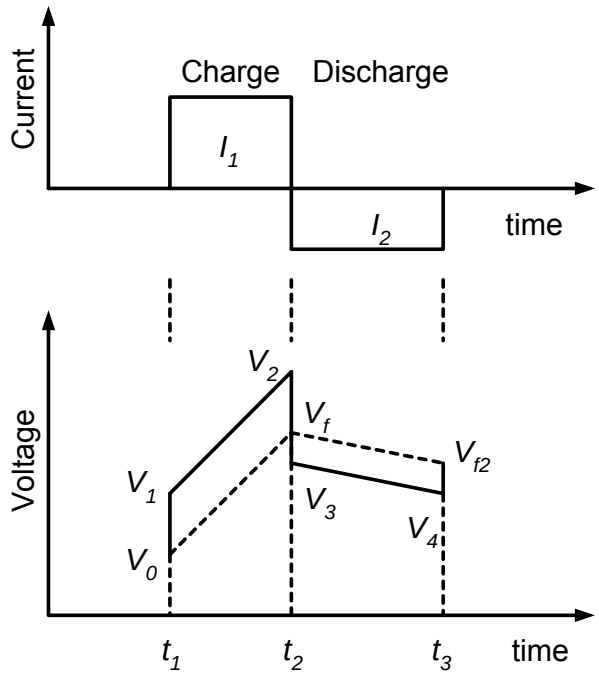


Figure 58. General current and voltage profile of a simple RC circuit.

In the voltage profile, V_0 is the initial voltage on the capacitor during the charge phase. In some cases the initial voltage can be zero. This voltage rises linearly when a constant charge current is applied to a capacitor (C). To prove this case, the current in the capacitor is defined as

$$i = C\frac{dv}{dt} \tag{42}$$

Taking the integral between t_2 and t_1 and V_f and V_o, the above equation becomes

$$\int_{t1}^{t2} idt = \int_{V0}^{Vf} Cdv \tag{43}$$

Because I_1 is constant

$$I_1(t_2 - t_1) = C(V_f - V_0) \tag{44}$$

Solving for (t_2-t_1) gives

$$(t_2 - t_1) = \frac{C(V_f - V_0)}{I_1} \tag{45}$$

Solving for V_f then gives

$$V_f = \frac{I_1(t_2 - t_1)}{C} + V_0 \tag{46}$$

The voltage in the capacitor rises linearly from V_o to V_f because the current (I_1) is constant.

During the discharge phase V_f becomes the initial voltage on the capacitor and V_{f2} is the final capacitor voltage at time (t_3). The voltage decays linearly from V_f to V_{f2} on discharge, again due to the negative constant current (I_2). The voltage (V_1) is the initial voltage rise when a constant current, I_1, is applied at t_1 and is related to V_0 by the following equation:

$$V_1 = V_0 + I_1 R \tag{47}$$

Solving for V_0 gives

$$V_0 = V_1 - I_1 R \tag{48}$$

This voltage rise will be constant throughout the charge period because I_1 is constant; consequently, V_1 will also increase linearly until it reaches V_2. V_2 is related to V_f by the following equation:

$$V_2 = V_f + I_1 R \tag{49}$$

Solving for V_f gives

$$V_f = V_2 - I_1 R \tag{50}$$

At t_2, when a negative current (I_2) is applied, V_2 immediately drops to V_3 and is represented by the following equation:

$$V_3 = V_2 - I_1 R - I_2 R \tag{51}$$

Simplifying further yields

$$V_3 = V_2 - R(I_1 + I_2) \tag{52}$$

Similar to the charge case, and due to the constant-current discharge (I_2), V_3 will decrease linearly to V_4. V_3 can be expressed as a function of V_f as follows:

$$V_3 = V_f - I_2 R \tag{53}$$

Solving for V_f the equation becomes

$$V_f = V_3 + I_2 R \tag{54}$$

V_4 is related to V_{f2} by the following equation:

$$V_4 = V_{f2} - I_2 R \tag{55}$$

Solving for V_{f2} gives

$$V_{f2} = V_4 + I_2 R \tag{56}$$

The voltages V_1, V_2, V_3, and V_4 are known as operating voltages. These are the voltages monitored and controlled by the user. Often the operating voltage limit is set by V_2 and V_4. The voltages V_o, V_f, and V_{f2} can be obtained from experimental data by measuring the voltage drop when I_1 and I_2 are applied at t_1, t_2, and t_3. It should be noted that $V_{2\text{-}max}$ is determined by the SEC voltage limit, which is generally the voltage beyond which the electrolyte in the SEC starts to break down. For example, the Maxwell BCAP0010 2600-F capacitor has a rated voltage of 2.5 V [47]. The voltages $V_{1\text{-}min}$ and $V_{4\text{-}min}$ are both determined by the power conversion system that is tied to the SEC. The actual operating voltage, V_2, will be lower than $V_{2\text{-}max}$ to provide a margin in case the application requires charging the capacitor and to prevent exceeding the $V_{2\text{-}max}$ rating. The operating voltage limits will be discussed in more detail later in this chapter.

Because SECs are DC in nature, and in order for them to be useful in electric utility applications, their output must be converted to AC using a power conversion system. In general, there are two methods for integrating the SEC with the power conversion system: 1) The SEC can be tied to a bi-directional DC-to-DC converter which is then tied to the DC link of the bi-directional DC-to-AC converter or 2) the SEC can be tied directly to the DC link of the bi-directional DC-to-AC converter. Bi-directional refers to the flow of power both into and out of the converter. Other possible configurations exist—for example, the SEC could be charged using a unidirectional converter from the AC side to the DC side of the capacitor. Certainly many other configurations for achieving the same goal are possible, but such specific configurations will not be covered here. The two general approaches that will be covered are shown graphically in Figure 59 and Figure 60.

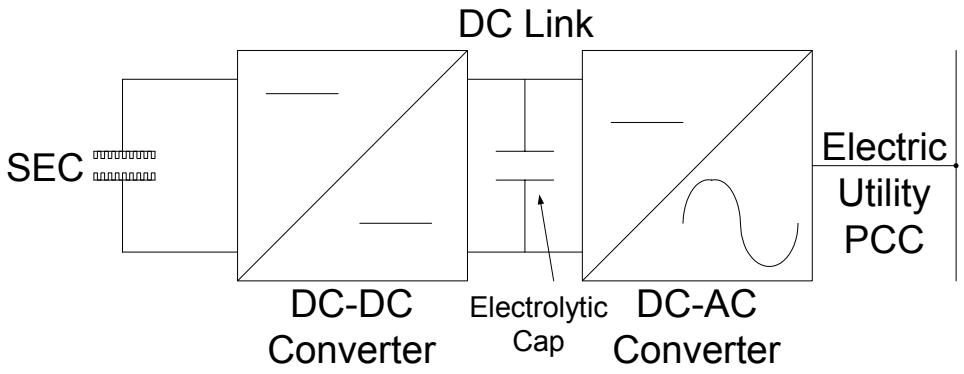


Figure 59. SEC integrated with DC-to-DC converter and DC-to-AC converter.

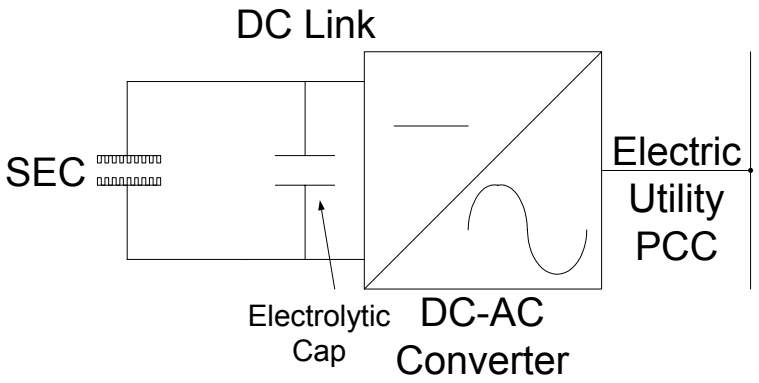


Figure 60. SEC directly tied to the DC link of the DC-to-AC converter.

The two configurations above are also known as energy storage systems, a term that collectively refers to the energy storage technology plus the power conversion system tied to the electric utility point of common coupling (PCC).

DC-to-AC inverters are known to have peak efficiencies in the low- to mid-90% range at maximum load for hard-switched solutions. Hard-switched refers to when the semiconductor switch is turned ON or OFF while the current is still flowing (which results in higher switching losses). Soft-switched refers to the situation when the semiconductor is switched ON or OFF when no current is flowing, which results in lower switching losses (or higher efficiencies) compared to hard-switched solutions. For example, a 3-kW Xantrex GT 3.0 inverter (hard-switched technology) has a peak efficiency of 94.6% [48].

DC-to-AC converters are typically tied to the utility via a transformer (which can have efficiencies as high as 97-98%). DC-to-DC 'buck-boost' converters are usually less efficient than DC-to-AC converters, with efficiencies in the low-80% to low-90% range for hard-switched solutions. As with the DC-to-AC converter, higher efficiencies can be achieved in the DC-to-DC converter using soft-switched technologies. These efficiency numbers are important when considering the overall round-trip efficiency of the system. The round-trip efficiency of the system refers to the efficiency from the electric utility PCC through the DC-to-AC converter, DC-to-DC converter, and the SEC during charge and from the SEC through the DC-to-DC converter, DC-to-AC converter, and back to the PCC during discharge. The system round-trip efficiency is thus the product of all power electronic and energy storage efficiencies from the point of view of the utility's PCC. The system round-trip efficiency will be discussed further later in this chapter.

An example of an SEC tied to a DC-to-DC converter and DC-to-AC converter is S&C's Electronic Shock Absorber. This application uses a 'buck-boost' type DC-to-DC converter where the input voltage from the SEC can be 'bucked' (or reduced) to a desired output or 'boosted' (increased) to a desired output. The steady-state input and output voltage related to the duty ratio of the buck-boost converter is determined by the following equation:

$$\frac{V_o}{V_i} = D\frac{1}{1-D} \tag{57}$$

where V_o is equal to the desired voltage output, V_i is the input voltage, and D is the duty ratio [49]. Solving for V_i gives

$$V_i = \frac{V_o(1-D)}{D} \tag{58}$$

The DC-to-DC converter controls the average output voltage by controlling the switch ON and OFF durations and the duty ratio is determined by the following equation:

$$D = \frac{t_{on}}{T_s} \tag{59}$$

where t_{on} is the time when the switch is ON and T_s is the total time period [50]. From equation (58), the theoretical minimum voltage of a buck-boost converter is zero when the duty ratio is equal to 1, but a practical minimum voltage would be determined by the maximum current the DC-to-DC converter can handle and the losses in the DC-to-DC converter. As the input voltage (V_i) decreases, the current required to keep the desired output voltage increases. At high currents the semiconductor switch's current limit may be exceeded. The electric and thermal stresses of other active and passive devices in the system may also be increased at high currents [51]. The minimum voltage can also be determined by the maximum operating current of the SEC, especially if the maximum current of the capacitor is lower than the maximum current rating of the DC-to-DC converter. The minimum voltage generally accepted by industry is 50% of the SEC's rated voltage [52]. The 50% point is where 75% of the energy can be extracted from the capacitor during discharge. Additionally, the practical upper voltage limit is not equal to the maximum SEC voltage, but is kept at a lower level to provide a margin in case the utility requires a recharge.

When the SEC is tied to directly to the DC-to-AC converter through the converter's DC link, the minimum voltage can also be limited by the maximum modulation index. This

type of converter is also known as a DC-to-AC inverter. Most DC-to-AC inverters use pulse width modulation (PWM) to achieve the desired AC output. To explain how PWM is implemented, consider a single-phase inverter that consists of two controllable semiconductor switches (SW1+, SW1-), two diodes (D1+, D1-) and an input capacitor (typically an electrolytic capacitor). A schematic of a simple single-phase inverter is shown in Figure 61.

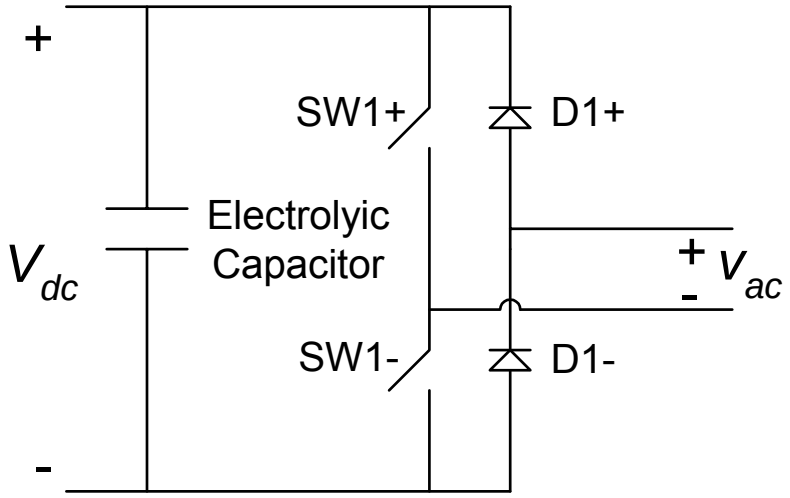


Figure 61. Schematic of a simple single-phase inverter.

V_{DC} is the input DC voltage, V_{AC} is the AC output voltage; SW1+ and SW1- are the semiconductor switches; and D1+ and D1- are the reverse recovery diodes. The DC link generally consists of a DC-link capacitor (typically electrolytic) to keep the voltage stable on the DC side. SW1+ and SW1- are controlled based on the comparison of $V_{control}$ and $V_{triangle}$, where $V_{control}$ is a sinusoidal waveform and $V_{triangle}$ is a triangular waveform. When $V_{control}$ is less than $V_{triangle}$ then SW1- is switched ON and SW1+ is switched OFF. Likewise, when $V_{control}$ is greater than $V_{triangle}$ SW1- is switched OFF and SW1+ is switched ON. A graphical representation of PWM is shown in Figure 62.

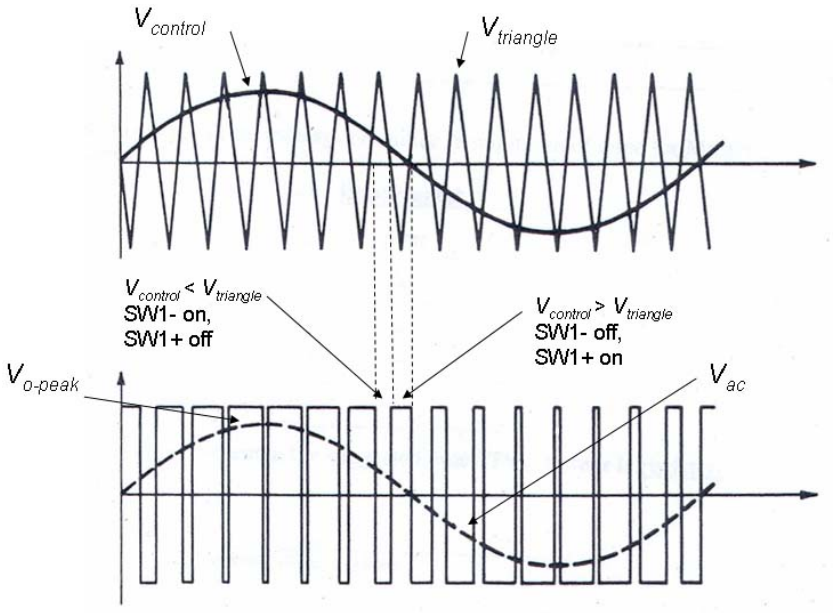


Figure 62. Graphical representation of the PWM switching scheme.

The output is a PWM waveform with a fundamental AC component (labeled V_{AC} in the figure). The mathematical relationship between the DC input and the AC output is

$$V_{ac} = \frac{V_{control}}{V_{triangle}} \frac{V_{dc}}{2} \sin(\omega t) = m \frac{V_{dc}}{2} \sin(\omega t) \tag{60}$$

where m is known as the modulation index. Based on equation (60), the peak output voltage is

$$V_{o-peak} = m \frac{V_{dc}}{2}, m \le 1.0 \tag{61}$$

Solving for V_{DC} gives

$$V_{dc} = \frac{2V_{o-peak}}{m} \tag{62}$$

Thus, V_{DC} minimum occurs when the modulation index (m) is maximum or equal to 1. Therefore,

$$V_{dc-\min} = 2V_{o-peak} \tag{63}$$

Returning to the simple RC circuit, the total net energy increase in the capacitor during charge is determined by the following equation:

$$E_{C-c} = \frac{1}{2}C\left(V_f^2 - V_0^2\right) \tag{64}$$

Using equations (48) and (50), the total energy increase as a function of the operating voltages (V_1 and V_2) becomes

$$E_{C-C} = \frac{1}{2}C\left(\left(V_2 - I_1R\right)^2 - \left(V_1 - I_1R\right)^2\right) \tag{65}$$

Expanding the above equation yields the following:

$$E_{C-C} = \frac{1}{2}C\left(V_2^2 - 2V_2I_1R + I_1^2R^2 - V_1^2 + 2V_1IR - I_1^2R^2\right) \tag{66}$$

Further simplifying yields

$$E_{C-C} = \frac{1}{2}C\left(V_2^2 - V_1^2 - 2I_1R\left(V_2 - V_1\right)\right) \tag{67}$$

The energy loss in the resistor during charge is determined as follows:

$$E_{R-C} = I_1^2R\left(t_2 - t_1\right) \tag{68}$$

Substituting equation (45) in equation (68) and simplifying the equation yields

$$E_{R-C} = I_1^2 R \frac{C}{I}(Vf - V0) = I_1 RC(Vf - V0) \tag{69}$$

Using equations (48) and (50), the energy loss in the resistor becomes

$$E_{R-C} = I_1 RC(V_2 - I_1 R - V_1 + I_1 R) \tag{70}$$

Further simplifying yields

$$E_{R-C} = I_1 RC(V_2 - V_1) \tag{71}$$

The charge efficiency is defined by equation (72). It is the ratio of the total net energy in the capacitor during charge to the total energy from the current source [53].

$$Eff_C = \frac{E_{C-C}}{E_{C-C} + E_{R-C}} \tag{72}$$

Substituting equation (67) and (71) into the above equation results in the following:

$$Eff_C = \frac{\frac{1}{2}C\left(V_2^2 - V_1^2 - 2I_1 R(V_2 - V_1)\right)}{\frac{1}{2}C\left(V_2^2 - V_1^2 - 2I_1 R(V_2 - V_1)\right) + I_1 RC(V_2 - V_1)} \tag{73}$$

Simplifying the above equation yields

$$Eff_C = \frac{\left(V_2^2 - V_1^2 - 2I_1 R(V_2 - V_1)\right)}{\left(V_2^2 - V_1^2 - 2I_1 R(V_2 - V_1)\right) + I_1 2R(V_2 - V_1)} \tag{74}$$

Further simplifying the above equation, the charge efficiency of the RC circuit as a function of V_1, V_2, I_1, and R is determined by the following:

$$Eff_C = \frac{V_2^2 - V_1^2 - 2I_1R(V_2 - V_1)}{V_2^2 - V_1^2} \tag{75}$$

To gain a better understand of equations (67), (71), and (75), the equations were plotted using the parameters given in Table 6. From equation (47), V_1 is V_0 plus voltage rise (I_1R), but in this case V_0 is equal to zero. In other words, the capacitor would be charged from I_1R to 2.5 V.

Table 6. Plotting Parameters for Charge Efficiency when V_o = 0 V and V_2 = 2.5 V

Parameters	Values
I_1	1 to 600 A
R	.0007 Ω
C	2600 F
V_2	2.5 V
V_1	I_1R (V)
V_0	0 (V)

The values for parameters I_1, R, and C were obtained from the Maxwell BCAP0010 2600-F capacitor's product specification data sheet [54]. The plot resulting from using these parameters in equations (67), (71), and (75) is shown in Figure 63.

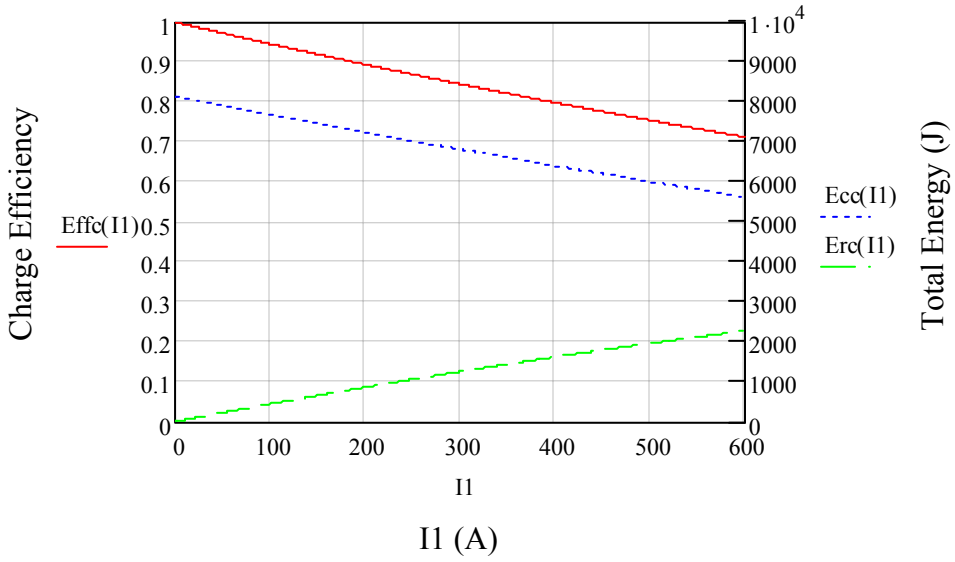


Figure 63. Charge efficiency, net capacitive energy, and resistive energy loss as a function of I_1 when V_0 = 0 V and V_2 = 2.5 V.

As seen in the graph, the efficiency (shown by the solid red line) decreases from essentially 100% to 71%. Likewise, the net energy in the capacitor during charge (shown by the blue dotted line) decreases from 8121 J to 5624 J. Energy loss in the resistor (shown by the green dashed line) increases from 4.5 J to 2271 J. Basically, these results indicate that the higher the charge current, the lower the charge efficiency, the lower the net energy in the capacitor, and the higher the energy loss in the resistor. These tradeoffs can be important for applications that require high rates of charge such as electric vehicle applications where the current can be high during stops and starts.

The time to charge a capacitor can also be important in power converter design and system studies and can give some baseline information regarding how quickly or slowly the capacitor can be charged or discharged within the chosen operating voltage limits. The system usually determines the maximum and minimum charge and discharge times. The charge efficiency versus I_1 and the time to charge versus I_1 are plotted in Figure 64.

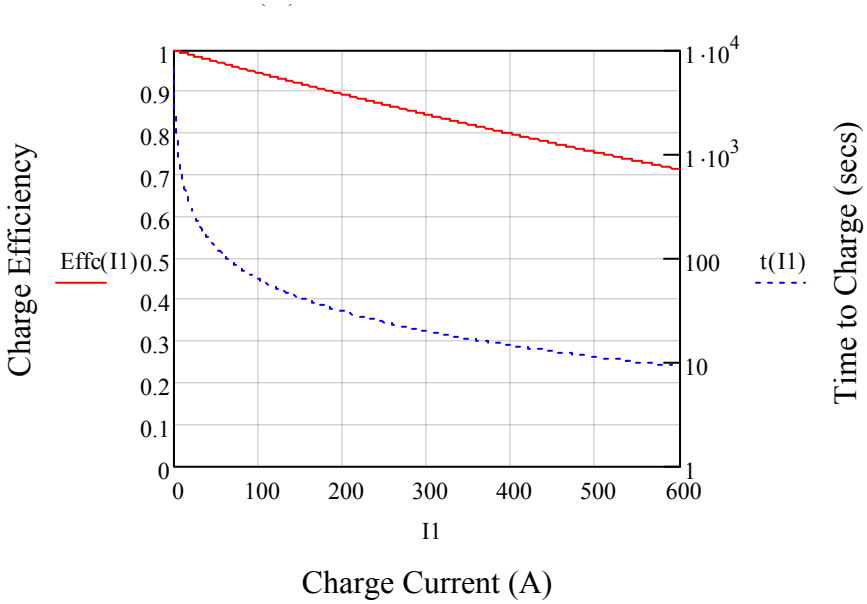


Figure 64. Charge efficiency versus I_1 and time to charge versus I_1 when V_0 = 0 V and V_2 = 2.5 V.

The charge efficiency versus I_1 is shown by the solid red line whereas the time to charge versus I_1 is shown by the blue dotted line. Note that the time to charge is plotted on log scale based on equation (45). From the above plot, the fastest charge time (about 9.01 seconds) is achieved when the maximum current (600 A) is applied. The 9.01 seconds applies to a capacitor charging from I_1R to 2.5 V minus the I_1R voltage drop at t_2. The efficiency at 9.01 seconds, however, is about 71%. At a minimal charge current (1 A), in contrast, the time to charge is about 6498 seconds. The charge efficiency approaches 100% in 6498 seconds but requires minimal charge current to achieve this efficiency. Such a low charge current may not be practical in some applications. Additionally, some applications cannot wait for a 6498-second recharge. In summary, the higher the charge current, the lower the energy utilization, the higher the resistive loss, and lower the charge efficiency.

The discharge efficiency can be found using a similar method. Again, referring to Figure 57 and Figure 58, during discharge the capacitor's initial voltage is equal to V_f at time t_2 and decays linearly to V_{f2}. Thus, the total energy of the capacitor during discharge is determined by the following equation:

$$E_{C-D} = \frac{1}{2}C\left(V_{f2}^2 - V_f^2\right) \tag{76}$$

By substituting, equations (54) and (56) into the above equation it becomes

$$E_{C-D} = \frac{1}{2}C\left(\left(V_4 + i_2R\right)^2 - \left(V_3 + i_2R\right)^2\right) \tag{77}$$

Expanding the above equation gives

$$E_{C-D} = \frac{1}{2}C\left(V_4^2 + 2V_4i_2R + i_2^2R^2 - V_3^2 - 2V_3i_2R - i_2^2R^2\right) \tag{78}$$

Simplifying the above equation yields

$$E_{C-D} = \frac{1}{2}C(V_4^2 - V_3^2 + 2i_2R(V_4 - V_3)) \tag{79}$$

Equation (79) is the total net energy discharged in the capacitor as a function of V_4, V_3, I_2, and R. The total energy loss in the resistor during discharge can be expressed by

$$E_{R-D} = I_2^2R\left(t_3 - t_2\right) \tag{80}$$

During discharge, the integral of the capacitor current would have the following limits:

$$\int_{t2}^{t3} i_2 dt = \int_{vf}^{vf2} Cdv \tag{81}$$

Because I_2 is constant,

$$I_2(t_3 - t_2) = C(V_{f2} - V_f) \tag{82}$$

Solving for (t_3-t_2) gives

$$(t_3 - t_2) = \frac{C(V_{f2} - V_f)}{I_2} \tag{83}$$

Substituting equation (83) into equation (80) gives

$$E_{R-D} = I_2 RC(Vf2 - Vf) \tag{84}$$

Then substituting equations (54) and (56) into (84) yields the following:

$$E_{R-D} = I_2 RC((V_4 + I_2 R) - (V_3 + I_2 R)) \tag{85}$$

Further simplifying yields

$$E_{R-D} = I_2 RC(V_4 - V_3) \tag{86}$$

The discharge efficiency is defined by the following equation [55]:

$$Eff_D = \frac{E_{C-D} - E_{R-D}}{E_{C-D}} \tag{87}$$

During discharge the capacitor becomes the source and the negative current source becomes the load. At the end of discharge the capacitor will deliver the total energy in the capacitor minus the total energy loss in the resistor to the constant-current load. Substituting equations (79) and (86) into equation (87) yields the following:

$$Eff_D = \frac{\frac{1}{2}C(V_4^2 - V_3^2 + 2I_2R(V_4 - V_3)) - I_2RC(V_4 - V_3)}{\frac{1}{2}C(V_4^2 - V_3^2 + 2I_2R(V_4 - V_3))} \tag{88}$$

Simplifying the above equation then gives

$$Eff_D = \frac{(V_4^2 - V_3^2 + 2I_2R(V_4 - V_3)) - 2I_2R(V_4 - V_3)}{(V_4^2 - V_3^2 + 2I_2R(V_4 - V_3))} \tag{89}$$

Further simplifying the above equation, the discharge efficiency of the RC circuit as a function of V_3, V_4, I_2, and R is determined as follows:

$$Eff_D = \frac{V_4^2 - V_3^2}{V_4^2 - V_3^2 + 2I_2R(V_4 - V_3)} \tag{90}$$

The discharge efficiency can also be represented as a function of V_2, V_4, I_2, and R when equation (52) is substituted in the above equation as shown below:

$$Eff_D = \frac{V_4^2 - \left(V_2 - R\left(I_1 + I_2\right)\right)^2}{V_4^2 - \left(V_2 - R\left(I_1 + I_2\right)\right)^2 + 2I_2R\left(V_4 - V_2 + R\left(I_1 + I_2\right)\right)} \tag{91}$$

To gain a better understanding of equations (79), (86), and (90), they were plotted using the parameters shown in Table 7, which are similar to those given in Table 6.

Table 7. Plotting Parameters for Discharge Efficiency when V_2 = 2.5 V and V_{f2} = 0 V

Parameters	Values
I_2	1 to 600 A
R	.0007 Ω
C	2600 F
V_2	2.5 V
V_3	2.5 V –R(I_2 + I_1) (V)
V_4	- I_2R (V)
V_{f2}	0 V

The above parameters allow the capacitor to achieve a full discharge from 2.5 V -$R(I_2+I_1)$ at currents I_2 and I_1 to $-I_1R$. In this case I_2 and I_1 are equal. The parameters in Table 6 and Table 7 allow the capacitor to charge from V_0 = 0 V to V_f and discharge to V_{f2} = 0 V. The resulting plot is shown in Figure 65.

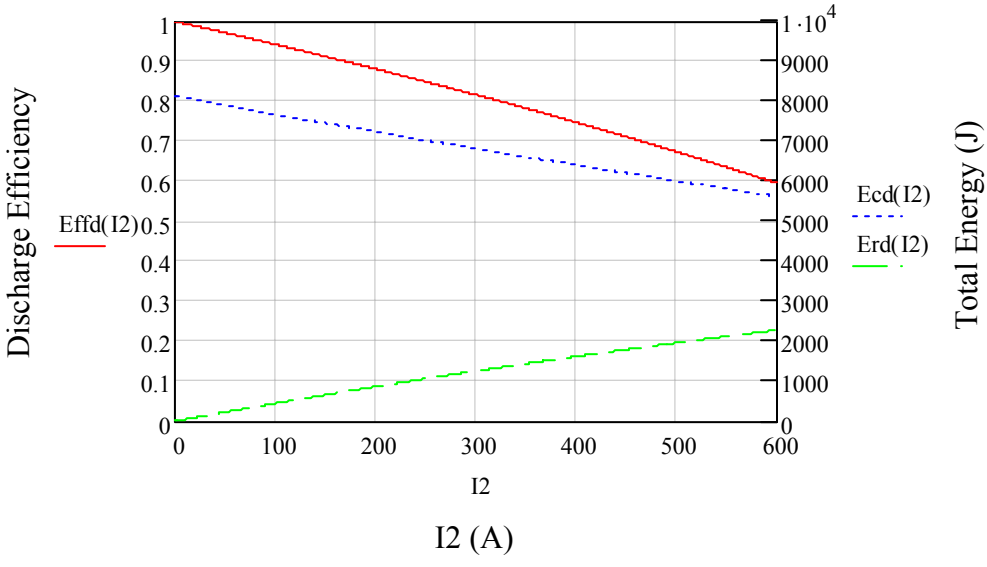


Figure 65. Discharge efficiency, capacitive energy, and resistive energy as a function of current when V_2 = 2.5 V and V_{f2} = 0 V.

The efficiency during discharge decreases from about 100% to 60%. The energy delivered by the capacitor decreases from 8121 J to 5624 J. The energy difference when I_2 increases from 1 to 600 A is the same as the energy difference when I_1 increases from 1 to 600 A during charge, which is as expected because V_0 and V_{f2} are equal and symmetric. The energy loss in the resistor increases from 4.5 J to 2271 J. The energy loss in the resistor is also the same during charge and discharge. The discharge efficiency, however, is different. At 600 A the charge efficiency decreased to 71% whereas the discharge efficiency decreased to 60%. This indicates that even in a symmetric charge and discharge voltage profile where V_0 is equal to V_{f2}, the discharge efficiency is worse than the charge efficiency by 11%. A similar conclusion could be drawn when comparing the charge efficiency, energy utilization, and resistive energy loss. The higher the discharge current, the lower the discharge efficiency and energy utilization of the capacitor, and the higher the resistive energy loss.

The discharge efficiency was also plotted against time. The resulting plot (shown in Figure 66) shows the discharge efficiency versus time (the solid red line) and the discharge current versus time (the blue dotted line). Again note that the time to discharge is plotted on log scale based on equation (83). The discharge current versus time is exactly the same as the charge current versus time. This is expected because V_0 and V_f are both equal to 0 V and symmetric. The discharge efficiency, however, differs from the charge efficiency. The discharge efficiency at the fastest discharge time (9.01 seconds) is about 60% at 600 A, compared to a 71% charge efficiency at the same current. In summary, the higher the discharge current, the lower the discharge efficiency and energy delivered by the capacitor and the higher the energy loss in the resistor.

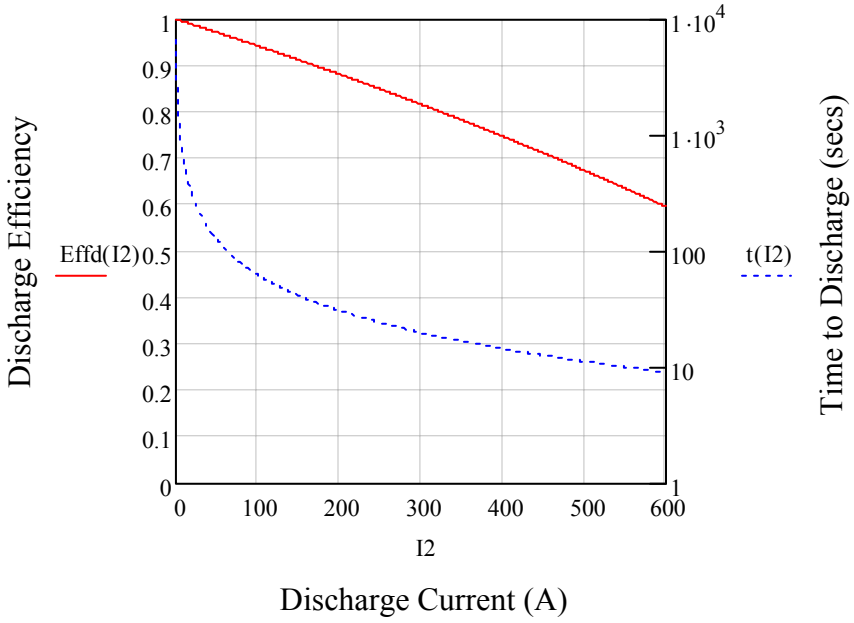


Figure 66. Discharge efficiency versus I_2 and time versus I_2 when V_2 = 2.5 V and V_{f2} = 0V.

To gain knowledge of the overall efficiency of the capacitor during charge and discharge, an analytical solution for the round-trip efficiency needs to be calculated. The round-trip efficiency can be determined by multiplying the charge efficiency (equation [75]) with the discharge efficiency (equation [90]). The round trip efficiency is, therefore,

$$RTeff = \frac{V_2^2 - V_1^2 - 2I_1R\left(V_2 - V_1\right)}{V_2^2 - V_1^2} \cdot \frac{V_4^2 - V_3^2}{V_4^2 - V_3^2 + 2I_2R\left(V_4 - V_3\right)} \qquad (92)$$

In a symmetric case (where I_1 and I_2 are equal and V_2^2 - $V_1^2 = V_4^2$ - V_3^2) V_0 and V_f are equal and the above equation becomes

$$RTeff = \frac{V_2^2 - V_1^2 - 2I_1R\left(V_2 - V_1\right)}{V_4^2 - V_3^2 + 2I_2R\left(V_4 - V_3\right)} \qquad (93)$$

To determine the round-trip efficiency due to a change in current, the round-trip efficiency was plotted using the parameters provided in Table 8.

Table 8. Plotting Parameters for Round-trip Efficiencies when V_0 and V_f = 0 V and V_2 = 2.5 V.

Parameters	Values
I_1	1 to 600 A
I_2	1 to 600 A
R	.0007 Ω
C	2600 F
V_1	I_1R (V)
V_2	2.5 V
V_3	2.5 V – $R(I_2+ I_1)$ (V)
V_4	- I_2R (V)
V_0	0 V
V_f	0 V

The round-trip efficiency plot based on the above parameters is shown in Figure 67.

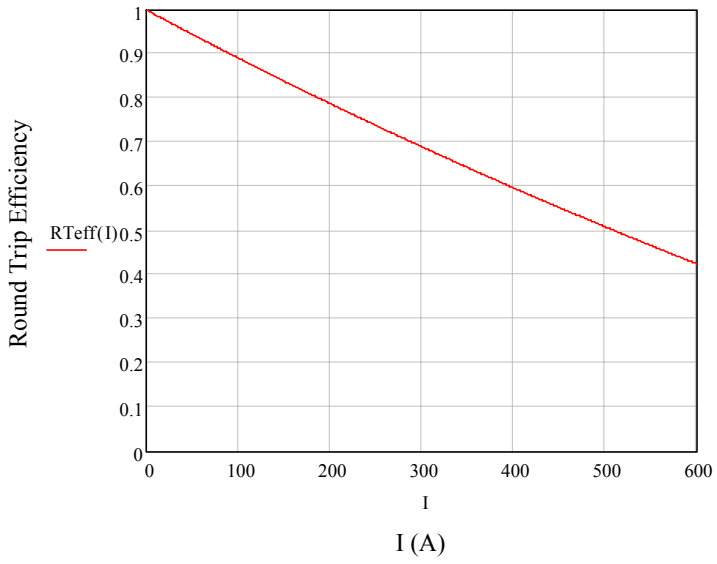


Figure 67. Round-trip efficiency versus I when V_0 and V_{f2} = 0 V.

In the above plot, because I_1 is equal to I_2, the current is simply labeled as I. As can be seen from the figure, the round-trip efficiency decreases from nearly 100% to 42% at 600 A. This decrease represents an important consideration in system studies, especially for applications with high charge and discharge rates. It is also important to note that, in actual applications, the current may not be constant during charge or discharge. How the current behaves in actual systems during charge and discharge is determined by how the control system is designed. The charge and discharge currents may be nonlinear in some applications. Actual efficiencies and total energies would have to be determined from simulated or experimental data, rather than analytically. Nevertheless, the simple RC-circuit approach provides the system designer a good starting point from which further evaluations can be made to determine the details of the design and efficiency and energy tradeoffs.

The round-trip efficiency for the RC circuit has been discussed for the case when V_0 and V_{f2} equal 0 V at the SEC level. Additionally, it is necessary to evaluate the round-trip efficiency of the entire SEC system (the SEC and the power conversion system). The system charge efficiency is the product of the DC-to-AC converter, DC-to-DC converter, and SEC charge efficiencies for the configuration shown in Figure 59. The system discharge efficiency is the same as shown in Figure 60 but without the DC-to-DC converter. The system discharge efficiency is the product of the discharge efficiency of the SEC, DC-to-DC converter, and the DC-to-AC-converter for the configuration shown in Figure 59. Again the system discharge efficiency is the same as that in Figure 60, but without the DC-to-DC converter. The system round-trip efficiency is thus the product of the system charge and discharge efficiencies. Consider the case of the configuration

shown in Figure 59. Assume the DC-to-AC converter is 95% efficient, the DC-to-DC converter is 90% efficient, and the SEC charge efficiency is 71% and the discharge efficiency is 60% at 600 A. The total charge efficiency is thus .95×.90×.71 = .61 or 61%. The discharge efficiency is thus .60×.90×.95 = .51 or 51%. Consequently, the system's round-trip efficiency is .61×.51 = .31 or 31%. For the configuration without the DC-to-DC converter the system charge efficiency is .95×.71 = .67 or 67%. The system discharge efficiency is .60×.95 = .57 or 57%. The system round trip efficiency is thus .67×.57 = .38 or 38%.

The case described above represents an extreme case, where the capacitor charged from V_0 = 0 V to V_f and discharged from V_f to V_{f2} = 0 V; as a result this case shows a grim outlook—38%—for the system's round-trip efficiency. In practical application, however, the capacitor may not be fully charged and discharged where V_0 and V_{f2} = 0 V but, rather, may operate at a higher operating voltage window, one much closer to the SEC's voltage rating. To study such a situation, consider the case where V_2 is equal to 2.0 V and V_4 is equal to half of V_2 or 1.25 V. In cyclic applications, the charge and discharge voltage cycles from V_2 to V_4 back to V_2. The operational voltage window during each cycle is determined by V_2 and V_4. The cyclic charge and discharge profile and its voltage window are shown graphically in Figure 68, which was plotted using the parameters provided in Table 9. The charge efficiency, total capacitor energy, and total energy loss in the resistor are plotted in Figure 69.

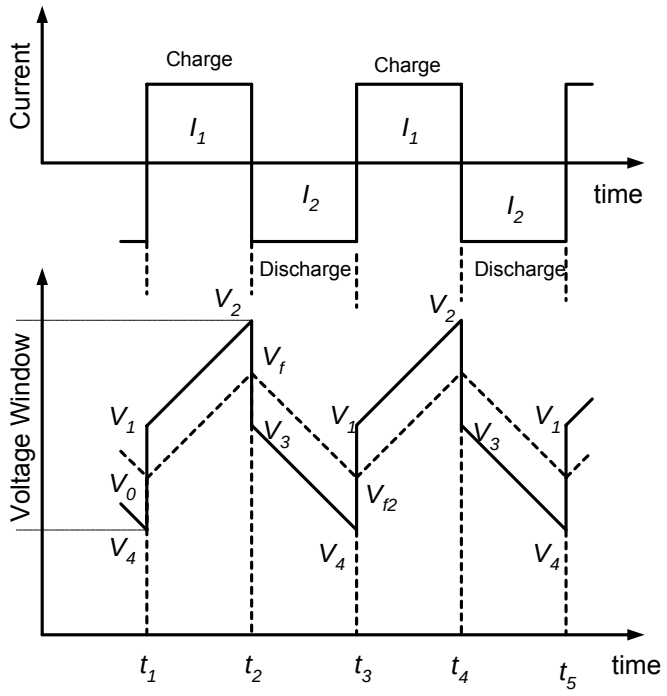


Figure 68. Cyclic charging and discharging and voltage widow.

Table 9. Plotting Parameters for Charge and Discharge Efficiencies when V_2 = 2.0 V and V_4 = 1.25 V

Parameters	Values
I_1	1 to 535 A
I_2	1 to 535 A
R	.0007 Ω
C	2600 F
V_1	$V_4 + 2I_1R$ (V)
V_2	2.0 V
V_3	2.0 V $-R(I_2 + I_1)$ (V)
V_4	1.25
V_o	$V_4 + I_1R$ (V)
V_f	$V_4 + I_1R$ (V)

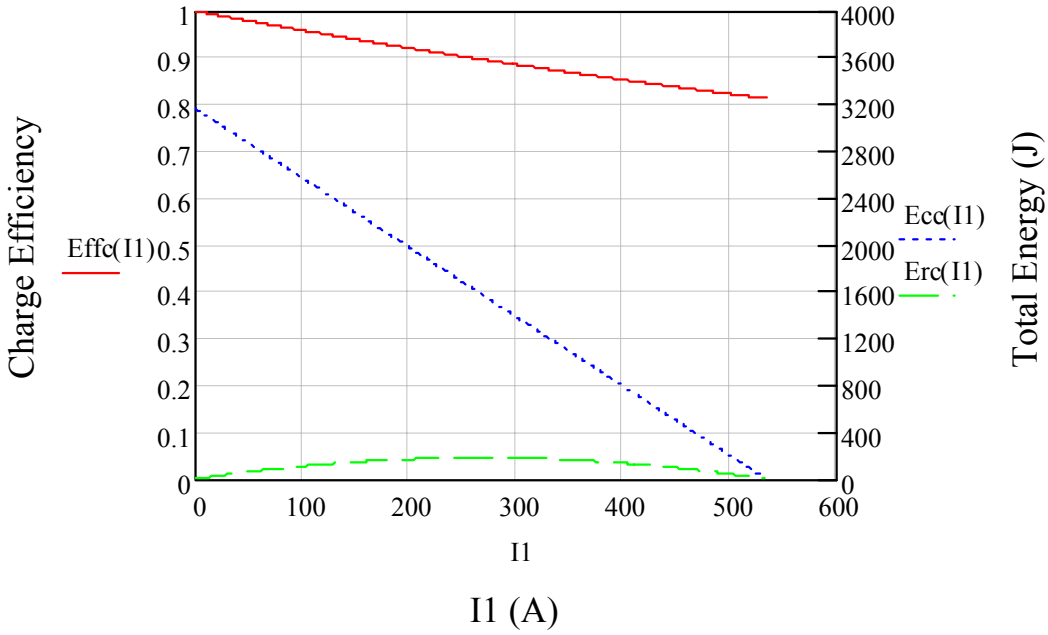


Figure 69. Charge efficiency, total capacitor energy, and total resistive energy loss versus I_1 when V_2 = 2.0 V and V_4 = 1.25 V.

As shown in Figure 69, the charge efficiency (the solid red line) decreased from 100% at 1 A to 81% at 535 A. The maximum current (535 A) will be explained below. The total capacitor energy (the blue dotted line) decreased from 3163 J at 1 A to 0 J at 535 A. The total resistive energy loss (the green dashed line) has an interesting curve. The total resistive loss increased until it reached a maximum value and then decayed back to zero. To investigate this further, the total resistive energy loss during charge was plotted alone against I_1; the resulting graph is shown in Figure 70.

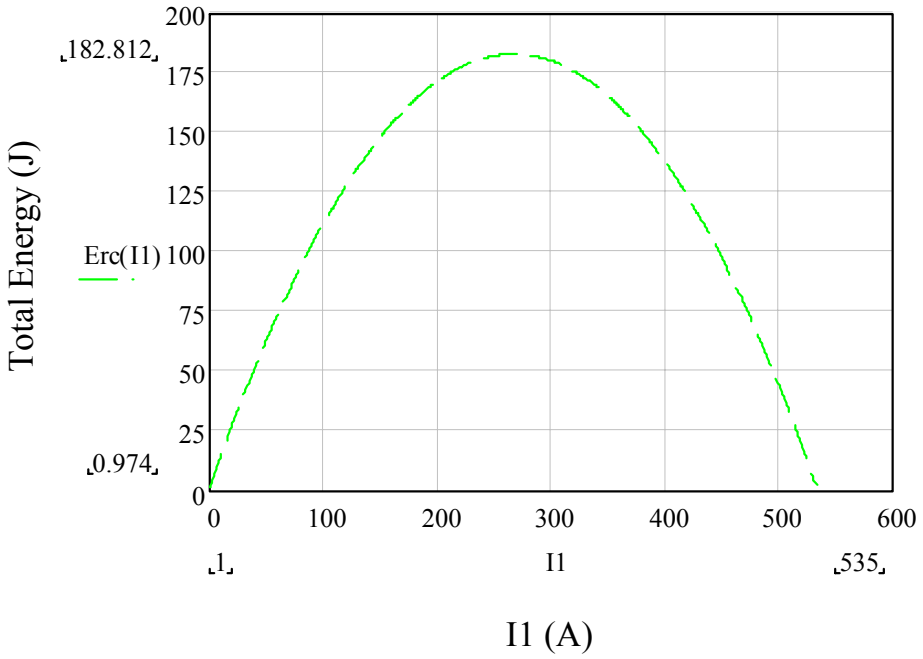


Figure 70. Total resistive energy loss versus I_1 when V_2 = 2.0 V and V_4 = 1.25 V.

To evaluate these results it is necessary to revisit equation (71), which determines the energy loss in the resistor as a function of I_1, R, C, V_2 and V_1. Recall that, as shown in Table 9, V_1 is equal to $V_4 + 2I_1R$ (V). Substituting this equation into equation (71) yields

$$E_{R-C} = I_1 RC\left(V_2 - V_4 - 2I_1 R\right) \tag{94}$$

Expanding and simplifying the above equation gives

$$E_{R-C} = I_1 RC\left(V_2 - V_4\right) - 2I_1^2 R^2 C \tag{95}$$

The maximum energy loss in the resistor as a function of current can be obtained by taking the derivative of the above equation and setting it equal to zero. The derivative of the energy loss equation is, therefore,

$$\frac{d}{dI}\left(E_{R-C}\right) = RC\left(V_2 - V_4\right) - 4I_1 R^2 C \tag{96}$$

Setting the above equation to zero and solving for I_1 the equation becomes

$$I_{1-E_{R-C}\max} = \frac{V_2 - V_4}{4R} \tag{97}$$

Because V_2 is equal to 2.0 V, V_4 is equal to 1.25 V, and R is equal to .0007 Ω, the $I_{1\text{-}ER\text{-}Cmax}$ is 267.86 A. Using equation (97), the maximum energy loss at 267.86 A is 182.81 J, which is verified by the graph in Figure 70. Also notice that the total resistive energy loss goes to zero at some I_1. To determine this value, set equation (94) to zero and solve for I_1 as follows:

$$I_{1-\max} = \frac{V_2 - V_4}{2R} \tag{98}$$

Consequently, when V_2 and V_4 are fixed, the current, I_1, has a maximum value equal to the above equation. Recall that V_1 is equal to V_4 plus two times the I_1R voltage drop. As I_1 increases, the I_1R voltage drop will increase to the point where V_1 equals V_2. At this critical point, there is no energy stored in the capacitor. The $I_{1\text{-}max}$ for this study is thus equal to 535.71 A, which can be seen in Figure 70.

The graph in Figure 69 shows the total energy in the capacitor as a function of I_1. The capacitive energy can also be represented as a percentage (known as energy utilization). The energy utilization in the capacitor during charge is 75% if V_0 is equal to half of V_f. Likewise the energy utilization is 75% if V_{f2} equals half of V_f during discharge. To prove this, refer to equation (99). This equation calculates the ratio of the total net energy in the capacitor between V_f and V_0 to the total energy in the capacitor when $V_0 = 0$ V.

$$\%EU_C = \frac{\frac{1}{2}C\left(V_f^2 - V_0^2\right)}{\frac{1}{2}CV_f^2} \tag{99}$$

Simplifying the equation gives

$$\%EU_C = \frac{V_f^2 - V_0^2}{V_f^2} \tag{100}$$

The energy utilization for discharge is similar to the charge utilization equation and is calculated as follows:

$$\%EU_D = \frac{V_{f2}^2 - V_f^2}{V_f^2} \tag{101}$$

The energy utilization can also be described in terms of V_2 and V_4. First, note that V_0 is equal to V_4 plus the I_1R voltage rise in Figure 68 at time t_1. Inserting V_0 as a function V_4 and equation (50) into equation (100) then gives

$$\%EU_C = \frac{\left(V_2 - I_1R\right)^2 - \left(V_4 + I_1R\right)^2}{\left(V_2 - I_1R\right)^2} \tag{102}$$

From equation (100), let V_0 equal half of V_f as follows:

$$\%EU_C = \frac{V_f^2 - \left(\frac{V_f}{2}\right)^2}{V_f^2} \tag{103}$$

Simplifying the above equation gives

$$\%EU_C = \frac{1-\frac{1}{4}}{1} = \frac{3}{4} \tag{104}$$

Therefore, 75% of the energy is stored during charge when V_0 is equal to half of V_f. The same is true during discharge. In the discharge case, however, the 75% of the energy is delivered or extracted when V_{f2} is equal to half of V_f.

The charge efficiency and energy utilization versus I_1 and current I_1 versus time are plotted in Figure 71. The graph indicates that, as the charge current increases, the charge efficiency (the solid red line) and capacitor energy utilization (the blue dotted line) decreases and the time to charge the capacitor (the green dashed line) is faster. The charge efficiency at 535 A is about 81%. Notice that at 1 A the capacitor energy utilization is, at best, 61%. System designers typically strive for 75% energy utilization.

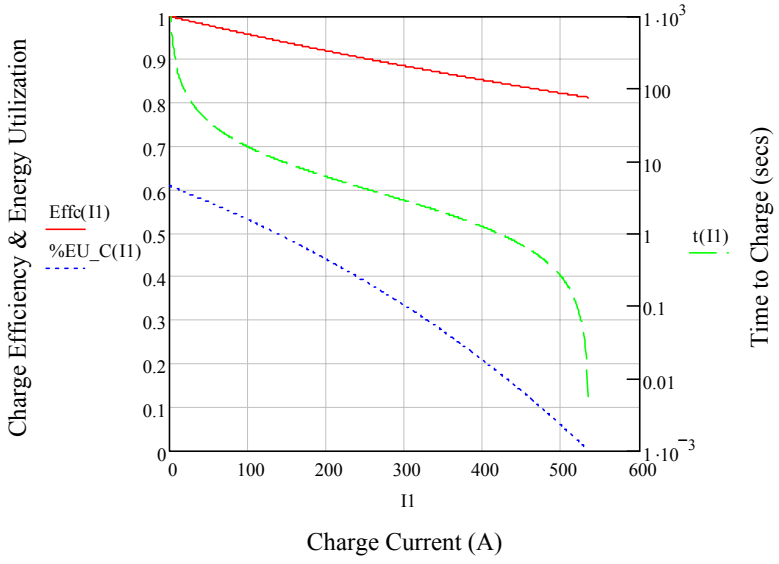


Figure 71. Charge efficiency and energy utilization versus I_1 and time versus I_1 when V_2 = 2.0 V and V_4 = 1.25 V.

To increase the energy utilization, the operating window needs to be increased. Increasing the operating window to V_2 = 2.25 V and V_4 = 1.0 V gives results shown in Figure 72. As the operating window increases from V_2 = 2.0 V and V_4 = 1.25 V to V_2 = 2.25 V and V_4 = 1 V, the energy utilization improves. The energy utilization at 1 A is 80%, whereas with the previous operating voltage window the energy utilization at 1 A was 61%. A 75% energy utilization is achieved when I_1 equals 119 A. Beyond this current, the energy utilization decreases to a minimum of 40% at 600 A. Energy efficiency is not changed much in this scenario. The fastest charge time (1.8 seconds) occurs when I_1 equals 600 A.

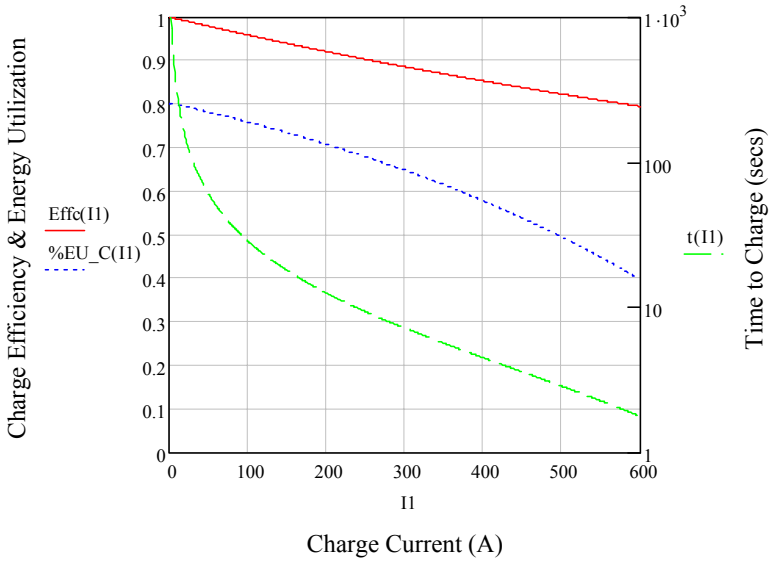


Figure 72. Charge efficiency and energy utilization versus I_1 and time to charge versus I_1 when V_2 = 2.25 V and V_4 = 1.0 V.

Based on the results above, one should be able to find a voltage window where the 75% energy utilization is always achievable between 1 and 600 A. To find this voltage window set the equation (102) to .75 as follows:

$$\frac{(V_2 - I_1 R)^2 - (V_4 + I_1 R)^2}{(V_2 - I_1 R)^2} = .75 \tag{105}$$

After cross multiplication and simplifying the above equation it becomes

$$(V_2 - I_1 R)^2 (1 - .75) = (V_4 + I_1 R)^2 \tag{106}$$

Solving for V_4 and simplifying then yields

$$V_4 = \frac{1}{2}(V_2 - 3I_1 R) \tag{107}$$

Returning to the above case (where V_2 = 2.25 V, I_1 = 600 A, and R = .0007 Ω) and using the above equation, V_4 would equal .495 V at 600 A. The plot where V_2 = 2.25 V and V_4 = .495 V is shown in Figure 73. The energy utilization at 600 A is 75% and is kept above 75% from 1 to 600 A. The charge efficiency from the previous case was 80%; in this case the charge efficiency drops to 77% (a 3% decrease). Likewise, the minimum time to charge from the previous case was 1.8 seconds; in this case the time to charge increased to 3.96 seconds (a 2.16 second increase). Widening the operating voltage window increases the minimum charge time. In some cases the charge time may be too slow, especially if the system requirement is less than this time. Therefore, 75% energy utilization can be achieved by a proper voltage window but this improved utilization comes at the expense of efficiency and results in a slower time to charge. Tradeoffs need to be made with actual systems to determine the best efficiency, energy utilization, and response time.

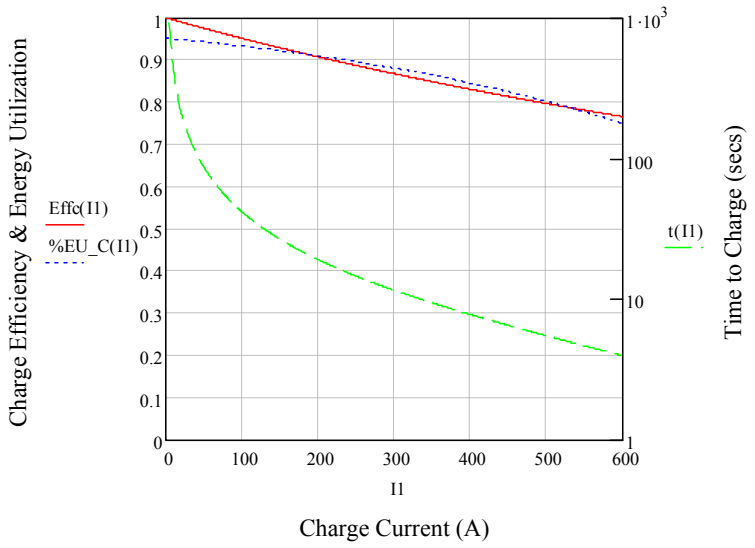


Figure 73. Charge efficiency and energy utilization versus I_1 and time to charge versus I_1 when V_2 = 2.25 V and V_4 = .495 V.

The discharge efficiency was also plotted using the parameters in Table 9. The discharge efficiency plotted versus I_2 and the total energy in the capacitor and the energy loss in the resistor are shown in Figure 74. The discharge efficiency (the solid red line) decreases from 100% at 1 A to 77% at 535 A. Comparing the charge efficiency at 535 A, the charge efficiency decreases to 81%—a 4% difference from the discharge efficiency. The total charge in the capacitor during charge is the same as during discharge. This is expected because V_0 is equal to V_{f2} at every charge and discharge cycle. Likewise, the resistive energy loss is also the same at all I_2 and has the same maximum energy loss.

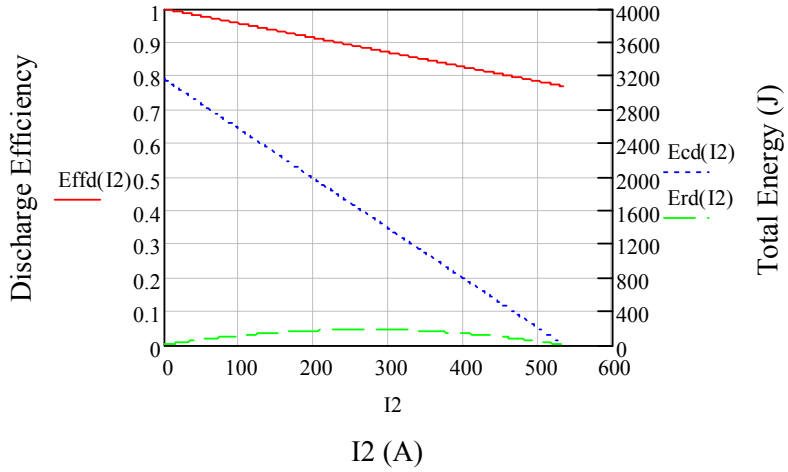


Figure 74. Discharge efficiency, total capacitor energy, and total resistive energy loss versus I_1 when V_2 = 2.0 V and V_4= 1.25 V.

The discharge efficiency, energy utilization, and time to discharge are shown in Figure 75. As with the charge efficiency, energy utilization, and time to charge, as the current increases, the energy utilization and time to discharge decrease. The efficiency also decreases; the charge efficiency at 535 A is 81%, the discharge efficiency is about 77% (a 4% difference). The energy utilization during discharge is the same as during charge for this scenario, which is expected due to symmetry.

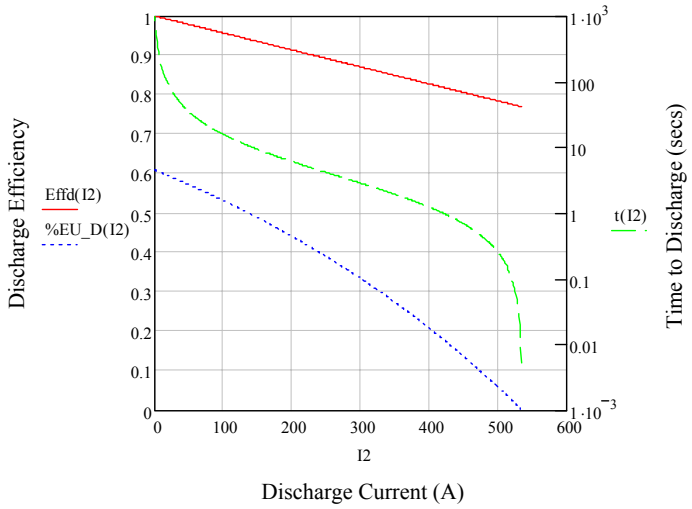


Figure 75. Discharge efficiency and energy utilization versus I_2 and time to discharge versus I_2 when V_2 = 2.0 V and V_4 = 1.25 V.

For a case similar to that shown in Figure 73 where V_2 = 2.25 V and V_4 = .495 V, the discharge results are shown in Figure 76. The energy utilization and time versus I_2 are the same as the energy utilization and time to discharge versus I_1, which is as expected because of symmetry. The discharge efficiency, however, decreases to 69% at 600 A; in contrast the charge efficiency was about 75% (a 6% difference). The energy utilization is above 75% from 1 to 600 A.

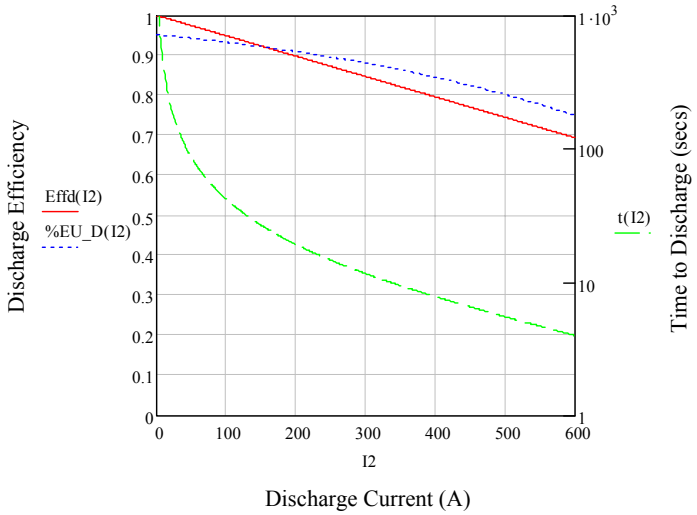


Figure 76. Discharge efficiency and energy utilization versus I_1 and time to charge versus I_1 when V_2 = 2.25 V and V_4 = .495 V.

The round-trip efficiency as a function of current for the case where V_2 = 2.0 V and V_4 = 1.25 V case is plotted in Figure 77. In this case, the round-trip efficiency decreases from 100% to 63% at 535 A. Comparing these results with the round-trip efficiency when V_0 and V_f = 0 V (see Figure 67), the efficiency was 42% (a 21% difference). The round-trip efficiencies are higher because the operating voltages V_2 and V_4 are fixed at 2.0 V and 1.25 V, respectively. The total resistive losses are thus smaller than when the operating voltage window was larger.

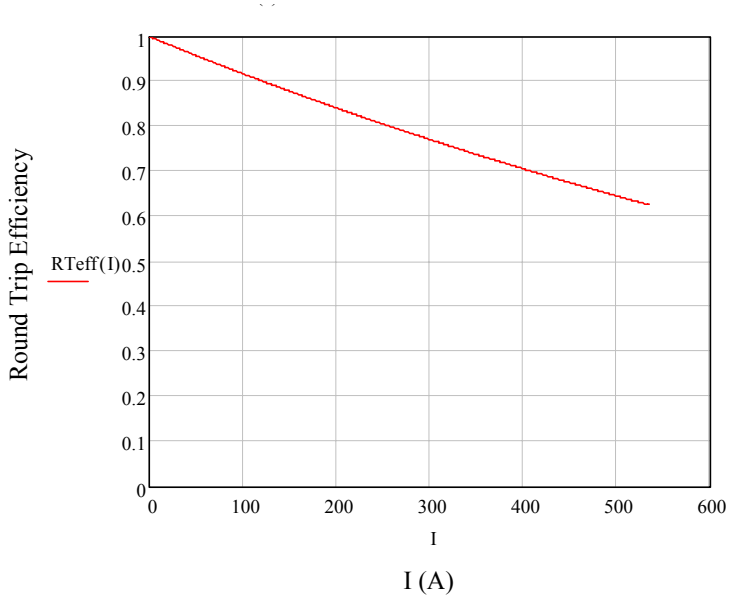


Figure 77. Round-trip efficiency versus *I* when V_2 = 2.0 V and V_4 = 1.25 V.

The simple RC circuit can reveal a lot of baseline information regarding charge and discharge efficiencies, round-trip efficiencies, and energy utilization of the capacitor. This baseline information can assist system designers with integrating and using the SEC in their systems. Early in the design phase such information can provide insight on the performance of various SEC devices from different SEC manufacturers to help designers determine which of the available devices will give them the desired results. Knowing if a particular SEC will work in a given design early in the design process can save a lot of headaches and money. Several conclusions can be drawn from this study.

1. The electrolyte resistance plays a significant role in determining the energy utilization and efficiency in the capacitor. Reducing the electrolyte resistance is a key SEC manufacturing goal.
2. The SEC's maximum voltage rating determines the maximum operating voltage window. From this study it has been shown that widening the operating voltage window can increase the energy utilization. Not only does increasing the

maximum voltage rating decrease the number of SECs it is necessary to connect in series for utility applications, but it also results in increased energy utilization. The maximum operating voltage limit is less than the SEC maximum limit to provide a margin in case the utility requires a recharge.

3. The minimum voltage is determined by the power converter's current limit. Another area not studied in the research that remains a much needed focus area is the optimal power conversion configuration based on the information covered in this report. Future research would focus on this topic.
4. It is known in industry that 75% of energy can be stored in the capacitor during charge when V_0 is equal to half V_f or extracted during discharge when V_{f2} is half V_f. When the operating voltage window is fixed, the energy utilization decreases with increased current either during charge or discharge. 75% energy utilization can be achieved if the voltage window follows the equation $V_4 = \frac{1}{2}(V_2 - 3I_1R)$, but the time to charge or discharge can be increased (*i.e.,* response time is reduced) and the energy efficiency can be decreased.
5. The system's round-trip efficiency must be considered in the overall energy storage system design. The overall system design can reduce the SEC's performance.

14. Conclusion

SECs are attractive in that they have higher energy densities than conventional capacitors and higher power densities than batteries (as well as longer cycle life) which makes them amenable to high-power, pulse-type applications. Within the last few years, interest has

been increasing in using SECs in electric utility applications. SECs, when integrated with a power conversion system, could be used to assist electric utilities by providing voltage support, power factor correction, active filtering, and reactive and active power support. With the advent of sophisticated dynamic simulation software programs such as PSPICE™, MATLAB Simulink™, and PSCAD™, good electrical models become essential to gaining better insights on the electrical performance SECs and are much needed.

Experimental data shows that the ionic resistance and double-layer capacitance are a function of applied voltage. As a result, a better response is obtained from a voltage-dependent RC network model compared to a simple RC network model that uses constant Rs and Cs and a simple RC circuit. From the energy standpoint, simulations show that the voltage-dependent model gives results similar to those from experiments using an actual SEC. It has been shown that the voltage-dependent model fits the constant-current charge and discharge voltage profiles very well at 100 A, 75 A, 50 A, and 25 A. Additionally, when charging the constant RC network and the simple RC circuit, the voltage rises linearly. In contrast, the voltage-dependent model has a charging curve associated with it—just like an actual SEC.

It has been shown that the maximum energy transfer to a resistive load increases, in general, with increasing temperature. This is because the ionic resistance changes with temperature. Simulation results also show that during constant-current discharge, a higher internal voltage drop is experienced when temperature decreases.

Analytical solutions pertaining to round-trip efficiency and energy utilization can be obtained from a simple RC circuit as a function of the SEC's operating voltages, constant

current, and ionic resistance. Using these analytical solutions, the effect of the operating voltage window on efficiency and the effects of current and ionic resistance can be studied. The SEC's operating voltage limits are important because these limits are set by the power conversion system. The round-trip efficiency and energy utilization of a simple RC circuit provide a good baseline for the initial phases of energy storage system design. They can provide a 'go' or 'no go' on a project early on, thus saving time and money for the system integrator. It has been determined from the analytical solutions that the ionic resistance has a significant effect on efficiency and energy utilization. From a system standpoint, overall system efficiency needs to be considered from the electric utility PCC; overall system efficiency includes both the SEC's round-trip efficiency and the power conversion system efficiencies. The 50% voltage window is generally accepted in industry to indicate a 75% energy utilization from an SEC. From the energy utilization study, this 75% rule applies to situations when the current is very low. When the current increases, the energy utilization decreases substantially. A 75% energy utilization can be achieved throughout the operating current by selecting an appropriate operating voltage window.

15. Contributions

This dissertation introduces several new concepts and methods for evaluating ECs for use in electric utility applications. These concepts and methods include:

- Using the energy profile to compare the voltage-dependent model to experimental SEC data and to the constant RC network model and simple RC circuit.

- Developing voltage-dependent equations based on EIS data to be used in a voltage-dependent model. The resulting voltage-dependent model mimics a charging curve similar to the experimental SEC device.
- Developing analytical solutions for SEC efficiency and energy utilization as a function of operating voltages, constant current, and ionic resistance.
- Developing an analytical solution derived from the energy utilization equation that optimizes the SEC's operating voltage limits. The optimal voltage limits allow for a 75% energy utilization throughout the operating current limits.
- Providing a means of expressing the energy stored in the capacitor and the loss in the resistor in terms of the operating voltage limits. The energy loss in the resistor can determine the maximum operating current of the capacitor based on the operating voltage limits. If the operating voltage window is too small, the maximum operating current of the capacitor can be less than the current limit given in the product specification data sheets thus reducing the overall performance of the device.

16. Future Research

Ideas for future research that were discussed in the body of the report are summarized below:

- Preliminary simulation has been done on a StatCom device with and without SECs. The direct control method was used, but may not be the best choice. The direct control method typically minimizes the active power injection into the electric utility and maximizes the reactive power, which does not fully utilize the SEC's potential. Being a DC source, the SEC can provide active power to the

electric utility. A control methodology is needed for SEC-based systems that maximizes both active and reactive power injection into the utility.

- In the StatCom simulation the SEC was tied directly to the DC link of the converter. The SEC can also be tied to a DC-to-DC converter then to a DC-to-AC converter. More research is needed to determine the best possible power conversion system configurations for utility applications. Cost versus performance also needs to be better understood.
- The voltage-dependent model had to be adjusted to better simulate the voltage profile of the experimental SEC. This was because the EIS data collected was based on equilibrated data. The equilibrated data meant that the ions had settled on the active carbon area and thus were not moving. During an actual charge and discharge situation, the ions are in motion. Settled ions (*i.e.,* equilibrated data) give higher values for double-layer capacitance compared to ions in motion. In other words, the active carbon area is used less when the ions are in motion. More research is needed to determine the exact difference between capacitance based on equilibrated data and capacitance in a dynamic voltage situation.
- The efficiency and energy utilization results were based on constant-current charge and discharge. In real systems, the current can be nonlinear between the operating voltage limits. Continued research would focus on other current charge and discharge profiles such as ramp current, exponentially increasing or decreasing current, and sinusoidal current and their effect on the efficiency and energy utilization of the SEC.
- The current ripple caused by the power conversion system was not discussed in this report. More research is needed to determine the effects of current ripple on

the SEC. Single-phase systems inherently can have a 120-Hz ripple, which could cause an increase in the internal temperature of the SEC; under worst-case conditions, such a temperature rise may lead to thermal runaway and ultimately failure of the device.

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Appendix A—EIS Equipment

As mentioned in the body of the report, EIS is very useful for determining the electrolyte resistance, capacitance and inductance of the SEC. The Solartron SI 1287 electrochemical interface and 1255 HF frequency response analyzer were used to make EIS measurements for all SECs in this report. The Solartron 1287 is a wide-bandwidth amplifier used to control the voltage (also known as potentiostat) and current (also known as galvanostat) waveforms to the electrochemical device being tested. The Solartron 1255 analyzes waveforms going into and out of the measured electrochemical device and calculates the impedance and phase angles based on the waveforms. All EIS measurements in this report used a 0.01-Hz to 10-kHz sweep frequency to get EIS measurements. Pictures of the Solartron 1287 and 1255 are shown in Figure A-1 (a and b).

(a) Solartron 1287 Electrochemical Interface

(b) Solartron 1255 Frequency Response Analyzer

Figure A-1. EIS Equipment—Solartron 1287 and 1255.

Large SECs (SECs rated in the thousands of Farads), can have electrolyte resistance on the order of hundreds of μΩ. To see if resistance in the hundreds of μΩ could be measured fairly accurately, a 250-μΩ calibration resistor was used to make the

measurement. The resistor was obtained from the calibration center at SNL. The resistor is rated at 250 μΩ with ±1% accuracy. The resistor is shown is in Figure A-2.

Figure A-2. SNL calibration resistor.

The typical setting for Solartron testing is a 5-mV excitation voltage, but for measurements in the hundreds of μΩ this voltage was adjusted to .3 mV to make the low impedance measurement. Once the adjustments were made, the EIS measurement was made on the resistor. The EIS results are shown in Figure A-3.

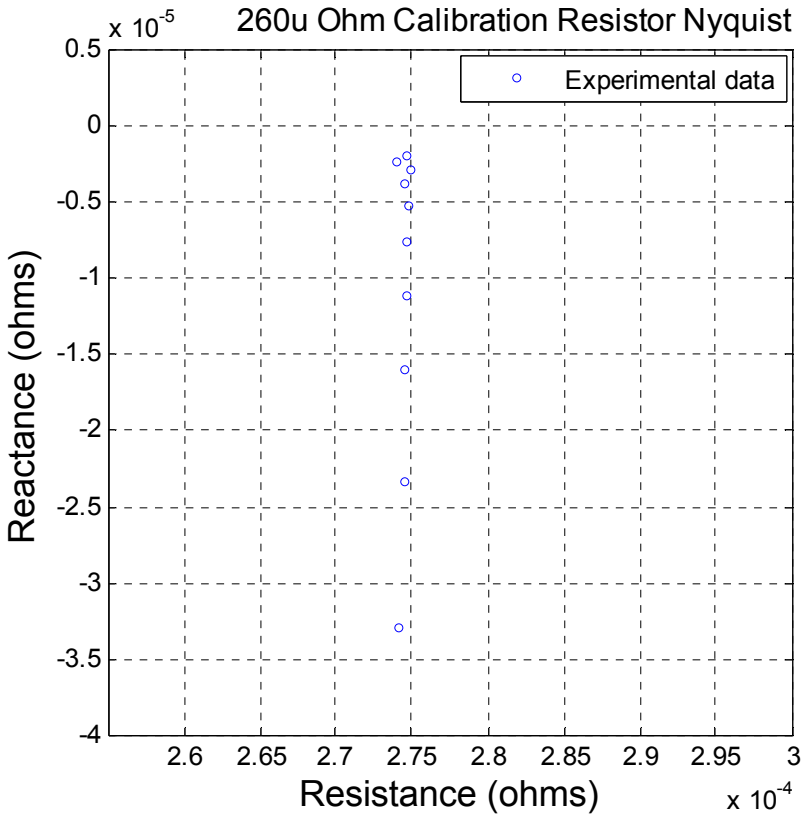

Figure A-3. EIS for 250-μΩ calibration resistor.

As can be seen from the above results, the tester measured the resistor at 275-μΩ and has a 10% margin of error. This amount of error is reasonable and comparable to manufacturer error calculations. Solartron develops a Model 1290 power booster that mates with the Solartron 1287 to measure low impedance by increasing the output current to the electrochemical device being tested. The impedance measurement error chart for the Solartron 1290 power booster is shown in Figure A-4.

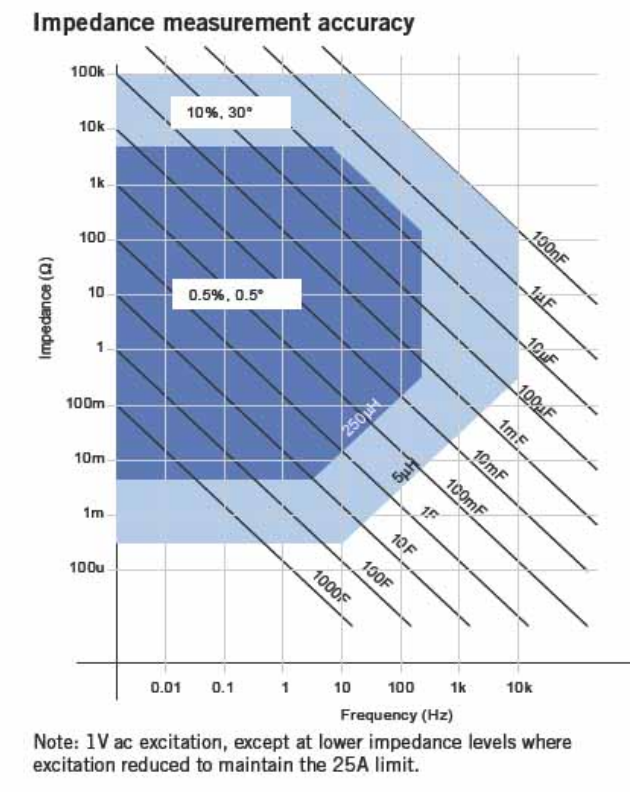

Figure A-4. Solartron SI 1290 power booster impedance measurement error.*

The impedance measurement error chart from Solartron was made with a 1.0-V excitation voltage. As can be seen from the measurement error chart, the lowest impedance measurement error calculation is between 100 micro and 1 mili-Ω and the margin of error is about 10%. In conclusion, the measurement method used in this study accomplishes a 10% margin of error without an external power booster. This is significant because the additional equipment space and cost for the power booster are avoided, which saves companies money and resources while obtaining measurements at reasonable accuracy. Because EIS is used in developing the RC networks, it is important to get measurements that are as accurate as possible.

* http://www.solartronanalytical.com/downloads/datasheets/1290.pdf

Appendix B—Acronyms and Abbreviations

AEC	asymmetric electrochemical capacitor
DOE	Department of Energy
EC	electrochemical capacitor
EIS	electrochemical impedance spectroscopy
EPRI	Electric Power Research Institute
ESS	energy storage system(s)
ESR	equivalent series resistance
ETO	emitter turn-off thyristor
FACTS	flexible AC transmission system(s)
HELCO	Hawaiian Electric Light Company
IR	current times resistance
NCSU	North Carolina State University
NEC	Nippon Electric Company
PCC	point of common coupling
PVDF	polivinylidene difluoride
PWM	pulse width modulation
RC	resistor-capacitor
redox	reduction oxidation
RMSE	root-mean-square error
RRMSE	relative root-mean-square error
SEC	symmetric electrochemical capacitor
SEM	scanning electron micrograph(y)
SMES	superconducting magnetic energy storage

SNL	Sandia National Laboratories
SOC	state of charge
Sohio	Standard Oil Company of Ohio
SSSC	series static synchronous compensator
StatCom	static synchronous compensator
TEATFB	tetraethylammonium tetrafluoroborate
TUCAP	Transmission UltraCAPactior
TVA	Tennessee Valley Authority
UPFC	unified power flow controller
U.S.	United States