High-κ Gate Dielectric on Tunable Tensile Strained Germanium Heterogeneously Integrated on Silicon: Role of Strain, Process, and Interface States

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ABSTRACT: Tensile strained germanium (ε-Ge) layers heterogeneously integrated on Si substrates have technological importance for nanoscale transistors and photonics. In this work, the tunable tensile strained (0% to 1.2%) ε-Ge layers were grown by solid source molecular beam epitaxy using GaAs and linearly graded $In_xGa_{1-x}As$ as intermediate buffers, and their structural and metal-oxide semiconductor capacitors (MOS-Cs) properties were analyzed as a function of strain and process conditions. X-ray topography measurements displayed no visible thermal crack and low thermal stress of ~50 MPa. Temperature dependent strain relaxation properties, studied by x-ray and Raman analyses confirmed that the tensile strain amount of 1.2% was well preserved within the ε-Ge layer when annealed up to 550ºC. Further, transmission electron microscopic study revealed good quality of 1.2% strained ε-Ge/$In_{0.17}Ga_{0.83}As$ heterointerface. In addition, unstrained Ge (0% ε-Ge) MOS-Cs with atomic layer deposited Al_2O_3 and thermally grown GeO_2 composite gate dielectrics of varying oxidation times (0.25 min to 7.5 min) at 550ºC exhibited low interface state density (D_{it}) of ~2.5×10^{11} $eV^{-1}cm^{-2}$ at 5 min oxidation duration. The minimum oxidation time needed for good capacitance-voltage (C-V) characteristics on 0.2% ε-Ge is inadequate to accomplish similar C-V characteristics on 1.2% ε-Ge MOS-C, due to the higher strain field impeding the formation of GeO_2 interface passivation layer at lower oxidation duration. In addition, with trade-off between the minimum D_{it} and minimum equivalent oxide thickness values, ~1.5 min is found to be an optimum oxidation time for a good quality 1.2% ε-Ge MOS-C. The minimum D_{it} values of 1.36×10^{11} $eV^{-1}cm^{-2}$ and 2.06×10^{11} $eV^{-1}cm^{-2}$ for 0.2% and 1.2% ε-Ge, respectively, were determined for 4 nm Al_2O_3 with 5 min thermal oxidation at 550ºC. Therefore, the successful monolithic integration of tunable tensile strain Ge on Si with the structural, defects, and MOS-Cs analyses, would offer a path for the development of tensile strained Ge-based nanoscale transistors.

KEYWORDS: *Germanium, Al_2O_3, Molecular Beam Epitaxy, X-ray Photoelectron Spectroscopy, Lifetime, atomic layer deposition*

1. INTRODUCTION

Group IV based materials - germanium (Ge), silicon-germanium (SiGe) and germanium-tin (GeSn) are under consideration for nanoelectronics and photonics.[1-21] Due to their high carrier mobilities, supplementing these materials along with tunable compositional $In_xGa_{1-x}As$ ($0.1 \leq x \leq 0.4$) as channel materials will boost the on-current and ultimately device/circuit performances in an alternate channel CMOS,[6, 19] tensile-strained Ge/$In_xGa_{1-x}As$ based tunnel transistors[4, 22], energy-efficient SRAM cell architecture for ultra-low voltage applications [23], and photonic devices. [2, 5, 24, 25] For high-performance ultra-low voltage CMOS logic, RF circuits, and mixed signal low-noise amplifier circuits, it is widely accepted that InGaAs and Ge will serve as *n*-channel and *p*-channel transistor materials, respectively.[19, 26-28] However, implementing these two different materials (*i.e.*, Ge and InGaAs) on a Si wafer requires defect-controlled buffer engineering for the monolithic heterogeneous integration process rather than direct growth of Ge or SiGe on Si. Furthermore, Ge is an excellent choice for CMOS logic due to its 2.8 × and 4.2 × higher electron and hole mobilities, respectively, compared to Si. In addition, Ge offers the highest hole mobility in comparison with any semiconductor material.[29] Recently, we have experimentally demonstrated the 2 × increase in electron mobility of the biaxially tensile strained (1.6 %) epitaxial Ge (ε-Ge) layer through $In_{0.24}Ga_{0.76}As/In_xGa_{1-x}As$ strain template.[30] Although, potential success of this material and its related compounds (*i.e.*, GeSn, SiGeSn) is achievable in photonics,[1, 2, 5, 8, 9] there are many challenges that need to be dealt by the microelectronic industries before Ge or SiGe can be considered as viable candidates for a transistor channel material, listing two of them- (i) monolithic heterogeneous integration of Ge or ε-Ge on Si, and (ii) high-κ/ε-Ge heterointerface. The potential solution in the former is to bridge the lattice constant between the upper layer of interest (*i.e.*, Ge, SiGe, or ε-Ge) and the Si substrate, and the latter is to insert an interface passivation layer (IPL) between high-κ/Ge or ε-Ge interface to reduce interface defects. In addition, one needs to control the thickness of the IPL layer on the unstrained Ge or ε-Ge layer prior to high-κ dielectric deposition. Note that the thermal oxidation has been relatively a popular method for the formation of high-quality GeO_x/Ge interface in addition to the Si capping on Ge or SiGe layer.[31-37]

The 4% (or higher) lattice mismatch between the unstrained Ge (or ε-Ge) layer and the Si substrate results in the formation of defects and dislocations within the Ge (ε-Ge) layer. These dislocations have a deleterious impact

on device performances by reducing both carrier mobility and carrier lifetime while increasing junction leakage. Recent studies demonstrated the high carrier lifetime[38] of Ge on GaAs and high carrier mobility of 0.2% ε-Ge on Si[39] and 1.6% ε-Ge on GaAs[30]. In addition to the 4% lattice mismatch between Ge epilayer and the Si substrate, there is also a thermal mismatch between them due to the large differences in the thermal expansion coefficients of Ge ($\alpha_{Ge} = 5.9\times10^{-6}$ K^{-1}) and Si ($\alpha_{Si} = 2.6\times10^{-6}$ K^{-1}),[29] resulting in 0.2% tensile ε-Ge. The thermal mismatch will introduce (i) radius of curvature (*i.e.*, wafer bow), (ii) thermal stress to film/substrate and resulting thermal crack,[40] and (iii) thermal mismatch induced defects. Therefore, design of a buffer architecture (*i.e.,* graded $Si_{1-x}Ge_x$, III-V materials) to bridge the lattice constant of epitaxial Ge with the Si substrate is imperative for monolithic heterogeneous integration of device-quality Ge on Si rather than direct growth of Ge on Si.[21] Direct growth of Ge on Si exhibited poor carrier lifetime.[41] Whereas, Ge grown on Si using 10 µm thick graded $Si_{1-x}Ge_x$ buffer minimizes defects and dislocations however it creates thermal cracks,[40] and induces parallel conduction to the active Ge channel from SiGe buffer.[42, 43] Hence, this warrants an alternate III-V compound semiconductor buffer architecture design between the Ge and the Si substrate. Such a buffer architecture prevents generation of thermal crack, provides minimal thermal stress and confines the defects and dislocations within the buffer layer,[44] and reduces parallel conduction to the Ge layer due to large bandgap buffer. In addition, the buffer architecture imparts tensile strain to the Ge layer, thereby improving the carrier mobility.[30] While high-*κ* dielectrics have successfully been demonstrated on Si-based CMOS down to 3 nm node,[10-12, 45-49] finding a suitable high-*κ* gate-dielectric for Ge (ε-Ge) that is comparable in quality remains a challenge, and extensive research efforts are currently been devoted.[20, 21, 31-37, 50-52] The primary requirement for a good quality high-κ/Ge interface is to have an atomically smooth interface with minimal defects. An IPL, which is purposefully inserted between the high-κ dielectric and Ge, is a solution to improve the quality of a high-κ/Ge interface and reduce the interface state density (D_{it}). The IPL helps to passivate the surface by reducing defect concentration, thereby forming a higher quality interface with Ge. By careful selection and control of the oxidation temperature and oxidation time, Nakakita *et al.*[53] were able to demonstrate metal-oxide-semiconductor capacitors (MOS-Cs) and MOSFET gate stacks consisting of $Al_2O_3/GeO_x/Ge$ with low D_{it} of ~2×10^{11} - 4×10^{11} $eV^{-1}cm^{-2}$, where the GeO_x was thermally formed at 450-550°C oxidation temperature for

different thickness. This lower D_{it} value is correlated with higher peak hole mobility of 575 $cm^2V^{-1}s^{-1}$ and I_{ON}/I_{OFF} of ~ 10^5 of a Ge MOSFET.

In this work, we present the epitaxial growth of unstrained and tunable tensile ε-Ge (0% to 1.2%) on GaAs and on Si substrates with appropriate buffer architectures, grown by solid-source molecular beam epitaxy (MBE) growth system. These layer structures were systematically investigated to study: (i) the thermal mismatch induced thermal stress and thermal crack *via* x-ray topography, (ii) temperature dependent strain relaxation properties *via* high-resolution x-ray diffraction and Raman spectroscopy, and (iii) interface and defect properties *via* cross-sectional transmission electron microscopy (TEM) to qualify the epitaxial Ge films. The different oxidation times (0.25 min to 7.5 min) at 550°C for the formation of GeO_2 IPL layer on Ge prior to the atomic layer deposited (ALD) 4-5 nm thick Al_2O_3 high-κ dielectric, were carried out to study the interface passivation by investigating the value of minimum D_{it}. We correlate the D_{it} at the interface of Al_2O_3 high-κ dielectric on tunable tensile ε-Ge as well as annealing temperature extents to preserve the strain within the ε-Ge by studying the electrical measurements of fabricated Ge MOS-Cs at temperature ranging from 80 K to 290 K. A trade-off between the lowest D_{it} and the lowest equivalent oxide thickness (EOT) for ε-Ge MOS-Cs is observed. In addition, the minimum oxidation time of 0.5 min on 0.2% ε-Ge is inadequate to realize good capacitance-voltage (C-V) characteristics on 1.2 % ε-Ge. This implies that the strain field prevents the formation of thicker GeO_2 layer on the 1.2% ε-Ge sample at 0.5 min of oxidation, where the minimum IPL thickness needed for an unstrained Ge is inadequate for good quality ε-Ge MOS-C properties and requires higher oxidation time to devise good C-V characteristics. Thus, this work will open up further study of the ε-Ge MOS-C with GeO_2 or SiO_2 IPL layer for the development of high-κ gate stack for future ε-Ge transistor implementation.

2. EXPERIMENTAL SECTION

2.1 Materials synthesis. Heterostructures consisting of (a) 280 nm thick epitaxial Ge layer on (100)/2° GaAs substrate with an intermediate 170 nm AlAs buffer (0% ε-Ge, *Sample A*), (b) 240 nm thick epitaxial Ge layer on (100)/6° off-cut Si with intermediate 170 nm AlAs/2.2 µm GaAs metamorphic buffer to accommodate the lattice mismatch strain between the Ge and the Si substrate (0.2% ε-Ge, *Sample B*), and (c) 30 nm thick 1.2% tensile

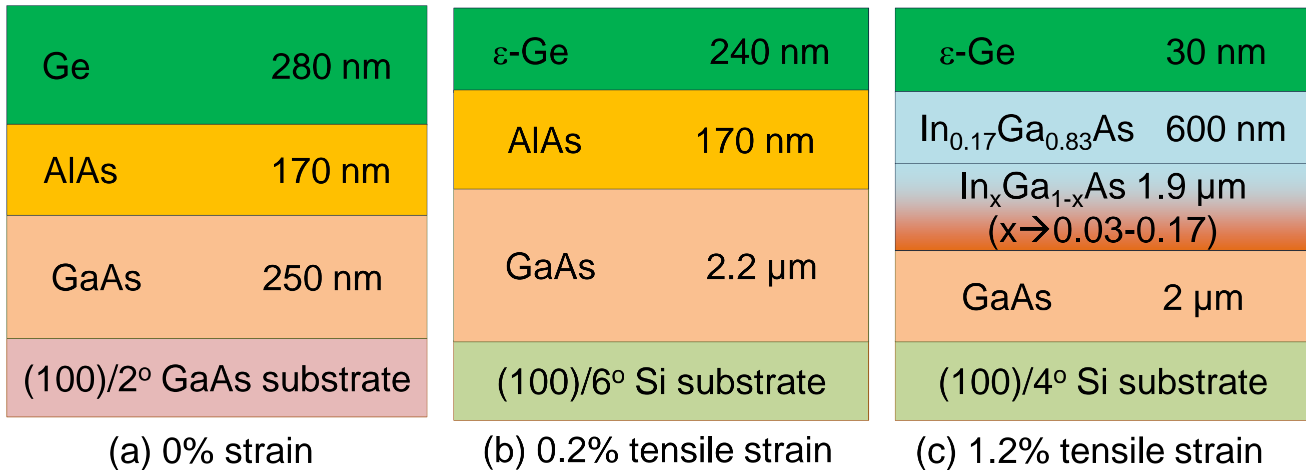

Fig. 1: Schematic representation of layer structure used in this work: (a) 280 nm Ge on semi-insulating (100)/2° GaAs substrate (0% ε-Ge) (*Sample A*), (b) 240 nm Ge on (100)/6° Si substrate with AlAs/GaAs composite buffer layer (0.2% ε-Ge) (*Sample B*), and (c) 30 nm Ge on (100)/4° Si substrate with composite graded $In_xGa_{1-x}As$/GaAs buffer (1.2% ε-Ge) (*Sample C*).

strained Ge (ε-Ge) on (100)/4° off-cut Si substrate with linearly graded $In_xGa_{1-x}As$ metamorphic buffer starting from GaAs buffer to the ε-Ge (*Sample C*), were synthesized by solid-source MBE, as shown in **Fig. 1**. For the unstrained Ge layer, an intermediate AlAs buffer layer was used to suppress or block interdiffusion of As, Ge and Ga atomic species. SUMO® effusion cells for gallium (Ga) and germanium (Ge), 60 cc capacity of aluminum (Al), and 125 cc capacity of indium (In) effusion cells as well as arsenic valved cracker source, were used for this work. The bulk and cracker temperatures of arsenic source were set at 340°C and 900°C, respectively, for required As_2 flux during growth and oxide desorption. The flux ratio of >22 (the ratio between the beam equivalent pressure of As_2 and Ga (Al) constituents) was used during growth. For the strained Ge layer growth on (100) Si substrates that are off-cut in the 4°-6° range towards <110> direction on the elimination/suppression of anti-phase domain boundary and stacking faults due to the polar (GaAs)-on-nonpolar (Si) growth formation is well-supported in the literatures[5, 40, 44, 54, 55] and was applied in this work to realize GaAs on Si epitaxy. Each Si substrate oxide desorption was carried out in the temperature range of 900°C to 950°C without As_2 over pressure, and similarly for GaAs substrates at 750°C under As_2 flux of ~10^{-5} torr. During the GaAs or Si substrate oxide desorption and periodically throughout each layer growth, *in-situ* reflection high energy electron diffraction (RHEED) system attached to the group III-V growth system was used to monitor the surface reconstruction of GaAs, AlAs and graded $In_xGa_{1-x}As$ buffers. After the

oxide desorption of GaAs substrate at 750°C, the substrate temperature was reduced to 650°C growth temperature for 250 nm GaAs growth and 170 nm AlAs layer growth at 670°C. Growth temperature referred here is the thermocouple temperature. Growth rate of GaAs and AlAs is ~ 0.4 µm/hr and ~ 0.25 µm/hr, respectively. After completion of the AlAs/GaAs layer growth within the group III-V chamber, *Sample A* was cooled down < 200°C under As_2 flux and then transferred to the group IV chamber for unstrained Ge layer growth. The growth temperature and growth rate of Ge layer were 400°C and ~ 25 nm/hr, respectively. The 400°C growth temperature was selected to prevent the interdiffusion of atomic species and abrupt heterointerface of Ge/AlAs.[56] After the Ge layer growth, *Sample A* was slowly cooled down to < 100°C to avoid thermal cracking and unloaded from the chamber for material analysis.

In the case of strained Ge layers (*Samples B* and *C*) on off-cut Si substrates, the 5 thermal cycle annealing steps (1-step: 400°C→650°C→400°C) were incorporated into the GaAs buffer layer to mitigate the lattice mismatch induced defects and dislocations prior to the growth of AlAs or linearly graded metamorphic $In_xGa_{1-x}As$ buffer, that bridges the lattice mismatch between the ε-Ge and the Si substrate. The linearly graded $In_xGa_{1-x}As$ metamorphic buffer was grown at 525°C growth temperature on GaAs/Si. After the growth of graded $In_xGa_{1-x}As$ buffer on GaAs/Si substrates (*Samples B* and *C*) in group III-V chamber, they were transferred to group IV chamber for strained Ge epitaxy. The Ge layer was grown at 400°C growth temperature with ~ 25 nm/hr growth rate. Both the MBE growth chambers are vacuum interconnected to minimize cross contamination of atomic species. The resulting structures were characterized using high-resolution x-ray diffraction for structural and strain analysis, cross-sectional transmission electron microscopy (TEM) for defect microstructure, Raman analysis for strain in Ge, capacitance-voltage (C-V) and conductance-voltage (G-V) transport properties of fabricated Ge MOS capacitors.

2.2 Materials analysis. After each heterostructure growth, the structural properties were evaluated *via* high-resolution x-ray analysis by PANalytical X'pert Pro x-ray diffraction system. Symmetric (004) x-ray rocking curves from each layer structure were recorded to observe the crystallinity, composition, and relaxation state. Reciprocal space maps of both symmetric (004) and asymmetric (115) reflection planes were recorded from the 1.2 % ε-Ge layer stack (*Sample C*) as a function of annealing temperature (till 550°C) to determine the strain relaxation as a

function of temperature. In addition, the radius of curvature and thermal stress from the 0.2 % ε-Ge layer stack (*Sample B*) were determined by collecting several x-ray rocking curves as a function of the length traversed. Furthermore, x-ray topography measurement was performed on *Sample B* at Arizona State University's materials analysis laboratory to evaluate the thermal induced crack of the layer structure grown on Si. Raman spectra were collected in the (001) backscattering geometry using a JY Horiba LabRam HR800 system, and were used to identify the vibrational properties of the 1.2 % ε-Ge epitaxial layer as a function of annealing temperature, in addition to the layer structures (*Samples A-C* and bulk Ge) studied here. Excitation wavelength of 514.53 nm (green) by Laser Physics Ar^+ laser and the gratings of 1800 lines/mm were used during measurement. Laser power at the sample was ~10 mW. The structural integrity of the 1.2 % ε-Ge layer stack (*Sample C*) was evaluated by cross-sectional TEM using a JEOL 2100 transmission electron microscope. TEM specimen was prepared using mechanical polishing and low energy Ar^+ ion milling, where the sample stage was cooled by liquid nitrogen to avoid depositing materials during milling process. The carrier density of the unintentionally doped Ge layer (*n*-type) is in the range of 2-4×10^{18} cm^{-3} and it was determined using Hall effect *via* van der Pauw method.

Prior to oxidation, the surface of each heterostructure (*Samples A, B,* and *C*) was degreased using acetone, isopropanol, and deionized water for about 60 s each. After degreasing, each sample was loaded into thermal oxidation furnace for the formation of GeO_2, where ultra-high purity oxygen gas was used for oxidation. Different oxidation durations were selected, as discussed below, for the formation of GeO_2 interface passivation layer. We have reported that the Ge^{4+} peak was predominant on a thermally grown GeO_x on (100)Ge surface, resulting in the formation of stoichiometric GeO_2.[33] After the GeO_2 formation at different oxidation duration (t_{GeO2}), samples were immediately loaded into the Cambridge NanoTech atomic layer deposition (ALD) system for high-κ dielectric (*i.e.*, Al_2O_3) deposition at 250ºC using trimethyl aluminum (TMA) and deionized water for Al and oxygen source, respectively, where TMA precursor was kept at room temperature. Approximately, 4 nm to 5 nm thick Al_2O_3 high-κ gate dielectric was deposited on each sample surface. Each sample was removed from the ALD reactor and MOS capacitors were fabricated using 0.8 nm TiN/100 nm Al as gate metal and 0.8 nm TiN/100 nm Al/10 nm Ti/30 nm Ni as back contact. Ultra-thin layer of TiN layer was used as an adhesion layer prior to the deposition of Al metals.

Metal depositions were performed using a Kurt J. Leskar PVD 250 deposition system. The post deposition metal annealing was performed at 250ºC for 2 min under forming gas (mixture of 5 % H_2: 95 % N_2). Multi-frequency C-V and G-V measurements of the fabricated Ge MOS capacitors were performed as a function of measurement temperatures. HP4284A precision LCR meter with frequencies ranging from 100 Hz to 1 MHz and Keithley SCS4200 semiconductor parameter analyzer along with ARS Cryo probe station capable of C-V/I-V measurements from 4.2 K to 500 K under ultra-high vacuum, were used for MOS capacitor measurements. The series resistance removal step as discussed in Ref. [57, 58] was used for C-V analysis. Several important MOS-Cs parameters namely, EOT, frequency dispersion (Δf), and D_{it} were evaluated as a function of tunable tensile strain in Ge.

3. RESULTS AND DISCUSSION

3.1 Strain analysis via x-ray measurement of ε-Ge (0 %, 0.2 %, 1.2 %). The structural quality, relaxation state of the linearly graded $In_xGa_{1-x}As$ metamorphic buffer, and amount of strain present within each Ge layer, were evaluated using high-resolution x-ray diffraction measurements. **Fig. 2** shows the x-ray rocking curves (RCs) from the (004) Bragg lines of epitaxial Ge thin films grown on GaAs and Si substrates (structures shown in **Fig. 1**). The angular separation between the (004) diffraction peaks of GaAs and Si resulting from the difference in lattice plane spacing, along with their diffraction line profiles, provided information about the microstructural quality of the GaAs films, which in turn affect the quality of Ge film in *Sample B* and *Sample C*. For the graded $In_xGa_{1-x}As$ metamorphic buffer, the x-ray RC confirms the gradual change in lattice constant from the GaAs buffer (*Sample C*) to the uppermost composition of $In_{0.17}Ga_{0.83}As$ for 1.2 % tensile strain in Ge. The ε-Ge layer thickness was

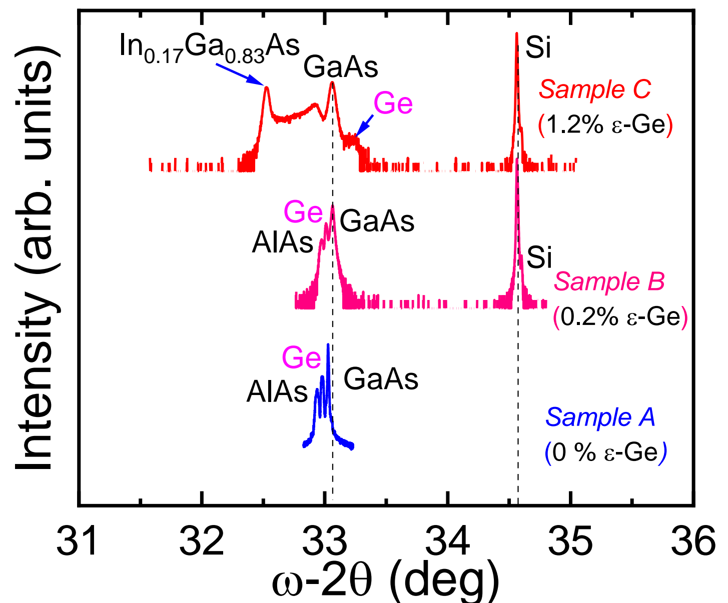

Fig. 2: Symmetric (004) x-ray rocking curves obtained from the layer structure studied in this work. Each layer peak position is identified and listed on this figure.

limited to 30 nm to prevent the strain relaxation due to lattice mismatch between the constant composition $In_{0.17}Ga_{0.83}As$ and the epitaxial ε-Ge layer. As observed in **Fig.2**, the location of the epitaxial GaAs peak position on Si (*Samples B* and *C*) is slightly different than GaAs substrate (*see Sample A*) and it was due to the thermally induced tensile strain, although minimal, in GaAs when grown on Si. The 0.2% strain in Ge is due to the thermal mismatch between the GaAs and the Si substrate. The similar strain amount inside the Ge layer grown on Si substrate was reported in Ref. [59]. Based on the peak separation of the GaAs buffer layer with respect to the Si substrate, the GaAs buffer layer is almost fully relaxed. **Fig. 2** also shows the peak position of the Ge layer as lying between the AlAs and GaAs layer peaks, which is expected due to the lower lattice constant of Ge than AlAs. The peak separation between the AlAs and Ge is narrower for *Sample A* than *Sample B*, which is expected since the latter was grown on Si substrate. The tensile strain between the Ge and the GaAs substrate or buffer is limited to ~ 0 % (*Sample A*) and ~ 0.2 % (*Sample B*). The peak position of 30 nm thick Ge layer is clearly evident and it is located between the GaAs and Si peak positions in *Sample C* and the tensile strain within the Ge layer is ~1.2 %. If there is no tensile strain present within the Ge layer, then the peak position of the Ge layer with respect to the GaAs buffer peak position should be similar to *Sample A*.

3.2 Thermal mismatch, radius of curvature and film stress (0.2% ε-Ge). In addition to the lattice mismatch between the GaAs buffer layer and Si substrate, thermal mismatch due to the differences in thermal expansion coefficients between them is also challenging in monolithic integration of compound semiconductors on Si. Here, the thermal expansion coefficient of Si ($\alpha_{Si} = 2.6\times10^{-6}$ K^{-1}) compared to GaAs ($\alpha_{GaAs} = 5.7\times10^{-6}$ K^{-1}) implies that the Si substrate will expand less when heated and contract less when cooled down during the growth process of GaAs on Si. This leads to the larger contraction of the GaAs lattice with respect to the Si substrate when cooling down from the growth temperature, results in the incorporation of small amount of tensile strain in the GaAs layer, supported in Fig. 2 (*Sample B*). The simplified form of the thermal strain (assuming a constant thermal expansion coefficient) is $\varepsilon_{\alpha} = \Delta\alpha \times \Delta T$ and at 300 K, the thermal strain to be ~2×10^{-3}, less than 10% of the lattice mismatch strain (~ 4%) of GaAs and Si. However, the thermal strain can become significant at large epitaxial layer thicknesses,[40] and thinner buffer layer is often considered in order to reduce the thermal mismatch induced strain.

It has been reported that if the lattice mismatch strain is compressive (*i.e.,* GaAs or Ge on Si) but the thermal strain is tensile (*i.e.*, Ge or GaAs on Si), it is possible to have some strain compensation at 300 K and the resulting film is ~ 0.2% tensile strain.[59] Although, some thermal strain can be relaxed by dislocation glide at growth temperature, however, as the temperature decreases, the wafer will experience a thermal stress resulting in a wafer curvature. Various techniques such as, selective area epitaxy, growth on patterned/mesa substrates,[60-62] have been attempted to minimize the effect of epilayer cracking and wafer bowing. In order to address this, we have performed x-ray topography measurement on 240 nm Ge/170 nm AlAs/2.2 μm GaAs layer stack on Si substrate (*Sample B*) at the Goldwater Materials Science Facility, Arizona State University, as shown in **Fig. 3a**. This layer stack consisting of the different thermal expansion coefficient materials (*i.e.*, Ge, AlAs, GaAs, and Si) and exhibited no visible thermal mismatch induced cracks. This process allows us to synthesize a 1.2% ε-Ge on Si using GaAs and linearly graded $In_xGa_{1-x}As$ buffer architecture (*Sample C*).

As the different thermal expansion coefficient materials can produce wafer deformation, we have analyzed the x-ray measurements of *Sample B*. **Fig. 3b** shows the x-ray RCs of the layer stack as a function of length traverse. One can find from this rocking curve that the Ge, AlAs, and GaAs layers peak were clearly visible along with Si substrate peak. From this RC, the lattice curvature was measured from the peak shift during x-ray measurement as a function of distance and the radius of curvature, R and film stress, σ_f for *Sample B*, is given by;[63-65]

$$R = 57.295\frac{\Delta x}{\Delta \omega} \text{ (m)}, \quad (1)$$

$$\sigma_f = \frac{E}{6(1-\nu)}\frac{t_s^2}{t_f}\frac{1}{R} \text{ dyn/cm}^2, \quad (2)$$

where, Δx is the length of the traverse, $\Delta\omega$ is the total deflection in degrees observed over this length, E is the Young's modulus, υ is the Poisson's ratio, t_s and t_f are the thickness of the substrate and film, respectively. Using the value of R of the uncoated Si substrate and epilayer-grown Si substrate (**Fig. 3b**), a mean radius of curvature, R_{mean} of -60.20 m (tensile) and the resulting estimated film stress σ_f of ~50 MPa were determined on 3" (100)Si substrate using the E and υ values reported in Refs. [63-65] for (100)Si. The resulting film stress is quite low (*e.g.*, 0.28 GPa corresponds to 0.2% in-plane strain in Ge[59]) and this was possible by selecting growth and annealing

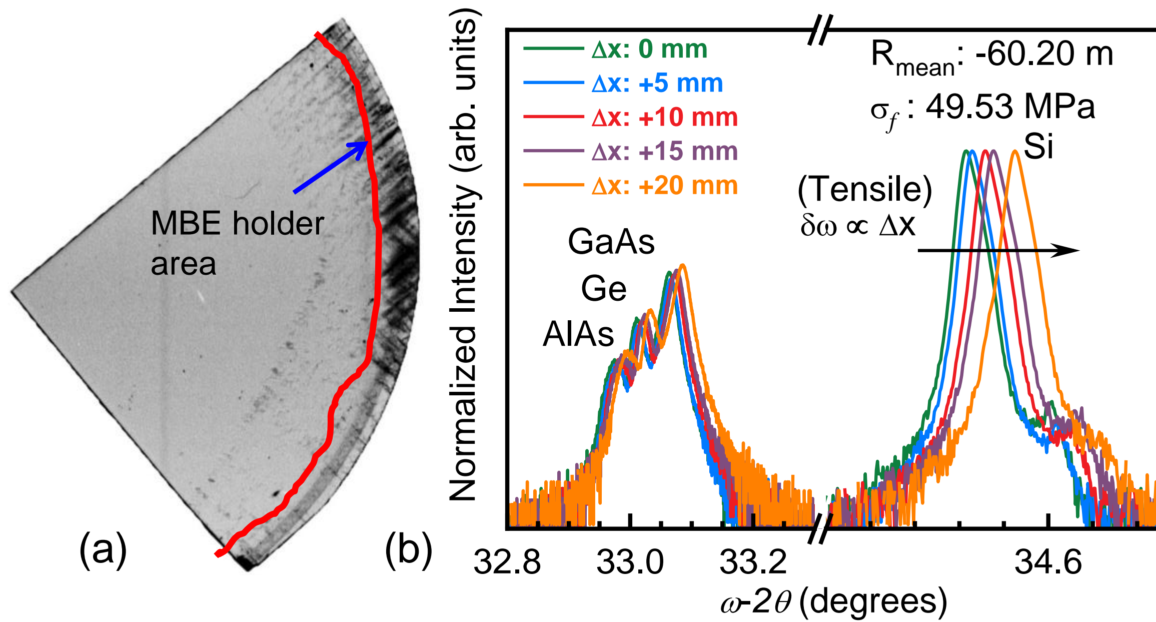

Fig. 3: X-ray topography of (a) 240 nm Ge/170 nm AlAs layer grown on 3-inch (100)/6° off-cut *n*-Si substrate with 2.2 µm thick GaAs buffer (*Sample B*), with 5 TCA steps (1-step: 400°C→650°C→400°C) incorporated into the GaAs layer, exhibiting no visible thermal mismatch induced cracks. (b) X-ray rocking curves of Ge/AlAs/GaAs/Si (*Sample B* or 0.2% ε-Ge) as a function of length traverse during measurement. The R_{mean} of -60.20 m and film stress of ~50 MPa were estimated.

temperatures during growth, as described above. Hence, the process conditions used in this work enables one to achieve the crack-free layer structure for the integration of multilayer materials stack on 6° off-cut (100)Si substrate.

3.3 Temperature dependent strain relaxation properties of 1.2% ε-Ge via X-ray and Raman analyses.

Strain relaxation properties of the 1.2 % ε-Ge on Si (*Sample C*) at each annealing temperature were measured by collecting the symmetric (004) and asymmetric (115) reciprocal space maps (RSMs) using high-resolution PANalytical X'pert Pro x-ray diffraction with pixel detector. The 4 pieces of 1.2 % ε-Ge sample were *ex-situ* annealed under forming gas (5% H_2:95% N_2) at different temperatures inside a tube furnace starting from 400°C to 550°C for 10 min in 50°C each step since the growth temperature of the ε-Ge was at 400°C. The duration of this annealing was selected based on the combined duration of GeO_2 formation and contact annealing of fabricated MOS-C. Each piece of 1.2 % ε-Ge sample was cooled down to a room temperature after *ex-situ* annealing, and the (004) and (115) RSMs data were recorded by x-ray analysis. **Figs. 4** and **5** show symmetric (004) and asymmetric (115) RSMs for the structure at 25°C and 550°C annealing temperature, respectively. The (004) and

(115) RSMs at 400°C, 450°C and 500°C are shown in Supporting Information S1. Each layer's reciprocal lattice point (RLP) was assigned in **Figs. 4** and **5**. Here, epilayers with different materials involved during epitaxy exhibited separate RLPs. One can find that there are four distinct RLP maxima corresponding to Si substrate, GaAs buffer, constant composition $In_{0.17}Ga_{0.83}As$, ε-Ge and the linearly graded $In_xGa_{1-x}As$ metamorphic buffer at each temperature. The relaxation of the constant composition $In_{0.17}Ga_{0.83}As$ layer was determined to be > 85% with temperature with respect to GaAs buffer since it is fully relaxed with respect to Si substrate, and higher relaxation number was obtained at 550°C. Tensile strain amount within the Ge layer is ~1.2 ± 0.014 %, and this tensile strain amount starts decreasing above 550°C annealing temperature, where the RLPs separation between the ε-Ge and the GaAs buffer decreases. Calculated strain relaxation values of $In_{0.17}Ga_{0.83}As$ layer and amount of tensile strain in Ge at each temperature were summarized in **Table I**. The nearly identical strain relaxation values of $In_{0.17}Ga_{0.83}As$ layer at different annealing temperature steps indicate that the pseudomorphic nature of 1.2% ε-Ge layer was well maintained until 550°C and starts to decrease above 550°C.

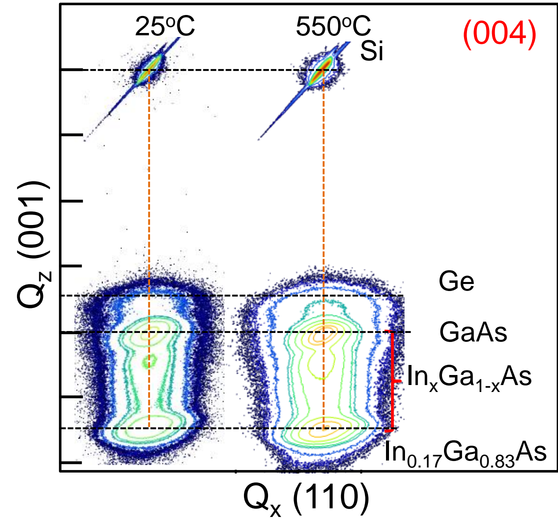

Fig. 4: Symmetric (004) RSMs of the 1.2% ε-Ge grown on (100)/4° Si substrate (*Sample C*) at room temperature (25°C) and 550°C ex-situ annealing temperature. The peak separation of the ε-Ge layer with respect to GaAs buffer at 550°C temperature suggests the similar strain value measured at 25°C, indicating the strain relaxation properties of this structure keep stable up to 550°C.

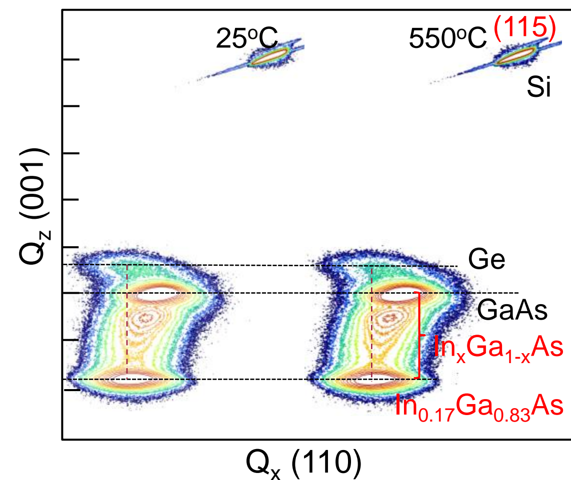

Fig. 5: Asymmetric (115) RSMs of the 1.2% ε-Ge grown on (100)/4° Si (*Sample C*) at 25°C and 550°C ex-situ annealing temperature. The peak separation of the ε-Ge layer with respect to GaAs buffer at 550°C indicate that the strain relaxation properties of this structure remain stable up to 550°C.

As the industry is adopting high mobility Ge and SiGe channel materials,[1-21] and the ε-Ge has recently been experimentally reported to increase the carrier mobility than

unstrained Ge,[30] alternate measurement method to independently confirm strain in Ge is important for scientific research as well as for technological considerations. The strain relaxation values were further substantiated *via* Raman spectroscopy. This measurement technique is extensively used by semiconductor industry to measure the strain in source and drain of a nanoscale transistor. **Figs. 6** shows the shift in Raman frequency (Δω) of tensile strained Ge (*Sample C*) with respect to bulk Ge and epitaxial 0.2% ε-Ge (*Sample A*) before and after annealing at 550°C. Raman frequency shift at temperatures 400°C, 450°C and 500°C, are shown in Supporting Information S2. Raman measurements were performed at different spots of 1.2% ε-Ge layer. One can find from this figure that the tensile strain shifts the longitudinal optical (LO) phonon peak position towards the left side of bulk Ge or epitaxial Ge peak, where the magnitude and sign of the wavenumber shift (negative/tensile or positive/compressive) are representative of the type of strain present in the Ge layer. Using the relation[67] $\Delta\omega = -b\varepsilon_{//}$ cm^{-1}, where $\varepsilon_{//}$ is the amount of strain present within the Ge layer, Δω is the wavenumber shift and b is a material parameter, the tensile strain in Ge can be determined at room temperature and at 550°C. Using the b value of 415±40 cm^{-1} for Ge from Ref. [66], the calculated tensile strain was ~ 1.16% as a function of annealing temperature,

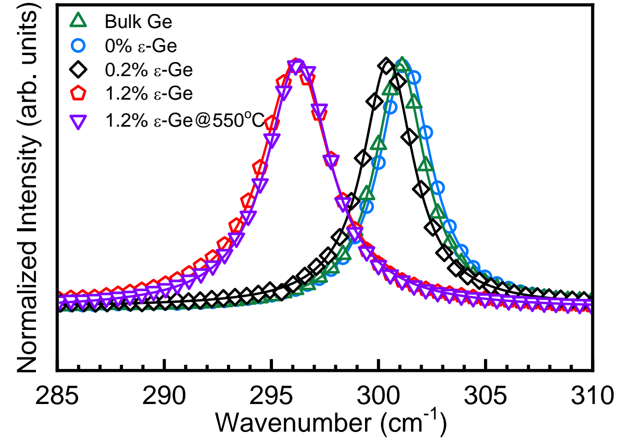

Fig. 6: Raman wavenumber shift due to strain-induced modulation of the Ge LO phonon modes of epi-Ge (*Sample A*), bulk Ge, and tensile strained Ge (*Sample C*): as grown and annealed at 550°C.

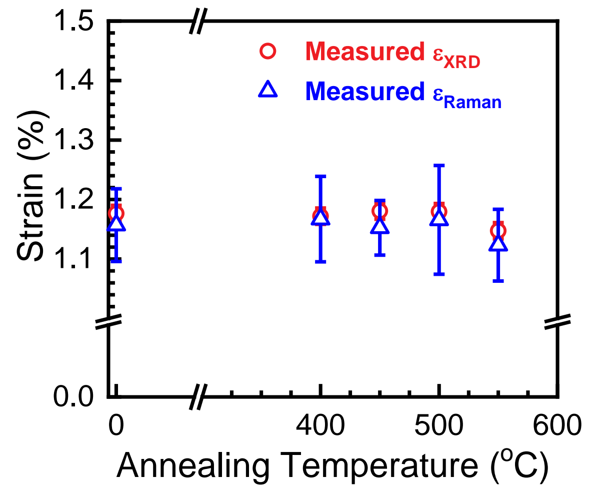

Fig. 7: Comparison of x-ray and Raman-determined strain with annealing temperatures (*Sample C*).

Table I

Summary of strain relaxation values of $In_{0.17}Ga_{0.83}As$ and tensile strain in Ge at annealing temperatures (*Sample C*).

Temperature	X-ray analysis		Raman analysis
	$In_{0.17}Ga_{0.83}As$ relaxation (%)	ε-Ge (%)	ε-Ge (%)
25°C	85	1.18	1.16
400°C	88	1.17	1.17
450°C	88	1.18	1.15
500°C	87	1.18	1.17
550°C	92	1.15	1.12

tabulated in **Table I**. The amount of tensile strain in Ge is slightly decreased at 550°C annealing temperature, reinforcing the earlier x-ray analysis. One can find from **Fig. 6** that Δω shift at 550°C decreases compared to as-grown tensile strained Ge. **Fig. 7** shows the strain versus annealing temperature of ε-Ge on Si. It is observed that the amount of tensile strain (red) determined from x-ray analysis is in agreement with the tensile strain (green) measured from Raman spectroscopy. Thus, temperature dependent x-ray and Raman analysis independently confirm the pseudomorphic nature of 1.2% ε-Ge on Si substrate with graded $In_xGa_{1-x}As$ buffer, annealed up to 550°C.

3.4 Heterointerface analysis of 1.2% ε-Ge on Si via cross-sectional TEM. Cross-sectional TEM micrograph of the 1.2% ε-Ge on Si using graded $In_xGa_{1-x}As$ and GaAs composite buffer is shown in **Fig. 8a**. The starting off-cut (100)Si substrate, combined with a thermal treatment, migration enhanced epitaxy process with arsenic pre-layer, two-step growth process[4,5,32] were used to create two-atomic layer steps on the Si surface, and thereby eliminating/minimizing antiphase domains (APDs). The lattice mismatch induced defects and threading dislocations (TDDs) due to the 4 % strain relaxation of the GaAs and Si could not be avoided but could be minimized using TCA during the GaAs buffer layer to reduce TDDs.[60-62] **Figs. 8b-c** show the high-resolution cross-sectional TEM micrograph (*i.e.*, lattice indexing) at the ε-Ge/$In_{0.17}Ga_{0.83}As$ heterointerface along with the fast Fourier transform (FFT) patterns from the different regions of the heterointerface. Examining the FFT patterns in **Fig. 8c**, one can find that the Ge layer is tensile strained with the constant composition $In_{0.17}Ga_{0.83}As$ buffer layer and the lattice constant of Ge is closely matched with the in-plane lattice constant of $In_{0.17}Ga_{0.83}As$ strain template. In addition, the FFT pattern suggests lack of considerable relaxation induced misfit dislocations (MDs) by the absence of satellite reflections in **Fig. 8c**. This further confirms the pseudomorphic heterointerface of ε-Ge/$In_{0.17}Ga_{0.83}As$, which is further reaffirmed by the previous high-resolution x-ray analysis. In addition, the inverse FFT pattern taken from the part of the ε-Ge/$In_{0.17}Ga_{0.83}As$ interface (*see* green region) where the MDs were observed, as shown in **Fig. 8d**. These MDs are linear defects and are considered as an insertion of an extra half-plane of atoms (*see* pink region). This would suggest that some degree of micro-scale lattice mismatch occurred at this interface that resulted in MDs formation by strain relaxation. Such MDs are absent within the upper 1.2 % ε-Ge layer, which will be used for the

investigation of MOS-Cs. The estimated defect density in ε-Ge is ~10^8 cm^{-2}, based on our recent studies reported in Ref. [30].

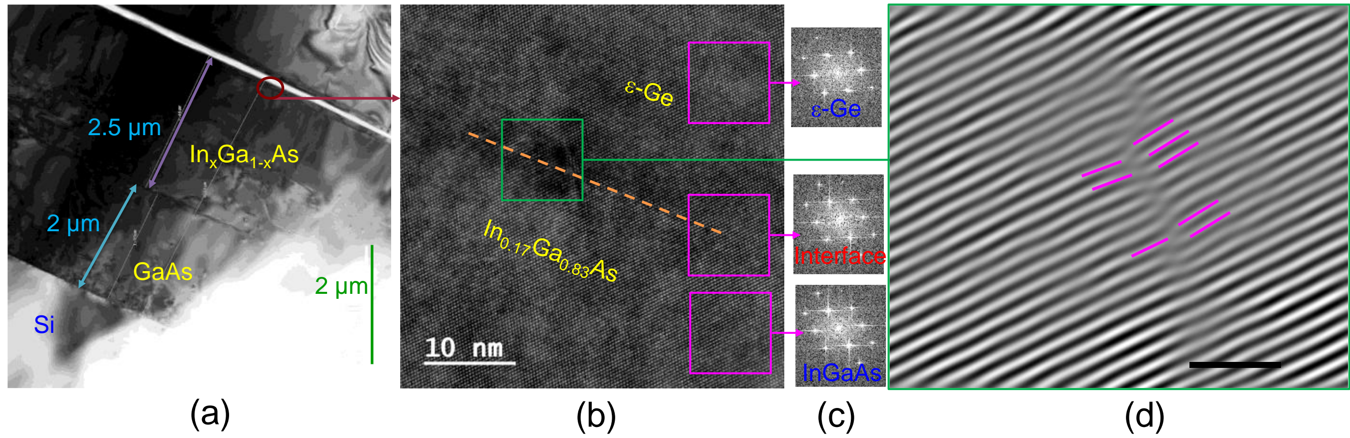

Fig. 8: (a) Cross-sectional TEM micrograph of the 1.2 % ε-Ge grown on (100)/4° Si substrate using composite graded $In_xGa_{1-x}As$/GaAs buffer layer (*Sample C*). The thickness of each layer is shown in (a). (b) Cross-sectional TEM micrograph of the interface of ε-Ge/$In_{0.17}Ga_{0.83}As$. The lattice matched defects and dislocations are confined within the graded $In_xGa_{1-x}As$ buffer layer. (c) FFT patterns were taken from the different part of the structure and absence of satellite peaks reaffirm the pseudomorphic epitaxy. (d) Inverse FFT pattern was taken from the specific region of the ε-Ge/$In_{0.17}Ga_{0.83}As$ heterointerface, showing MDs formation due to some degree of strain relaxation.

3.5 Evolution of ε-Ge (0 %, 0.2 %, 1.2 %) C-V characteristics *versus* GeO_2 passivation: Impact on EOT and Δ*f*.

MOS-Cs were fabricated on the Ge/AlAs/GaAs (*Sample A*) first to develop the process conditions prior to the implementation on ε-Ge. Since the GeO_2 IPL layer is required at the interface between Al_2O_3 and the Ge layer, different oxidation times varying from 0.25 min to 7.5 min at 550°C (the maximum annealing temperature) were carried out. This enables to select the best process conditions, discussed below, on tunable ε-Ge MOS-Cs. **Fig. 9** shows the D_{it} distribution and comparison as a function of energy within the Ge layer with different oxidation times of Ge layer (*Sample A*). The value of D_{it} was extracted using conductance method as a function of measurement temperature (T), and it is expressed as, [57, 58]

$$D_{it} = \left(\frac{G_p}{\omega}\right)_{max} \{f_D(\sigma_s)qA\}^{-1}, \quad (3)$$

where $(G_p/\omega)_{max}$ is the maximum parallel conductance G_p normalized by angular frequency ω, q is the charge, $f_D(\sigma_s)$ is the universal function of the standard deviation of band bending σ_s, and A is the capacitor area. The measurement was performed from 80 K-290 K to allow sampling of the D_{it} distribution at various ranges of the bandgap of Ge

at different temperatures, where above equation can be applied to show the distribution of D_{it} as a function of energy within the Ge bandgap. $f_D(\sigma_s)$ is determined by fitting the approximate width of the conductance (G_p/ω) plot to established metrics, as discussed in Refs. [57, 58]. The T represents the measurement temperature and various lines represent temperature dependent Ge bandgap energy ranges accessible using the conductance (G_p/ω) plot. Here, the 5 nm thick ALD Al_2O_3 was used as a gate dielectric. One can find that the D_{it} is low at 7.5 min oxidation at the cost of EOT (~ 7.6 nm EOT for 7.5 min oxidation time), indicating a trade-off between the lowest D_{it} and the lowest EOT of unstrained Ge MOS-Cs.

Once we optimized the process conditions on unstrained Ge, MOS-Cs were fabricated on epitaxial 0.2 % ε-Ge (*Sample B*) and 1.2 % ε-Ge (*Sample C*) material stacks, where 4 nm ALD Al_2O_3 was used as a gate oxide. The lower Al_2O_3 thickness was selected for lower EOT. As high-quality GeO_2[25, 32, 33, 47] IPL layer is necessary for passivating surface defects of Ge, thermal oxidation of 0.2 % ε-Ge and 1.2 % ε-Ge stack was carried out at 550°C (which is the highest oxidation temperature one can select in order to prevent the strain relaxation in this work) for different oxidation duration. **Figs. 10a-d** show the C-V characteristics of the Ge MOS-Cs of (a) 0.2 % ε-Ge, where GeO_2 oxidation was performed only for 0.5 min, and (b)-(d) 1.2 % ε-Ge where oxidation duration was varied from 0.5 min to 2.5 min, respectively. This offers to clarify whether the shorter duration (*i.e.*, 0.5 min) of Ge surface oxidation is sufficient enough for 1.2 % ε-Ge to attain good quality C-V characteristics. It was observed that 0.5 min GeO_2 formation is not enough for 1.2 % ε-Ge sample (**Fig. 10b**) unlike the lower tensile strained 0.2 % ε-Ge layer (*Sample B*) (**Fig. 10a**). Also inferred from **Fig. 10b**, is higher D_{it} and higher frequency dispersion (Δ*f*). Both samples (*A* and *B)* were placed at the same time inside an oxidation furnace for 0.5 min GeO_2 growth followed by 4 nm Al_2O_3 deposition and formation of metal contacts. One can find a better C-V characteristics from 0.2% ε-Ge at 0.5 min oxidation duration (**Fig. 10a**) than from 1.2% ε-Ge at same

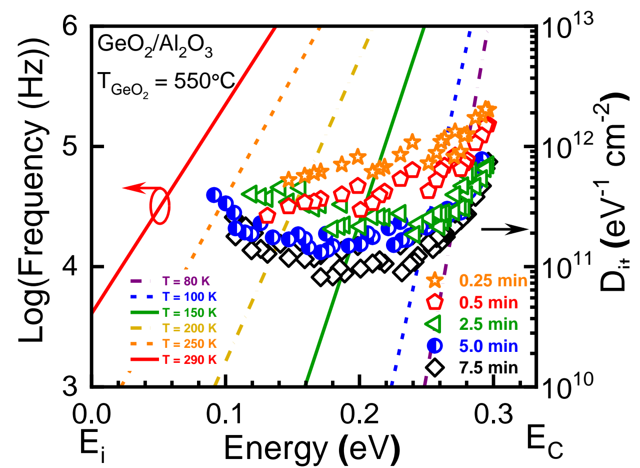

Fig. 9: D_{it} distribution and comparison as a function of energy within the band gap of Ge (*Sample A*) with different oxidation duration.

oxidation duration (**Fig. 10b**). Here, we believe that there is no contact issue affecting the dispersion of the C-V characteristics. This implies that the strain field hinders the formation of thicker GeO_2 layer on the 1.2 % ε-Ge sample and requires higher oxidation duration or temperature. However, as discussed above, the higher temperature beyond 550ºC, relaxes the strain in Ge. The C_{max} capacitance in the accumulation region is higher in 1.2% ε-Ge than 0.2 % ε-Ge, as expected if the thickness of the GeO_2 layer is thinner than 0.2 % ε-Ge. In addition, the shorter

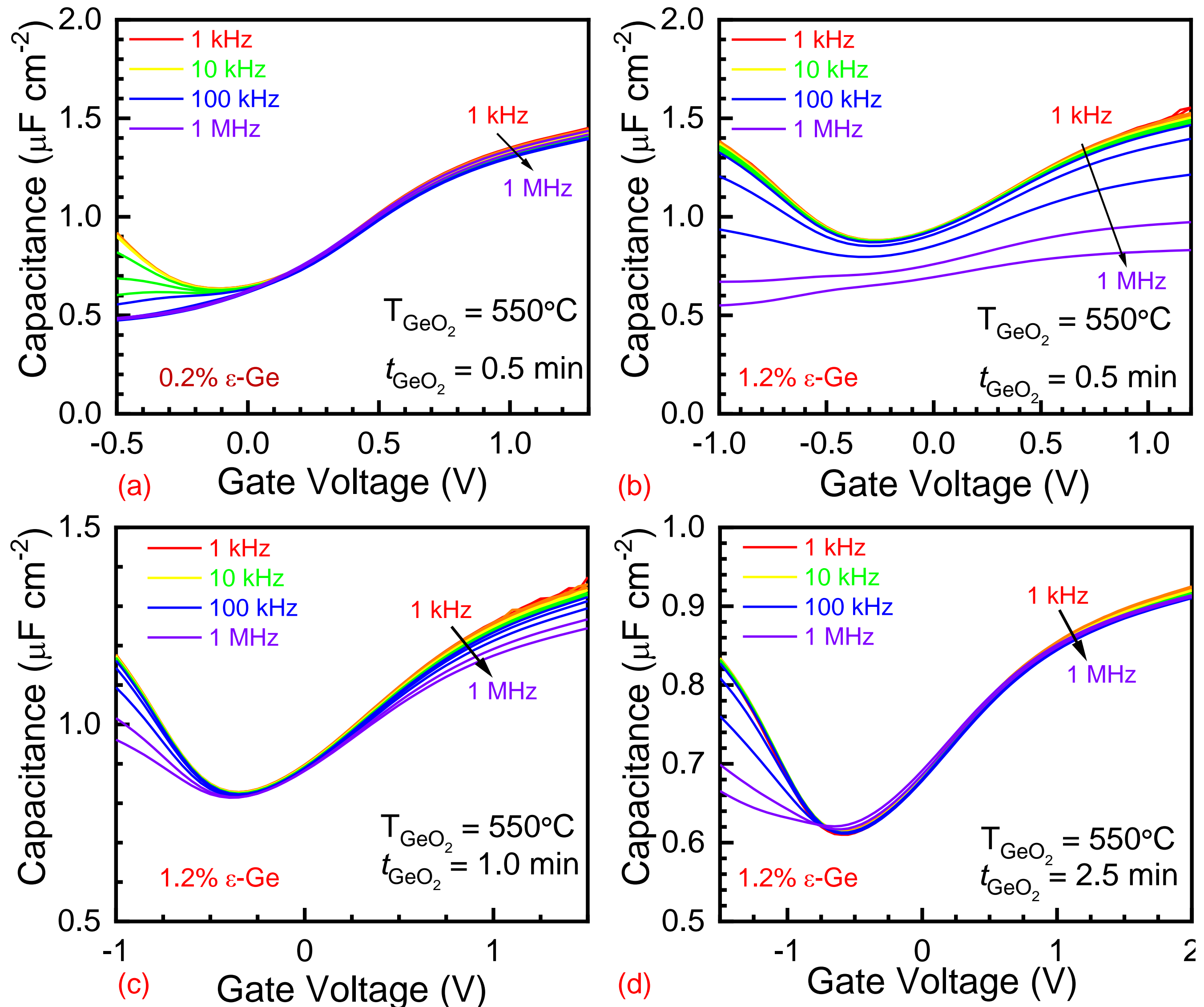

Fig. 10: Room temperature C-V characteristics of the (a) 0.2 % Ge MOS-C on Si (*Sample B*) with 0.5 nm GeO_2 interface passivating layer (IPL) between 4 nm Al_2O_3 and Ge layer, (b) 1.2 % Ge with 0.5 nm GeO_2 IPL (*Sample C*), (c) 1.2 % Ge with 1.0 nm GeO_2 IPL (*Sample C*), and (d) 1.2 % Ge with 2.5 nm GeO_2 IPL (*Sample C*), respectively. In all cases, the GeO_2 were formed at 550ºC annealing temperature inside a tube furnace with ultra-high purity oxygen source.

duration was selected initially for lower EOT if one can devise good C-V characteristics from 1.2 % ε-Ge. At the oxidation time of 2.5 min, the 1.2 % ε-Ge MOS-Cs exhibit low frequency C-V characteristics in the inversion region in the frequency ranges from 1 kHz to 1 MHz. This is attributed due to the shorter minority carrier response time of strain induced lowered bandgap of Ge, and the minority carriers could respond to high frequency ac signal in the inversion region. It has been reported that for low bandgap semiconductors such as InAs[67], SiGe[52] or unstrained Ge[32, 33], GeSn[50], the C-V curves can gradually change from low frequency behavior (room temperature) to high frequency behavior (low temperature).[32, 32, 67] This gradual change is indicative of the free movement of Fermi level at the high-κ/semiconductor interface.[32, 33, 67] The EOT value is calculated from extracted C_{ox} value obtained using the Maserjian *et al.*[68] method. As the oxidation duration of 1.2 % ε-Ge increases, it is observed that both D_{it} and Δf decreases. Wherein at 2.5 min oxidation duration, one can observe the minority carrier response at higher frequency (*i.e.*, 1 MHz) due to the strain induced reduction of the bandgap[50-52, 67] compared to unstrained Ge MOS-Cs.[32, 33] However, one achieves lowest Δf at the cost of higher EOT. Thus, there is a trade-off between the EOT and the Δf of ε-Ge as a function of GeO_2 growth time.

To establish a relation between the EOT and Δf as a function of GeO_2 growth time, we have characterized the 1.2 % ε-Ge MOS-Cs as a function of GeO_2 growth time. **Figs. 11a, b,** and **c** show the C-V characteristics of unstrained Ge (*Sample A*), 0.2% ε-Ge (*Sample B*), 1.2 % ε-Ge (*Sample C*) MOS-C at 5 min oxidation time at 550°C, and EOT/Δf versus GeO_2 growth time, respectively. There is a clear effect of strain on the C-V characteristics of tunable tensile strained Ge MOS-C properties. One can find from **Fig. 11a** and **11b** that the accumulation capacitance at 750 kHz and 1 MHz is higher than the low frequency capacitance. The high-frequency capacitance should show less trap response and consequently have a lower accumulation capacitance. The higher accumulation capacitances at both 750 kHz and 1 MHz frequencies are related to contact problem (parasitic contribution from the contact reducing the accumulation capacitance value). In addition, it is evident from **Fig. 11c** that the value of C_{max} in the accumulation region (positive gate voltage) at 5 min GeO_2 growth decreases compared with 2.5 min oxidation duration, as shown in **Fig. 10d**. Comparing the EOT and Δf as a function of GeO_2 growth time, the lowest Δf is achieved at 5 min oxidation time; however, the EOT increases significantly with this oxidation duration,

demonstrating proper surface passivation as well as trapped oxide charges, thereby resulting in a decrease in Δ*f*. However, the increasing EOT with increasing oxidation duration is a concern. One can find from **Fig. 11d** that the EOT shows a significant increase beyond an oxidation duration of 2.5 min. Comparing both EOT and Δ*f* with GeO_2 growth times from **Fig. 11d**, ~1.5 min would be an optimum GeO_2 growth time at 550ºC oxidation temperature. One can also find from **Figs. 10a-d** and **11a-c** the flat-band voltage of MOS capacitor depends on the tensile strain in Ge layer. The flat-band voltage shift with bi-axial strain is related to strain-induced conduction and valence band-edge shifts and changes in the work function of the semiconductor. [69, 70]

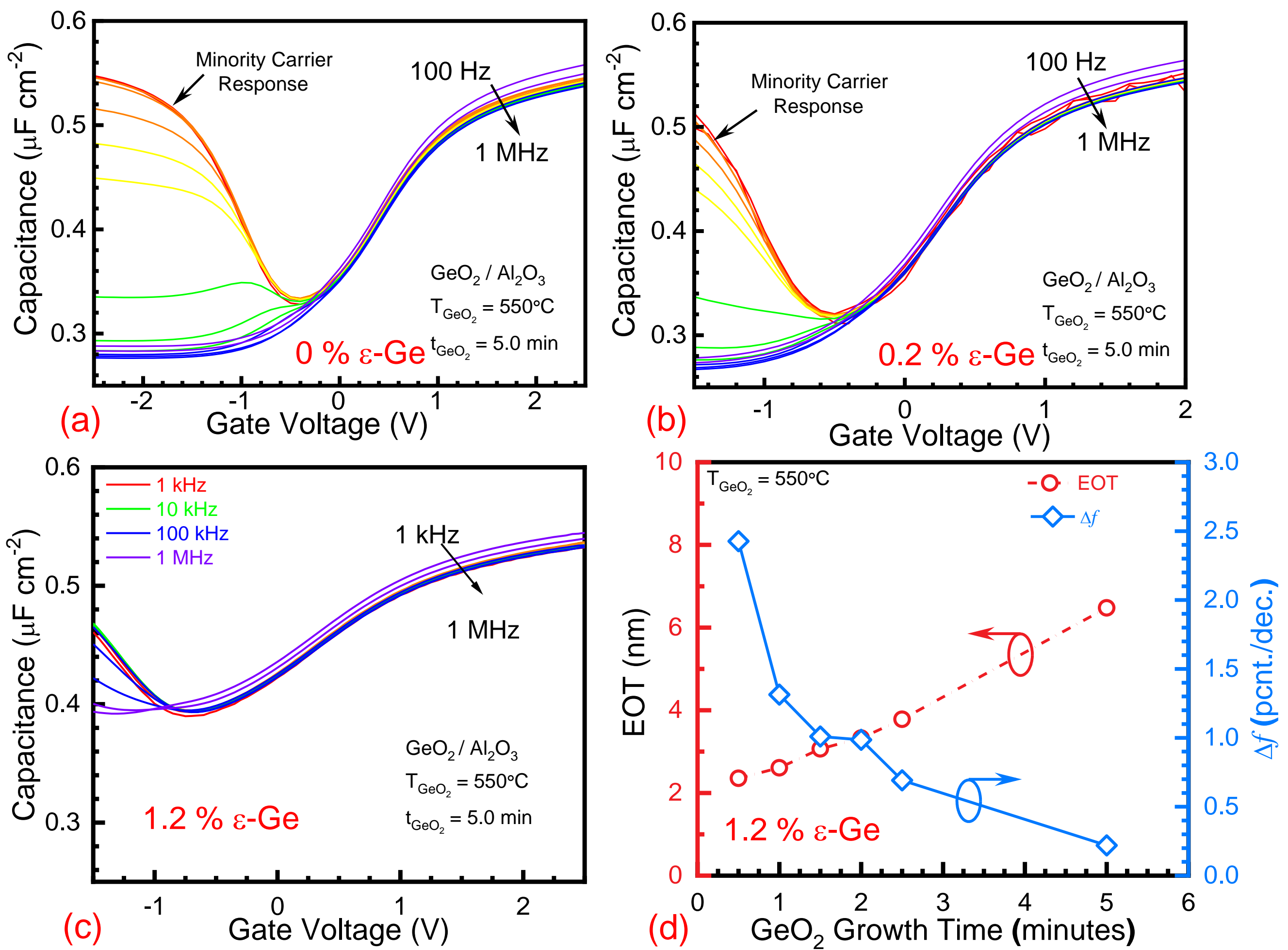

Fig. 11: Room temperature C-V characteristics from (a) unstrained n-type Ge (*Sample A*), (b) 0.2% n-type ε-Ge (*Sample B*), and (c) 1.2% n-type ε-Ge (*Sample C*) MOS capacitors, where 4 nm Al_2O_3 was used as gate oxide along with 5 min thermal oxidation time at 550ºC, respectively. (d) EOT and low frequency dispersion, Δ*f* as a function of GeO_2 growth time at 550ºC oxidation temperature of 1.2% ε-Ge MOS-C.

Table II summarizes the strained Ge MOS capacitors with various gate dielectrics on both compressive and tensile strained Ge, reported in the literatures. [3, 5, 31, 36, 37, 50] We found that no strained Ge MOS capacitor structure has an intermediate compound semiconductor buffer layer. In addition, an IPL between the high-κ dielectric and the Ge layer in these works were realized *via* plasma oxidation. Furthermore, the effect of the amount of strain on the interfacial layer formation (GeO_2) has not been reported yet. This has been explicitly detailed in the present work, where the strain field inhibits the formation of GeO_2 layer and varying oxidation duration is needed to realize

Table II

Comparison of compressive and tensile strained Ge MOS-Capacitors grown on Si substrates.

MOS-C	Structure	Gate Stack	Strain	C_{max} (μF/cm^2)	C_{min} (μF/cm^2)	Measurement Conditions	Ref.
Ge QW	Ge/$Si_{0.3}G_{0.7}$	2 nm HfO_2 0.6 nm SiO_2 0.6 -1.4 nm Si-cap s-Ge	c-1.3%	~ 2.15-2.3	~0.5	f = 1 MHz at 300 K	[5]
p-Ge	Ge/GeSn/Ge	5 nm HfO_2 s-Ge	t-1.1%	~1.48	~0.38	f = 1 MHz at 300 K	[50]
			t-1.4%	~1.55	~0.38		
		4 nm HfO_2 1 nm Al_2O3 s-Ge	t-1.1%	~1.48	~0.25	f = 10 kHz at 80 K	
				~1.45	~0.23	f = 100 kHz at 80 K	
				~1.25	~0.125	f = 1 MHz at 80 K	
p-Ge QW	Ge/$Si_{0.3}Ge_{0.7}$	2.2 nm HfO_2 0.5 nm Al_2O_3 GeO_x s-Ge	c-1.3%	~2.65	~0.1	f = 1 MHz	[31]
n-Ge QW	Ge/$Si_{0.6}Ge_{0.4}$	4 nm HfO_2 0.8 nm Si s-Ge	c-2.45%	~1.5	-	f = 10 kHz, 100 kHz, 1 MHz	[3]
n-Ge	Ge/$Si_{0.56}Ge_{0.44}$	4 nm HfO_2 GeO_x s-Ge	c-2.2%	~2.6	~0.1	f = 1 MHz	[37]
n-Ge	Ge/$Si_{0.57}Ge_{0.43}$	2.2 nm HfO_2 0.2 nm Al_2O_3 0.35 nm GeO_x s-Ge	c-2%	~3.1	~1.25	f = 5 kHz	[36]
				~3.1	~1.25	f = 10 kHz	
				~3	~0.75	f = 100 kHz	
				~2.9	~0.45	f = 500 kHz	
				~2.9	~0.4	f = 1 MHz	
n-Ge	Ge/AlAs/GaAs	4 nm Al_2O_3 GeO_2 s-Ge	t-0.2%	~ 1.4	~ 0.5	f = 1 MHz at 300 K	This Work
	Ge/$In_{0.17}Ga_{0.83}$As/In_xGa_{1-x}As/GaAs	4 nm Al_2O_3 GeO_2 s-Ge	t-1.2%	~ 1.35	~ 0.8	f = 1 MHz at 300 K	

good C-V characteristics, similar to unstrained Ge layer. Note that these assimilated strained Ge (compressive and tensile) MOS capacitors using high-κ dielectrics do not include any comparison to Ge based planar or 3D (FinFET) transistor results. There is a limited information related to C-V characteristics of MOS capacitors from the most up-to-date strained Ge (compressive and tensile) devices, where the main objective was to demonstrate the fabrication and characterization of the transistors.

3.5 Role of strain (0 %, 0.2 %, 1.2 %) on D_{it} evaluation

The conductance method as a function of measurement temperature of Ge MOS-Cs was used to determine and compare D_{it} as a function of amount of strain in Ge. In order to obtain the full distribution of D_{it} within the bandgap of Ge, it is necessary to probe the Ge MOS-Cs over a wide range of measurement temperatures. During the C-V measurement of each Ge MOS-C, the conductance was measured as a function of frequency, ω and is shown in Supporting Information S3. One of the important parameters to assess the quality of the gate oxide/semiconductor interface is the D_{it}. The D_{it} values were evaluated from these conductance plots as a function of energy within the bandgap of Ge. **Figs. 12a** (0% and 0.2% ε-Ge) and **b** (1.2 % ε-Ge) show the D_{it} as a function of energy at different measurement temperatures. The D_{it} values are almost similar for the Ge MOS-Cs grown on GaAs (0% strain) and on Si (0.2 % strain) (**Fig. 12a**). A minimum D_{it} value of 1.36×10^{11} $eV^{-1}cm^{-2}$ was determined approximately 0.15 eV away from the conduction band edge, E_c for Ge MOS-Cs on Si and the D_{it} of 2.50×10^{11} $eV^{-1}cm^{-2}$ was obtained on

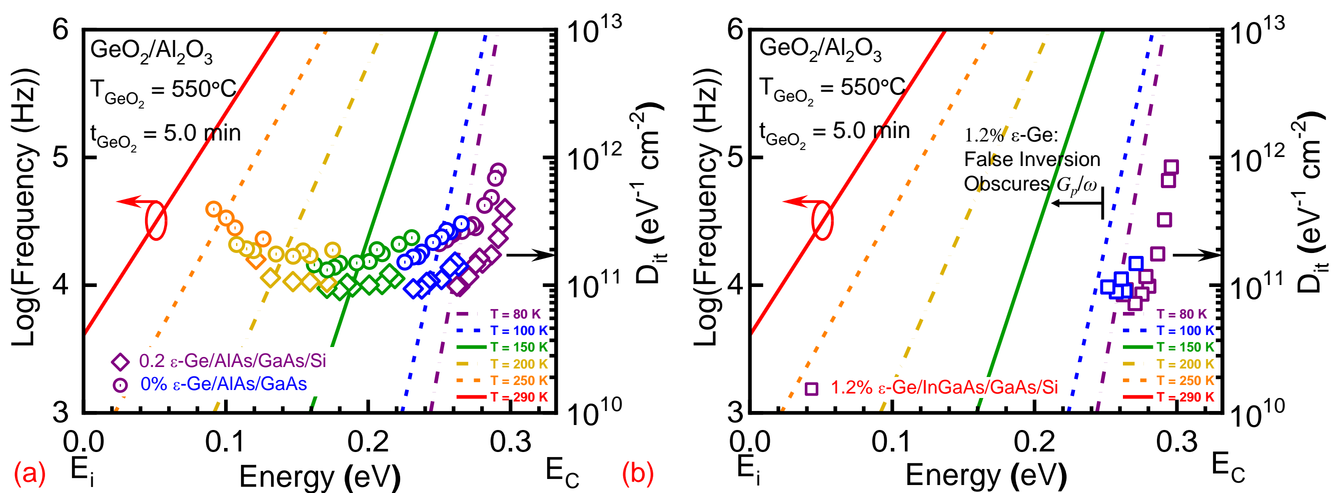

Fig. 12: D_{it} distribution and comparison as a function of energy within the band gap of Ge: (a) 0% (*Sample A*) and 0.2 % ε-Ge (*Sample B*), and (b) 1.2 % ε-Ge (*Sample C*).

GaAs substrate, as shown in **Fig. 12a**. Similarly, the D_{it} value of 2.06×10^{11} $eV^{-1}cm^{-2}$ was obtained from 1.2 % ε-Ge and the false inversion in 1.2 % ε-Ge above 150 K obscures the G_p/ω peak at higher temperature than low strained or unstrained Ge MOS-Cs. The D_{it} evaluation was possible only at lower temperature for samples with higher strain due to the false inversion of minority carrier response. D_{it} values from this work are comparable to the corresponding values reported in literature of Ge MOS devices,[32, 33] which suggests both excellent passivation of the Ge surface as well as a defect-minimal Ge epitaxy on Si. **Table III** summarizes D_{it} versus strain determined from temperature dependent conductance data.

Table III
Summary of D_{it} versus strain determined from temperature dependent conductance data.

Sample	Ge strain (%)	D_{it} ($cm^{-2}eV^{-1}$)
A	0	2.5×10^{11}
B	0.2	1.36×10^{11}
C	1.2	2.06×10^{11}

4. CONCLUSIONS

Tunable tensile strained epitaxial Ge layers have been monolithically integrated on Si substrates using appropriate buffer layers by dual chamber solid source molecular beam epitaxy and their structural and MOS capacitor properties were evaluated. Both x-ray analysis and topography measurements were performed to evaluate the materials quality, thermal mismatch induced radius of curvature, thermal stress, and thermal crack. At a lower thermal stress of ~50 MPa, no visible thermal crack was observed, and it was due to the specific selection of thermal cycle annealing temperatures during the growth of GaAs on Si. Temperature dependent strain relaxation properties were determined by x-ray and Raman analyses, and it was found that the tensile strain of 1.2% can be preserved within the ε-Ge layer up to 550°C *ex-situ* annealing temperature, which is essential for the formation of GeO_2 IPL on Ge layer through thermal oxidation. In addition, cross-sectional transmission electron microscopic study revealed the strained heterointerface of ε-Ge/$In_{0.17}Ga_{0.83}As$. The unstrained Ge MOS-Cs with Al_2O_3/GeO_2 gate stack of varying oxidation time at 550°C for the formation of GeO_2 IPL exhibited an D_{it} of ~2.5×10^{11} $eV^{-1}cm^{-2}$. For the ε-Ge layer, the minimum oxidation time of 0.5 min on 1.2% ε-Ge is inadequate to accomplish a good C-V characteristics from 1.2 % ε-Ge MOS-C, due to the strain field hindering the formation of the GeO_2 IPL layer and longer oxidation time was needed. In addition, there must a trade-off between the minimum D_{it} and minimum EOT and ~1.5 min of oxidation time is an optimum duration for 1.2% ε-Ge. Minimum D_{it} values of 1.36×10^{11} $eV^{-1}cm^{-2}$ and

2.06×10^{11} $eV^{-1}cm^{-2}$ were determined from 0.2% and 1.2% ε-Ge MOS-C, respectively. However, false inversion in the 1.2% ε-Ge MOS-C due to short minority carrier response time, which could respond to high frequency ac signal as well as strained induced lowered bandgap at room temperature obscures actual quantification of the D_{it} value at higher temperature, which is a signature of low bandgap semiconductors. Hence, the tunable tensile strained Ge materials' synthesis with minimal thermal stress, preserving strain within the Ge layer at higher temperature as well as analyzing the role of strain and process conditions on ε-Ge MOS-C properties open an option for the development of Ge-based transistors.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.xxx/acsaelm.xxxxxxx.

> Temperature dependent x-ray reciprocal space maps of 1.2% ε-Ge at 400ºC, 450ºC, and 500ºC; temperature dependent Raman spectra of 1.2% ε-Ge at 400ºC, 450ºC, and 500ºC; conductance plots of 1.2% ε-Ge for interface state density extraction (pdf).

CONFLICTS OF INTEREST

The authors declare no competing financial interest.

AUTHOR CONTRIBUTIONS

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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