

Low Pressure and Short-time Silver-Sintering for Power Modules

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ABSTRACT

silver-sintering has become one of the main chip interconnect technologies in wide band-gap (WBG) semiconductor power modules due to its excellent thermal conductivity, high temperature stability and mechanical reliability. However, the traditional silver-sintering process generally has the problems of long sintering time and high auxiliary pressure, which not only restricts the industrial production efficiency, but also may cause mechanical damage to the brittle chip.

In this study, an innovative low-pressure and short-time silver-sintering process, namely the Paste+Film method, was proposed and systematically verified. Through controlled experiments, the results showed that the Paste+Film method can achieve high-quality silver connections with a shear strength of more than 40 MPa under the conditions of only applying a mild pressure of 5–10 MPa and shortening the sintering time to 3–5 minutes.

In addition, the process was successfully applied to the packaging preparation of double-sided cooled SiC MOSFET half-bridge modules, and the overall sintering time was shortened by about 75% compared with the traditional method. Electrical testing and mechanical performance evaluation further verified the superiority of the Paste+Film process in ensuring chip structural integrity, improving process yield and material utilization, and provided a new path for achieving large-scale manufacturing of next-generation high-power density and high-reliability power modules.

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GENERAL AUDIENCE ABSTRACT

Electric vehicles, renewable energy systems, and other modern technologies demand high-power, efficient, and thermally reliable power modules. To meet these needs, advanced chip-attachment techniques are required, especially for handling wide band-gap semiconductors like SiC and GaN.

This thesis introduces the Paste+Film method, a silver-sintering approach that combines silver paste with a porous silver film. The paste improves surface contact and acts as an adhesive layer, while the film provides structural rigidity and allows solvent to escape during direct sintering. This dual-layer configuration enables strong bonding under low pressure (5-10 MPa) in just 3-5 minutes, significantly faster and gentler than conventional processes.

The method was tested on both Ag-Ag and Au-Ag bonding interfaces. For Ag-Ag connections, a shear strength above 40 MPa was achieved using only 5 MPa of assist pressure and a sintering time of 3 minutes at 240°C. For Au-Ag connections, a bonding strength of 25 MPa was attained with 10 MPa pressure in 5 minutes at 240°C. These results highlight the adaptability of the method to different metallization types while ensuring robust joint quality.

Applied to double-sided cooled SiC MOSFET power modules, the Paste+Film method reduced total process time by approximately 75% compared to traditional approaches. It protects brittle chips from pressure-induced damage and simplifies manufacturing, offering a practical path toward scalable, high-performance power electronics.

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Chapter 1

Introduction

1.1 - Overview of Power Electronics Packaging

1.1.1 - Introduction to Power Electronics

Today, power electronics broadly encompasses the conversion, control, and regulation of electrical energy at high voltages and currents with minimal losses [1-3]. As a foundational technology, power electronics underpins nearly all modern energy systems—from electric vehicles (EVs) [4] and renewable energy sources such as solar panels and wind turbines to data centers and industrial motor drives [5]. By precisely regulating voltage and current, power electronics enables efficient energy transmission and regulation in environments where performance, compactness, and reliability are critical.

In recent years, the demand for higher power density, faster switching speeds, and lower cooling costs has risen dramatically [6]. These trends are driven not only by economic factors but also by pressing environmental concerns such as greenhouse gas emissions and climate change due to the growing need of green energy [7]. At the same time, robust and efficient power electronic converters are essential to integrating intermittent renewable energy sources into the grid and maintaining stable power delivery and quality.

As industry continues to push the operating limits of silicon-based devices, packaging and materials technologies must also advance at the same time. High switching frequencies, high current densities, and elevated junction temperatures all place significant pressure on traditional packaging materials and package designs [8]. Therefore, innovations in package-level solutions are critical to achieving global energy efficiency goals, accelerating the energy transition, and meeting stringent environmental regulations.

Within this broader technology landscape, power modules play a key role in enabling high-voltage, high-current circuits on a single package. Typically, power modules integrate multiple semiconductor devices (e.g., diodes, transistors) and their interconnections into a rugged package that provides mechanical support, insulation, and heat dissipation. This modular design not only simplifies manufacturing and maintenance, but also addresses the need for enhanced thermal management—especially now that wide band-gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) can operate at higher temperatures and voltages [6].

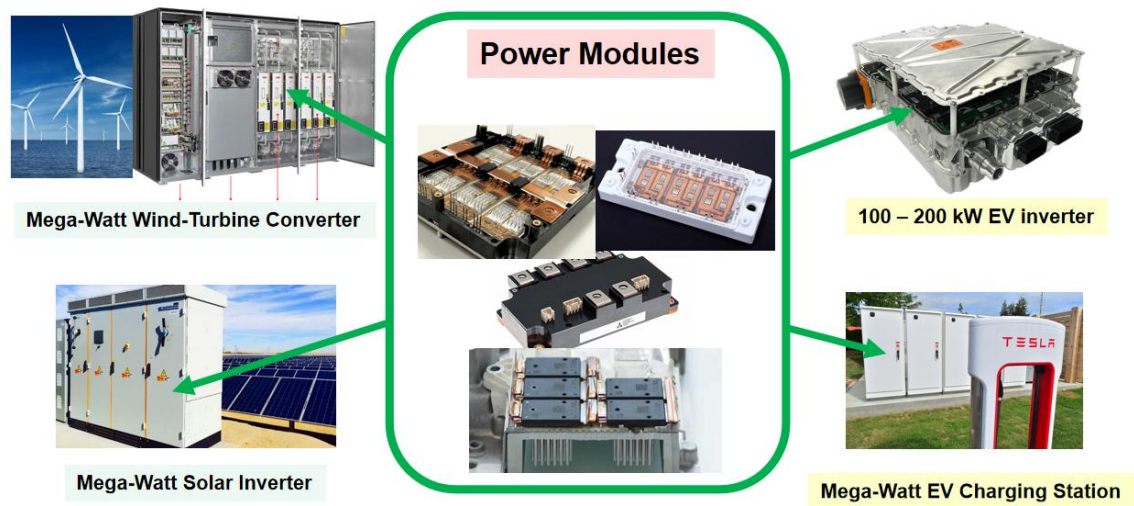


Fig.1 Important application of power modules.

The reliability of these power modules directly affects the lifetime and performance of the system in critical applications. Therefore, continued innovation in module packaging and die-attach materials is critical to driving efficient power conversion in next-generation transportation, renewable energy, and industrial systems. Advanced packaging approaches that meet the stringent requirements for higher power density and improved thermal performance ensure that power electronics remain at the forefront of technological advancements.

1.1.2 - Wide Band-Gap Power Semiconductor

With the rapid development of electric vehicles and electric aircraft, power electronic systems are facing increasing demands in terms of efficiency, power density, thermal performance, and size reduction. Traditional silicon insulated gate bipolar transistors (Si IGBTs) have relatively high on-state voltage drop, slow switching speed and limited thermal conductivity, which has gradually failed to meet the increasing needs of high-efficiency and high-frequency applications. In contrast, silicon carbide metal oxide semiconductor field effect transistors (SiC MOSFETs) have wider band gaps, higher breakdown voltages, lower on-resistance and excellent thermal characteristics, making them the first choice for next-generation power devices [9-11].

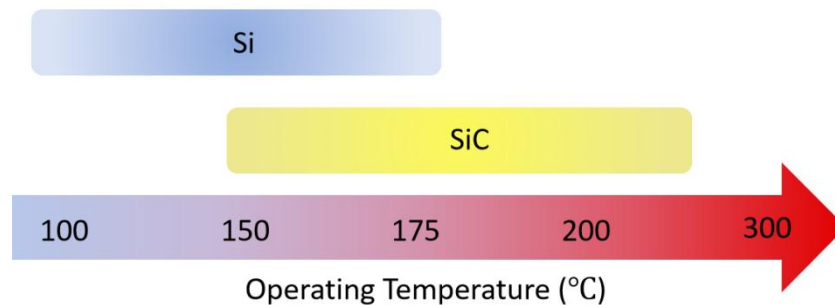


Fig. 2 Operating temperature of Si and SiC device

As pioneers in wide band-gap devices, SiC MOSFETs have quickly emerged as a key enabler of efficient power conversion, poised to replace traditional Si IGBTs in a wide range of applications. These devices not only offer superior electrical performance (such as high blocking voltage, low on-resistance, zero reverse recovery, and fast switching transitions) [9], but also strong thermal tolerance, with an operating junction temperature of over 200°C [10]. Leading manufacturers such as ROHM, Wolfspeed, and STMicroelectronics have commercialized automotive-grade silicon carbide (SiC) MOSFETs with rated voltages ranging from 650 V to 1700 V, targeting high-power applications such as traction inverters, on-board chargers (OBCs), DC-DC converters, photovoltaic inverters, and fast charging stations for EVs.

This Table 1 compares two mature commercial devices: Si IGBT (FGH40N120AN) [12] and SiC MOSFET (C3M0065100K) [13]. By comparing their key electrical performance parameters, it can be seen that SiC MOSFET devices have lower switching losses than Si IGBTs, which can achieve higher switching frequency operation and obtain better efficiency; at the same time, SiC MOSFET has lower conduction losses. Under the same current conditions, the conduction loss of SiC MOSFET is much lower than that of Si IGBT, because Si IGBT has a significant voltage drop when it is turned on. Therefore, SiC MOSFET is more suitable for medium and high frequency working occasions, such as 20 kW drive modules, where the efficiency is significantly improved, resulting in a decrease in system heat dissipation requirements [11]. Due to the minority carrier storage effect in the current carrying mechanism of IGBT, there is a long "tail current" when it is turned off, causing energy loss. SiC MOSFET is a fully controlled voltage type device with no tail current, fast turn-off speed, and lower loss, which is especially suitable for systems that require frequent PWM modulation.

Property	Si IGBT	SiC MOSFET
Band-gap	1.1 eV	3.2 eV
Max Junction Temp	$\leq 150\text{ }^{\circ}\text{C}$	$\geq 200\text{ }^{\circ}\text{C}$
Conduction Power Loss	$V_{CE,sat} \approx 2.9\text{ V (at 40 A)}$	$R_{DS(on)} \approx 65\text{ m}\Omega$
Switching Time (t_r/t_f)	$t_r \approx 20\text{ ns, } t_f \approx 40\text{ ns}$	$t_r \approx 10\text{ ns, } t_f \approx 8\text{ ns}$
Switching Frequency	$\leq 50\text{ kHz}$	$\geq 150\text{ kHz}$
Temp Rise at 20 kW	+40 $^{\circ}\text{C}$	+13 $^{\circ}\text{C}$

Table. 1 Comparative conduction characteristics of Si IGBT (FGH40N120AN) [12] and SiC MOSFET (C3M0065100K) [13].

In general, SiC MOSFET provides better efficiency, higher power density, wider operating temperature range and better EMI performance. These advantages make it gradually replace traditional Si IGBT in new energy vehicles, power grids, photovoltaic inverters, server power supplies and other occasions with extremely high requirements for efficiency and compactness, and become the core of the next generation of power modules.

According to projections by Yole Intelligence, the global SiC power device market surpassed USD 1.5 billion in 2022 and is expected to exceed USD 10 billion by 2030,

with a compound annual growth rate (CAGR) of more than 30% as reported by Yole Intelligence. Automotive, grid infrastructure, and industrial drives are identified as the dominant market drivers. This explosive growth underscores not only the intrinsic advantages of SiC materials and devices but also brings about unprecedented challenges for power module packaging. As SiC chips become smaller, more power-dense, and operate at higher switching frequencies and temperatures, packaging is no longer merely a mechanical or electrical interface—it has become a critical determinant of overall system performance, thermal efficiency, and long-term reliability [14].

Consequently, designing next-generation power module packaging structures capable of accommodating the unique characteristics of SiC devices has become a focal point of power electronics research. Key considerations include suppressing parasitic inductance, optimizing heat dissipation paths, enhancing insulation and dielectric strength, and supporting system-level integration [14, 15].

1.2 - Introduction to Power Module Packaging

In power electronic systems, power devices (such as IGBT, MOSFET, etc.) are core switching elements. Their performance depends not only on the design of the body, but also on the packaging structure of the device. Packaging refers to the process and technology that combines semiconductor chips with peripheral electrical, thermal management and mechanical structures. Good packaging can not only provide stable mechanical support and electrical connection for the device, but also achieve effective heat dissipation and environmental protection, thereby improving the reliability and service life of the device [16, 17].

The main purposes of power module packaging include the following aspects: (1) Provide efficient and stable electrical connection to reduce conduction loss and parasitic parameters; (2) Achieve efficient heat dissipation path to ensure the thermal stability of the chip at high power density; (3) Provide protection against external environmental influences such as high voltage, high temperature, and corrosion; (4) Alleviate thermal

expansion mismatch between different materials, reduce thermal stress, and improve structural stability [16].

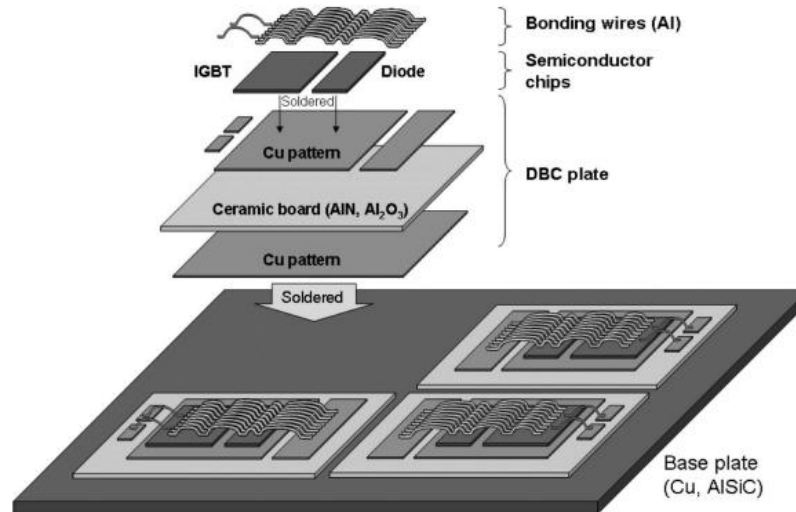


Fig. 3. The typical structure of the conventional single sided cooled power module architecture [18].

A complete power module packaging structure shown in Fig. 3 usually includes the following key components:

- (a) Die: Usually Si IGBT or SiC MOSFET, it is the core device to realize the switching function.
- (b) Chip substrate (Substrate): Mainly uses DBC (direct copper bonding) or AMB (active metal brazing) substrates with Al₂O₃, AlN or Si₃N₄ ceramic dielectrics, which have both electrical insulation and thermal conductivity functions [18].
- (c) Die-Attach: Common materials include solder (such as SnAgCu), eutectic alloys (such as AuSn) or sintered silver (Ag), which are used for electrical, mechanical and thermal connections between chips and substrates.

(d) Wire bond: Traditionally, aluminum (Al) or copper (Cu) wires are used. In recent years, a variety of bond-free wire structures have also appeared; connect the chip with the lead-out terminal or busbar to achieve electrical interconnection.

(e) Heat sink (Base plate): Commonly used materials include copper, Al, SiC, Si₃N₄, etc., which are used to collect and conduct the heat generated by the chip when it is working to the external cooling system.

(f) Encapsulant: Such as silicone gel, epoxy resin, etc., used to protect the internal structure from humidity, dust and chemical corrosion. It also provides dielectric insulation to prevent electrical discharge between conductive components.

(g) Housing: Engineering plastics such as PBT (polybutylene terephthalate) and PPS (polyphenylene sulfide) are used to provide external physical protection and electrical isolation. The housing not only shields the internal components from mechanical impact and environmental contaminants, but also helps maintain the structural integrity of the entire module under thermal and mechanical stress.

The packaging structure of Si IGBT and SiC MOSFET is very similar, however, SiC devices have higher switching frequencies and operating temperatures, so there are higher requirements on the thermal stability, insulation strength and parasitic parameters of the packaging materials. For example, SiC devices are more suitable for advanced processes such as Ag sintering, double-sided cooling, and low-inductance packaging to maximize their performance potential [16].

However, power modules also face a variety of reliability challenges in long-term operation. The first is the mismatch of the coefficient of thermal expansion (CTE). Different materials will produce stress concentration during thermal cycles, resulting in chip cracks, solder layer peeling or substrate warping. The second is the partial discharge phenomenon, which often occurs in the weak insulation area under high voltage, and may cause breakdown failure in the long term. Chip overheating is also a common problem. If

the heat dissipation path is not designed properly, it is easy to cause thermal runaway. Furthermore, the presence of voids or bubbles in the packaging material, such as gaps inside the potting resin or solder layer, will form stress concentration points during the thermal cycle, accelerate aging and even cause breakdown. The above factors are all important reasons for the reduction of module life and failure [18, 19].

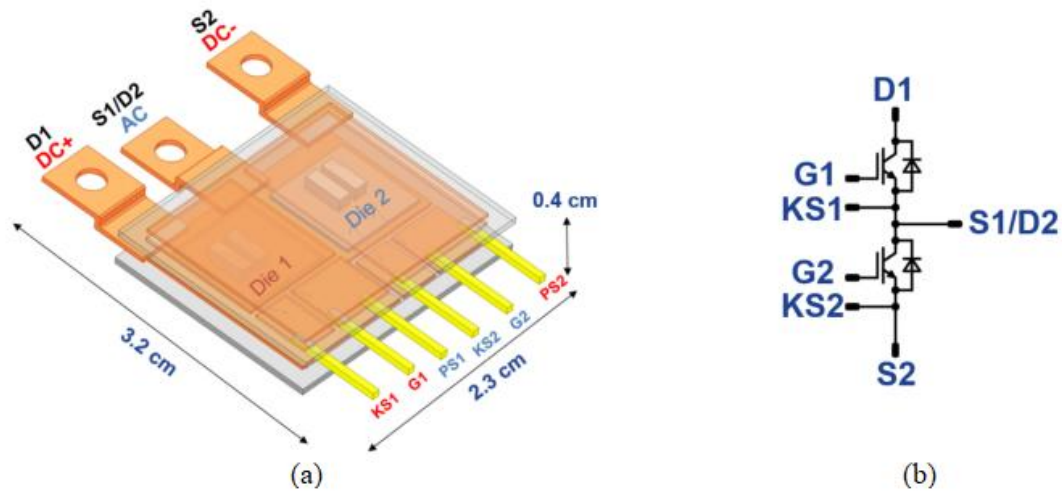


Fig. 4. (a) A three-dimensional view of the DSC 3.3 kV SiC MOSFET phase-leg module layout design; (b) the module circuit [20].

With the development of high power density, double-sided cooled half-bridge module (shown in Fig. 4) has become an important packaging solution. Compared with the traditional single-sided heat dissipation method, the double-sided cooling structure allows heat dissipation in both the upper and lower directions at the same time, significantly reducing thermal resistance and junction temperature, and improving the rated power and reliability of the module. This type of module usually adopts a sandwich structure, symmetrically arranging the DBC or AMB substrates on the upper and lower sides through the middle metal bracket, the chip is sandwiched between the two, and sintered silver or solder interconnection is used to connect the chip to the upper and lower substrates. This structure not only improves the thermal management efficiency, but also significantly reduces the parasitic inductance, which is conducive to the high-frequency, fast-switching SiC devices to realize their full potential [20].

In summary, packaging technology, especially heat dissipation design, is an important supporting link for power module performance and reliability. In the future, with the widespread application of wide band-gap semiconductors, the design of heat dissipation paths and heat sinks, as well as the improvement of module reliability will continue to be the focus of power module research and development.

1.3 - Introduction to Silver-sintering Die-Attach

1.3.1 - Conventional Die-Attach Approach

Die-Attach is one of the most critical connection structures in the power module because it is responsible for providing electrical connection and main heat dissipation channel for the chip. The reliability of the chip bonding material directly affects the reliability of the entire power module. Therefore, the material must establish a strong bond with the chip and substrate, and have a coefficient of thermal expansion similar to both to avoid interface failure caused by thermal stress [21-24].

At present, there are many types of chip bonding materials, covering high-temperature and low-temperature application requirements, which can be mainly divided into six categories: epoxy adhesives, alternative resins, eutectic solders, soft solders, silver glass composite materials and metal sintering materials. In the field of power module packaging, the most widely used are lead-free solder, silver-filled adhesives (Ag filled adhesive) and silver-sintering materials.

Silver-filled adhesive is an adhesive material with silver particles as filler and UV-curing or heat-curing resin as the matrix, which is suitable for high-temperature applications within a certain temperature range [25]. In order to improve its thermal and electrical conductivity, this type of material usually introduces silver flakes or silver particles as fillers. They have good process adaptability, are suitable for automated chip mounting processes, and help alleviate stress concentration during chip operation.

However, silver-filled adhesives also have significant defects. During the dispensing and curing process, a continuous and dense thermal/electrical conductive channel may not be formed between the silver fillers, especially when the connection between the silver sheet and the silver particles is poor. This structural defect limits its thermal conductivity. As shown in Table 3, the thermal conductivity of this type of material after sintering is usually less than $10\text{W}/(\text{m}\cdot\text{K})$, which is difficult to meet the strict thermal management requirements of double-sided cooling power modules for chip bonding materials.

Bonding Materials	SAC Solder	Ag Filled Adhesive	Sintered Silver
Min. Process Temp.	260°C	200°C	180°C
Processing Time	3-5 min	120 min	5-20 min
Failure Temp.	220°C	100-150°C	$\geq 900^\circ\text{C}$
Compatible Surfaces	Most metal	Most metal	Ag, Au, Cu

Table 2. Process parameters of different die-attach materials [25, 26, 27].

In recent years, lead-free solder has gradually replaced traditional Sn-Pb solder and become the mainstream chip bonding material in the field of electronic packaging due to the restrictions of the RoHS Directive. The typical Sn-Ag-Cu (SAC) series solder has good wettability and reliability, and its eutectic temperature is about 217°C , which is suitable for general low to medium temperature packaging processes. However, due to the high isothermal ratio ($T_h > 0.5T_m$) of lead-free solder at service temperature, it will undergo obvious creep and microstructural aging even at room temperature, resulting in a significant decrease in its mechanical properties (such as yield strength and shear strength) in long-term operation. In addition, the thermal conductivity of SAC solder is low ($\leq 57\text{W}/\text{m}\cdot\text{K}$), and its electrical conductivity is also inferior to that of metal bonding materials, which limits its heat dissipation ability in high power density applications [27].

In contrast, silver materials show great advantages in power module packaging due to their excellent thermal conductivity ($> 200\text{W}/\text{m}\cdot\text{K}$), excellent electrical conductivity

($\leq 0.01 \text{ m}\Omega \cdot \text{cm}$) and high failure temperature ($\geq 900^\circ\text{C}$) as shown in Table 3. Sintered silver materials can complete solid-phase sintering connection at a lower temperature (e.g., 180°C [26]) and in a shorter time (e.g., 3 min [32]), and the formed joints have high strength and low thermal resistance, which greatly improves the thermal management efficiency and reliability of the packaging system, and is especially suitable for the high-temperature and high-frequency operating environment of SiC devices. Therefore, in the packaging of high-performance power modules, sintered silver is gradually replacing lead-free solder and becoming a new generation of ideal chip bonding materials [28].

Bonding Materials	SAC Solder	Ag Filled Adhesive	Sintered Silver
Thermal Conductivity	57 W/(m·K)	≤ 10 W/(m·K)	> 200 W/(m·K)
Electrical Conductivity	0.020 mOhm·cm	0.010 mOhm·cm	≤ 0.010 mOhm·cm
Die-Shear Strength	≥ 30 MPa	10–20 MPa	≥ 40 MPa
CTE(~4 for Si)	27.9 ppm/K	38 ppm/K	10-20 ppm/K

Table 3. Performance characteristics of die-attach joints [25, 26, 27].

1.3.2 - Silver-Sintering Materials

Silver-sintering is a metal bonding material with silver particles as the main component. It is heated to promote the diffusion and bonding of atoms between particles in the solid phase, thereby achieving dense connection [27-32]. Unlike traditional solder, silver-sintering does not rely on the melting process, but completes bonding at a lower temperature and controllable pressure through a solid-state diffusion mechanism. It has excellent thermal conductivity, electrical conductivity, high melting point and high-temperature stability, and is particularly suitable for packaging requirements of wide band-gap devices (such as SiC and GaN) under high junction temperature, high frequency and high power density conditions.

The development of silver-sintering technology can be traced back to the 1990s. It was first proposed and conducted preliminary experimental research by European companies such as Infineon and Semikron in Germany. They tried to reduce the silver-sintering temperature to below 300°C by controlling the composition of nano silver paste and sintering process parameters to replace traditional solder for high-temperature power module packaging [33]. To achieve this goal, researchers such as Scheuermann [34] and Schwarzbauer [35] proposed applying assist-pressure (about 40 MPa) to the chip and substrate assembly to accelerate the diffusion and densification reaction of silver particles at low temperature, so that the chip bonding layer can achieve up to 80% densification at 250°C [36].

Since the beginning of the 21st century, silver-sintering technology has made rapid progress. Lu et al. proposed a composite particle size nanosilver paste formula, which mixes nanosilver particles with submicron or micron silver particles, while ensuring low-temperature sintering activity and optimizing the fluidity and sintering stability of the paste [28-31]. This material system has obvious process advantages, not only can the sintering time be shortened from several hours to 30 minutes, but also the required auxiliary pressure can be reduced from 40 MPa to less than 10 MPa [30, 37]. Furthermore, if nano-scale silver powder with smaller particle size is used, reliable sintering can be achieved without external pressure, which greatly simplifies the process flow [28].

In recent years, with the rise of high-power density modules and double-sided cooling structures, Researcher has further expanded the application boundaries of silver-sintering. They no longer use sintered silver only for chip bottom bonding, but also develop it into an internal module component with a porous structure, which is used as a deformable post or post connection material in high-temperature packaging. This design not only enables the module to operate normally at higher junction temperatures, but also significantly optimizes the distribution of thermal-mechanical stress. According to literature reports, this structure can reduce the parasitic inductance of the module power loop by about 23% and the thermal resistance by about 30%, while improving the yield of the packaging process and reliability under high-temperature operation [30].

In general, silver-sintering materials are gradually developing from an "alternative option" for traditional solders and adhesives to an indispensable mainstream technology route in high-end power device packaging, and show broad application prospects in high-demand scenarios such as new generation SiC modules, server power supplies, and high-speed railway traction power supplies [30-33].

1.3.3 - Formulation of Silver-Sintering Paste and Silver-Sintering Film

Silver-sintering materials (including silver-sintering paste, silver-sintering film and silver-sintering preform) are mainly composed of silver particles, which form a dense metal bonding structure through solid-phase sintering reaction under medium and low temperature conditions. As shown in Fig. 5, its precursor morphology is generally obtained by mixing nano-silver particles or micron silver particles coated with surfactants with organic solvents and binders, and then different processes are used to obtain film-like silver-sintering films and paste-like sintered silver pastes [26].

In the formulation of silver-sintering slurry and silver film, organic components mainly include binders (Binder), surfactants (Surfactant) and thinners (Thinner), which play a key role in the dispersion stability, rheological control and sintering behavior of the slurry. The main function of the binder is to provide initial mechanical strength and adhesion in the printing or coating stage. Commonly used materials include polyvinyl butyral (PVB), acrylic resin and vinyl acetate, etc. Its decomposition behavior will directly affect the stability of the intermediate structure before sintering and the level of carbon residue. Surfactants are mainly used to prevent silver particles from agglomerating during storage and dispersion. Common types include lauric acid, stearic acid or their metal salts. Adding an appropriate amount can significantly improve the dispersibility and storage stability of the slurry; but excessive or insufficient decomposition will inhibit the formation of particle sintering necks. Diluents are used to regulate the viscosity and construction performance of the slurry to ensure that it is suitable for process operations such as screen printing and dispensing. Common solvents include butyl acetate, acetone, pinene alcohol, etc. The ratio of the three needs to be finely optimized according to the

target sintering temperature, sintering method (with/without pressure) and usage scenario to achieve high-density, low-porosity and high-strength silver sintered joints [26].

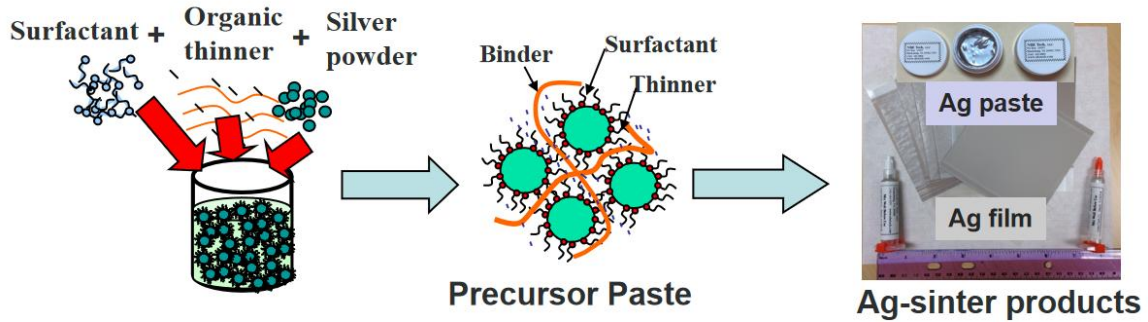


Fig. 5 Formulation and product forms of silver-sintering materials from NBE Tech [26].

1.3.4 - Mechanism of Silver-Sintering

Silver-sintering is a typical solid-state sintering process. Unlike traditional solders that achieve connection through melting and solidification, silver-sintering relies on atomic diffusion and bonding between nano-silver particles under temperature excitation.

Type of solid	Mechanism	Source of matter	Sink of matter	Densifying
Polycrystalline	Surface diffusion	Surface	Neck	No
	Lattice diffusion	Surface	Neck	No
	Vapor transport	Surface	Neck	No
	Grain boundary diffusion	Grain boundary	Neck	Yes
	Lattice diffusion	Grain boundary	Neck	Yes
	Lattice diffusion	Dislocations	Neck	Yes
Amorphous	Viscous flow	Unspecified	Unspecified	Yes

Table 4. Sintering mechanisms in polycrystalline and amorphous solids [38].

Sintering is often divided into several types based on the mechanism that causes shrinkage or densification. Sintering by solid-state diffusion is a type of solid-state sintering [38, 39]. Polycrystalline materials are often sintered by this process. The entire

sintering process is generally considered to be divided into three stages [40-42]: initial stage, intermediate stage, and final stage.

At the beginning of the sintering process, particles shift into thermodynamically more favorable configurations through mechanisms such as rotation and sliding, driven by the sintering force. This rearrangement leads to volume shrinkage and a gradual increase in overall density. As the particles reposition, their contact areas grow, initiating the formation of necks at the interfaces. The growth of these necks can occur through several mechanisms, including surface or lattice diffusion, vapor transport, plastic deformation, and viscous flow. This initial sintering stage continues until the neck radius expands to approximately 40–50% of the particle radius [26].

Once the pores within the structure evolve into a stable configuration defined by surface and interfacial energy minimization, the intermediate sintering stage begins. At this point, the material remains porous, and the voids are still interconnected. Further densification is primarily driven by the reduction of the cross-sectional area of these pores. As sintering progresses, the pores eventually become unstable, collapse, and merge, leading the system into the final stage of sintering [39].

Sintering in polycrystalline materials is governed by at least six distinct mechanisms, which are summarized in Table 4. Among these, only mass transport via bulk diffusion from grain boundaries or neck dislocations directly contributes to densification. Nonetheless, other mechanisms—though non-densifying—play a critical role in modifying neck geometry, thereby influencing both the driving force and the rate of densification [43].

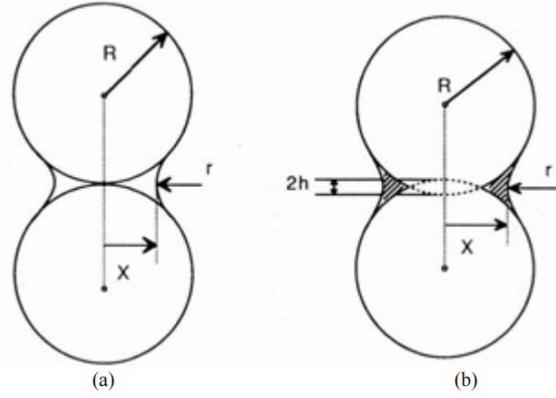


Fig. 6. Two-particle geometric model for the initial stage of sintering [38].

In these models, the particles are assumed to be spherical, of equal size, and uniformly packed. Then, the entire system is represented by one unit of the powder (called the geometric model). For the assumed model, the sintering equation can be obtained by formulating the corresponding mass transfer equation and solving it using appropriate boundary conditions.

In the analysis of the initial stage of sintering, a model consisting of two spheres of equal size and contacting each other with radius R is usually assumed [38]. The models for the densification and de-densification mechanisms are slightly different to reflect the changes caused by the relevant mechanisms. The geometric model is shown in Fig. 6. The neck growth equation can be expressed in the general form of equation 1.1:

$$\left(\frac{X}{R}\right)^m = \frac{H}{R^n} t \quad (1.1)$$

Mechanism	m	n	H
Surface diffusion	7	4	$56D_s\delta_s\gamma_{sv}\Omega/kT$
Lattice diffusion from surface	4	3	$20D_l\gamma_{sv}\Omega/kT$
Vapor transport	3	2	$3p_0\gamma_{sv}\Omega/(2\pi mkT)^{1/2}kT$
Grain boundary diffusion	6	4	$96D_{gb}\delta_{gb}\gamma_{sv}\Omega/kT$
Lattice diffusion from grain boundary	5	3	$80\pi D_l\gamma_{sv}\Omega/kT$
Viscous flow	2	1	$3\gamma_{sv}/2\eta$

Table 5. Values for the constants m and n in equation 1.1 [38].

Where, X represents the radius of the neck formed between adjacent particles, while m and n are constants that vary depending on the dominant sintering mechanism. H serves

as a mechanism-specific coefficient, and t denotes time. The relationship describing neck growth under viscous flow conditions was first developed by Frenkel [44]. The relevant values of the constants and coefficients for different sintering mechanisms are summarized in Table 5.

It is important to note that the geometrical model describing the intermediate stages of sintering in polycrystalline materials differs from that used for amorphous systems. A widely adopted model for polycrystalline sintering is the one proposed by Coble, who formulated expressions for densification driven by lattice diffusion and grain boundary diffusion. In Coble's model, the powder compact is idealized as being composed of equally sized, tetradecahedral particles, with cylindrical pores located along the edges. Using this framework, the densification rates associated with lattice and grain boundary diffusion mechanisms can be approximated accordingly [42].

$$\text{Lattice diffusion: } \frac{\dot{\rho}}{\rho} \approx \frac{AD_l\gamma_{sv}\Omega}{\rho G^3 kT} \quad (1.2)$$

$$\text{Grain boundary diffusion: } \frac{\dot{\rho}}{\rho} \approx \frac{4}{3} \frac{D_{gb}\delta_{gb}\gamma_{sv}\Omega}{G^4 kT(1-\rho)^{1/2}} \quad (1.3)$$

where ρ is the density, $\dot{\rho}$ is the changing rate of densification, A is a constant and G is the grain size [45-47].

1.4 - Limitation of Silver-Sintering Paste and Silver-Sintering Film

Although pressure-assisted sintering can significantly improve the bonding strength and thermal performance of the silver film, excessive external pressure can cause serious potential damage to the chip body during the sintering process. Studies have shown that under high auxiliary pressure, stress is often concentrated on the edge and interface area of the chip, especially for GaN or SiC devices based on brittle silicon substrates, which can easily cause crack initiation and expansion inside the chip or at the interface, ultimately leading to insulation breakdown, thermal runaway and other failure problems as it shown in Fig. 7 [48-50]. In addition, in embedded packaging structures, high local pressure will further increase the risk of device rupture. In general, the stress applied to

the surface or inside of the chip under high auxiliary pressure can easily exceed the fracture toughness limit of the material, thus becoming the main cause of reduced reliability [50].

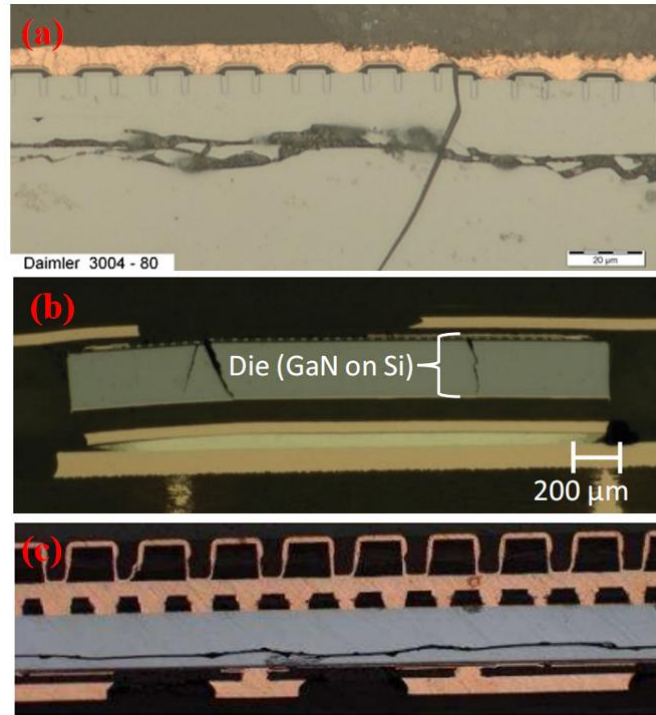


Fig. 7. Failure modes in sintered silver die-attach structures under high-pressure conditions: (a) Interfacial delamination and horizontal cracking [48]; (b) Vertical fracture through GaN-on-Si die [49]; (c) Interfacial cracking along die bottom [50].

Further research has pointed out that the damage to the chip during sintering depends not only on the peak value of the applied pressure, but also on the duration of the pressure and the microscopic evolution of the sintered silver film. Taking micron-level silver paste as an example, in order to form sufficient mechanical strength, it usually takes a long time to sinter, which causes the chip to be in a high stress environment for a long time, further increasing the risk of damage. In contrast, silver-sintering paste or silver-sintering film can quickly establish a high initial rigidity in the early stage of sintering, inhibit chip bending deformation, and significantly reduce local stress concentration. Therefore, the direction of process optimization should be to reduce the applied pressure during sintering as much as possible and shorten the sintering duration, thereby reducing potential damage to the chip structure.

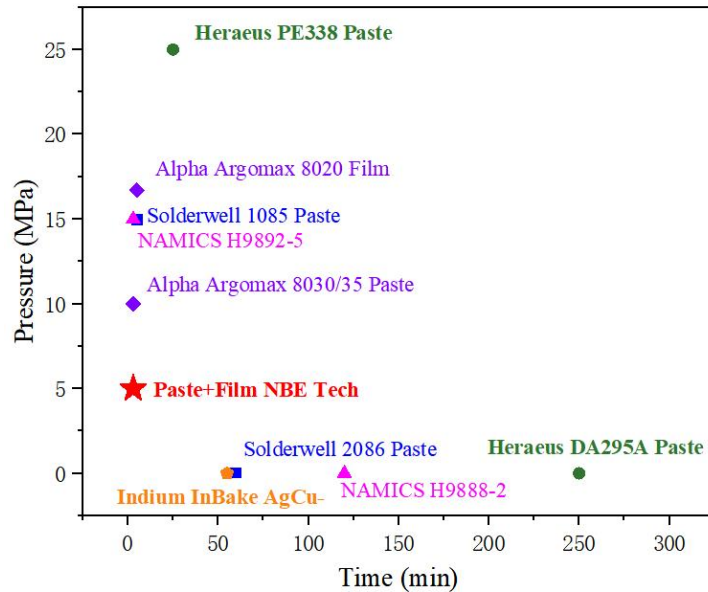


Fig. 8 Sintering pressure and time requirements for 40 MPa die-shear strength of common commercial silver materials versus Paste+Film [32, 51, 52, 53, 54, 55].

Fig. 8 shows the assist pressure and process time for common commercial silver materials to achieve a 40 MPa bond. A clear trend showing the current commercial silver-sintering materials generally are facing a trade-off between "high pressure and short time" and "low pressure and long time". On the one hand, auxiliary pressure helps to accelerate the densification process; on the other hand, to avoid potential damage to the device structure, low-pressure or even pressureless sintering becomes a safer option, but at the cost of significantly extending the sintering time. At present, Alpha Argomax® [32], Namics Co [51], Solderwell Inc. [52] and Indium Co. [53] are the world's major suppliers of silver-sintering materials. According to the sintering conditions of their latest products listed in the figure, it can be seen that rapid sintering products using auxiliary pressure usually require a pressure of about 15 MPa, while the shortest total sintering time for materials suitable for pressureless processes is more than 60 minutes.

Based on the above technical bottlenecks, if the advantages of silver-sintering film and silver-sintering paste can be combined and integrated into the same bonding process, it is possible to achieve reliable bonding within 3 minutes with only 5 MPa of auxiliary pressure. Once this process path is mature and can be stably applied to the packaging

process of power devices, it will significantly improve manufacturing efficiency and throughput.

Reducing the auxiliary pressure of silver-sintering film not only helps to avoid the formation of cracks and delamination inside the chip, but also effectively prevents voids, defects and overall connection strength degradation at the silver film interface, thereby improving the long-term reliability of the packaging structure. Especially for wide band-gap semiconductor devices with high brittleness and strong thermal stress sensitivity, such as GaN and SiC, low-pressure sintering technology can maximize the retention of the structural integrity of the device body, while ensuring the density and thermal conductivity of the sintered silver layer, thereby laying the foundation for achieving high power density and long life power modules [28, 35, 49, 50].

1.5 - Thesis Structure

This thesis is organized into five chapters.

Chapter 1 introduces the background and motivation of this research, focusing on the development trend of power electronics toward higher power and higher junction temperatures. To meet these demands, advancements in packaging design and materials — especially die-attach materials — are essential. This chapter highlights the formulation, sintering mechanisms, and processing methods of sintered silver materials. It particularly discusses the limitations of commercial silver-sintering products, such as the need for high assist pressure and long sintering time. To address these issues, a novel “Paste+Film” sintering approach is proposed.

Chapter 2 presents the experimental design and methodology based on the proposed Paste+Film approach in Chapter 1. A series of experiments were conducted to: (1) evaluate the electrical performance of SiC and Si Schottky diodes sintered under different assist pressures; (2) compare the shear strength of Paste+Film joints with that of film-only joints; and (3) identify the optimal processing parameters for the Paste+Film method.

Chapter 3 presents the experimental results, including: (1) the electrical performance and failure conditions of Schottky diodes of different materials under various assist pressures; (2) the improved shear strength and lower variation of Paste+Film joints compared with film-only and paste-only joints under identical conditions; (3) the influence of paste thickness on the shear strength of Paste+Film joints; and (4) the optimal combination of sintering time, temperature, and pressure for the Paste+Film method.

Chapter 4 applies the optimized parameters obtained in Chapter 3 to power module assembly. Shear strength tests were conducted on the bonding of pins, posts, and dies in both as-sintered and annealed states. The total process time of the Paste+Film method was compared with that of using paste or film alone. The results demonstrated the promising application potential of the Paste+Film method in power module packaging.

Chapter 5 summarizes the main findings of this research, emphasizing the effectiveness of the Paste+Film method in both Au-Ag and Ag-Ag sintering, as well as its potential for power module packaging. It also outlines future work, including evaluation of material properties (e.g., electrical/thermal conductivity and CTE), long-term reliability testing, and microstructural characterization using TEM, SEM, and image analysis. These studies will further validate the method and support its broader application in high-performance power electronics.

Chapter 2

Experimental Procedure

2.1 - Characterization

To compare the bonding quality of different die-attach method and different sintering profile — and to optimize the process parameters for silver-sintering, it is essential to establish a set of evaluation standards for the resulting as-sintered silver joints. The primary characterization technique employed in this study is the die-shear strength test, which quantitatively assesses the mechanical integrity of the bond under shear loading. In addition to shear testing, cross-sectional analysis provides insights into the microstructural features of the bonding interface, such as porosity distribution, neck formation, and element distribution [31]. Furthermore, electrical testing (e.g., forward I-V measurements or blocking test) can be used to evaluate whether the semiconductor device is damaged after sintering. Together, these methods form a comprehensive assessment framework to validate and optimize the Paste+Film sintering process in comparison to conventional approaches.

2.1.1 - Die-Shear Test

The key evaluation indicators of sintered silver joints include mechanical strength, thermal conductivity, electrical conductivity and reliability (such as stability under thermal cycles and power cycles). However, since sintered silver usually presents a porous silver structure with a porosity of 10%-30% [26], its electrical conductivity and thermal conductivity are difficult to measure directly after die-attach. On the one hand, the silver sintered joint is enclosed between the chip and the substrate after sintering, and it is difficult to obtain an effective cross-section for testing; on the other hand, even if the simulation method is used to estimate, its value is easily affected by the porosity distribution and interface state, resulting in poor accuracy. Therefore, in actual characterization, mechanical strength, especially shear strength, is usually used as the main indicator to measure the quality of silver sintered joints.

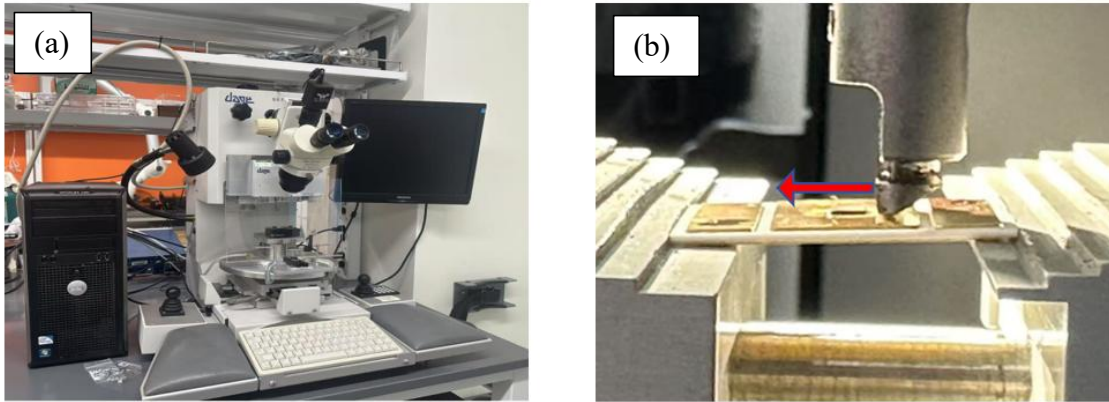


Fig. 9 (a) DAGE 4000 die-shear tester and (b) the shear test schematic.

Shear strength testing is usually carried out by DAGE 4000 equipment as shown in Fig. 9. After the sample is fixed, the chip is pushed at a constant loading rate to cause shear failure relative to the substrate, and the maximum failure load is recorded. Previous studies such as M. Wang et al. pointed out that the thermal impedance of sintered silver joints and reliability are often positively correlated with its shear strength, indicating that shear strength can not only reflect the mechanical reliability of the joint, but also indirectly reflect its thermal performance [56]. The equation 2.1 shows the relationship between thermal impedance Z_{th} and thermal conductivity λ :

$$Z_{th} = \frac{d}{A_{eff} \cdot \lambda} \quad (2.1)$$

Where d is the thickness of the heat conduction path and A_{eff} is the effective cross-sectional area for heat conduction. The equation 2.1 and Fig.10 combined indicates that die-shear strength is positively related to thermal conductivity of the sintered-silver joints.

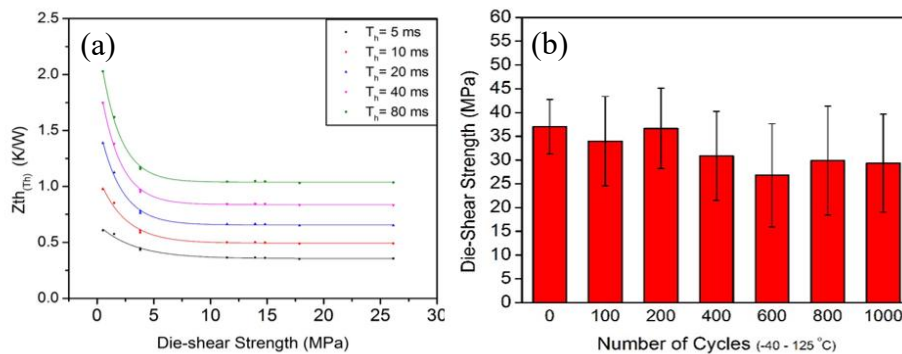


Fig. 10 Relation between (a) transient thermal impedance and (b) number of cycles against die-shear strength [56].

2.1.2 - Electrical Test

To evaluate the damage that auxiliary pressure may cause to Si IGBT and SiC MOSFET devices during silver-sintering, we used a pressure-assisted sintering method using only silver-sintering film to test on Schottky diodes with corresponding materials. Specifically, silver-finished Si diodes (5mm × 5mm) and SiC diodes (3mm × 3mm) were sintered onto silver-finished substrates. Subsequently, electrical performance tests were performed using a probe station (shown in Fig. 11) or wire bonds to detect whether the device functions remained intact after sintering.



Fig. 11 Probe station and the curve tracer for electrical test.

Forward characteristic tests were performed at 25°C using a custom-made curve tracer. The current was gradually increased to 2.5 A, and the maximum open circuit voltage and on-resistance under each pulse were recorded. The reverse characteristic test was performed by continuously increasing the applied voltage to 1.2 kV (for SiC Schottky diodes) and 800 V (for Si Schottky diodes) until the diode broke down.

2.1.3 - Surface Roughness Analysis

Due to the silver film could deform and crack during storage, transport, and transfer process, it is very important to observe the surface morphology of the silver film at different stages. A scanning laser microscope (SLM) was used to obtain 3D surface images and calculate arithmetical mean roughness R_a , shown in equation 2.2.

$$R_a = \frac{1}{L} \int_0^L |Z(x)| dx \quad (2.2)$$

Where L is the sampling length, $Z(x)$ is the deviation of the profile height at position x from the mean line. Here, we used SLM to measure the silver-sintered film both before and after the transfer process, in order to characterize the changes in surface morphology induced by the transfer.

2.1.4 - Cross-section Analysis

Scanning electron microscopy (SEM) enabled direct visualization of the microstructural features, allowing quantitative analysis of porosity distribution and neck growth. In order to study the internal structure of embedded power semiconductor devices, this paper adopts the metallographic cross-section sample preparation method for analysis. The sample preparation process is shown in Fig. 12 and Table 6, first, the sample is embedded with CRAFT RESIN 51oz resin. Then, in order to avoid the damage to the sample caused by the mechanical stress of cutting wheel, we use P180 SiC sandpaper to remove the excess resin and unwanted parts of the cured sample instead of cutting with cutting wheel. Then, the material between the target surface (Plane B in Fig. 12) and the open surface (Plane A in Fig. 12) is gradually removed by mechanical grinding with finer SiC sandpaper (P320 to P1200). Finally, a three-step polishing process is performed, using 5 μm and 3 μm diamond suspensions and 0.05 μm Al_2O_3 suspension with polishing cloth in turn to obtain a scratch-free flat surface suitable for microscopic observation. This process abandons traditional production to minimize the mechanical stress caused by grinding, thereby reducing the generation of sample preparation artifacts such as transverse cracks with the cost of longer processing time.

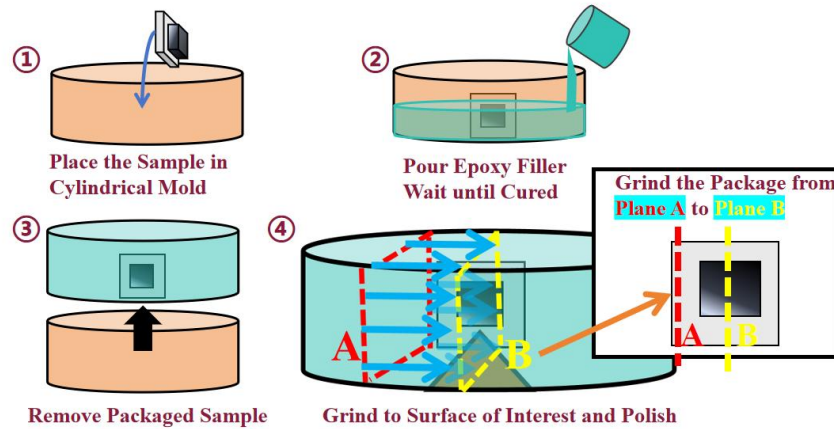


Fig. 12 Schematic of cross-section sample preparation procedure

Step	Grit/ μm	Material	Speed (rpm)	Time (min)
1	P180	SiC	200	10:00
2	P240	SiC	300	3:00
3	P320	SiC	300	3:00
4	P800	SiC	300	5:00
5	P1200	SiC	300	5:00
6	5 μm	Al_2O_3	150	10:00
7	3 μm	Al_2O_3	150	10:00
8	0.05 μm	Al_2O_3	150	10:00

Table 6. Grinding and polishing process for cross-section sample.

After achieving a mirror-like surface, the cross-section was examined using scanning electron microscopy (SEM). Elemental distribution maps were acquired via EDS analysis, while porosity distribution (quantified with ImageJ) and neck growth features were also analyzed from the high-resolution SEM images.

2.2 - Silver-Sintering Profile

To address the issue that the use of Ag film alone typically requires excessively high auxiliary pressure, we propose that deformation of the silver film during storage, transport, and transfer may lead to poor interfacial contact at the sintering interface. To mitigate this problem, two modified bonding approaches were developed: the Film+Film method and the Paste+Film method (as illustrated in Fig. 13). These methods aim to compensate for the limited contact area and thereby enable milder and more efficient sintering conditions—specifically, lower auxiliary pressure and shorter sintering time.

To evaluate the effectiveness of the Film+Film and Paste+Film methods, we conducted sintering at a target temperature of 240°C under an auxiliary pressure of 5 MPa for 10 minutes, followed by natural cooling to room temperature. The shear strength of the resulting joints was measured using a DAGE 4000 die-shear tester and compared with that of the control group using the Film-Only method under the same conditions.

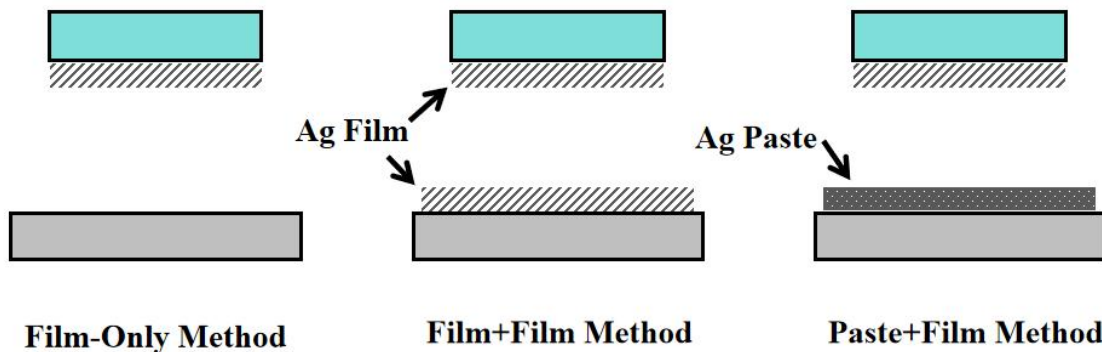


Fig. 13 Schematic illustration of three silver-sintering assembly methods: Film-Only, Film+Film, and Paste+Film.

The silver-sintering paste and the silver-sintering film were obtained from NBE Technologies, LLC, Blacksburg, VA, USA. Substrates were made of 1-mm thick alumina (96.0% Al_2O_3) that was e-beam evaporated with 100-nm thick titanium and 100-nm silver with PVD-250. Mechanical chips were made of a 1-mm thick silicon wafer evaporated

with the same metallization as the alumina substrate. The substrates are 6 mm × 6 mm while the mechanical chips are 3 mm × 3 mm.

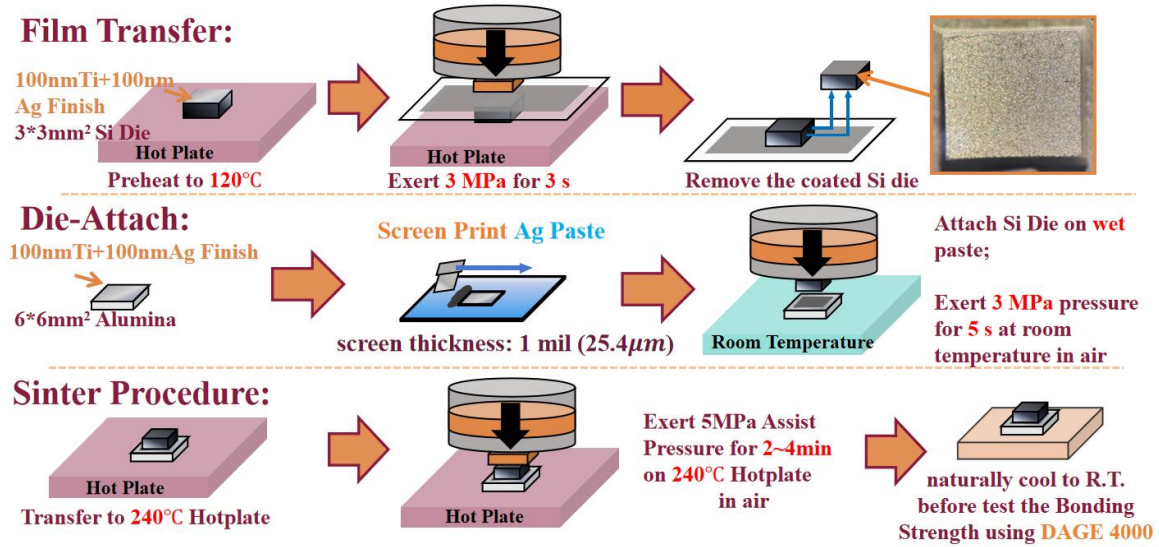


Fig. 14 Process flow of film transfer, paste printing and low-temperature sintering.

The sample made by Paste+Film method were fabricated following the workflow illustrated in Fig. 14. The process consisted of four key steps: (i) film transfer: the silver-sintering film was transferred to the backside of the die at 120 °C under 3 MPa for 3 seconds; (ii) paste printing: a thin layer (8-20 μm) of the silver paste was screen-printed on the substrate; (iii) die placement: the die with the film was mounted on the substrate with the paste at room temperature under 3 MPa for 5 s; and (iv) sintering: the sample was directly placed on a hotplate heated at a sintering temperature between 230 °C and 260 °C under 5 MPa pressure for 2 to 4 minutes. The die-shear strengths of bonded samples were measured at room temperature on Dage 4000 (Nordson).

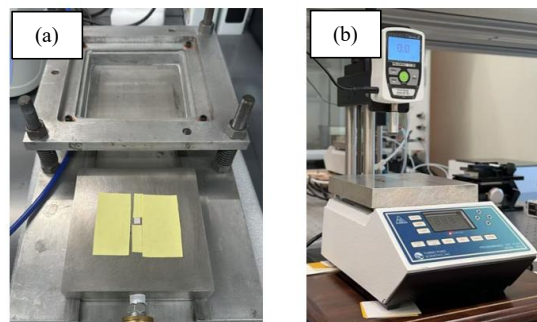


Fig. 15 (a)Screen printer for silver-sintering paste and (b) hotplate for film transfer and sintering.

The Film+Film Method, is performed with transferring a Ag-film to the substrate instead of printing the Ag-paste to it. And the Film-Only Method exert no extra modification expect necessary cleaning on the Ag-finished alumina substrates before the die-attach process. All screen printer and the hotplate used in both three set of experiment are the same and all shown in Fig. 15.

2.3 - Thickness Control of Silver Paste

In the Chapter 2.2, we recognized a need to establish a process that can quantitatively control the thickness of the silver-sintering paste. By using different thicknesses of steel mesh or polymer screen printing templates and adjusting the printing speed and the normal pressure applied to the template, different desired thicknesses of silver paste layers can be achieved.

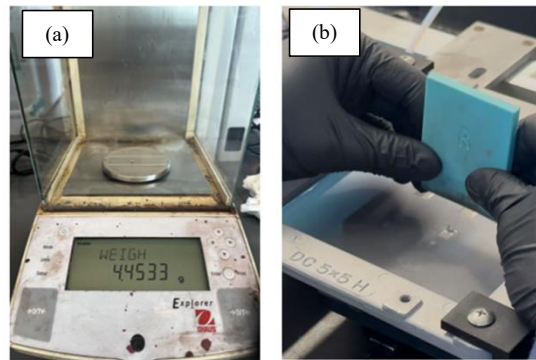


Fig. 16 (a) Analytical balance and (b) the screen printing process.

The simplest way to quantify the thickness h of the Ag-paste is calculate by the weight change of the substrate before and after the printing process shown in equation 2.3.

$$h = \frac{m}{\rho \cdot A} \quad (2.3)$$

Where A is the printing area (determined by the template opening area), m is the mass of the silver paste after printing (which can be obtained by weighing on an analytical balance in Fig. 16 (a)), and ρ is the silver paste density, referring to the data provided by NBE Tech. Using different types of printing templates (e.g. steel stencil and nylon screen of 1 mil and 2 mil), Ag-paste layer thicknesses ranging from about 10-50 μm could be obtained.

Chapter 3

Results and Discussion

3.1 - Electrical Test Result

After bonding the devices to a silver-treated substrate, electrical performance tests were performed to evaluate the functionality of Si and SiC Schottky diodes. The tests included measurements of forward conduction characteristics and reverse breakdown voltage, all performed at room temperature (25°C). As shown in Fig. 17, for a 3mm × 3mm SiC Schottky diode, there was no significant difference in turn-on voltage (V_{on}) and on-resistance (R_{on}) compared with the control group under an auxiliary pressure of 5 – 20 MPa, indicating that the electrical performance of the device was not damaged, also, all 4 test group perform normally blocking ability of 1.2 kV.

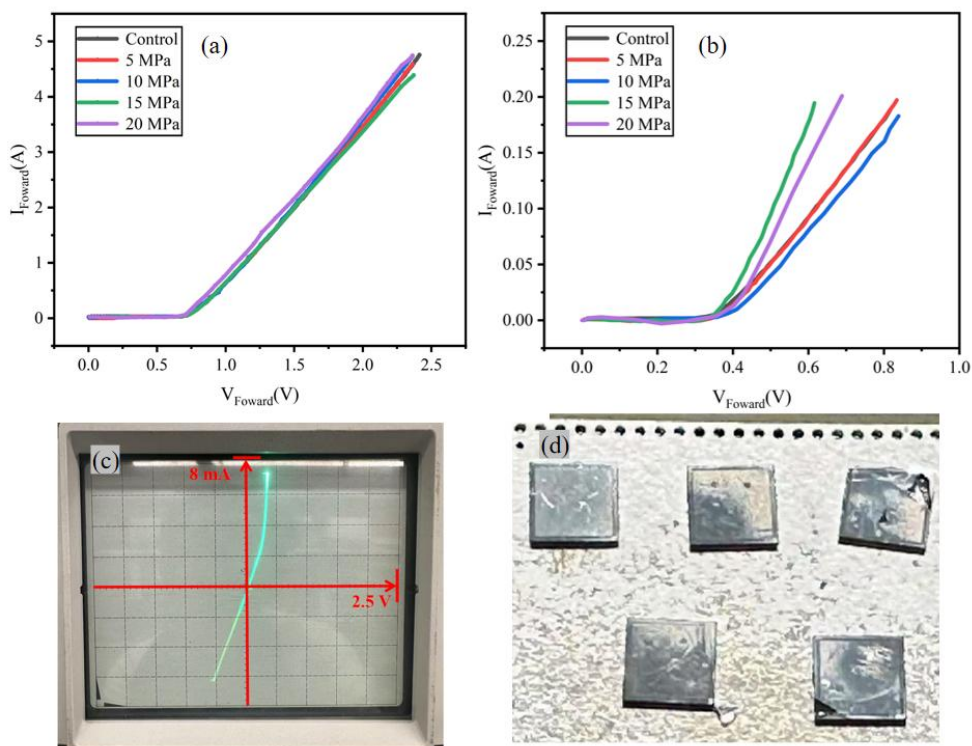


Fig. 17 (a) Forward characteristics of SiC Schottky diodes sintered under various assist pressure. (b) Forward characteristics of Si Schottky diodes sintered under various assist pressure. (c) An AC signal

showing the reverse conduction of a failed Si Schottky diode. (d) Photograph of Si Schottky diodes after pressure-assisted sintering of 20 MPa.

In contrast, a 6mm × 6mm Si Schottky diode showed a significant decrease in on-resistance under 15 MPa and 20 MPa pressures, while the on-resistance decreased abnormally. More seriously, in the sample with a pressure of 20 MPa, the device completely lost its cut-off capability during the reverse test and showed reverse conduction as shown in Fig. 17 (c). In response, we conducted five sets of repeated experiments and found that the chip failure rate under 20 MPa conditions was as high as 80%, and all failed samples appear reverse conducting and surface cracks.

We speculate that the failure of Si Schottky diodes is mainly due to chip cracking and partial penetration of the junction area caused by uneven pressure distribution because we observe the diode can conduct in the reverse direction as shown in Fig, 14 (c). Although a rubber buffer has been used in the pressurization system and a PTFE cushion has been added between the chip and the pressure head, the natural warping of the substrate itself causes the existing micro-cracks on the chip surface to further expand during the pressurization process and eventually penetrate the junction area, causing the device's electrical performance to deteriorate or even fail. The IGBT and MOSFET chips are usually in 6 mm × 6 mm sizes and larger, which points out that the necessity to lower the auxiliary pressure to a safety zone, for example, lower than 10 MPa for a 6 mm × 6 mm MOSFET chip.

3.2 - Evaluation of Paste+Film Method

The connection behavior of sintered silver film can be understood from two levels: microscopic diffusion mechanism (equation 3.1) and macroscopic bond strength expression (equation 3.2) :

$$\left(\frac{d\rho}{dt}\right)_{\text{constrained-film under uniaxial applied stress}} = C\left(\frac{P_a}{3} + \frac{\gamma}{3r}\right) \cdot \left(\frac{D_a}{k_B T}\right) \quad (3.1)$$

$$S_b = Q_b \cdot N_b = Q_b \cdot (R_a \cdot f(P_a)) \quad (3.2)$$

The equation 3.1 describes the volume fraction change rate of constrained silver film under uniaxial stress, and its main controlling factors include applied pressure P_a , interfacial energy tension γ , diffusion coefficient D_a , temperature T and silver particle radius r . This shows that to achieve sintering densification, sufficient driving force (such as pressure or high temperature or surface energy) must be provided to overcome interface barriers, especially when the material itself lacks fluidity.

The equation 3.2 is an empirical expression used in this study to describe the bonding strength S_b , where Q_b represents the quality per unit bonding area (such as the degree of diffusion channel patency and microstructural integrity), and N_b represents the total number or total area of bonding areas. The formula points out that the joint strength depends not only on the interface bonding quality of the material itself, but also on its effective diffusion area during the contact process, which is controlled by the roughness of the adhesion interface R_a and the impact of auxiliary pressure, expressed as a function of P_a .

These two formulas explain why it is difficult to achieve effective bonding of sintered silver film without a uniform auxiliary pressure from the two dimensions of physical driving force and interface structure, and provide a theoretical basis for the discussion of the relationship between pressure distribution and shear strength in the following text. Next, we will combine the experimental results to further analyze the sintering performance of silver film under different pressure conditions, and how to improve the joint quality by optimizing the pressurization method.

Compared with sintered silver paste, which can obtain high-strength silver joints through long-term sintering under extremely low or even no external pressure, sintered silver film must rely on auxiliary pressure to achieve reliable bonding. The reason is that the sintered silver film itself has no fluidity and high rigidity, resulting in insufficient contact area between it and the substrate. When the minimum temperature required for solid diffusion is reached, the number of effective diffusion channels at the interface is limited, which ultimately leads to extremely low shear strength, often less than 5 MPa.

Referring to the sintering parameters of Alpha Argomax® 8020 silver film on gold-finished PCB, if a shear strength of about 40 MPa is required, we usually need to sinter at 250°C and 10 MPa for 6 minutes, as shown in Fig. 18 [32]; if we want to compress the sintering time to 3 minutes, the auxiliary pressure needs to be increased to about 16.2 MPa to maintain the strength level.

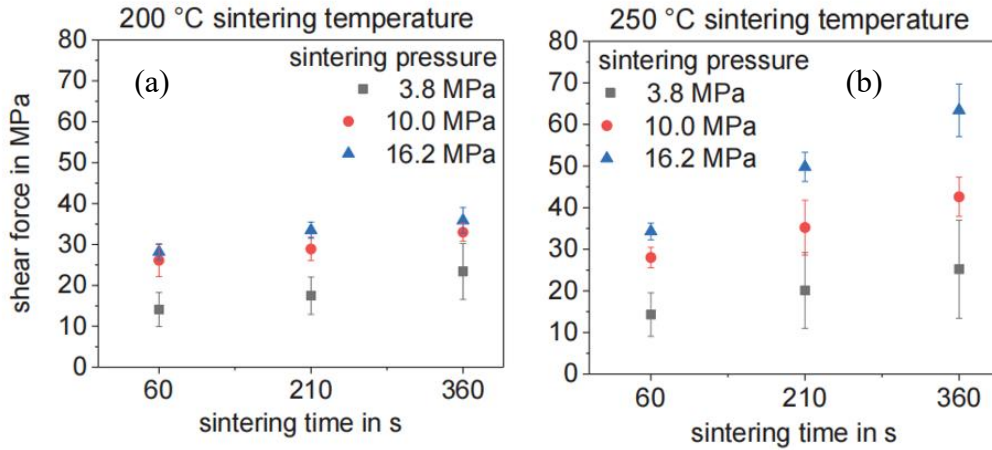


Fig. 18 Shear strength of sintered silver joints as a function of sintering time under different pressures at two temperatures: (a) 200 °C and (b) 250 °C [32].

With the data shown in Chapter 3.1, we conclude that the assist pressure should not exceed 15 MPa, and would be better if we could keep lowering the assist pressure, considering that a sintered silver material should function effectively on both Si and SiC chips without causing damage. Therefore, an assist pressure of 5 MPa was used for all methods (Paste+Film, Film+Film and Film-Only) in this study.

According to the data provided by NBE Tech, the elastic modulus of the sintered silver film is about 30 GPa, and the strain is about 0.017% when a stress of 5 MPa is applied; for a 50- μm -thick joint layer, the axial compression deformation is about 8.33 nm. According to the SLM result, the surface roughness of Ag-film before transfer is 0.430 μm , and 5.720 μm for substrate metallization, however, increases to 3.358 μm after the film transfer, on the edge this number even goes up to 5.121 μm . Which means we must have a buffer layer having a thickness greater than the surface roughness R_a of substrate

metallization and transferred Ag-film combined to fill up the hills and valley in the sintering surface.

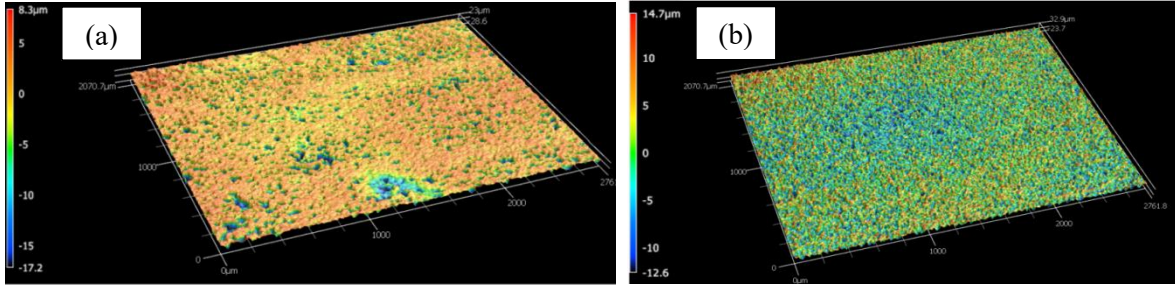


Fig. 19 The 3D-image of (a) The Ag-film after transferred on the chip-back metallization with $R_a=3.358 \mu\text{m}$ and (b) the substrate metallization with $R_a=5.720 \mu\text{m}$.

With the Paste+Film method, we first transfer the silver film to the chip, print a silver paste about $50 \mu\text{m}$ thick on the substrate with 2 mil steel stencil, then preheat on a 120°C hot plate for 30 seconds, and sinter at 250°C , 5 MPa for 10 minutes. The corresponding shear strengths of the two methods (Paste+Film and Film+Film) compared to control group (Film-Only) are shown in Fig. 20.

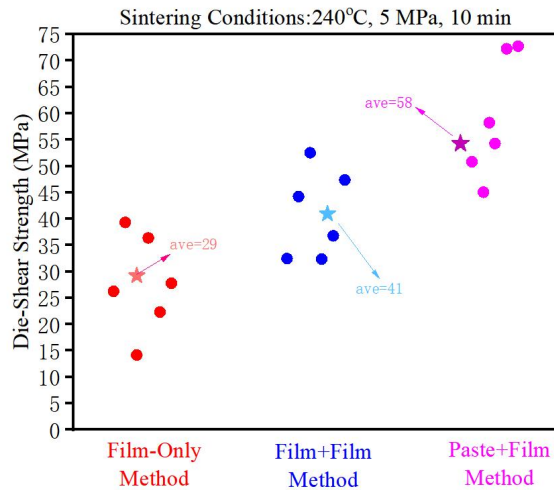


Fig. 20 Comparison of joint strength using different enhancement strategies: Film-Only, Film+Film, and Paste+Film methods.

It can be observed from these three sets of experimental data that, compared with a Film-Only, Film+Film and Paste+Film significantly enhance the mechanical strength of the joint. Among them, although the combination of silver paste and silver film requires additional preheating treatment, its improved shear strength is the most significant. Given

that the target bonding strength is 40 MPa, both the Paste+Film and Film+Film methods meet this standard. However, to further enhance die-attach throughput, we aim to reduce the sintering time to below 5 minutes. Therefore, we selected the Paste+Film method and focused on unlocking its potential to achieve a sintered Ag bond with die-shear strength exceeding 40 MPa within a 5-minute-process. The following section details our optimization strategies for this combined approach.

3.3 - Optimization of Paste+Film Method

In Chapter 3.2, we preliminarily concluded that the silver paste plus silver film (Paste+Film) method exhibits improved bonding strength and joint stability compared to the single-layer sintered silver film. Building on that analysis, Fig. 21 provides further insight into the underlying mechanism that contributes to this improvement, particularly in terms of solvent evaporation and die handling during assembly.

Unlike the issues observed in configurations where the solvent evaporates too quickly but lacks sufficient escape pathways, such as the condition illustrated in Fig. 22 (b), the Paste+Film structure introduces a more controlled and favorable drying behavior. As shown in Fig. 21, the porous microstructure of the Ag film provides multiple lateral evaporation paths for the organic solvent contained in the Ag paste. This allows the solvent to diffuse and gradually escape through the interconnected voids of the film, reducing the risk of rapid solvent accumulation at the interface that can compromise interfacial contact and bonding quality.

This "wet-attach" behavior presents an additional industrial advantage: when the Ag-film-coated chip is placed onto the paste-printed substrate, the residual solvent in the paste generates capillary adhesion forces. These forces temporarily hold the chip in place, effectively preventing it from shifting or sliding off before pressure is applied. This natural alignment stabilization during the pre-sintering stage simplifies handling and greatly reduces the likelihood of die displacement during substrate transfer or loading into the sintering fixture.

Such a self-aligning effect is especially beneficial for automated production lines where mechanical alignment precision and process robustness are critical. In essence, the Paste+Film configuration not only improves bonding integrity but also introduces passive mechanical benefits that enhance throughput and yield in volume manufacturing.

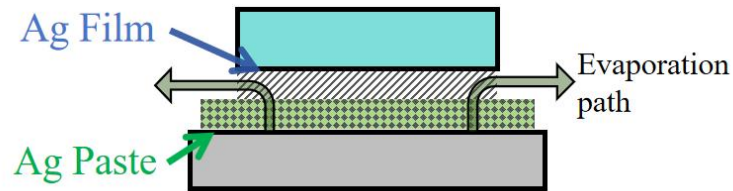


Fig. 21 Schematic illustration of solvent evaporation pathways in the Paste+Film structure.

Through the method introduced in Experimental to quantitatively control the thickness of the silver film, we used stencils and screens with thicknesses of 1 mil and 2 mil to make a series of paste+film samples with different Ag-paste thicknesses, with the hypothesis of if the paste is thin enough, the solvent in Ag-paste could evaporate through the porous structure of the Ag-film on chip-back metallization. So we want to attach the die without preheat and sinter directly after die-attach, the as-sinter die-shear strength is tested by DAGE 4000 afterwards. As shown in Fig. 22 (a), we found that when the silver paste thickness is controlled below 30 μm , the shear strength can achieve a satisfactory value (40 MPa) in 10min sintering. This is because as the proportion of silver paste in the bonding layer decreases, the total organic content also decreases. The organic content in the silver film usually does not exceed 5%. In order to further explore the optimal silver paste thickness, the shear strength under different silver paste thickness conditions was tested. The results are shown in the Fig. 22 (a) below, showing the relationship between silver paste thickness and final shear strength.

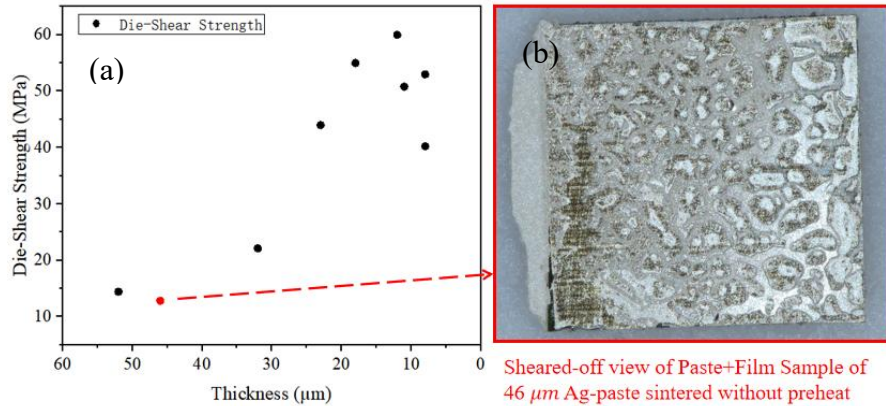


Fig. 22 (a) Die-shear strength of joints versus printed silver paste thicknesses in the Paste+Film method without preheat. (b) A failure interface of a paste+film sample with Ag-paste of 46 μm-thick

Based on the above experimental results, the Paste+Film process shows the best joint performance when the thickness of the sintered silver paste is controlled within the range of 10 μm to 20 μm. In order to achieve stable and controllable thickness in this range, a polymer screen with a wire diameter of 1 mil (about 25 μm) is required for silver paste printing.

Controlling the thickness of the silver paste between 10μm and 20μm has another significant advantage: in the bonding process for small-area chips of 6mm × 6mm and 3mm × 3mm, the preheating step can be omitted and the die-attach can be completed directly. The specific process is: first print the silver paste on the surface of the substrate, then mount the chip, and then directly sinter it on a 240°C hot stage. During this process, a small amount of white smoke often escapes. This phenomenon is mainly caused by the rapid evaporation of the residual solvent in the silver paste at high temperature and liquefaction when cooled.

After the chip was sintered, shear tests and fracture analysis showed that the process did not produce airways or large-sized holes caused by instantaneous solvent volatilization. This is mainly due to the porous structure of the sintered silver film itself, which can provide effective escape channels for the solvent in the early stage of sintering, and these channels will gradually close during the sintering process.

To further verify this mechanism, we observe the failure interface of the sheared-off sample with the Ag-paste thickness of $46\ \mu\text{m}$. The shear test results and fracture morphology show that in thicker silver pastes, the solvent is difficult to escape smoothly, resulting in a large number of cavitations at the sintering interface, which ultimately significantly reduces the shear strength of the joints.

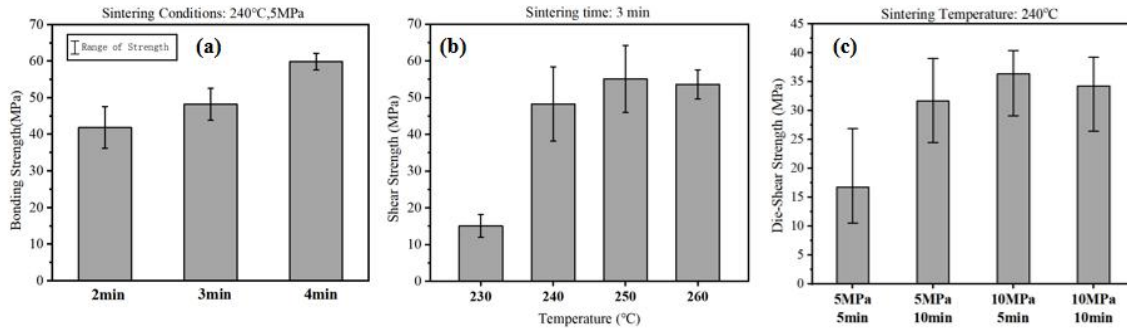


Fig. 23 Die-shear strength results of silver joints: (a) Time v.s. shear strength on Ag-Ag connection; (b) Temperature v.s. shear strength on Ag-Ag connection; (c) Different time and assist-pressure v.s. shear strength on Ag-Ag connection.

In Fig. 23, we present the bonding performance of the optimized method at both Au-Ag and Ag-Ag interfaces. Our objective is to achieve sufficient shear strength under the mildest possible conditions. For the Ag-Ag interface, we define 40 MPa as the threshold for “sufficient” bonding strength, while for the Au-Ag interface, the target is set at 25 MPa.

As shown in Fig. 23 (a), a minimum sintering temperature of $240\ ^\circ\text{C}$ is required to achieve complete bonding within 3 minutes. In Fig. 23 (b), we observe that a 3-minute sintering duration is the most efficient for reaching 40 MPa shear strength. According to the max-min distribution shown in the figure, the optimal parameters to achieve 40 MPa are a sintering temperature of $240\ ^\circ\text{C}$, 5 MPa assist pressure, and 3-minute duration. In Fig. 23 (c), we identify that for the Au-Ag interface, the optimal parameters to achieve 25 MPa shear strength are $240\ ^\circ\text{C}$, 10 MPa assist pressure, and 5-minute sintering duration.

Interestingly, in Fig. 23 (a), the average shear strength increases with sintering temperature from 230 °C to 250 °C, but slightly decreases at 260 °C. We attribute this to the fact that the measured values are approaching the upper detection limit (approximately 100 kg-f) of the DAGE 4000 tester, so the observed drop is likely due to sample size limitations rather than an actual reduction in strength. Additionally, the narrowing of the max–min range with increasing sintering temperature suggests that the bonding becomes more uniform. This indicates greater neck coarsening driven by stronger sintering forces, resulting in more consistent shear strength across samples.

Chapter 4

Application on Double-Side Cooled SiC MOSFET Half Bridge Module Packaging

4.1 - Chip and Module Structure Design

With the optimized Paste+Film method presented in Chapter 3, we propose an upgraded die-attach strategy for the double-side cooled SiC MOSFET half-bridge packaging scheme previously reported by Ding et al. [20]. In Ding's design, both the die-attach and post-attach processes were completed using a 15-minute sintering cycle with Ag paste shown in Fig. 24. However, applying a thick layer of Ag paste directly on the die-top metallization poses a significant risk of shorting the gate and source pads, potentially leading to device failure.

In contrast, the Paste+Film method enables the precise deposition of a small quantity of non-flowable Ag paste only on the intended die-top region, significantly reducing the likelihood of shorts. Furthermore, the solvent in the paste generates capillary forces at the interface, allowing the chip to temporarily adhere to the post before sintering. This pre-alignment effect helps prevent chip displacement during transfer or pressure-assisted sintering.

Most importantly, the Paste+Film method reduces the required assist pressure during bonding. This not only improves the compatibility of the process with brittle SiC devices but also mitigates the risk of chip cracking caused by uneven pressure distribution.

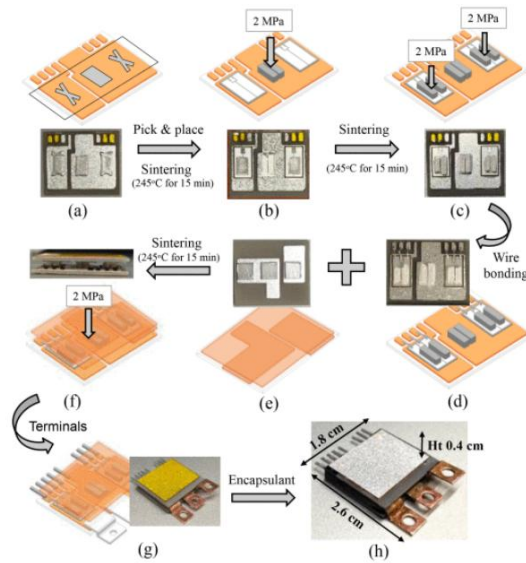


Fig. 24 Fabrication steps of the double-side half-bridge module [20].

The chip used in this study is a quarter unit of a gold-plated SiC MOSFET mechanical chip provided by Wolfspeed, with a size of approximately $2.5 \text{ mm} \times 2.5 \text{ mm}$, which is precisely cut by a diamond cutter. The upper and lower surfaces of the chip are metallized to form an Au finish. According to the designed power module packaging structure, the chip needs to be pre-sintered to a silver-plated ceramic substrate, and a silver post is installed on its top as a subsequent lead connection structure.

The silver post used is a plastic structure with a size of approximately $1.5 \text{ mm} \times 2.0 \text{ mm}$. It is made of nano-silver paste and pressureless sintering in a special mold [20], and has certain mechanical strength and shape stability. In order to enable the chip and the post to be bonded directly on the heating plate at the set sintering temperature, the silver-sintering film needs to be transferred to the bottom of the chip and the post respectively before formal sintering to form a dry and uniform initial bonding interface (as shown in Fig. 26).

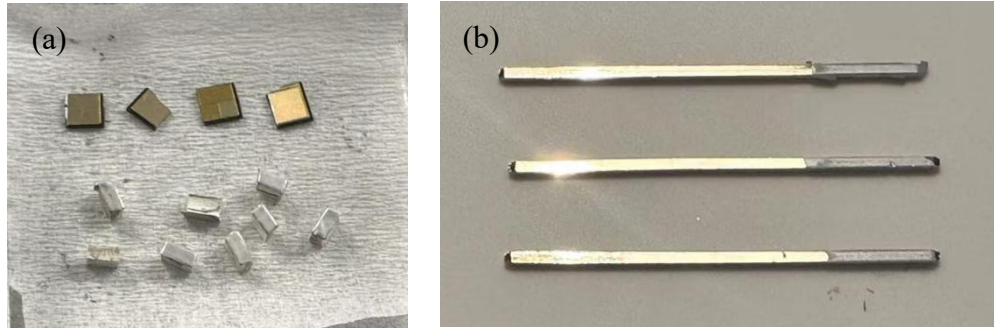


Fig. 26 (a) Au finished die and deformable silver posts and (b) Au finished pins after film transfer.

4.2 - Process Flow for Die, Post, and Pin Attach

In order to test the shear strength of the silver post and the chip (die) and reduce material waste, the two need to be sintered to the silver-plated ceramic substrate mentioned above for testing the sintering performance of the silver-silver interface through the Paste+Film process. Subsequently, the shear strength test is performed using the DAGE 4000 to verify the effect of the sintered silver bonding.

For the sintering connection between the SiC MOSFET chip with a gold (Au finish) metallized surface and the silver-finished alumina ceramic substrate, sintering is completed at 240°C for 5 minutes with an auxiliary pressure of 10 MPa.

Before sintering the silver post to the top of the gold-finished chip, the silver post needs to be bonded to the silver-finished ceramic substrate using the Paste+Film process, and the feasibility of applying auxiliary pressure in the subsequent chip sintering is confirmed by the DAGE 4000 shear strength test. In particular, it is necessary to ensure that the pressure applied by the pressure head can be vertically and evenly transmitted to the sintering interface.

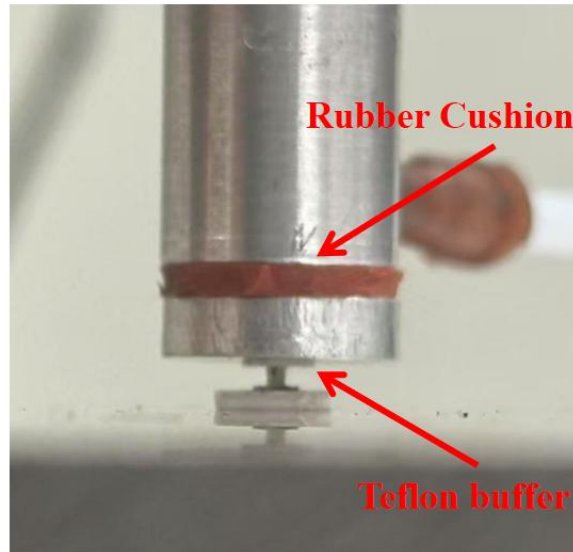


Fig. 27 Sintering configuration showing the use of rubber pad and Teflon cushion for uniform pressure distribution during bonding of silver post to Au-finished chip.

As shown in Figure 27, to ensure uniform pressure distribution, a 1 mm thick orange rubber pad is used during the sintering process to help distribute the pressure evenly in the sintering area, and a 100 μm thick Teflon cushion is superimposed to avoid direct contact between the Ag-post and the pressure head.

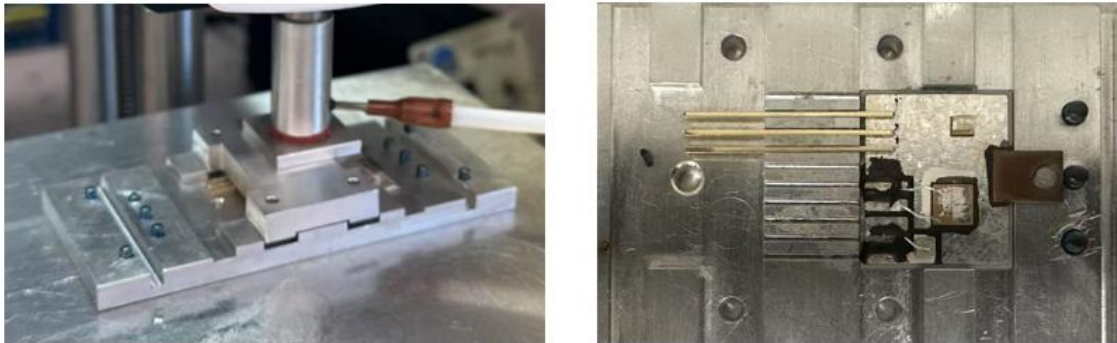


Fig. 28 Sintering setup for simultaneous bonding of three Au-finished pins using a customized fixture and aluminum pressure-spreading block.

For the bonding of gold-finished pins, due to their small cross-sectional area (approximately $0.62\text{ mm} \times 0.65\text{ mm}$), applying pressure directly through the pressure head is prone to uneven distribution. Therefore, as shown in the Fig. 28, a special fixture is used to fix the three pins, and an aluminum block is added between the pressure head and the fixture when applying pressure, so that the pressure can be distributed on the

three pins as even as possible, thereby achieving a one-time sintering connection of the three pins. However, due to the uneven pressure distribution across the three pins, it is necessary to increase the assist pressure and extend the sintering time to compensate.

4.3 - Shear Strength Evaluation

As shown in Fig. 29, both the chip-to-substrate and post-to-substrate joints were fabricated using the Paste+Film method under a sintering condition of 10 MPa for 5 minutes (or 5 MPa for 10 minutes) at 240 °C. The measured average shear strength was 34.5 MPa for the chip bond and 26.3 MPa for the post bond. For the pin-to-substrate joints, a clamping fixture with a 25 lbs (11.3 kg-f) auxiliary force was applied to ensure uniform pressure distribution. Sintering was performed for 20 minutes at 240 °C, resulting in shear strengths of 25 MPa, 30 MPa, and 51 MPa, respectively. These results suggest that the Paste+Film method is not only effective for die-attach but also adaptable to post-attach and pin-attach applications.

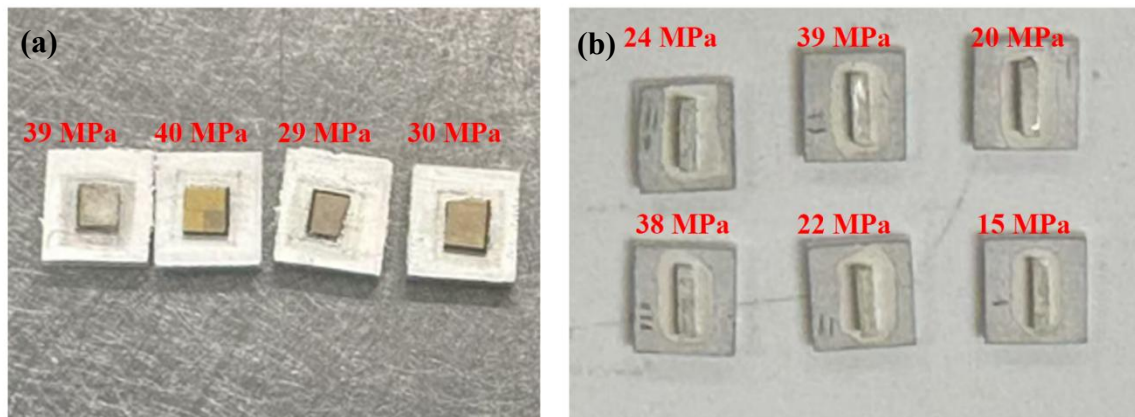


Fig. 29 Die-shear strength of (a) Au-finished SiC die and deformable silver posts and (b) Au-finished pins after silver film transfer.

For the double-side cooled module, we referred to C. Ding et al.'s work to estimate the total sintering time required for each bondline when using the Paste+Film method. The results are summarized in Table 6 [20]. To evaluate the influence of the Kirkendall effect at the Au/Ag interface, we conducted post-sintering annealing experiments. After assembling all components onto Ag-finished substrates, the samples were annealed on a

240°C hotplate for 30 minutes and 60 minutes, respectively. The corresponding shear strengths were evaluated and presented in Fig. 31.

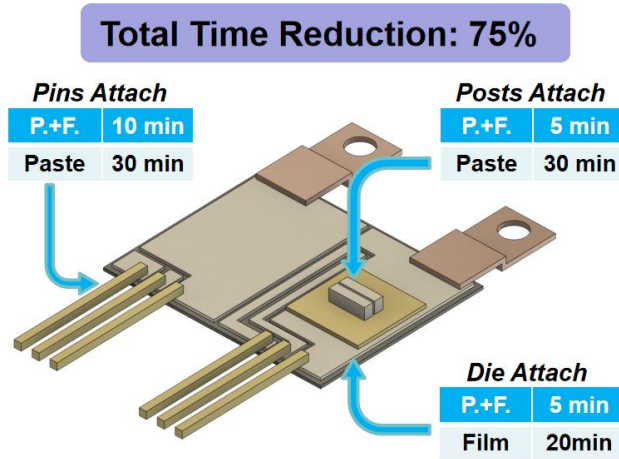


Fig. 30 Comparison of total sintering time required for conventional silver materials versus the Paste+Film method in a double-sided cooled SiC MOSFET module.

Overall, the Paste+Film method significantly simplifies the fabrication process of double-side cooled power modules. For die-attach applications, it reduces the required auxiliary pressure to a gentle 5 MPa compared to film-only sintering, while eliminating the need for pre-drying steps required by silver paste. For instance, commercial pastes like those from Heraeus typically require 20 minutes of pre-drying. Moreover, due to the large temperature gap between drying and sintering stages, additional thermal equipment is often needed in industrial settings, increasing both cost and process complexity.

For post-attach structures, the Paste+Film method provides mechanical protection to brittle dies, helping to prevent cracks caused by uneven pressure on the top surface. For pin-attach, the Paste+Film method improves yield by avoiding excessive paste usage. Since the three pins are typically placed in close proximity, traditional paste-only processes require a large printed area to ensure bonding, whereas Paste+Film allows more targeted material usage and reduces silver waste.

Posts-Substrate	Posts-Die	Die-Substrate	Pins-substrates
40 min	70 min	80 min	30 min

Table. 7 Total time on 240°C hotplate for each bondline in double-side cooled modules [20].

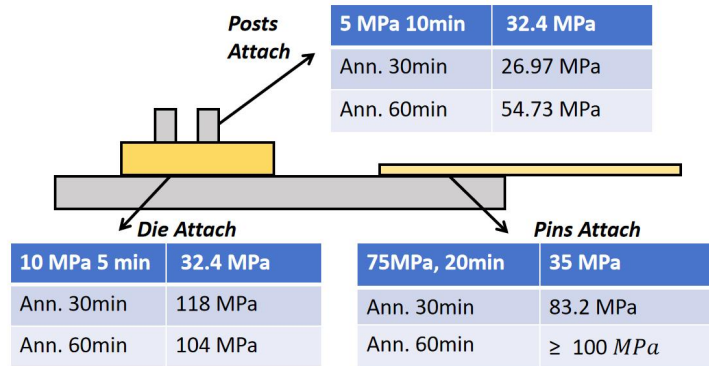


Fig. 31 Evolution of shear strength of sintered joints between silver posts and Au-finished SiC die as a function of sintering time at 240°C on hotplate.

From the above discussion, it becomes clear that implementing the Paste+Film method across all critical bonding steps—including die-attach, pin-attach, and post-attach—offers significant advantages in both process efficiency and reliability. By adopting this approach, the total processing time can be reduced by up to 75% compared to traditional silver-sintering methods (shown in Fig. 30), primarily due to the elimination of extended pre-drying and long sintering durations.

Moreover, the Paste+Film configuration minimizes the risk of short circuits at the die-top by allowing precise control over the paste deposition area. Unlike conventional paste application, which may overflow and bridge adjacent pads (such as gate and source), the non-flowable nature of the paste and the spatial confinement of the Ag film ensure clean separation between electrodes. In addition, the capillary forces induced by the solvent at the interface temporarily secure the chip in place prior to sintering, effectively preventing misalignment or sliding during module transfer or pressure application.

Most importantly, the Paste+Film method significantly reduces the assist pressure required for bonding. In conventional processes, pressures as high as 20 MPa are often necessary to achieve sufficient bonding strength. With Paste+Film, the assist pressure can

be reliably lowered to 10 MPa or even 5 MPa without compromising mechanical integrity. This substantial reduction in mechanical stress not only enhances yield but also greatly decreases the risk of chip cracking, especially for brittle SiC devices with strict tolerances on stress and alignment.

In summary, the Paste+Film method offers a robust, efficient, and reliable solution for next-generation power module packaging, particularly suited for double-sided cooled SiC MOSFET structures.

Chapter 5

Summary and Future Works

5.1 - Summary

In this study, a new sintering scheme combining silver paste and silver film, namely Paste+Film method, was proposed to solve the problems of high auxiliary pressure, long sintering time and high process complexity in the traditional silver-sintering process in power electronic module packaging. Through systematic experimental verification, the Paste+Film process can form a high-density silver connection interface with a shear strength exceeding 40 MPa under a mild pressure of only 5 MPa in a short sintering process of 3-5 minutes in Ag-Ag connection and 25 MPa in Au-Ag connection with assist pressure of 10 MPa in 5 minutes. Compared with the traditional method of using silver paste [20] or silver film alone [32], the Paste+Film process effectively compensates for the hole problem caused by solvent volatilization in the silver paste process, while avoiding the risk of chip damage caused by high-pressure compaction in the silver film process, providing a new way for efficient and reliable power module packaging.

In practical application, this study applies the Paste+Film process to the packaging and manufacturing process of double-sided cooling SiC MOSFET half-bridge modules, covering multiple key connection links such as die-attach, post-attach and pin-attach. Experiments show that this process not only successfully reduces the sintering auxiliary pressure in chip connection and avoids the problem of cracks in brittle chips due to uneven force, but also significantly reduces the waste of silver materials during pin connection and improves the overall process yield. Compared with the traditional silver-sintering process, the Paste+Film method effectively shortens the total sintering time of each connection interface, shortens the overall packaging cycle by about 75%, significantly improves manufacturing efficiency, and reduces equipment and energy consumption costs.

From the perspective of reliability, after subsequent annealing treatment and shear strength test verification, the silver connection layer prepared by the Paste+Film process shows good mechanical strength and thermal stability, which can meet the long-term application requirements in high power density and high temperature environments. In summary, the Paste+Film method greatly simplifies the packaging process while ensuring the connection quality, improves the manufacturability and reliability of power module packaging, and has broad application prospects, especially suitable for the module packaging development needs of new generation wide band-gap semiconductor devices such as SiC and GaN.

5.2 - Future Works

Although preliminary results have verified the potential of this method in terms of process adaptability and efficiency, a series of in-depth experiments are still needed to systematically explore the performance characteristics of the Paste+Film structure under actual working conditions and its connection mechanism. Subsequent research recommendations include the following aspects:

(a) Measure the electrical conductivity, thermal conductivity and thermal expansion coefficient (CTE) of the Paste+Film joint, and compare and analyze the performance of the joint prepared with traditional silver film (Film-Only) or silver paste (Paste-Only) to clarify its material performance advantages;

(b) Perform thermal cycle and power cycle tests on the Paste+Film joint structure to evaluate its thermal-mechanical reliability under long-term service environment;

(c) Use transmission electron microscopy (TEM) to characterize the microstructure of the gold-silver interface in the Paste+Film joint to check whether there is a risk of interface voids such as the Kirkendall effect, and further optimize the sintering process parameters accordingly;

(d) Use scanning electron microscopy (SEM) to observe the cross-sectional morphology of the Paste+Film joint, and use ImageJ software to quantitatively analyze the pore

distribution parallel to and perpendicular to the bonding interface to further verify the improvement effect of the Paste+Film structure in terms of interface contact area.

The above research will help to further improve the theoretical understanding and engineering applicability of the Paste+Film process, and lay the foundation for its large-scale application in high-performance power modules.

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