

# **Advanced Control Schemes for Voltage Regulators**

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Kisun Lee

## (ABSTRACT)

The microprocessor faces a big challenge of heat dissipation. In order to enhance the performance of the microprocessor without increasing the heat dissipation, the leading microprocessor company, Intel, uses several methods to reduce the power consumption. These methods include enhanced sleep states control, the Speed Step technology, and multi-core architecture. These are closely related to the Voltage Regulator (VR), a dedicated power supply for the microprocessor and its control method. The speed of the VR control system should be high in order to meet the stringent load-line requirements with the high current and high  $di/dt$ , otherwise, a lot of decoupling capacitors are necessary. Capacitors make the VR cost and size higher. Therefore, the VR control method is very important. This dissertation discusses the way to increase the speed of VR without degrading other functions, such as the system efficiency, and the required control functions (AVP, current sharing and interleaving).

The easiest way to increase the speed of the VR is to increase the switching frequency. However, higher switching frequency results in system efficiency degradation. This paper uses two approaches to deal with this issue. The first one is the architecture approach. The other is the fast transient control approach.

For the architecture approach, a two-stage architecture is chosen. It is already shown that with a two-stage architecture, the switching frequency of the second stage can be increased, while keeping the same system efficiency. Therefore with the two-stage architecture, a high performance VR can be easily implemented. However, the light-load efficiency of two-stage architecture is not good because the bus voltage is designed for the full-load efficiency which is not optimized for the light load. The light-load efficiency is also an important factor and it should be maximized because it is related to the battery life of mobile application or the energy utilization. Therefore, Adaptive Bus Voltage

Positioning (ABVP) control has been proposed. By adaptively adjusting the bus voltage according to the load current, the system efficiency can be optimized for whole load range.

The bus voltage rate of change is determined by the first stage bandwidth. In order to maintain regulation during a fast dynamic load, the first stage bandwidth should be high. However, it is observed from hardware when the first stage bandwidth is higher, the ABVP system can become unstable. To get a stable system, the first stage bandwidth is often designed to be slow which causes poor ABVP dynamic response. The large number of bus capacitors necessary for this also increases the size and cost. In this dissertation, in order to raise the first stage bandwidth, a stability analysis is performed. The instability loop ( $T_{ABVP}$ ) is identified, and a small signal model to predict this loop is suggested.  $T_{ABVP}$  is related to the first stage bandwidth. With the higher first stage bandwidth, the peak magnitude of  $T_{ABVP}$  is larger. When the peak magnitude of  $T_{ABVP}$  touches 0dB, the system becomes unstable. Two solutions are proposed to reduce this  $T_{ABVP}$  magnitude without decreasing the first stage bandwidth. One method is to increase the feedforward gain and the other approach is to use a low pass filter. With these strategies, the ABVP system can be designed to be stable while pushing first stage bandwidth as high as possible. The ABVP-AVP system and its design are verified with hardware.

For the fast transient control approach hysteretic control is chosen because of its fast transient and high light-load efficiency with DCM operation. However, in order to use the hysteretic control method for multiphase VR applications interleaving must be implemented. In this dissertation, a multiphase hysteretic control method is proposed which can achieve interleaving without losing its benefits. Using the phase locked loop (PLL), this control method locks the phase and frequency of the duty cycles to the reference clocks by modifying the size of the hysteretic band, to say, hysteretic band width. By phase shifting the reference clocks, interleaving can be achieved under steady state. During the load transient, the system loses the phase-locking function due to the slow hysteretic band width changing loop, and the system then reacts quickly to the load change without the interruption from the phase locking function (or the interleaving function).

The proposed hysteretic control method consists of two loops, the fast hysteretic control loop and the slow hysteretic band width changing loop. These two nonlinear loops are difficult to model and analyze together. Therefore, assuming these two loops can be separated because of the speed difference, the phase plane model is used for the fast hysteretic control loop and the sampled data model is then used for the slow hysteretic band width changing loop. With these models, the proposed hysteretic control method can be analyzed and properly designed. However, if the transient occurs before the slow hysteretic band width changing loop settles down, the transient may start with the large hysteretic band width and the output voltage peak can exceed the specification. To prevent this, a hysteretic band width limiter is inserted.

With the hardware, the proposed hysteretic control method and its design are verified. A two-phase VR with 300kHz switching frequency is built and the output capacitance required is only 860 $\mu$ F comparing to 1600 $\mu$ F output capacitance with the 50kHz bandwidth linear control method. That is about 46% capacitor reduction.

The proposed hysteretic control method saturates the controller during the transient and the transient peak voltage is determined by the power stage parameters, the inductance and the output capacitors. By decreasing the inductance, the output capacitors are reduced. However, small inductance results in the low efficiency. In order to resolve this, the coupled inductor is used. With the coupled inductor, the transient inductance can be reduced with the same steady state inductance. Therefore, the transient speed can be faster without lowering down the system efficiency. The proposed hysteretic control method with the coupled inductor can be implemented using the DCR current sensing network.

A two-phase VR with the proposed hysteretic control and the coupled inductor is built and the output capacitance is only 660 $\mu$ F comparing to 860 $\mu$ F output capacitance with the proposed hysteretic control only. A 23% capacitor reduction is achieved. And compared to the 50kHz bandwidth linear control method, a 60% capacitor reduction is achieved.

*To my parents*

*Soon-Hyung Lee*  
*Young-Hae Park*



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## Chapter 1. Introduction

### 1.1. Research Background

#### 1.1.1. Microprocessors

The microprocessor (Central Processing Unit: CPU) is widely used in many applications such as computer systems, embedded systems, and handheld devices. Those applications demand good performance of a microprocessor with limited size because customers want smaller systems. Thus, more transistors are integrated in the microprocessor. Since 1971 when the first microprocessor, the Intel's 4-bit 4004 chipset, was released, transistors have been integrated more and more in accordance with Moore's Law. Figure 1.1 shows the historical data of the transistor number integrated in the Intel's microprocessor [1]. The Dual-Core Itanium 2 Processor, which was released in 2006, has more than a billion transistors in it and it is about a million times more than the first 4004 microprocessor.

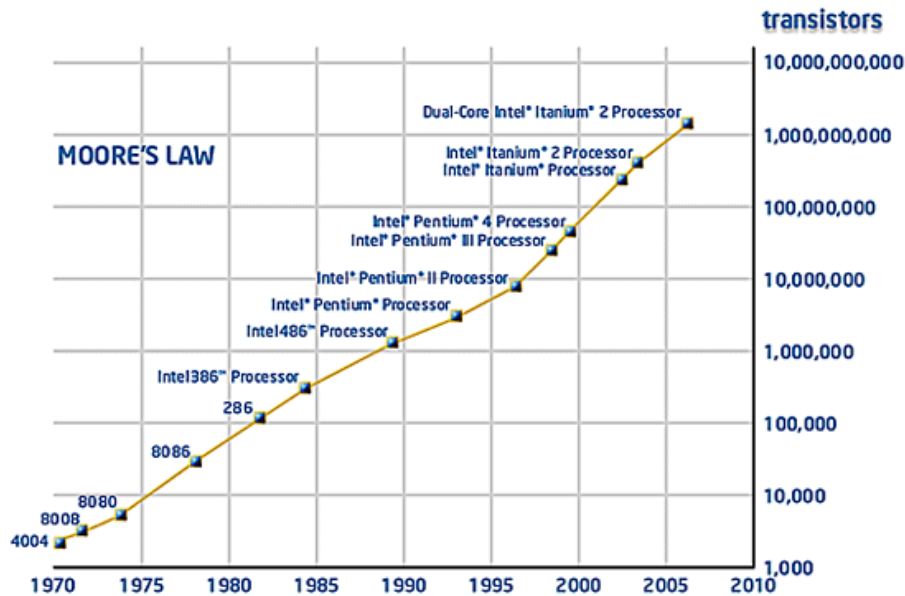


Figure 1.1 The number of transistors integrated on the die for Intel microprocessors [1].

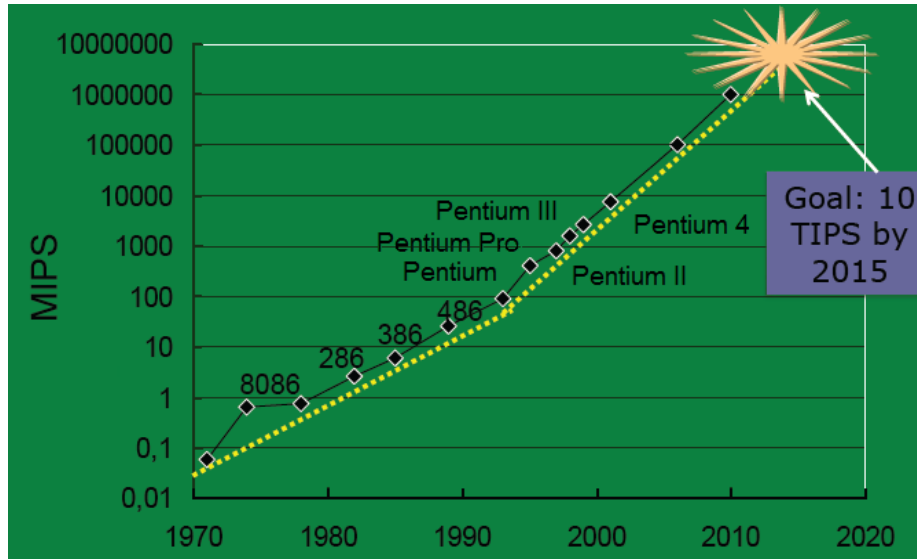


Figure 1.2 The speed of Intel microprocessors [2].

With more transistors integrated in the microprocessor, better performance is achieved. Figure 1.2 shows the speed of Intel microprocessors [2]. Million instructions per second (MIPS) is a measure of a computer's process speed. Intel targets to build the microprocessor with ten trillion instructions per second (TIPS) by 2015; this is about ten billion times faster than the first 4004 microprocessor.

The microprocessors consume more power when they have a larger number of transistors and a higher operating speed [2, 3]. With the single microprocessor, the power consumption is roughly proportional to the clock frequency and the square of the core voltage [4][5], so that

$$P_{CPU} \propto C \cdot V_{CC}^2 \cdot f \quad (1.1)$$

where,  $P_{CPU}$  is the power consumption by the microprocessor,  $C$  is the lumped capacitance of all the logic gates,  $V_{CC}$  is the core voltage and  $f$  is the clock frequency of the microprocessor. In order to get higher operating speed, the clock frequency should be higher and the power consumption increases accordingly. Moreover, the scaling of the microprocessor will increase the capacitance  $C$ , and the power consumption increases as well. This power consumption eventually results in the large heat dissipation, and this is a huge challenge for the thermal management of the microprocessors. Furthermore, this heat dissipation is bad for the system energy utilization. For the mobile microprocessor, this means a reduced battery running time which is a very important factor for battery operated devices.



Intel uses several methods to enhance performance without increasing power consumption in the latest microprocessors [3].

In order to save leakage power, they use enhanced sleep states control and dynamic cache sizing. When the computer is in the hibernate mode or when there is no software running, the operating system (OS) sends a signal through the Advanced Configuration and Power Interface (ACPI), allowing the system to go into the sleep mode. Then the cache size is reduced and several unused chipsets are turned off in order to reduce the leakage power. In the latest microprocessors, there are different levels of sleep modes, and each of the states represents a more efficient way to save power. The expense is a longer time to bring the system back into operational mode.

In order to control the active power consumption, a technique based on Intel's Speed Step technology is used. The system defines a set of working points, and each one has a different frequency and voltage; that is, a different power consumption. The OS uses the ACPIs to define at what working point it works in order to strike a balance between the performance needs and the dynamic power consumption. Figure 1.3 shows how the system moves from one working point to another. In order to move from a "high" working point to lower one, the system can switch the clock frequency almost immediately, but it will take the system some time to lower the voltage because the output voltage is moved not by the microprocessor, but by the voltage regulator, which is the dedicated power supply for the microprocessor. When moving from a low working point to a higher one, the system needs to increase the voltage first and only then the frequency can be increased [4][5][6]. With these technologies, the average power consumption can be saved.

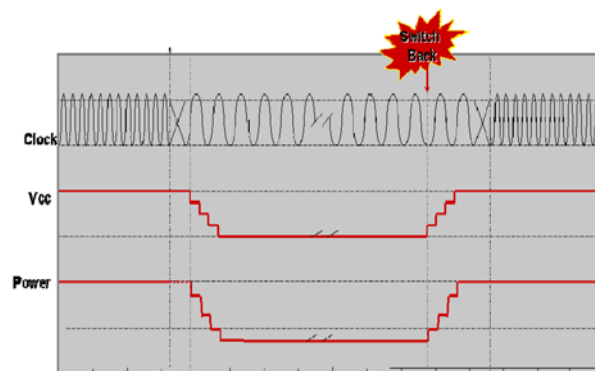


Figure 1.3 Changing working point in Intel Core Duo processor [3].

Intel not only uses the technologies mentioned above, but also changes the microprocessor structure from a single core to the Core Multi-Processor (CMP); i.e. multiple cores on a die which is also called Dual-Core or Quad-Core. Figure 1.4 shows the benefits of the Dual-Core microprocessor [2]. Assuming the maximum performance of the single core is 1.00x with the power consumption 1.00x, in order to increase the performance to 1.13x, the clock frequency is increased by 20% and the supply voltage ( $V_{CC}$ ) should be increased proportionally. The power consumption is increased as 1.73x ( $\approx 1.2^3$ ) according to the equation 1.1. Meanwhile, if the clock frequency is reduced by 20%, the supply voltage can be reduced by 20% and the power consumption becomes 0.51x ( $\approx 0.8^3$ ) with 0.87x performance. The Dual-Core Processor uses two under-clocked cores like those in Figure 1.5, and the performance is increased to 1.73x, with the almost same power consumption. CMP can definitely increase the performance without the power consumption increase, but the supply voltage is lowered down and the processors demand more current. To get more performance with the same power consumption, more cores on the die are necessary; the Dual-Core was released in 2006, Quad-Core was released in 2007, and 4 core+ will be introduced in 2008 [3]. This will result in a much lower supply voltage, and the processors will demand more current.

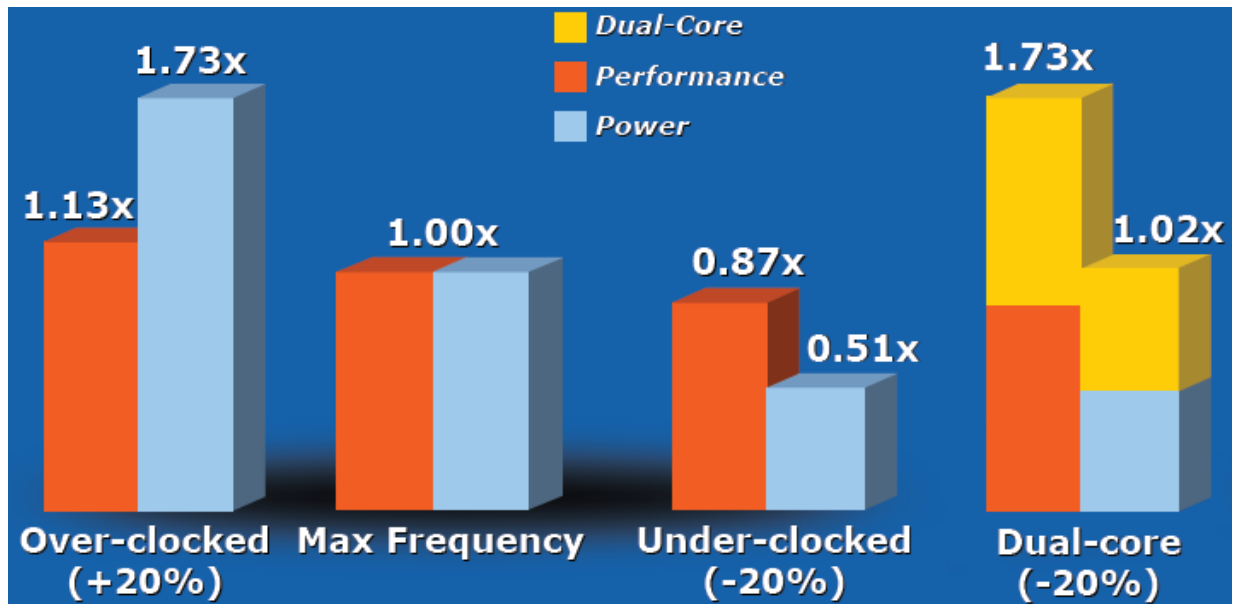


Figure 1.4 Relative microprocessor performance and power consumption [2].

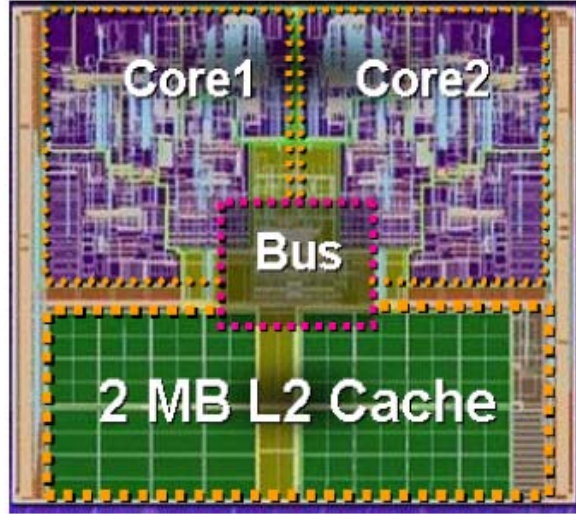


Figure 1.5 Intel Core Duo processor floor plan [3].

Before the year 2006, the processor clock frequency had been increased over time, the power consumption had been increased accordingly, and the supply voltage had been reduced while the current demand has been increased [7][8][21][22]. After introducing the CMP structure in 2006, the supply voltage has also continued to be reduced and the current demand has kept increasing but the power consumption has been only slightly increasing. Figure 1.6 shows the power road map of Intel’s microprocessors [9][10][11][12][13][14][15][16][17][18][19][20]. In the near future, the voltage will be under 1V and the current demand will be larger than 140A.

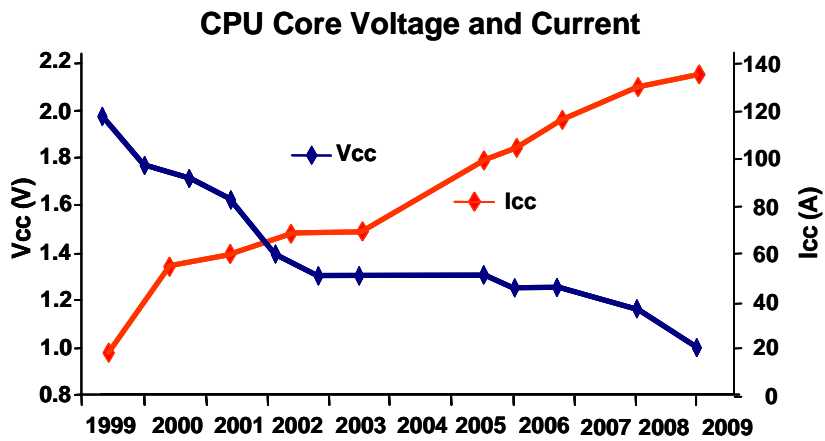


Figure 1.6 Intel microprocessors’ power road map.

### 1.1.2. Voltage Regulators

In order to supply the power to the microprocessor with high current and low voltage demand, a dedicated power supply, the voltage regulator (VR), is used. Figure 1.7 shows the desktop motherboards for Intel processors and the marked areas indicate VRs. Figure 1.7 (a) shows the old motherboard for the Intel Pentium processor, which was released in 1994, and (b) shows the latest desktop motherboard for the Intel Core™2 Duo processor. The interleaved multiphase synchronous Buck converter is generally used as today's VR (Figure 1.8) [27][28][29][30][31][32].

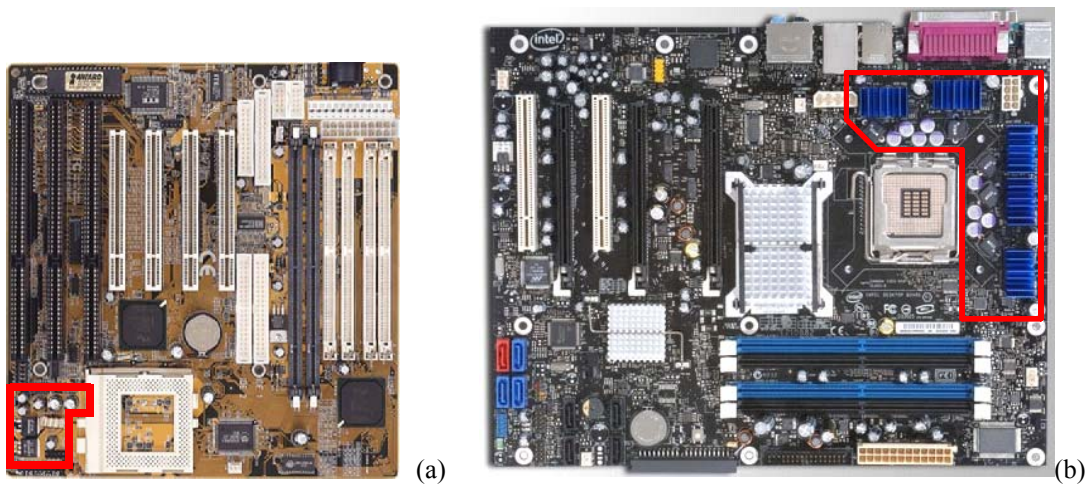


Figure 1.7 Motherboards for Intel processors and VR (a) for Intel Pentium processor (b) for Intel Core™2 Duo processor.

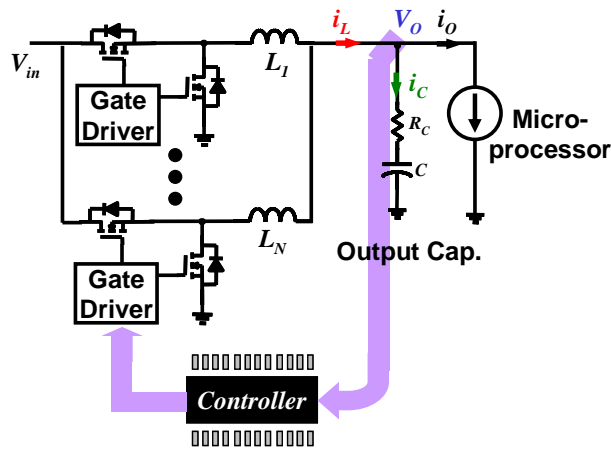


Figure 1.8 An interleaved multiphase synchronous Buck converter for VR.

The current demand of the Intel Pentium processor was approximately 10A and the single phase VR was used as shown in Figure 1.7 (a). The VR accounts for only 2% of the motherboard space. However, with a larger CPU current, VR is used for a larger number of phases. With today's technology, the VR for the desktop computer system delivers about 25A current per phase with around a 300kHz switching frequency. Therefore, five or six phases are used to supply up to 125A current for the latest microprocessor, like the one in Figure 1.7 (b). The greater number of phases means there are a larger number of components. This VR occupies almost 14% of the motherboard space; it has been observed that the size of the VR has increased with the larger phase number due to the increased CPU current demand. In the future, it is expected that the VR phase number will be much larger due to the larger current demand from the microprocessor and the size of VR will increase more, while the users want a smaller system size. Therefore, the size of VR is one of the big challenges in future design.

Today's VR faces a stringent challenge, not only by the high current but also by the strict transient response requirement. The microprocessor performs as a fast dynamic load with high  $di/dt$  current slew rate like the one in Figure 1.9. In the Intel VRD 11.0 specification, the maximum current step is 95A with 50ns transient time, and  $di/dt$  is almost 190A/us at the CPU socket. Figure 1.10 shows the VR output load line from the Intel VRD 11.0 specification [16]. The vertical axis is the VR output voltage deviation from the Voltage Identification ( $VID$ : A code supplied by the processor that determines the reference output voltage), and the horizontal axis is the CPU current ( $I_{CC}$ ). The  $V_{max}$  load line is defined by Equation (1.2),

$$V_{CC} = VID - R_{LL} \cdot I_{CC} \quad (1.2)$$

where,  $R_{LL}$  is the load-line impedance and there is a tolerance band. The VR output voltage should be within this load-line band for both static and transient operation.

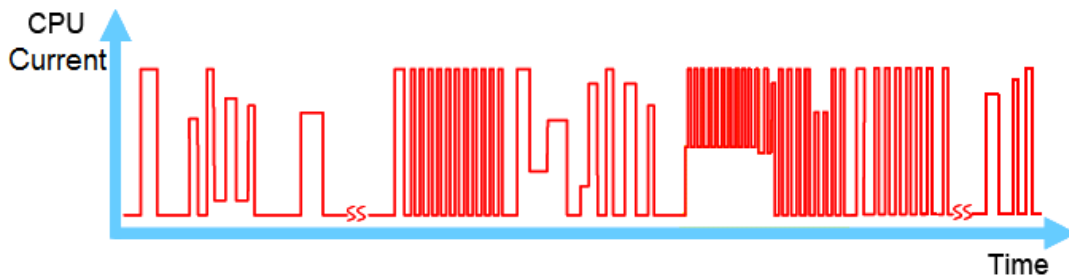


Figure 1.9 An example of CPU current profile.

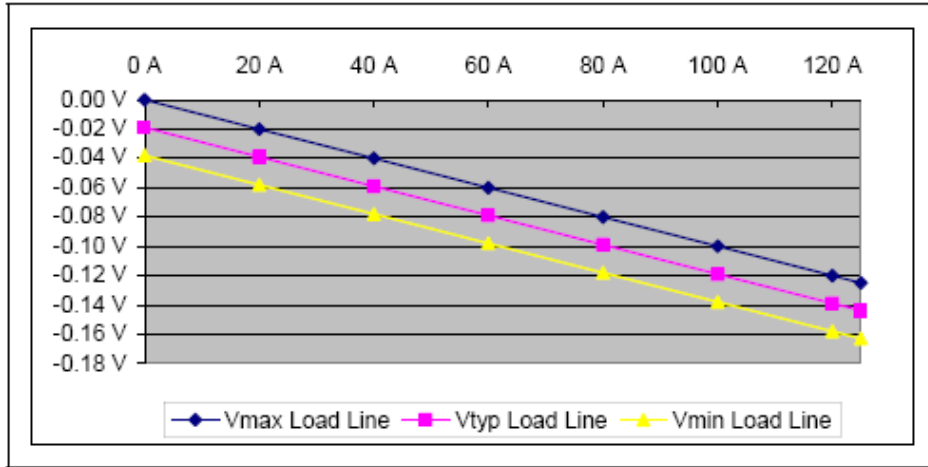


Figure 1.10 Load-line specifications from Intel VRD 11.0.

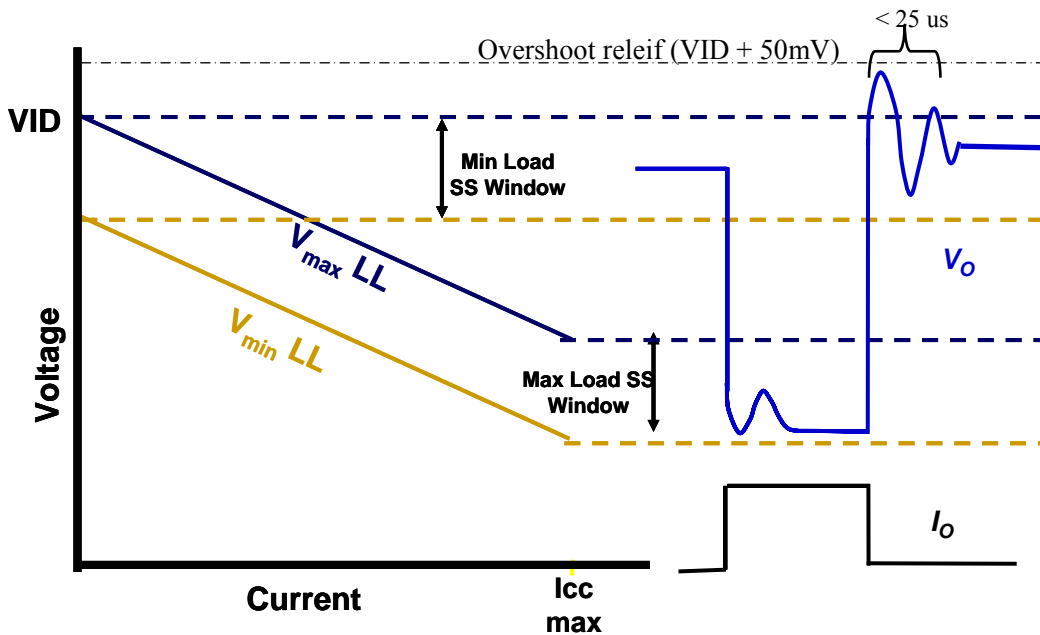


Figure 1.11 The relationship between the load-line specifications and the time domain waveforms.

Figure 1.11 shows the relationship between the load-line specification and the time domain waveforms. When the CPU current ( $I_o = I_{CC}$ ) is low, VR output voltage should be high and when the CPU current is high, VR output voltage should be low. This is achieved by the VR controller and the process is called adaptive voltage positioning control (AVP). The VR output voltage must also follow the load line during the transient with one exception. The load step down transient can be over  $V_{max}$  of the load line for 25us. This overshoot should not exceed the overshoot relief ( $VID + 50mV$ ; in VRD 11.0 specification). The voltage overshoots, which cannot

meet this specification, will cause higher processor operating temperature, and this may result in damage or a reduced processor life span. The processor temperature rise from higher functional voltages may lead to operation at low power states which directly reduces processor's performance. The voltage undershoots may cause system lock-up, "blue screening", or data corruption [16].

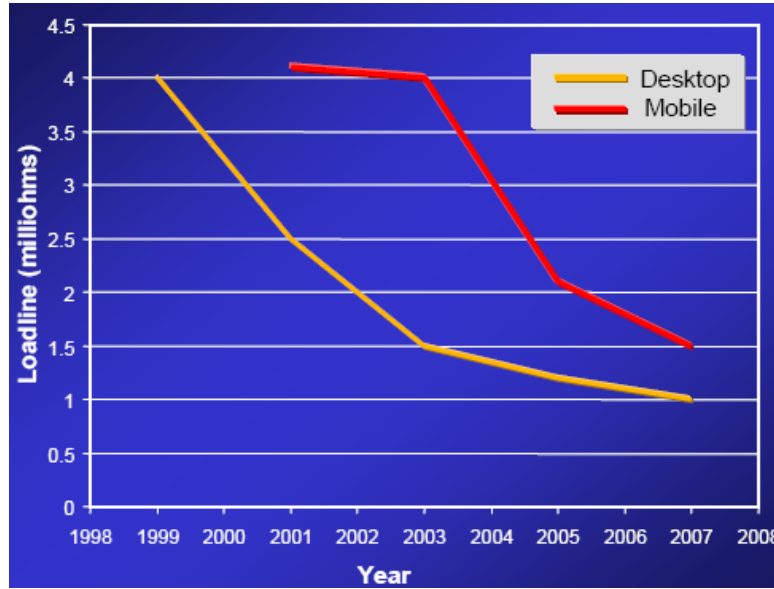


Figure 1.12 Historical data of the load-line slope specification.

As the CPU voltage decreases and the current demand increases, as illustrated in Figure 1.6, the load-line impedance ( $R_{LL}$ ) decreases, as shown in Figure 1.12. This makes the transient requirement stricter, as explained with Figure 1.13. In this figure,  $\langle i_o \rangle$ ,  $\langle i_L \rangle$ , and  $\langle i_C \rangle$  represents the average value of the CPU current, VR inductor current, and VR output capacitor current respectively (cf. Figure 1.8). When the CPU current (that is, the load current from VR side) steps down, the VR inductor current tries to follow the CPU current but the speed of the inductor current ( $di_L/dt$ ) is limited by the VR control speed. The current difference between the CPU current and the inductor current charges the VR output capacitors. Therefore there is a transient output voltage peak following equation (1.3),

$$\Delta V_o = R_C \cdot i_C(t) + \frac{1}{C} \cdot \int i_C(t) \cdot dt \quad (1.3)$$

where,  $i_C = i_L - i_o$ ,  $R_C$  is ESR of the VR output capacitor, and  $C$  is the total VR output capacitance. The larger CPU current demand, while the voltage and  $R_{LL}$  are smaller, will increase

the CPU current step magnitude ( $\Delta I_{O2}$ ), and the current charge to the VR output capacitor will be larger because the inductor current speed is still limited by the VR control speed. Thus, the transient voltage magnitude ( $\Delta V_{O2}$ ) will be much larger [50][51][52][53][54]. Meanwhile,  $V_{O2}$  is similar to  $V_{O1}$  because  $R_{LL2}$  is smaller than  $R_{LL1}$  and the transient voltage can be higher than the specification.

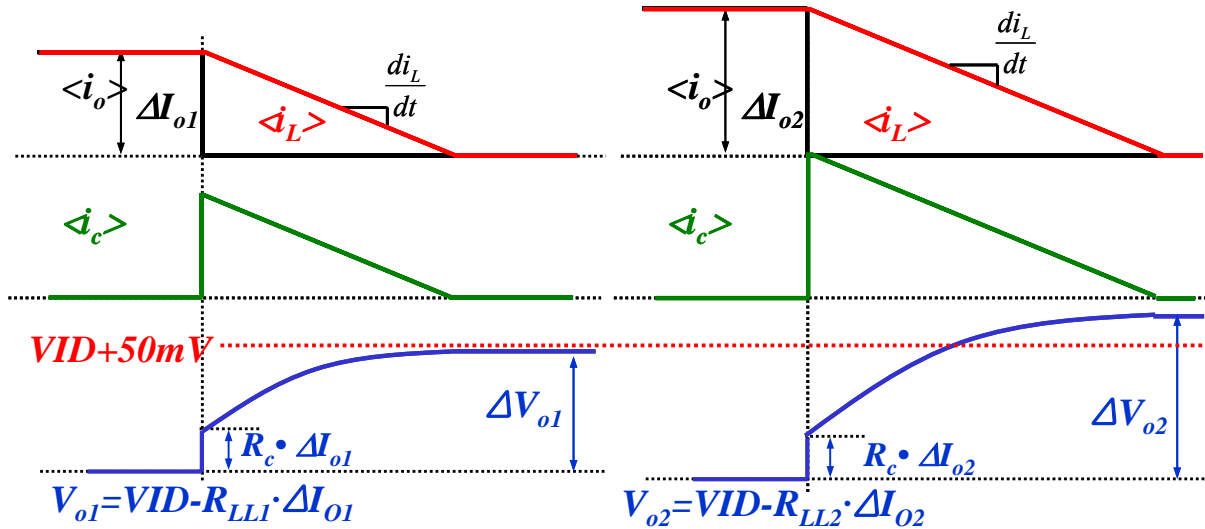


Figure 1.13 Transient output voltage overshoots and the specifications.

To deal with this transient VR output voltage, the recent VR makes use of a lot of decoupling capacitors. Figure 1.14 shows the typical power delivery path, and Figure 1.15 shows the lumped circuit model of this power delivery path [23][24][25][26]. The closest decoupling capacitors to the VR are called “bulk” capacitors. In most of today’s designs, the high-density aluminum polymer capacitors with  $560\mu\text{F}$  or  $820\mu\text{F}$ , and  $5\text{m}\Omega$  average ESR are used as the bulk capacitors. Following the bulk capacitors, Multi-Layer Ceramic Capacitors (MLCCs) are used as the mid-frequency decoupling capacitors. A typical value would be  $10\mu\text{F}$ ,  $22\mu\text{F}$  or  $47\mu\text{F}$ . Intel recommends putting these MLCCs in the socket cavity, and these capacitors are called “cavity” capacitors. For the Intel Core<sup>TM</sup>2 Duo in Figure 1.7,  $9 \times 560\mu\text{F}$  bulk capacitors and  $18 \times 22\mu\text{F}$  cavity capacitors are used. The footprints of these capacitors are huge and the cost is also high. Therefore, the VR size becomes larger and larger not only because of the larger number of phases, but also because of the larger number of output capacitors needed due to the stricter transient requirement. In order to reduce the size and cost of VR, the output capacitors should be reduced by increasing the VR control speed.



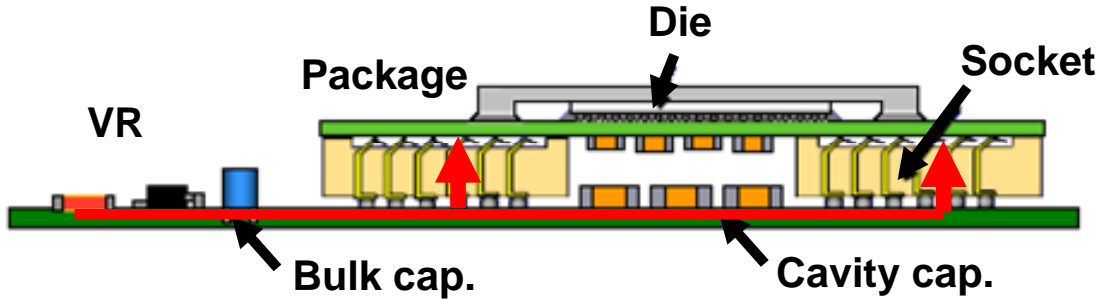


Figure 1.14 A typical power delivery path for today's processors.

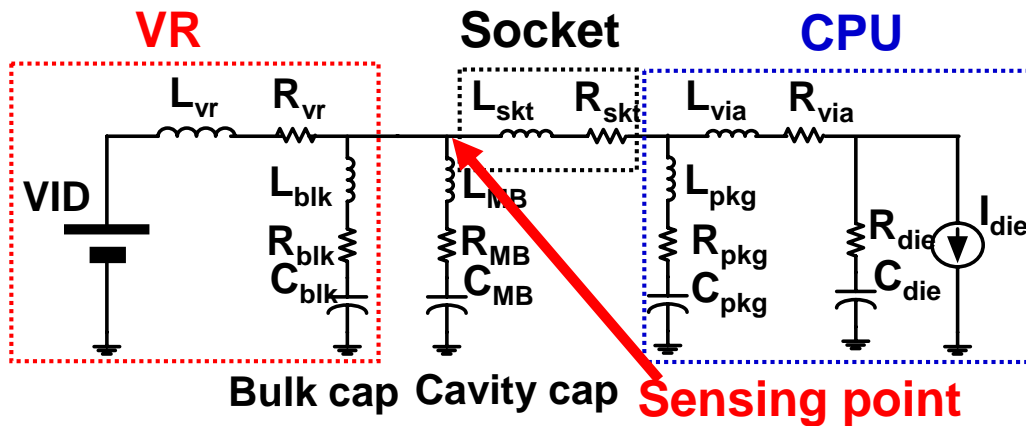


Figure 1.15 A lumped circuit model of the power delivery path of today's microprocessor.

So far, the challenges of the microprocessor and its VR are discussed. The power consumption in the microprocessor is the biggest challenge. Intel uses several technologies to reduce the power consumption of microprocessor. They are closely related to the VR and its control method. In order to use the sleep mode effectively, the efficiency of the VR should be optimized for each sleep mode when the CPU current demand is very small. And this can be controlled by VR controller. For the Speed Step technology, the VR output voltage should quickly follow the VID change even during the active mode operation. This is specified by Intel as the dynamic VID. In the VRD 11.0 specification [16], VR output voltage should be able to change 0.7625V within 350 $\mu$ s. This transition speed is determined by the VR control speed. Thus, VR control should be faster. Moreover, as mentioned above, in order to reduce the VR size and cost, again, the VR control should be faster. Therefore, the control is the most important part in the VR and it should be faster for the next generation microprocessors.

## 1.2. Review of Control Methods for VR

The multiphase VR controller should have several functions [16].

- Adaptive Voltage Positioning (AVP): AVP is required not only for the load-line specification but also for the capacitor reduction [16][59][63][64][65][66].
- Current Sharing: The current of each phase should be shared well for the efficiency and the reliability [75].
- Interleaving: In order to reduce the steady-state output voltage ripple, interleaving is required.

In addition to these functions, the control speed needs to be very fast. In this section, the existing control methods for VR are discussed, with concentration on the control speed.

### 1.2.1. Typical Linear Control Method for VR

Figure 1.16 shows the block diagram of a typical linear control method for VR [33][35][36][38][39][40][41][42]. Generally, there are three loops; the voltage loop, the AVP current loop and the current-sharing loop. These loops can be analyzed with the small-signal model because the system with this control method can be easily linearized, and the performance and the stability of this linear control method are determined by the bandwidth ( $f_C$ ). In most cases, the current-sharing loop is designed to be smaller than that of the voltage loop or the AVP current loop, since the output voltage dynamic response is not affected by the current-sharing loop. The voltage loop and the AVP current loop are used to make the output load line in Figure 1.10, and the constant impedance concept is widely used to design this [60][61][62][63][64][65][66][67][68]. With this control method, by designing  $H_V$  properly, the VR output impedance can be constant as  $R_{droop}$  ( $=R_{LL}$ ) within VR bandwidth ( $f_C$ ).

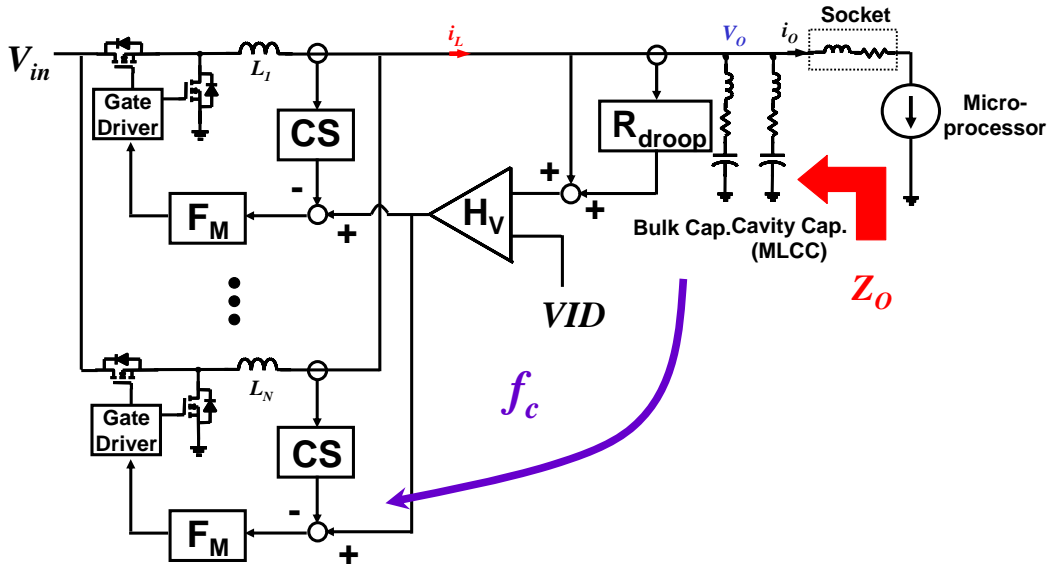


Figure 1.16 Block diagram of a typical VR controller.

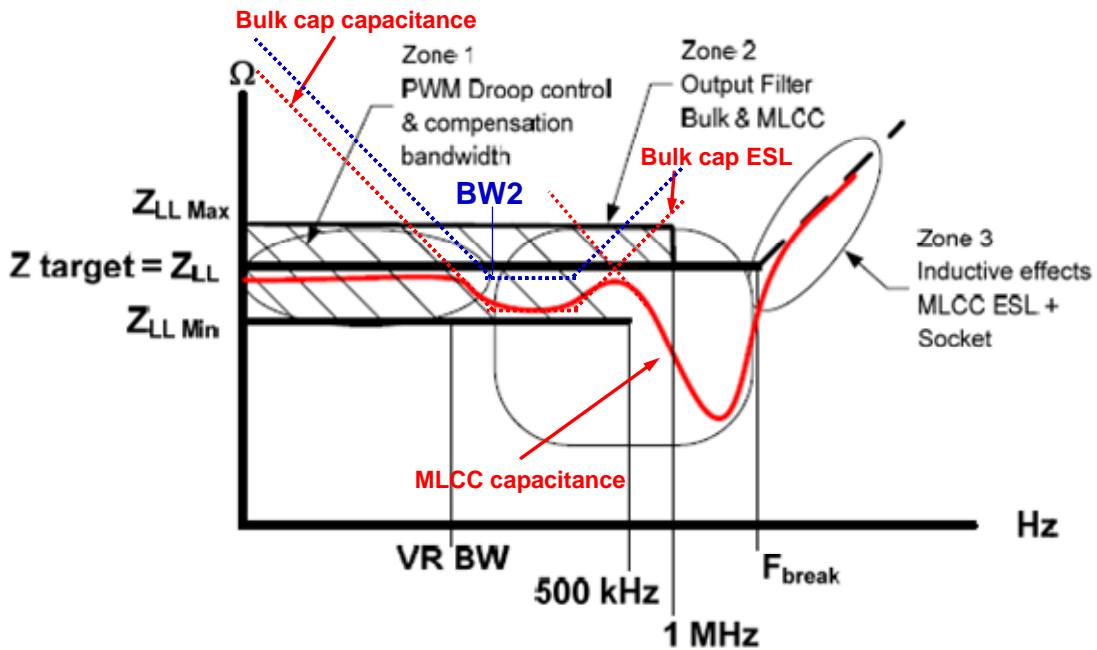


Figure 1.17 The output impedance before the socket and Intel specification.

Figure 1.17 shows the output impedance before the socket ( $Z_o$ ) and the impedance specification from Intel. Intel also specifies the output impedance before the socket with extended adaptive voltage positioning (EAVP) methodology [23]. The impedance should be smaller than  $Z_{LL}$  until  $F_{break}$ . For the VRD 11.0 specification,  $F_{break}$  is 2MHz. The impedance can be separated into three zones. In Zone 1, the impedance is determined by the VR control and the

bulk capacitors. In Zone 2, the decoupling capacitors (the bulk capacitors and the cavity MLCCs) determine the impedance. Zone 3 consists of the parasitics of the socket and MLCCs however, this zone is not of concern for VR. In Zone 1, the constant impedance is achieved by the VR control method and by increasing the bandwidth of VR ( $f_c$ ); this zone can expand, which can reduce the bulk capacitors. As shown in Figure 1.17, by increasing the VR bandwidth to  $BW_2$ , the bulk capacitors can be reduced to the blue dotted lines. If the bandwidth is enlarged near 500kHz, the bulk capacitors can be eliminated [101]. However, in the linear control method, the bandwidth is limited by the switching frequency [69][70][71][72][73][74] and the switching frequency is limited by the efficiency. With today's technology, the VR for the desktop computer system delivers power with around 300kHz switching frequency and the bandwidth can be only 50kHz ( $\approx f_s/6$ ). Therefore, in order to reduce the size and cost of the VR by reducing the number of output capacitors, new architecture is necessary to increase the switching frequency without a drop in efficiency; otherwise the fast transient control method, which is not limited by the bandwidth, should be studied.

### 1.2.2. Review of the Fast Transient Control Methods

There are many efforts to get the faster transient response without increasing the switching frequency. In this section, those methods are reviewed.

#### (a) Active Clamp

The active clamp circuit is the additional circuitry used to deal with the transient response [76][77][78]. Figure 1.18 shows the block diagram and the operating principles. The active clamp circuit deals with a very fast transient response, whereas the voltage regulator deals with a slow transient response and steady state power conversion. Therefore, the voltage regulator can be designed to be slow with the relatively low switching frequency and it can convert the power very efficiently. The active clamp circuit is designed to be very fast in order to satisfy the fast dynamic power demand of the microprocessor. The active clamp circuit supplies the current charge during the load step-up transient and it absorbs the current charge during the load step-down transient. However, the active clamp is not widely used in VR applications. The main drawback is the additional power loss, cost, and real estate. In the voltage regulator, the passive components deal with the transient and there is little loss. However, in the active clamp circuit,

the linear regulator regulates its output voltage within the linear region of the semiconductor devices, and the current charge or discharge during the transient becomes a power loss. Today's microprocessor works very fast and the load transient occurs very frequently. Therefore, the power loss in the active clamp is not too small even though it only works during the load transient. Moreover, industries don't like the additional cost and the real estate used.

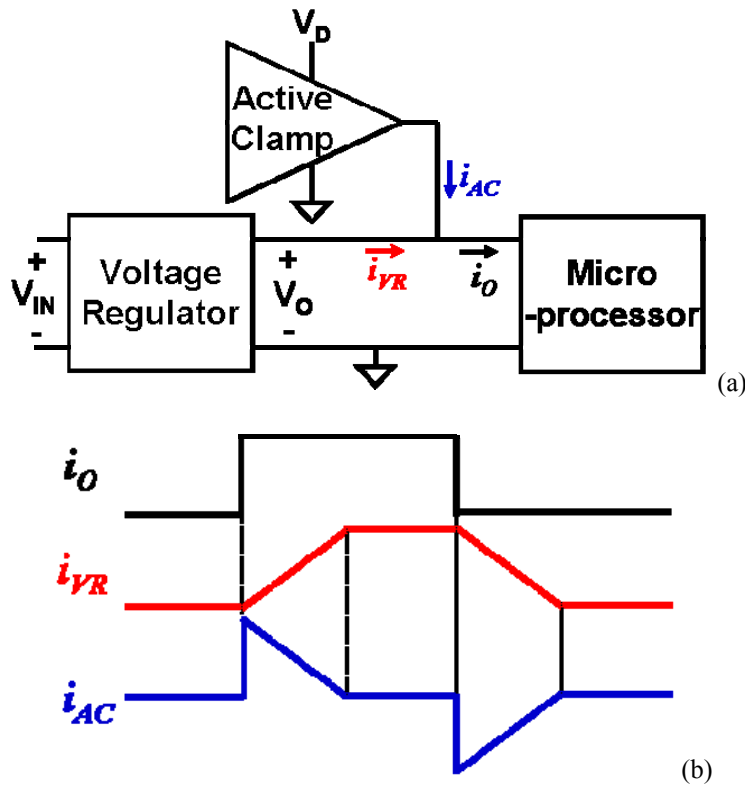


Figure 1.18 Active clamp (a) Block diagram (b) Operating principles.

## (b) Linear-Nonlinear Control Method

Instead of additional circuitry, a nonlinear control block can be added into the conventional linear control method. Figure 1.19 shows the block diagram and the operating principles of the linear-nonlinear (LnL) control method [79][80][81][82]. This example is the nonlinear control block with the hysteric band ( $V_{LT}-V_{HT}$ ) in the conventional linear control system. In this implementation, the field-programmable gate array (FPGA) is used to choose between the linear function and the nonlinear function [81][82]. At the steady state, the output voltage is inside the hysteric band and the nonlinear block does not work. Thus it behaves the same as the conventional linear control method with the bandwidth. Meanwhile, during the transient, the

output voltage touches the hysteretic band, and the nonlinear control block turns on or off all the phases as shown in Figure 1.19 (b). By doing this, the maximum inductor current slew rate ( $di_L/dt$ ) is achieved and the transient response is very fast.

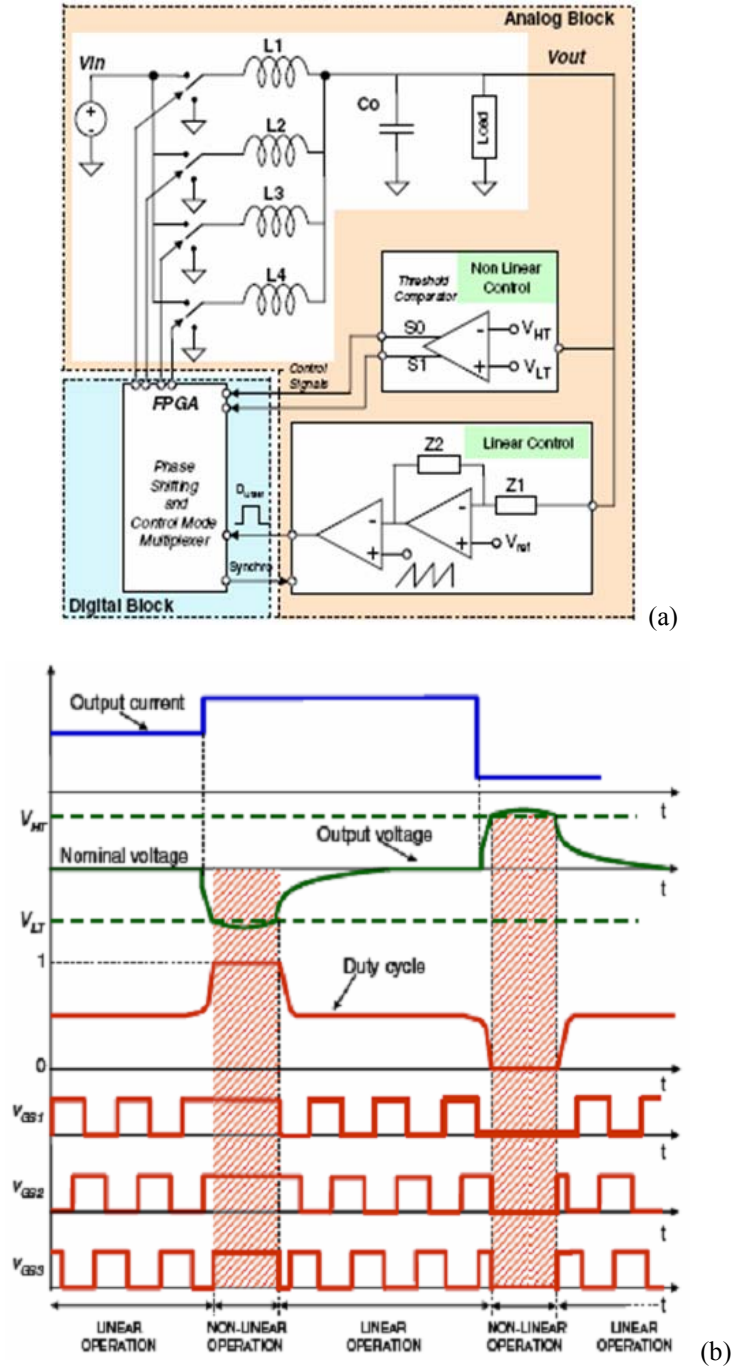


Figure 1.19 Linear-Nonlinear control method (a) Block diagram (b) Operating principles [82].

Figure 1.20 shows the simulation results from [82]. With the linear-nonlinear control, the output voltage is clamped to the hysteretic band, as in Figure 1.20 (a) with the relatively low switching frequency, and the inductor current slew rate is very high, as in Figure 1.20 (b). However, there is a chattering issue. In Figure 1.20 (b), the inductor current ripple is not normal with the linear-nonlinear control method. Without the proper design, the linear control and the nonlinear control are fighting near the hysteretic boundary, and there is chattering between the linear control and the nonlinear control. This causes very high-frequency switching action which may cause an efficiency drop and additional noise.

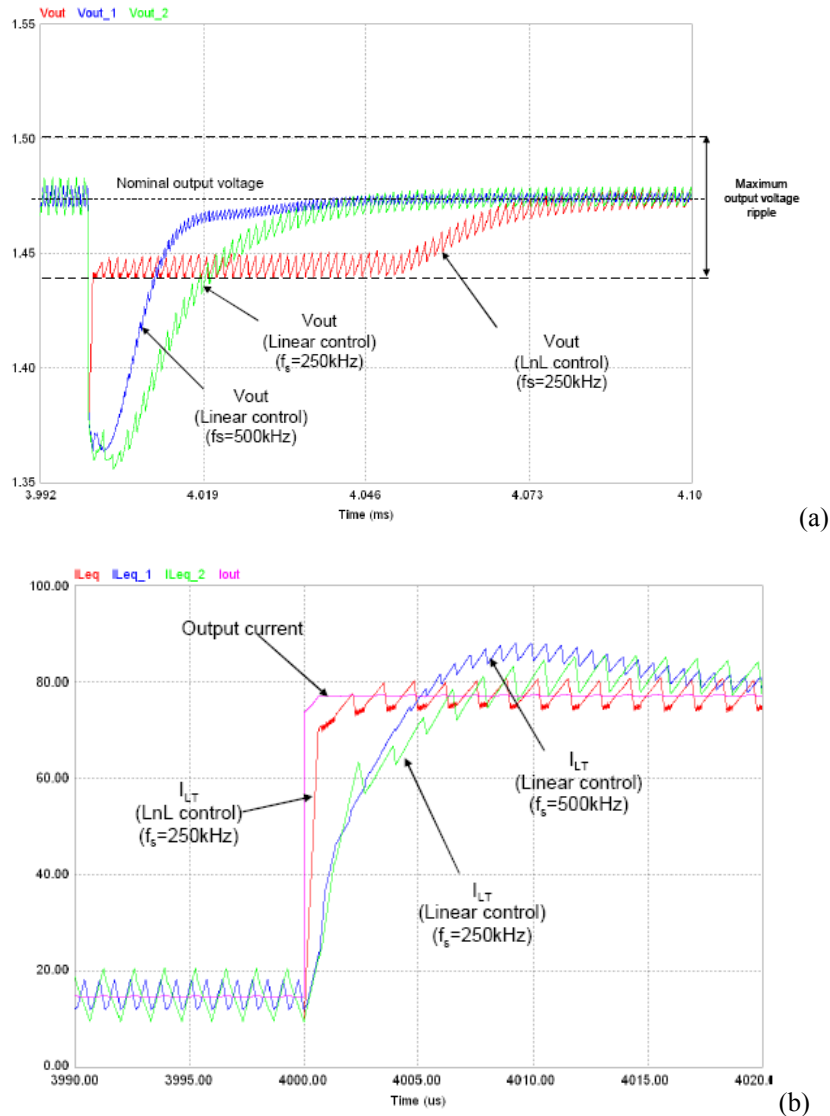


Figure 1.20 Simulation results of the Linear-Nonlinear control method and the linear control method varying the switching frequency (a) Output voltages (b) Inductor currents and the output current [82].

**(c)  $V^2$  Control Method**

Instead of injecting the output voltage information to the additional hysteretic comparator, it can be injected directly to the modulator. Figure 1.21 shows the block diagram of the  $V^2$  control method [83][84][85][86]. One more voltage loop is added to the conventional linear control method and there are two voltage loops and one current-sharing loop in this control. The first voltage information is fed back to the compensator and the other voltage information is directly injected to the modulator. The first voltage loop is slow because of the integrator (compensator) delay; however, with this loop, the output voltage is regulated without a steady state error. The second voltage feedback loop is very fast because there is no lead or lag compensator, and this loop makes the control reaction faster. In this control method, there is no chattering issue.

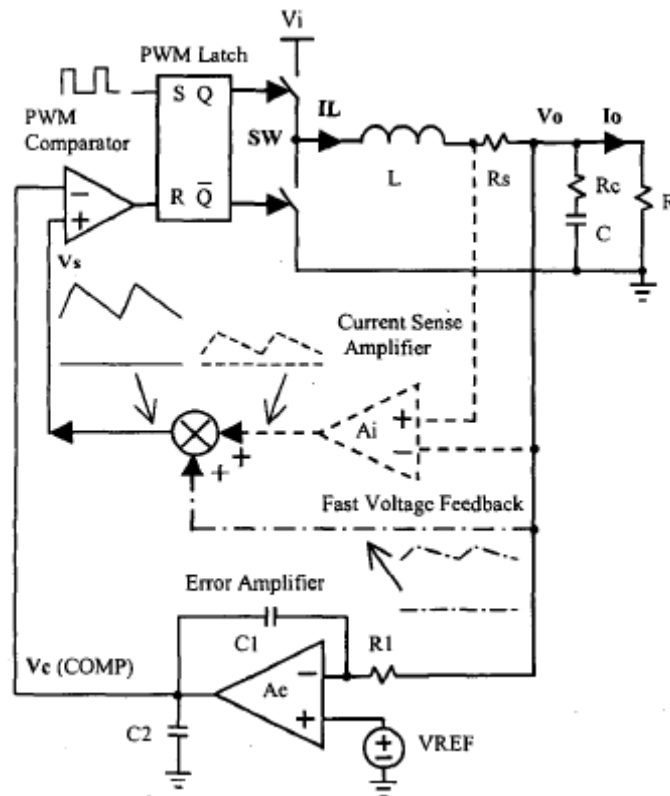


Figure 1.21 Block diagram of  $V^2$  control method [84].



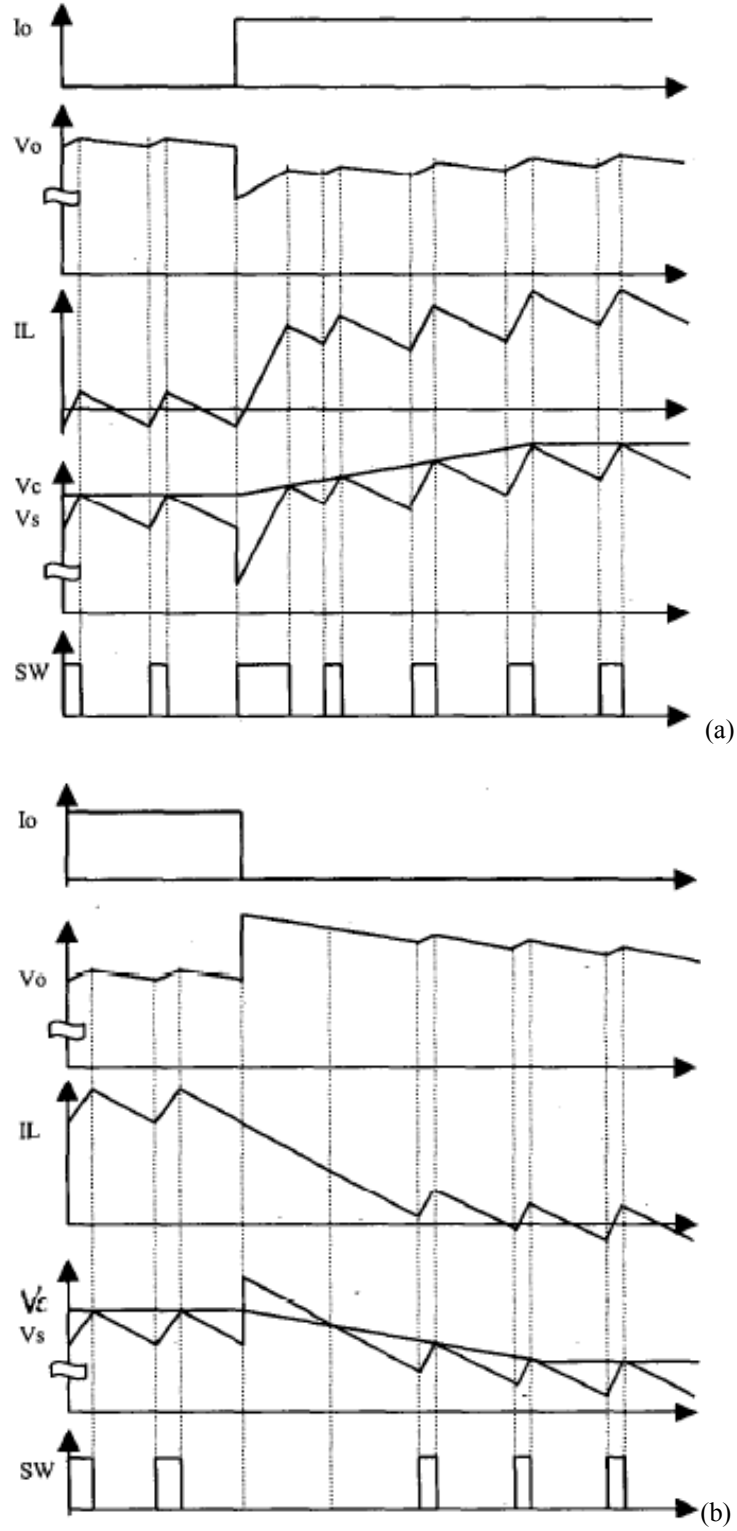
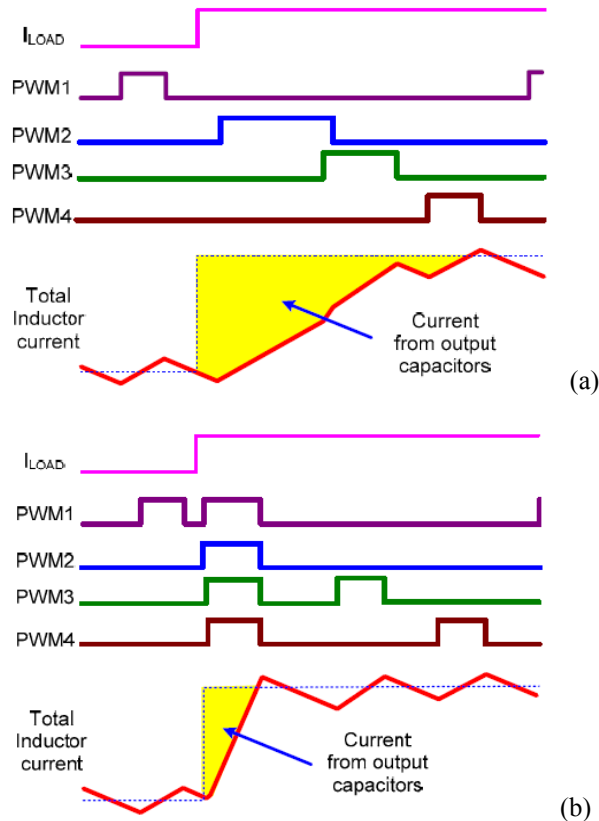


Figure 1.22 Operating principles of  $V^2$  control method [84] (a) The load step up (b) The load step down.

Figure 1.22 shows the operating principles of  $V^2$  control method from [84]. When the load current is step changed, the output voltage also step changes due to the parasitic resistance (ESR;  $R_C$ ) of the output capacitors. This information is fed back directly to the modulator through the fast voltage feedback loop and the duty cycles are quickly made according to this information. Therefore,  $V^2$  control is very fast for the load changes. This is like the load current feedforward action in [86][87][88][89].

$V^2$  control is based on the trailing edge modulation. In the controller, there are clocks and latches to ensure constant switching frequency and interleaving function. Because of these, the load step up transient is not very fast. Figure 1.23 shows the load step up transient of the trailing edge modulation and the ideal modulation [90][91]. The inductor current slew rate in Figure 1.23 (a) is much smaller than that in Figure 1.23 (b), because there are switching action delays in Figure 1.23 (a) due to the clocks. In summary,  $V^2$  control is very fast for the load step down transient, but the load step up transient is not so fast because of the switching action delays in the trailing edge modulation.



**Figure 1.23 The load step up transient [91] (a) Trailing edge modulation (b) Ideal modulation.**

### (d) Constant On-Time Control Method

The variable switching frequency control has no switching action delay because it does not use a clock. Maxim, one of the famous integrated circuit (IC) companies, released several VR controllers with the constant on-time control method [43][92]. Figure 1.24 shows an example of constant on-time control for the single phase VR. Similar to the  $V^2$  control method, there are two voltage loops; the fast voltage loop with the switching ripples and the slow voltage loop with integrator for steady state regulation. Figure 1.24 (b) shows the operating principles of this control method. When the output voltage ripple touches the control voltage ( $V_C$ ), the top switch turns on, and after the constant on time ( $T_{ON}$ ), it turns off. In this control, the inductor current ripple is constant because the top switch on time and the inductance is constant. At the steady state, the switching frequency is almost constant and it is immune to the output capacitor parasitics variance. The switching frequency is only changed with the input voltage or the system efficiency change.

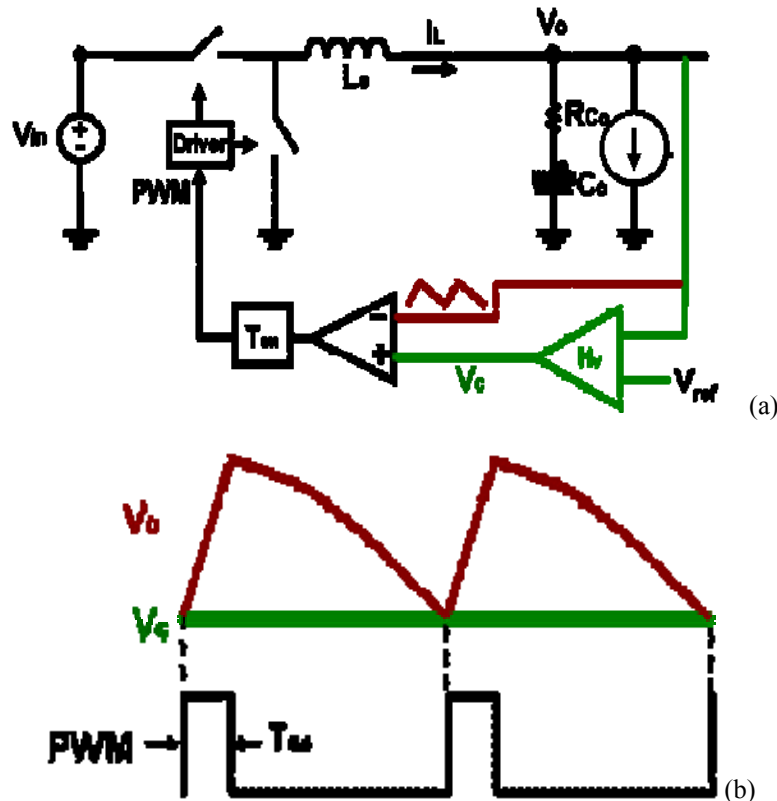


Figure 1.24 Constant on-time control (a) Schematics (b) Operating principles

The main benefit of this control is the light-load efficiency. Figure 1.25 shows the variable switching frequency action of the constant on-time control in the discontinuous current mode (DCM) operation; Maxim named this operation the pulse skip mode [92]. When it runs in DCM, the switching frequency is proportional to the load current. The inductor current peak value is constant and to supply the lower average current, the switching frequency should be smaller. At light load, the switching loss is the dominant loss, and the light load efficiency can be remarkably improved with a smaller switching frequency, like that in Figure 1.26. When the CPU is in sleep mode, the VR efficiency can be optimized with this control method. Therefore, this control method is widely used in mobile applications, where the light-load efficiency is very important for the battery life.

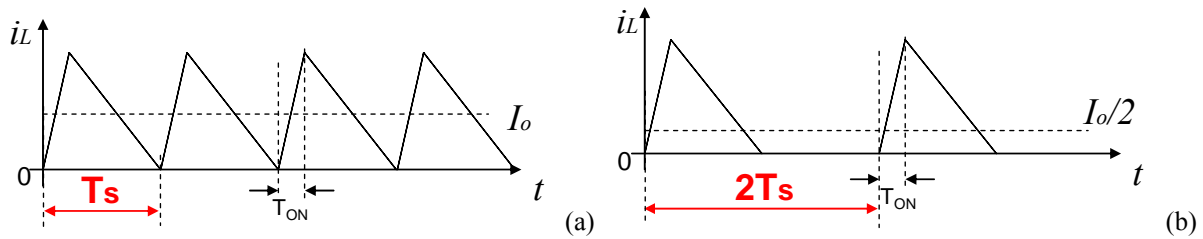


Figure 1.25 Pulse skip mode control (a) Critical current mode (b) Discontinuous current mode.

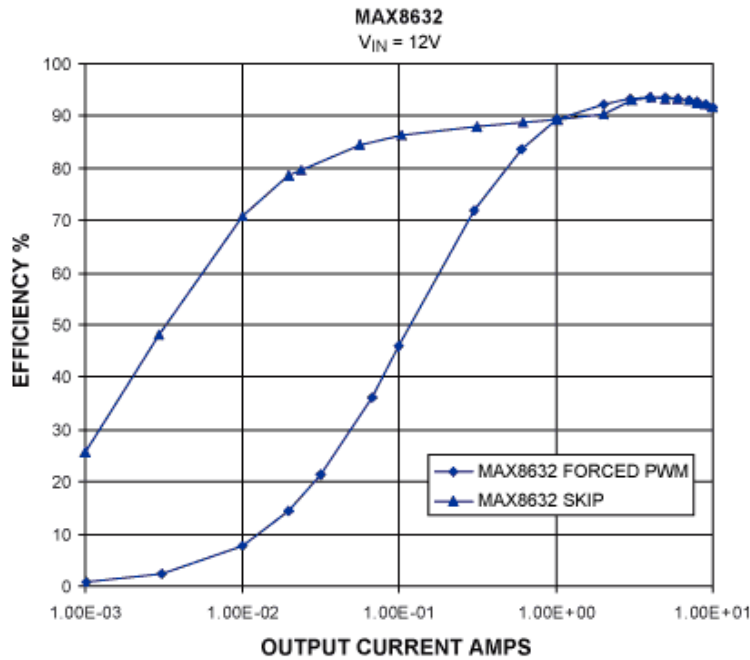
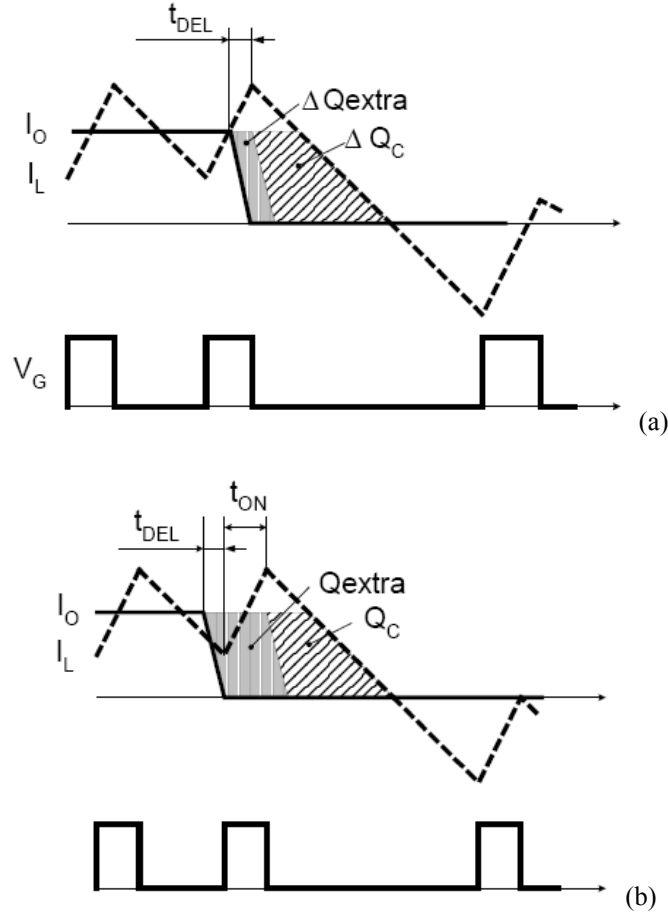


Figure 1.26 Efficiency comparison between Forced PWM and the pulse skip mode [92].



**Figure 1.27 Load step-down transient operations (a) Ideal control (b) Constant on-time control**

The constant on-time control is good for steady-state operation and light-load efficiency. However, the transient response is not perfect. As mentioned above, this control method includes two voltage loops like the  $V^2$  control method and the direct voltage feedback makes the regulation speed faster. For the load step-up transient, the direct output voltage feedback reacts very quickly to the load current disturbances and the duty cycle is made without any delay. However, for the load step-down transient, there is a delay due to the constant on-time period ( $T_{ON}$ ) [52][53][54]. Figure 1.27 shows the load step-down transient operations of the ideal control and the constant on-time control method. The ideal control method in Figure 1.27 (a) has the delay from the comparator and the driver ( $t_{DEL}$ ) whereas the constant on-time control method in Figure 1.27 (b) has the larger delay ( $t_{DEL} + t_{ON}$ ). This larger delay builds the larger charge to the output capacitors and it makes a larger output voltage peak.

**(e) Hysteretic Control Method**

So far, several control methods have been discussed; however, they each have their own disadvantages. The active clamp's disadvantages include larger power loss, large size and higher cost. The linear-nonlinear control method has the chattering issue. The  $V^2$  control method has the switching action delay at the load step-up transient operation. The constant on-time control method has the on-time delay for the load step-down transient operation. Comparing to these control methods, the hysteretic control method has much faster performance [52][107][108]. Figure 1.28 shows one type of the hysteretic control method for the single-phase VR. The inductor current is sensed with gain  $K$  and summed with the output voltage. Then, this information ( $I_L \cdot K + V_O$ ) is fed back to the hysteretic comparator. The hysteretic band is made inside the controller with the hysteretic band width signal ( $V_{HYST}$ ) and the reference voltage ( $V_{ref}$ ) following (1.4),

$$V_{BAND} = 2 \cdot (V_{ref} - V_{HYST}) \quad (1.4)$$

$V_{HYST}$  is chosen by the user for the switching frequency. When the feedback signal touches the bottom of the hysteretic band, the control switch turns on and when the signal touches the top, the control switch turns off. Therefore the feedback signal is regulated within the hysteretic band and the median of the feedback signal is regulated to be same as the reference voltage like,

$$[I_L \cdot K + V_O]_{Median} = V_{ref} \quad (1.5)$$

The sensing gain  $K$  can be designed to be same as the AVP load-line impedance ( $R_{LL}$ ) which is specified by Intel, and the median of the output voltage is regulated just like the AVP control.

$$[V_O]_{Median} = V_{ref} - K \cdot [I_L]_{Avg} = V_{ref} - R_{LL} \cdot [I_L]_{Avg} \quad (1.6)$$

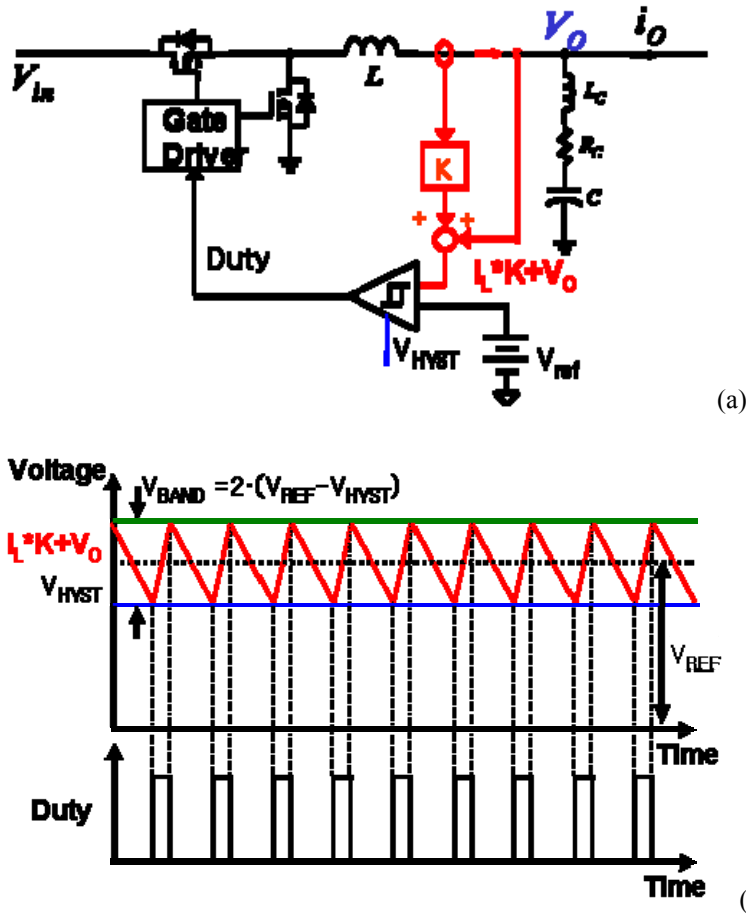


Figure 1.28 Hysteretic control method for the single phase VR (a) Schematics (b) Operating principles

Figure 1.29 shows the Simplis simulation results of the hysteretic control method. With this control method, the output voltage is fed back without any delay from the lead or lag compensators, and the load current change can be easily sensed with the ESR or ESL voltage jump in the output voltage. The duty cycle is made directly by the state variables, the inductor current and the output voltage without any time delay. Therefore it has very fast transient response. As soon as the load steps down, the duty cycle becomes zero and for the load step-up transient, the duty cycle changes to one immediately. In addition, the controller is saturated during the load step-down transient because the feedback signal is out of the hysteretic band, and the inductor current slew rate is maximized during this period. At the steady state, the feedback signal is well-regulated within the hysteretic band, which means this control doesn't need an integrator.

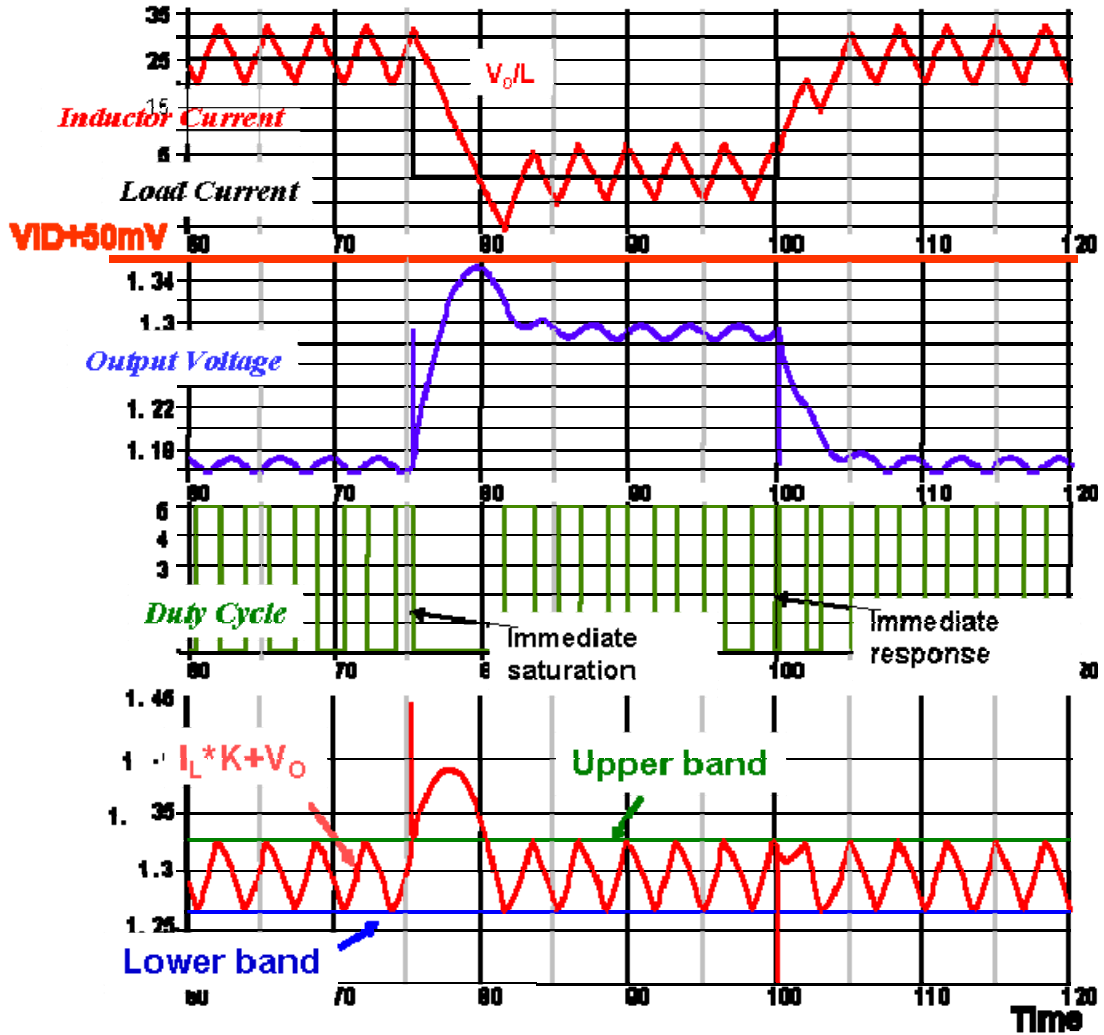


Figure 1.29 Simulation results of the hysteretic control method

Similar to the constant on-time control method, the hysteretic control method reduces its switching frequency at DCM operation, as illustrated in Figure 1.25. In this control method, the sum of the inductor current ripple and the output voltage ripple is constant. Assuming the output voltage ripple is dominated by the ESR of the output capacitors, the inductor current ripple is regulated as the constant value. This control has the same light-load efficiency as the constant on-time control method in Figure 1.26.

In summary, the hysteretic control method is a very good candidate for the next generation VR because of its fast transient response and the high light load efficiency with DCM operation. However, this control method cannot be used directly in the multiphase VR. The converter with this hysteretic control method is a self-oscillating circuit and it is very hard to implement the



interleaving function. In order to use this very fast hysteretic control method, the interleaving function should be studied.

### 1.3. Possible Solutions

Many efforts have been made to reduce the size and cost of VR by increasing the control speed. However, there is no good solution to satisfy all these requirements. In this dissertation, two approaches are explored to try to solve this issue. The first is the architecture approach, with which the converter switching frequency can be higher without a decrease in efficiency. The other approach explored in this dissertation is the control approach. Using the hysteretic control method which is one of the nonlinear control methods, the VR dynamic performance is faster than that of the conventional control methods with the given switching frequency, and a smaller and faster VR is achieved with good efficiency.

#### 1.3.1. Architecture Approach; Two-Stage VR

The easiest way to reduce the size and cost of a VR is to increase the switching frequency. With the higher switching frequency operation, the passive components, such as the inductors and the output capacitors, can be smaller due to the higher switching frequency and the higher control bandwidth. However, the high switching frequency results in low converter efficiency. Figure 1.30 shows a multiphase synchronous buck converter running at 300kHz and 1MHz [101]. The efficiency degrades around 5% from 300kHz to 1MHz.

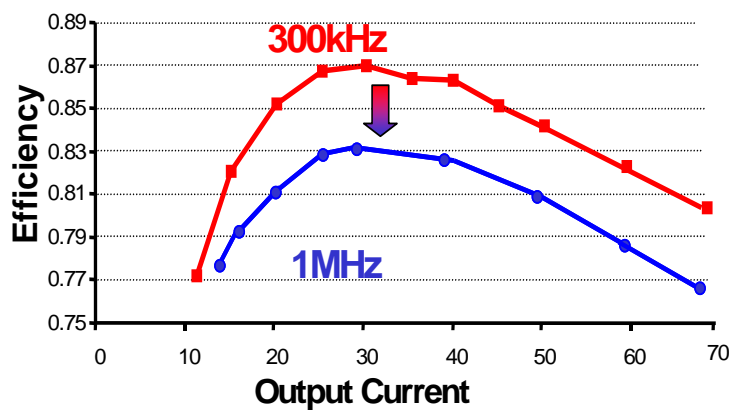


Figure 1.30 Conventional VRs' efficiency suffers as the switching frequency increases [101].

The main reason for this efficiency drop is the larger switching loss. By decreasing the input voltage, the switching loss can be reduced and high efficiency can be achieved [102]. The Center for Power Electronics Systems (CPES) has proposed a two-stage architecture for VR applications [96][97][100][101]. Figure 1.31 shows an example of the two-stage architecture [100]. The synchronous buck converter is used as the first stage to step down the input voltage in order to get higher efficiency, whereas the multiphase synchronous buck converter is used as the second stage to regulate the output voltage. The second stage switching frequency should be very high to deal with the fast dynamic load change.

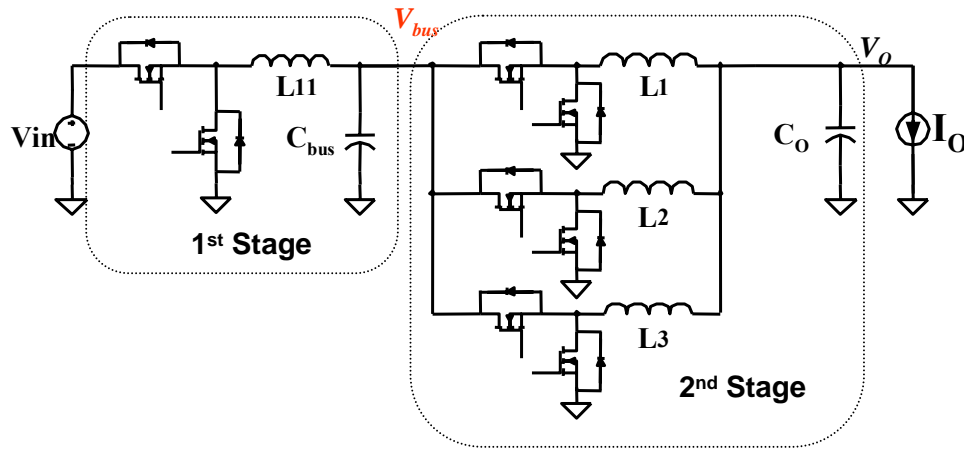


Figure 1.31 Two-stage architecture.

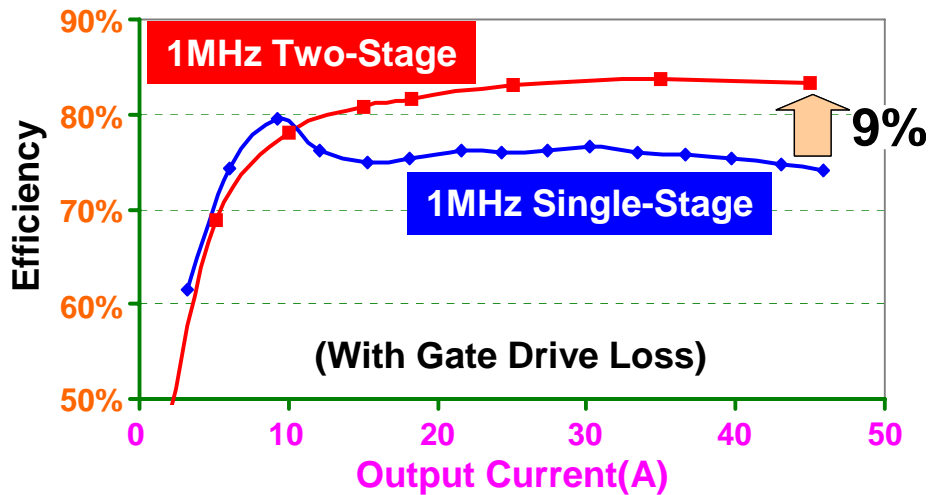


Figure 1.32 Efficiency comparison between the 1MHz single-stage VR and the 1MHz two-stage VR [100].

In [100], a hardware comparison between the single-stage and two-stage architecture is performed. Figure 1.32 shows the efficiency comparison. When the load is heavier, the two-stage solution is better. At 45A output, the two-stage solution is 9% more efficient than the single-stage solution. For second stage converters, low voltage rating devices can be used, and there is more room to enhance the efficiency. The two-stage solution is good not only because of the higher efficiency, but also because the second stage can be very small. This is because the inductor size is very small due to the smaller input voltage and the higher switching frequency, and the size of the output capacitors is also very small due to the higher bandwidth design [103]. Therefore the second stage is very small and it can be located near the CPU, as shown in Figure 1.33 [102]. It is well known that when there is a shorter power delivery path, the parasitic impedance in the power path is smaller and the system efficiency is better. Therefore the two-stage architecture is a very good candidate for future VRs.

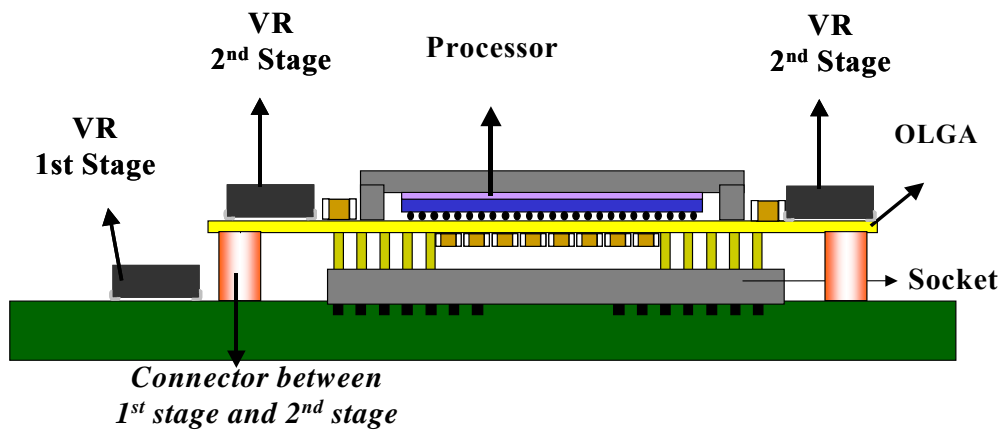


Figure 1.33 New architecture with the Two-Stage VR [102].

However, the two-stage architecture does have a disadvantage. As shown in Figure 1.32, the light-load efficiency is not very good; it is even worse than the single-stage architecture. As mentioned in the first section, the VR light-load efficiency is very important for sleep mode operation. Chapter 2 discusses the control method to increase the light-load efficiency in the two-stage architecture.

### 1.3.2. Fast Transient Control Approach; Hysteretic Control Method

In Section 1.2, the existing fast transient control methods for VR are reviewed. The hysteretic control method is a very good candidate for the next generation VR controller because of its very fast transient response and the high light-load efficiency capability. However, the multiphase VR applications require several basic functions; AVP, current sharing, and interleaving. Yet no hysteretic control can achieve those functions without degrading its advantages of fast transient response, and high light-load efficiency.

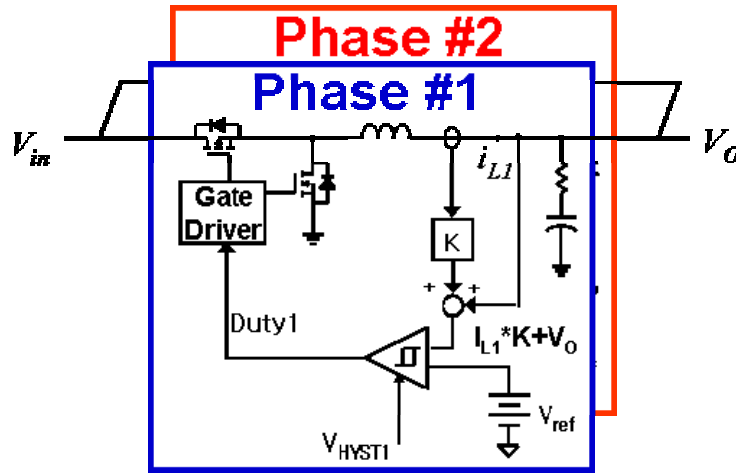


Figure 1.34 Hysteretic control method for the two-phase VR.

To achieve multiphase operation, two single-phase VRs with the hysteretic control method are paralleled like the illustration in Figure 1.34. Each phase regulates its inductor current and the output voltage in accordance with (1.6). They have the same output voltage, and the average value of each inductor current is also regulated to be the same following (1.7),

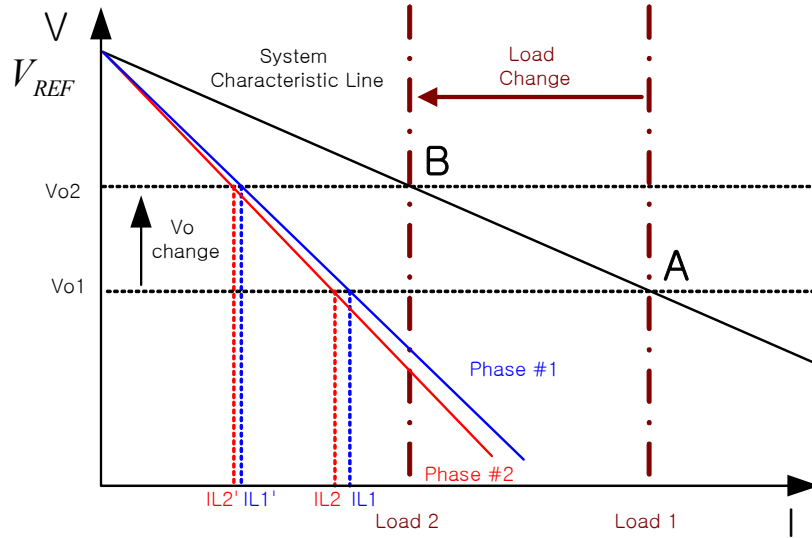
$$[V_O]_{Median} = V_{ref} - K \cdot [I_{L1}]_{Avg}, \quad [V_O]_{Median} = V_{ref} - K \cdot [I_{L2}]_{Avg} \quad (1.7)$$

where,  $I_{L1}$  is the first phase inductor current, and  $I_{L2}$  is the second phase inductor current. Therefore, current sharing is achieved.

From (1.7), the total inductor current and the output voltage relationship can be determined using (1.8),

$$[V_O]_{Median} = V_{ref} - K / 2 \cdot [I_{L1} + I_{L2}]_{Avg} \quad (1.8)$$

This can be generalized as (1.9),



**Figure 1.35 Characteristic lines with the two phase VR.**

$$[V_O]_{Median} = V_{ref} - K/N \cdot [I_{LT}]_{Avg} = V_{ref} - R_{LL} \cdot [I_{LT}]_{Avg} \quad (1.9)$$

where,  $I_{LT}$  is the total inductor current, and  $N$  is the phase number. By designing the current-sensing gain  $K$  of each phase as  $N \cdot R_{LL}$ , AVP is achieved. This concept can be explained with the system characteristic lines in Figure 1.35. Each phase's characteristic line is determined independently by using (1.7), and the system characteristic line is determined by (1.9). The operating point is  $A$  in Figure 1.35 with the load current,  $Load1$ , and the output voltage is  $V_{O1}$  as determined by (1.9). Each phase shares the same output voltage and each phase's inductor current shares  $I_{L1}$  and  $I_{L2}$  according to (1.7). Then, the load current is changed to  $Load2$ , and the operating point is changed to  $B$ . The output voltage is also changed to  $V_{O2}$  and each phase's inductor current is shared as  $I_{L1}'$  and  $I_{L2}'$ . As the load current decreases, the output voltage increases which is the adaptive voltage function. Current sharing is successfully achieved.

This hysteretic control has many advantages such as fast transient response, high light-load efficiency, current-sharing capability, and AVP. However, this control cannot be used in the multiphase VR, because the interleaving function is difficult to achieve. In this control, implementing the interleaving function without degrading the performance is the big challenge. This is discussed and a solution is proposed in Chapter 3.

## 1.4. Dissertation Outline

This dissertation consists of five chapters organized as follows:

Chapter 1 gives an introduction of the research background. The microprocessor faces a big challenge; the thermal wall. In order to enhance the performance of the microprocessor without increasing the heat dissipation, the leading microprocessor company, Intel, uses several methods to reduce the power consumption. These methods include enhanced sleep states control, the Speed Step technology, and multi-core architecture. These are closely related to the Voltage Regulator, a dedicated power supply for the microprocessor. The sleep states control is related to the light-load efficiency improvement in the VR, the Speed Step technology is related to the dynamic VID control of VR, and the dual core architecture results in the design challenges of a high current, high  $di/dt$ , and a stringent load line requirement. With today's technology many decoupling capacitors are necessary, which increases the VR's cost and size. Existing studies show that there is a close relationship between the VR control speed and the numbers of decoupling capacitors. Therefore, VR control method is very important because it is related to all three issues, the number of decoupling capacitors, the dynamic VID and light-load efficiency. Therefore increasing the speed of VR becomes the most important objective.

The easiest way to increase the speed of the VR is higher switching frequency operation. The higher switching frequency results in system efficiency degradation. Thus, many efforts are made to increase the speed of VR without increasing the switching frequency; however there is not currently a practical solution. This paper uses two approaches to deal with this issue. The first one is the architecture approach. Using the two-stage architecture, the VR can run with the higher switching frequency which may reduce VR cost and size. The low light-load efficiency of the two-stage architecture is a drawback. Therefore, finding a way to increase the light-load efficiency is the main concern for this approach. The other approach to increase the VR speed without decreasing efficiency is the fast transient control approach. Using a nonlinear control method such as the hysteretic control method, the VR speed can be enhanced without increasing the switching frequency. However, VR control must meet all the requirements of AVP, current-sharing capability, and interleaving, whereas no existing fast transient method can meet all these requirements. Therefore, implementing the fast transient control in the multiphase VR is a subject to be researched. In this dissertation these two approaches are explored.

In Chapter 2, using the Adaptive Bus Voltage Positioning (ABVP) control method to increase the light-load efficiency for the two-stage VR is studied. It is already shown that the optimal bus voltage for the system efficiency is changing according to the load current, and by adaptively adjusting the bus voltage to this optimal bus voltage, the system efficiency can be optimized for whole load range. The bus voltage changing speed is determined by the first stage bandwidth. In order to follow the fast dynamic load, the first stage bandwidth should be high. However, when the first stage bandwidth is higher, the ABVP system becomes unstable. To get a stable system, the first stage bandwidth is designed to be too low such as one hundredth of the switching frequency and this causes slow ABVP dynamics which degrades the ABVP performance. The large number of bus capacitors necessary for this also increases the size and cost.

In order to raise the first stage bandwidth, a stability analysis must be performed. There is the positive feedback loop in ABVP system because the second stage inductor current is fed back to the first stage with the positive gain ' $R_{tilt}$ '. To analyze this, the small signal model is suggested and the new feedforward small signal model is derived. The previous feedforward small signal model is not accurate enough to predict this positive feedback loop ( $T_{ABVP}$ ). With the new feedforward small signal model proposed in Chapter2,  $T_{ABVP}$  can be predicted. The ABVP system is stable when the magnitude of  $T_{ABVP}$  is smaller than 0dB. The  $T_{ABVP}$  magnitude can be reduced by designing the second-stage feedforward gain to be as large as possible. The peak magnitude of  $T_{ABVP}$  is made at the first stage bandwidth, and using a low-pass filter with the corner frequency slightly lower than the first stage bandwidth, the peak magnitude can be reduced. With these strategies, the ABVP system is designed to be stable while pushing first stage bandwidth as high as possible (about one tenth of the switching frequency in the example). Then, in the design example, the ABVP dynamics is improved to be about five times faster, and the bus capacitors are reduced about tenfold. With the hardware, the ABVP-AVP system and its design are verified.

In Chapter 3, in order to get the faster system and reduce the size and cost, a hysteretic control method for the multiphase VR is proposed. The hysteretic control method is very good because of its fast transient capability and the high light-load efficiency. With parallel operation, AVP and current-sharing are achievable. However, in order to use the hysteretic control method for the multiphase VR applications, these are not enough; the interleaving function must also be

implemented. There are some interleaving methods for the hysteretic control, however, with these methods, the load step up dynamics are not good and the system needs more output capacitors. With the existing interleaving method, the system is interleaved not only at the steady state but also during the transient, and the duty cycles of each phase cannot be overlapped during the load step-up transient. This reduces the inductor current slew rates, which determine the speed of the system. For the four-phase VR design with VRD 11.0 specifications,  $9 \times 560\mu\text{F}$  Al-polymer bulk capacitors are necessary to deal with the load step up transient. In order to reduce the need for more output capacitors, the multiphase hysteretic control method is proposed. The basic concept is based on the constant switching frequency hysteretic control methods [110][113]. Using the phase locked loop (PLL), this control method locks the phase and frequency of the duty cycles to the reference clocks by modifying the hysteretic band width. By phase shifting the reference clocks, interleaving is achieved at the steady state. During the load transient state, the system loses the phase locking function by designing the PLL to be slow and the system reacts quickly to the load change without the interruption from the phase locking function (or the interleaving function). Therefore, during the load step up transient, the duty cycles of each phase can be overlapped to get the highest inductor current slew rate. With the proposed hysteretic control method, for the same four-phase VR design with VRD 11.0 specifications, the bulk output capacitors can be reduced from 9 to  $6 \times 560\mu\text{F}$  Al-polymer bulk capacitors.

In order to use the proposed hysteretic control method, it should be analyzed and designed to meet the required specifications. During the transient, the controller is saturated and the output voltage peak should be predicted. For this purpose, the phase plane analysis is suggested. Using the phase plane model, the load transient dynamics are analyzed, the output voltage peak is predicted, and the output capacitors are designed to meet the specifications. Although the output capacitors are properly designed for the output voltage peak during controller saturation, there can be another output voltage peak due to improper PLL design. A model that makes it possible to properly design the hysteretic band width changing loop is necessary. Using the sampled data modeling technique, the linearized model is derived. With this model, the hysteretic band width changing loop is designed, and the improper output voltage peak can be eliminated. However, the repetitive load dynamics raise another issue. If the transient occurs before the hysteretic band width changing loop settles down, the transient may start with the large hysteretic band width



and the output voltage peak can exceed the specification. To prevent this, the hysteretic bandwidth limiter is inserted. With the hardware, the proposed hysteretic control method and its design are verified. The two phase VR with 300kHz switching frequency is built and the output capacitance is only 860 $\mu$ F in contrast with a 1600 $\mu$ F output capacitance with the 50kHz bandwidth linear control method. This is about a 46% capacitor reduction.

Chapter 4 shows the performance enhancements of the proposed hysteretic control with the coupled inductor. The proposed hysteretic control method saturates the controller during the transient and the transient peak voltage is determined by the power stage parameters, the inductance and the output capacitors. It is shown that by decreasing the inductance, the output capacitors are reduced. However, small inductance results in low efficiency. In order to resolve this problem, coupled inductor is used. A coupled inductor is nonlinear inductor which has two separate inductances for the transient and the steady state. With the coupled inductor, the transient inductance can be reduced with the constant steady state inductance. Therefore, the transient speed can be faster without reducing the system efficiency. However, the coupled inductor cannot be used directly in the hysteretic control because each phase's inductor current with the coupled inductor has all the phase information, and with the switching noise it may ruin the interleaving function. Therefore, the current information which has only each phase's information is necessary. In the coupled inductor, it can be sensed with the DCR current sensing method. The proposed hysteretic control method with the coupled inductor can be implemented using the DCR current-sensing network. The two-phase VR with 300kHz switching frequency is built, and the output capacitance is 660 $\mu$ F lower than the 860 $\mu$ F output capacitance with the proposed hysteretic control only. That is about 23% capacitor reduction. Comparing with the 50kHz bandwidth conventional linear control method, there is about a 60% overall capacitor reduction.

Chapter 5 summarizes the conclusions and proposes the ideas for the future work.



## Chapter 2. Advanced Control Method for Two-Stage Architecture

As mentioned in Chapter 1, the voltage regulator for the next generation of microprocessors faces a stringent challenge because of a demand for the higher current and lower voltage. Furthermore, the processor performs as a fast dynamic load with high  $di/dt$  current slew rate. To satisfy this fast dynamic load requirement, a huge amount of output capacitors are necessary [23][24][25][26] [102], which increases the cost and the real estate used on the motherboard. The switching frequency should be higher to reduce this huge amount of output capacitors, but this reduces the system efficiency because of the larger switching loss. To resolve this problem, the two-stage concept has been proposed [96][97][100][101]. The two-stage structure can increase the full load efficiency by reducing the second stage loss (which is higher than the additional loss due to the first stage). However, as mentioned in Chapter 1, the light-load efficiency of the two-stage architecture is not good because the intermediate bus voltage ( $V_{BUS}$ ) is designed for efficiency at full load, and is not optimized for the light load. Therefore, by adaptively positioning the bus voltage according to the load current, the light-load efficiency can be improved [100]. Figure 2.1 shows this concept, which is called adaptive bus voltage positioning control (ABVP).

In this chapter, this ABVP control is analyzed. The challenges of this ABVP system are discussed, including the trade off between stability and the ABVP dynamics. In order to analyze this, the small-signal model is suggested, and the design guideline for the ABVP-AVP system is proposed. Then, the experimental results verify the proper design of ABVP-AVP system.

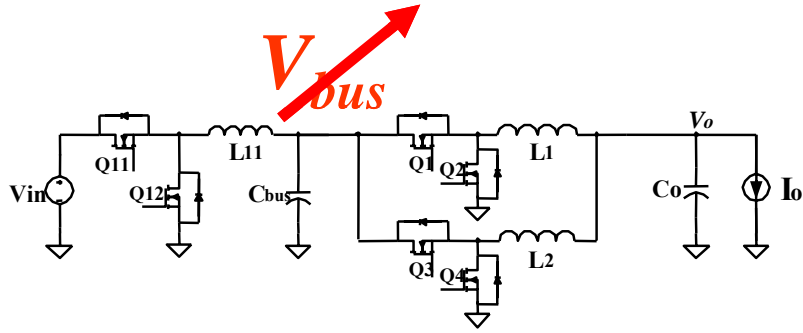


Figure 2.1 Two-stage architecture and the bus voltage.

## 2.1. Review of ABVP-AVP System

In [100] and [101], the ABVP control method is proposed for its high light-load efficiency. In order to know the relationship between the load current and the optimal bus voltage at the light load, the system efficiency is measured varying the load current and the bus voltage. Figure 2.2 shows the measured efficiency data from [100].

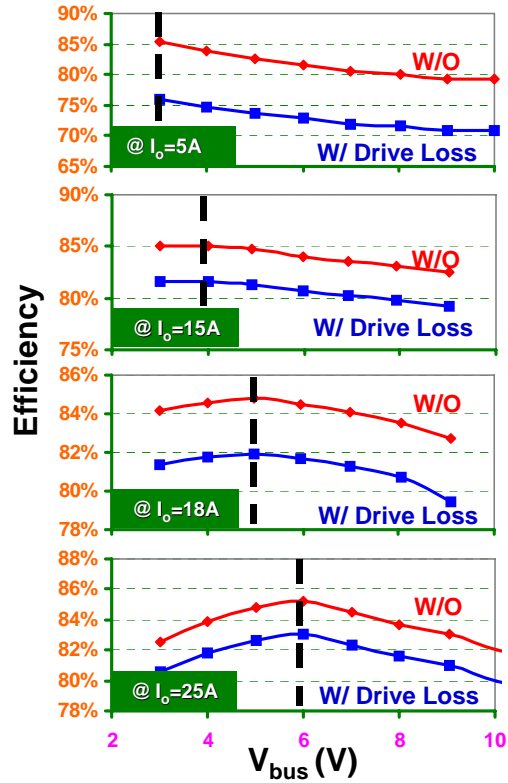


Figure 2.2 Experimental data showing that the optimal  $V_{bus}$  changes as the load changes [100].

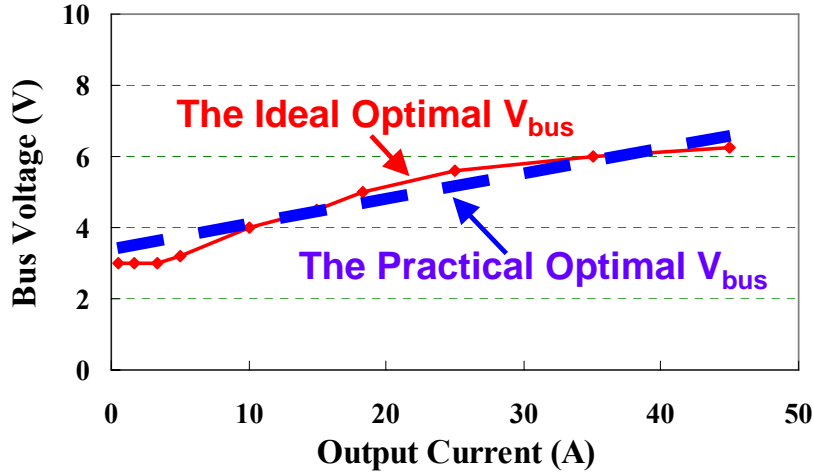


Figure 2.3  $V_{bus}$ - $I_O$  relationships [100].

With these data, the relationship between the optimal bus voltage (Optimal  $V_{bus}$ ) and the load current ( $I_O$ ) is found to be like Figure 2.3. In the analog control, it is very difficult to achieve the ideal optimal  $V_{bus}$  according to the load current, for that is the nonlinear relationship. Instead, the linear relationship, the practical optimal  $V_{bus}$  and the load current, can be implemented. Figure 2.4 shows the control strategy of the two stage ABVP-AVP voltage regulators. For the second stage, in order to achieve the load line characteristic which is specified by Intel [16], AVP control is employed. For the first stage, to increase the light-load efficiency, the bus voltage is modified with the load current information, which is ABVP. ABVP is the control that regulates the bus voltage proportional to the load current with the gain  $R_{tilt}$ , while AVP control regulates the output voltage inverse-proportional to the load current with the gain  $R_{droop}$ . Figure 2.5 shows the CPU power consumption and the ABVP control strategy. AVP is used for the output voltage regulation according to the specification and ABVP is used for light-load efficiency. Therefore, the AVP control is much more important than the ABVP control method. AVP should be optimized first and ABVP should be designed so that it does not degrade the AVP loop.

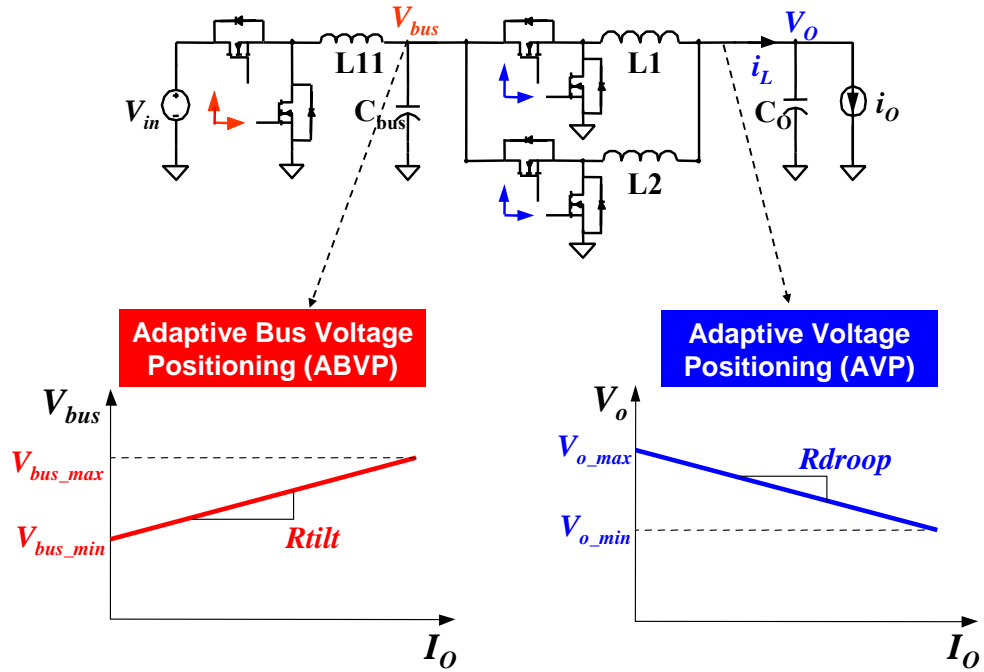


Figure 2.4 Control strategy of ABVP-AVP System.

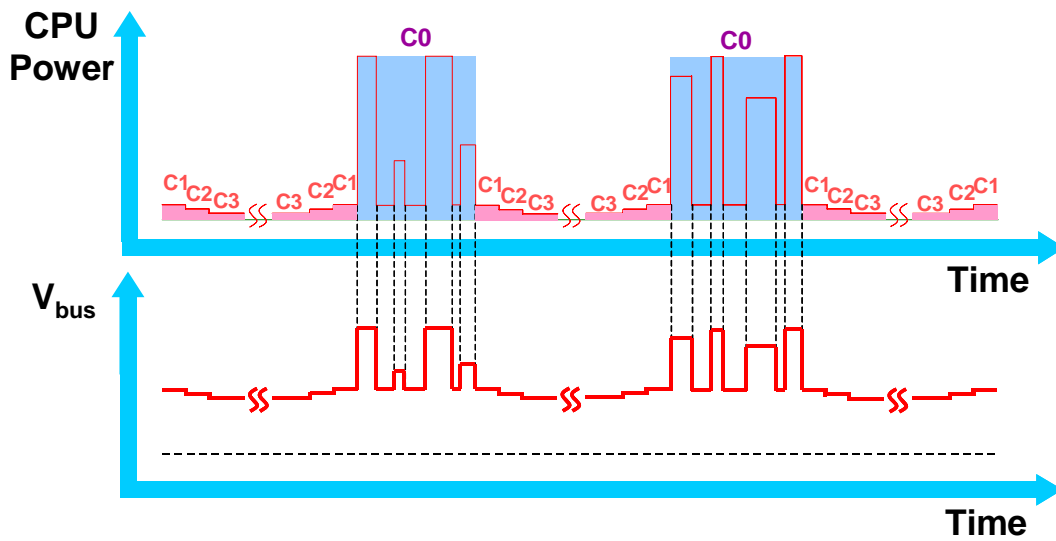


Figure 2.5 The CPU power consumption and the bus voltage following ABVP control strategy [100].

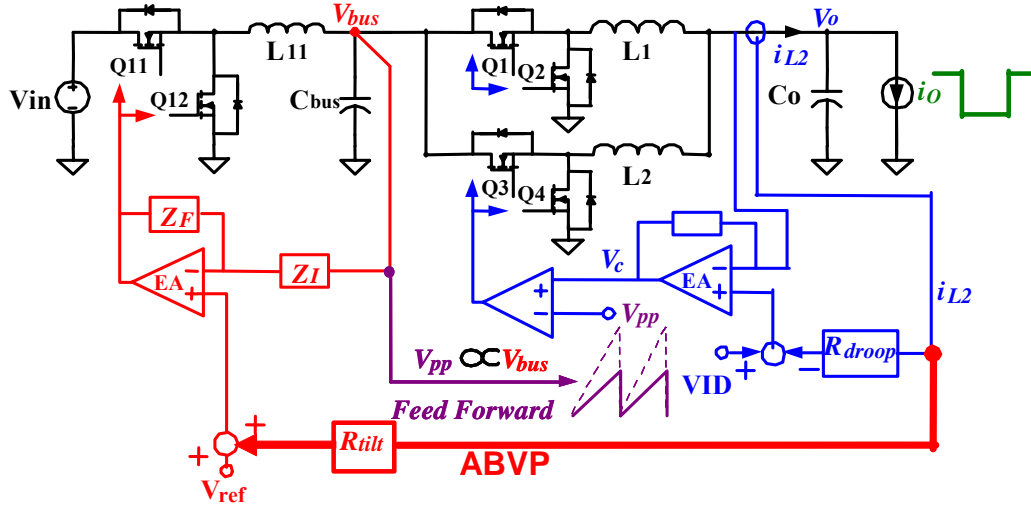


Figure 2.6 The control scheme for the ABVP-AVP system [100].

Figure 2.6 shows the proposed control schematic of the ABVP-AVP system used in [100]. It is a common practice for AVP that the inductor current is used instead of the load current because it is very difficult to sense the load current without any additional cost or power loss. In the second stage, the conventional AVP control is employed, which is discussed in Chapter 1. For the ABVP control, the second stage inductor current is fed back to the first stage instead of the load current, because the average value of the second stage inductor current is same as the load current during the steady state and the intent is to be efficient for the steady state. Thus, ABVP can be easily implemented without any additional load current sensing. In the second stage, to reduce the impact of the bus voltage change, the bus voltage feedforward loop is used. Once the load current increases ( $i_o$ ), the second stage inductor current increases ( $i_{L2}$ ), and the output voltage decreases for AVP ( $V_o$ ) while the bus voltage increases for ABVP ( $V_{BUS}$ ). Therefore, the control strategy in Figure 2.4 is implemented using the schematic in Figure 2.6.

Figure 2.7 shows the experimental results of an ABVP-AVP system like that in Figure 2.6 from [101]. The input voltage is 12V. The output voltage is transits from 1.28 to 1.3V as the load jumps from 0 to 20A, and the load-line impedance ( $R_{droop}=R_{LL}$ ) is designed to be  $1\text{m}\Omega$ . The bus voltage varies from 4.2 to 5.3V as the load changes from 20A to 0A, and the ABVP gain,  $R_{tilt}$  is designed to be  $50\text{m}\Omega$ . The inductance of the first stage is  $10\mu\text{H}$ . The inductance of the second stage is  $300\text{nH}$  for each phase. The switching frequency is  $200\text{kHz}$  for the first stage and  $1\text{MHz}$  for the second stage. The bus capacitance is  $1154\mu\text{F}$  with the first stage bandwidth  $2\text{kHz}$  and the output capacitance is  $1.08\text{mF}$  with  $80\text{kHz}$  bandwidth. It can be seen that the bus voltage

jumps from 4V to 5V as the output current transits from 0A to 20A. Both ABVP and AVP functions are realized.

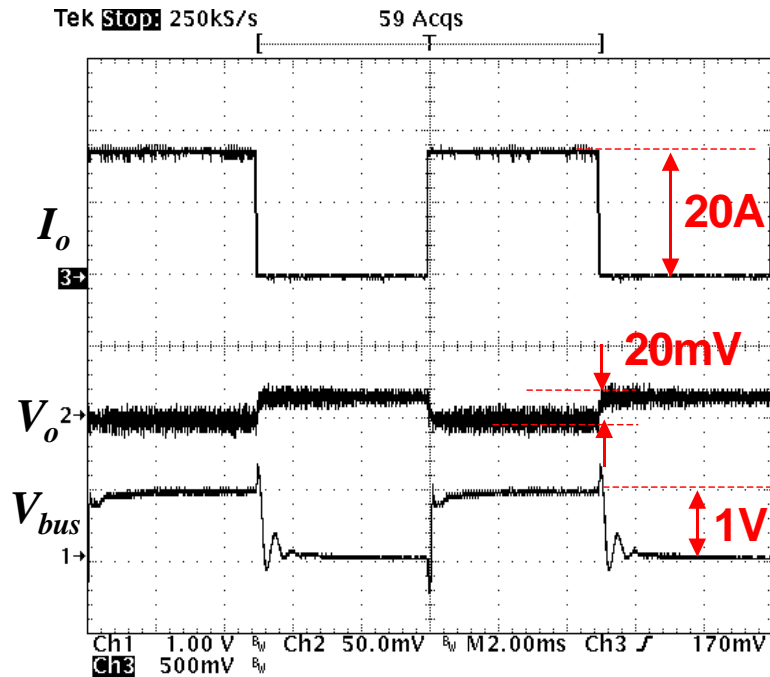


Figure 2.7 The experimental results of ABVP-AVP system (transient response) [100].

However, this implementation has some problems. The bandwidth of the first stage is too small as 2kHz with 200kHz switching frequency. Because of this, the bus capacitance is designed to be too large. Therefore, the size and cost is not so attractive, although the output capacitance is reduced from 1.6mF to 1.08mF. Furthermore, the dynamic performance of the ABVP is limited. This is discussed in the next section.

## 2.2. Dynamics and Stability of ABVP-AVP System

### 2.2.1. Dynamic Performance of ABVP-AVP System

The intent of using ABVP control is to position  $V_{bus}$  according to  $I_o$  at any time. However, when the CPU is in active mode, the software can create  $I_o$  transients with all possible amplitudes and recurrence frequencies up to several MHz. How the ABVP-AVP VR responds to various  $I_o$  transients is an interesting aspect to examine. This is described well in [100] and this section is the summary of [100].



The AVP load line describes the relationship between  $V_O$  and  $I_O$ . In the frequency domain, to achieve the load line the transfer function  $Z_O(s)=V_O(s)/I_O(s)$  is designed to be *Rdroop* [60][61][62][63][64][65][66][67][68]. Similarly, the ABVP describes the relationship between  $V_{bus}$  and  $I_O$ . A good way to achieve ABVP is to design the transfer function  $Z_{bus}(s)=V_{bus}(s)/I_O(s)$  to be *Rtilt* like Figure 2.8. If the transfer functions were constant for the entire frequency range, the bus voltage and the output voltage would follow the load current perfectly. However, this is not practical. In the real implementation, there are the bandwidths of the controllers to consider, and the transfer functions are only constant within their bandwidths. Figure 2.9 (a) shows the simulated transfer function  $Z_O(s)$ ; Figure 2.9 (b) shows the simulated transfer function  $Z_{bus}(s)$ . In this design,  $Z_O(s)$  is designed to be *Rdroop* until the second stage bandwidth ( $f_{c2}$ ) and  $Z_{bus}(s)$  is designed to be *Rtilt* until the first stage bandwidth ( $f_{c1}$ ). For meaningful design, the first stage switching frequency is much lower than the second stage switching frequency. Therefore, the first stage bandwidth is much lower than the second stage bandwidth.

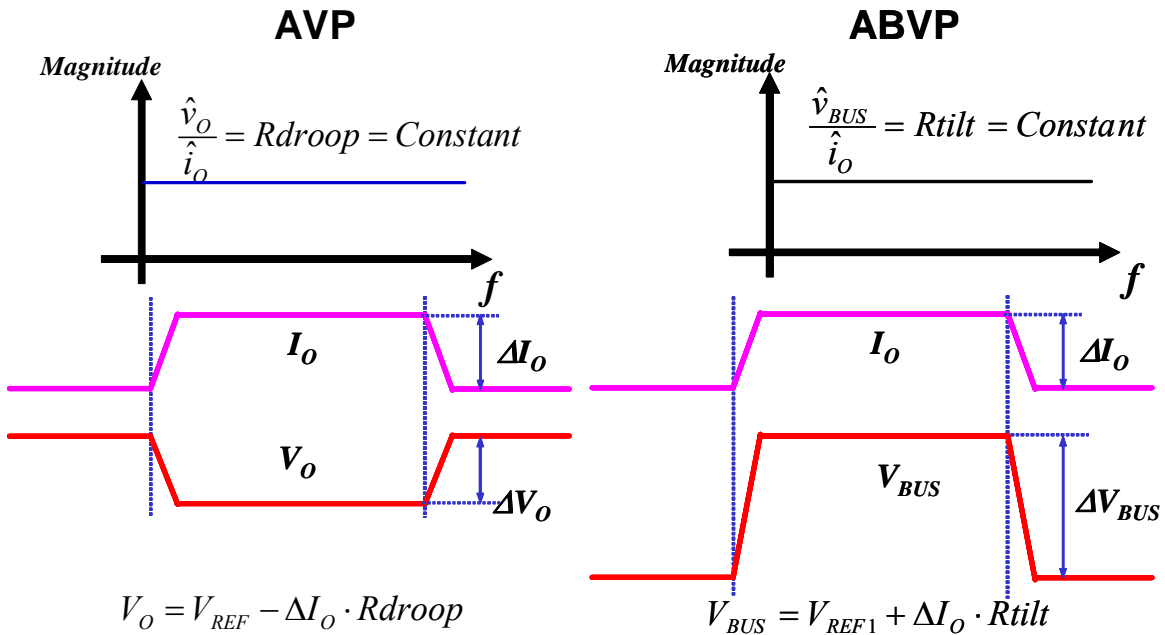
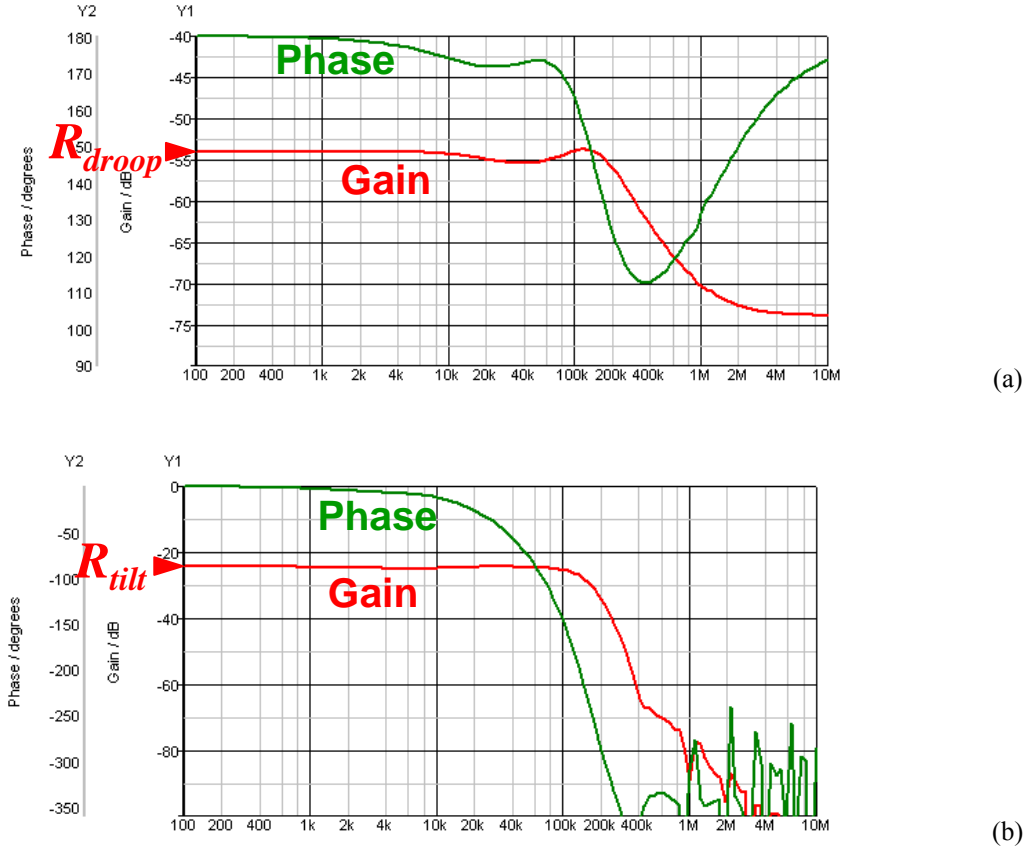


Figure 2.8 Desired dynamics of the output voltage and the bus voltage.



**Figure 2.9** Frequency-domain representations of the ABVP-AVP system: (a) AVP, and (b) ABVP [100].

When the load current transient recurrence frequency ( $f_{lo}$ ) is lower than  $f_{c1}$ ,  $f_{lo} < f_{c1} < f_{c2}$ . Then the first and the second stages are both fast enough to catch up with the load transient. Figure 2.10 shows the simulation waveforms. The load transients have random amplitudes, but the recurrence frequencies are low.  $i_{L1}$  is one phase inductor current of the second stage.  $i_L$  is 1/3 of the instantaneous  $I_O$  with the addition of some switching ripple. At any  $I_O$ ,  $V_{bus}$  is set at the value determined by the  $V_{bus}$ - $I_O$  line shown in Figure 2.4.  $V_{bus}$  is always optimal in this scenario.  $V_O$  is set at the value determined by the load line shown in Figure 2.4.

When the  $I_O$  transient recurrence frequency  $f_{lo}$  is higher than  $f_{c2}$ ,  $f_{c1} < f_{c2} < f_{lo}$ . Then the load transient is too fast to respond to for both the first and the second stages. Figure 2.11 shows the simulation transient response of the ABVP-AVP system. Compared with Figure 2.10,  $I_O$  has an additional 5MHz transient during  $t_a \sim t_b$ . During this period, the second stage inductor current cannot follow the load transient because of its bandwidth limitation.  $i_{L1}$  follows the average value of the load current and  $V_{bus}$  is set at the value determined by the  $V_{bus}$ - $I_O$  line shown in Figure 2.4,

according to the average value of  $I_O$ .  $V_{bus}$  is also always optimal in this scenario.  $V_O$  is set at the value determined by the load line shown in Figure 2.4, according to the average value of  $I_O$ .

When the  $I_O$  transient reoccurrence frequency  $f_{lo}$  is between  $f_{c1}$  and  $f_{c2}$ ,  $f_{c1} < f_{lo} < f_{c2}$ . Then the second stage is able to respond to the  $I_O$  transient, while the first stage cannot. In this simulations, the first stage switching frequency is 370KHz and its control bandwidth is  $f_{c1}=60$ KHz; and the second stage switching frequency is 1MHz and its control bandwidth is  $f_{c2}=160$ KHz. As shown in Figure 2.12,  $I_O$  swings between 50A and 5A at a 100KHz reoccurrence frequency, and  $i_{LI}$  is able to respond to the 100KHz  $I_O$  transient. As a result,  $i_{LI}$  is 1/3 of the instantaneous value of  $I_O$  with the addition of some switching ripple. Although the second stage sees the instantaneous  $I_O$ , the first stage is not fast enough to respond to the 100KHz transient power drawn by the second stage, so  $i_{LII}$  is still the result of the average  $I_O$ . Because the first and the second stages see  $I_O$  in two different ways, there is not an optimal  $V_{bus}$  defined for this scenario. It can be seen that the first stage tries to adjust  $V_{bus}$  according to the instantaneous value of  $I_O$ , but cannot quite do it due to the limited  $f_{c1}$ .  $V_{bus}$  then has a 100KHz ripple on top of the DC value determined by the average  $I_O$ . Meanwhile,  $V_O$  is set at the value determined by the load line shown in Figure 2.4, according to the instantaneous value of  $I_O$ .

Therefore, in order to maximize the optimal range in the ABVP-AVP system, the first stage bandwidth should be designed to be as large as possible. Keeping in mind the experimental results in [101], the first stage bandwidth is only 2kHz with 200kHz switching frequency, whereas the second stage bandwidth is 80kHz. In this case, the ABVP-AVP system is not optimized for the load when the load transient reoccurrence frequency is 2kHz~80kHz. The first stage bandwidth needs to be enlarged.

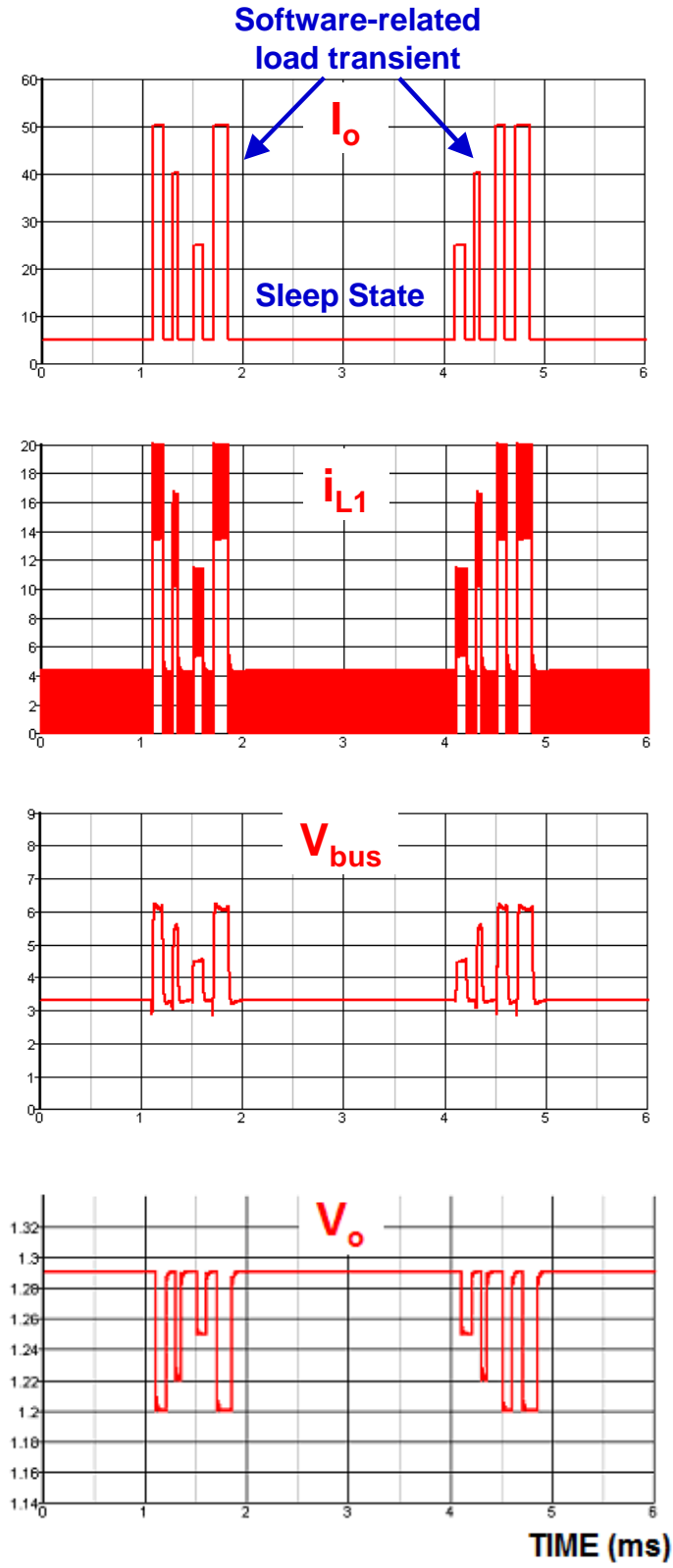


Figure 2.10 The ABVP-AVP response when  $f_{l0} < f_{c1} < f_{c2}$  [100].

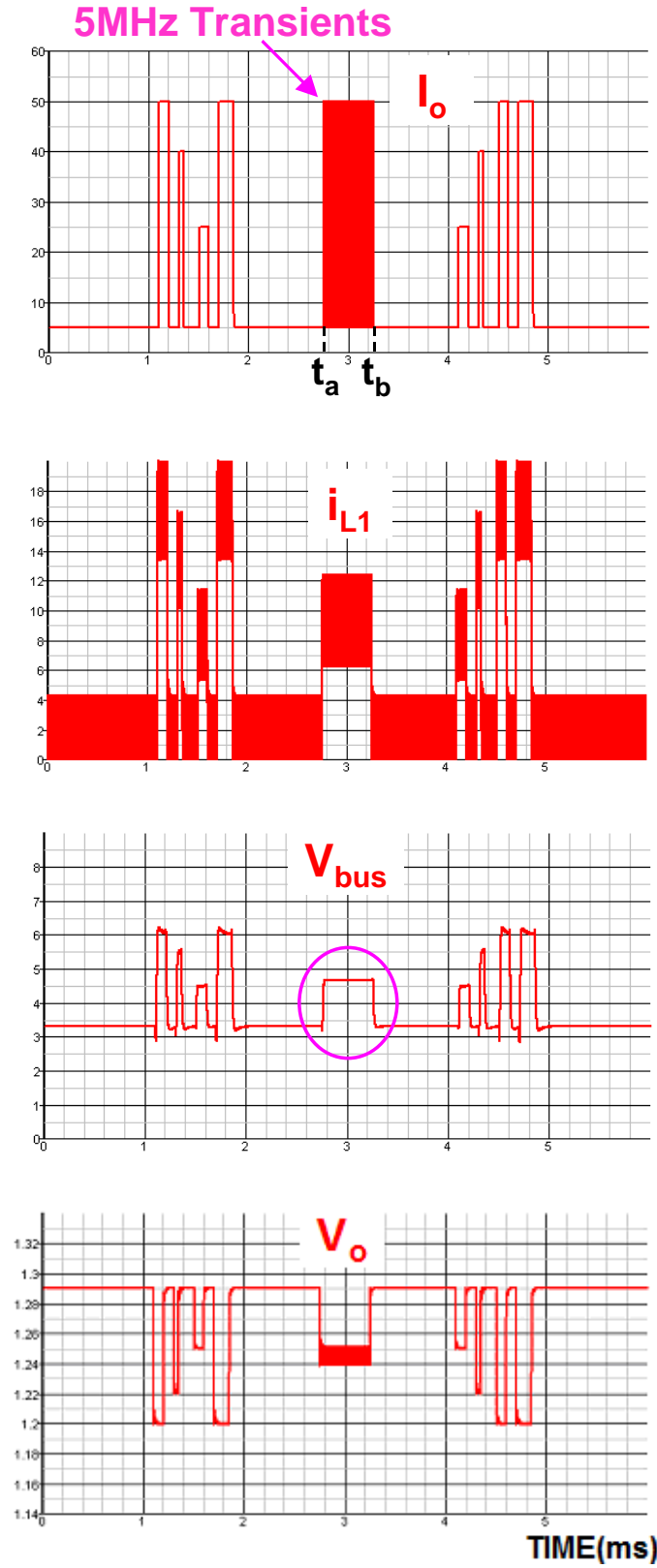


Figure 2.11 The ABVP-AVP response when  $f_{c1} < f_{c2} < f_{lo}$  [100].

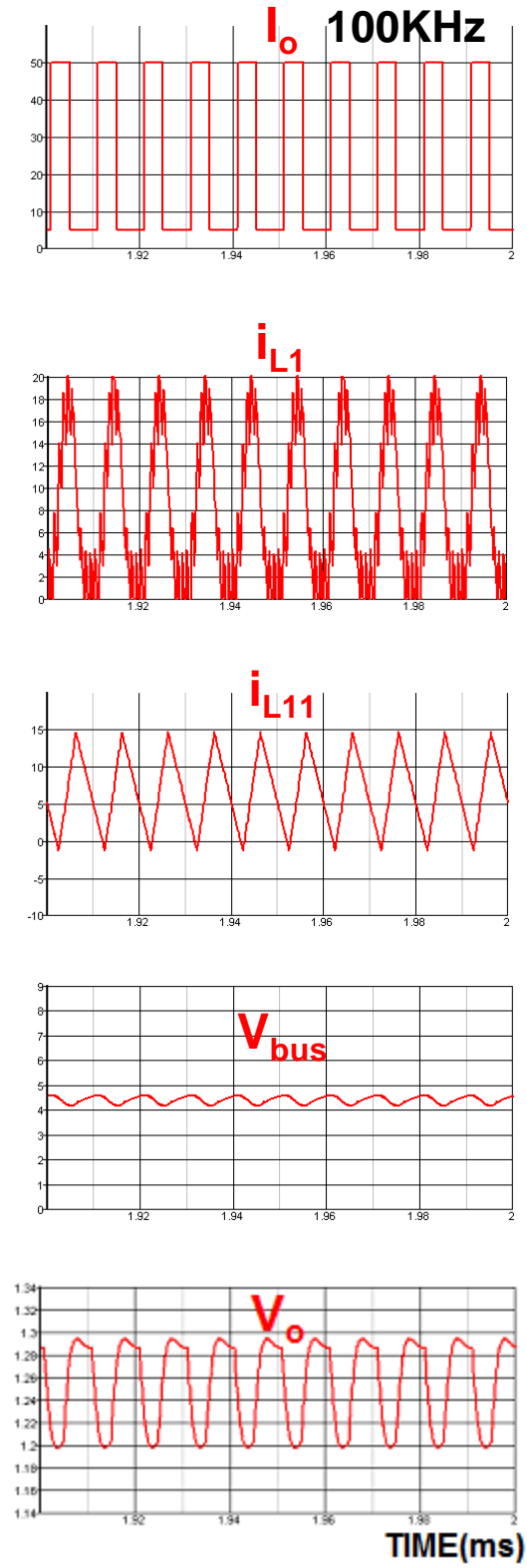


Figure 2.12 The ABVP-AVP response when  $f_{c1} < f_{Io} < f_{c2}$  [100].

### 2.2.2. Stability Issue in ABVP-AVP System

In the previous section, it is concluded that the first stage bandwidth ( $f_{c1}$ ) is very important for ABVP performance, and it should be designed to be larger to get better performance. In this section, the two-stage hardware is built with a large  $f_{c1}$ . The first stage bandwidth ( $f_{c1}$ ) is 25kHz with 200kHz switching frequency, and the second stage bandwidth ( $f_{c2}$ ) is 80kHz with 500kHz switching frequency. The bus capacitance is 176 $\mu$ F and the output capacitance is 940 $\mu$ F. The input voltage is 12V. The load line impedance ( $R_{droop}=R_{LL}$ ) is designed to be 2m $\Omega$ . The inductance of the first stage is 10 $\mu$ H. The inductance of the second stage is 300nH for each phase.

Compared to the ABVP-AVP hardware in the last section, the first stage bandwidth is increased more than ten times from 2kHz to 25kHz with the same switching frequency of 200kHz, and the bus capacitance is reduced from 1154 $\mu$ F to 176 $\mu$ F. Figure 2.13 (a) is the measured bus voltage waveform of the two-stage VR without the ABVP loop. The bus voltage is stable. However, when the ABVP loop is closed as it is in Figure 2.6 ( $R_{tilt}=125\text{m}\Omega$ ), the bus voltage becomes unstable as in Figure 2.13 (b). Both cases are the same except for the ABVP loop. Comparing Figure 2.13 (a) and Figure 2.13 (b), it is observed that the ABVP loop causes this instability issue. Comparing this hardware to the ABVP-AVP hardware with 2kHz  $f_{c1}$ , it is found that by reducing  $f_{c1}$ , the system can be stabilized. Therefore, it is expected that the maximum  $f_{c1}$  is determined by the stability and in order to design the ABVP-AVP system, the instability loop should be identified.

It is not so difficult to find the loop which makes the system unstable because there is a positive inductor current feedback from the second stage to the first stage. In Figure 2.6, if the load current increases ( $i_o$ ), the second stage inductor current increases ( $i_{L2}$ ), and the ABVP loop will increase the bus voltage ( $V_{bus}$ ). The bus voltage in turn will increase the second stage inductor current ( $i_{L2}$ ), which makes the bus voltage larger again, and this is the positive feedback loop. To quantify this positive feedback loop and to design a stable system, the model should be derived for the stability analysis and the system should be designed carefully.

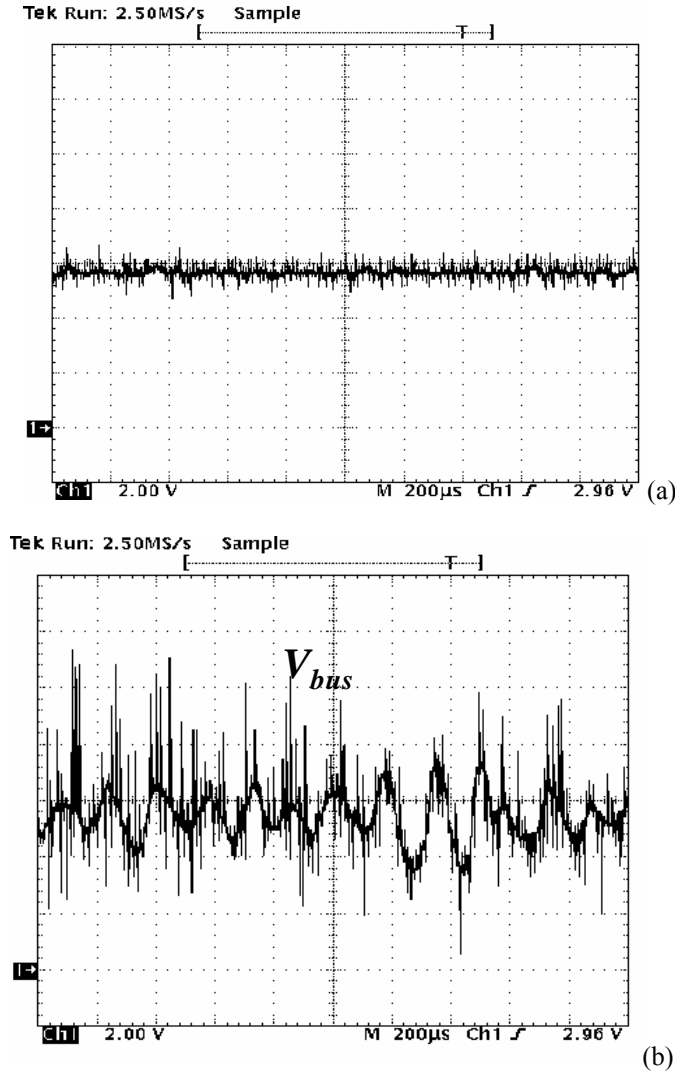


Figure 2.13 The bus voltage waveforms (measured) (a) Without ABVP loop (b) With ABVP loop.

### 2.3. Small-Signal Modeling and Analysis

The small-signal model is a very powerful tool to design the converter control loop. This tool matches the real hardware experimental results within the half of the switching frequency when linear control is used [124][125][126][132]. In this section, this small-signal model is used to model and analyze the ABVP-AVP system. In Section 2.3.1, the conventional small-signal models from [124][125][126][132] are used to model the ABVP-AVP system. In Section 2.3.2, the new small-signal model for the feedforward loop is derived. Using these models, the stability and the dynamics of the ABVP-AVP system will be analyzed in Section 2.3.3.



### 2.3.1. Small-Signal Model of ABVP-AVP System

Figure 2.14 shows the small-signal block diagram of ABVP-AVP system. The first stage consists of the voltage loop ( $T_{V1}$ ) only [124][125][126] and the second stage consists of AVP control loops ( $T_2$ ,  $T_{V2}$ ,  $T_{I2}$ ) [64][65][66]. The interaction loop between the first stage and the second stage is  $T_m$ . Each block operates according to the following equations,

$G_{vd1}$  is the transfer function from the first stage duty cycle to the bus voltage;

$$G_{VD1} = \frac{V_{IN} \cdot (1 + R_{C\_BUS} \cdot C_{BUS} \cdot s)}{\Delta l(s)} \quad (2.1)$$

where  $R_{C\_BUS}$  is the ESR of the bus capacitors and  $C_{BUS}$  is the capacitance of the bus capacitors.

$$\Delta l(s) = 1 + s / (Q1 \cdot \omega_{o1}) + s^2 / \omega_{o1}^2 \quad (2.2)$$

where  $\omega_{o1} \approx \frac{1}{\sqrt{C_{BUS} \cdot L11}}$ ,  $Q1 \approx \frac{\sqrt{L11/C_{BUS}}}{DCR1 + R_{C\_BUS}}$ ,  $L11$  is the first stage inductance, and  $DCR1$  is the parasitic DC resistance of the first stage inductor.

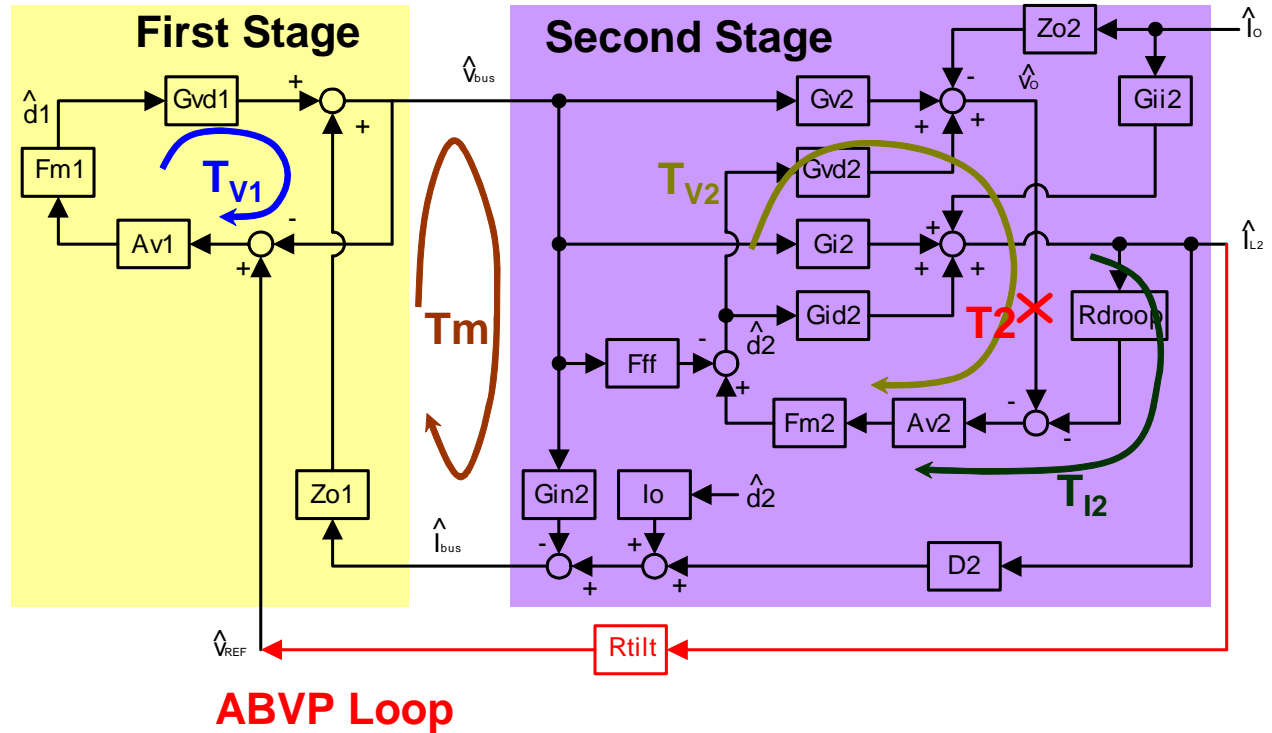


Figure 2.14 The small-signal model of ABVP-AVP system.

$Fm1$  is the modulator gain of the first stage controller;

$$Fm1 = \frac{1}{V_{RAMP1}} \quad (2.3)$$

where  $V_{RAMP1}$  is the ramp voltage magnitude of the first stage controller.

$Av1$  is the first stage voltage loop compensator. Generally, a three-pole two-zero compensator is used for the voltage model control [126].

$Zo1$  is the open loop output impedance of the first stage;

$$Z_{o1} = DCR1 \cdot \frac{(1 + s \cdot DCR1 / L1) \cdot (1 + s \cdot R_{C\_BUS} \cdot C_{BUS})}{\Delta1(s)} \quad (2.4)$$

Then the first stage voltage loop is

$$T_{V1} = F_{M1} \cdot G_{VD1} \cdot A_{V1} \quad (2.5)$$

$Gv2$  is the transfer function from the bus voltage to the output voltage;

$$G_{V2} = \frac{D2 \cdot (1 + R_C \cdot C \cdot s)}{\Delta2(s)} \quad (2.6)$$

where  $R_C$  is the ESR of the output capacitors,  $C$  is the capacitance of the output capacitors, and  $D2$  is the steady state duty cycle of the second stage.

$$\Delta2(s) = 1 + s / (Q2 \cdot \omega_{O2}) + s^2 / \omega_{O2}^2 \quad (2.7)$$

where  $\omega_{O2} \approx \frac{1}{\sqrt{C \cdot Le}}$ ,  $Q2 \approx \frac{\sqrt{Le/C}}{DCR2 + R_C}$ ,  $Le = \frac{L1 + L2}{2}$ ,  $L1$  is the second-stage first phase inductance,  $L2$  is the second-stage second phase inductance, and  $DCR2$  is the parasitic DC resistance of the second stage inductor.

$Gvd2$  is the transfer function from the second stage duty cycle to the output voltage;

$$G_{VD2} = \frac{V_{BUS} \cdot (1 + R_C \cdot C \cdot s)}{\Delta2(s)} \quad (2.8)$$

where  $V_{bus}$  is the steady state bus voltage.

$G_{I2}$  is the transfer function from the bus voltage to the second stage inductor current;

$$G_{I2} = \frac{D2 \cdot (1 + R_O \cdot C \cdot s)}{R_O \cdot \Delta 2(s)} \quad (2.9)$$

where  $R_O$  is the load resistance.

$G_{ID2}$  is the transfer function from the second stage duty cycle to the second stage inductor current;

$$G_{ID2} = \frac{V_{BUS} \cdot (1 + R_O \cdot C \cdot s)}{R_O \cdot \Delta 2(s)} \quad (2.10)$$

$G_{II2}$  is the transfer function from the load current to the second stage inductor current;

$$G_{II2} = \frac{(1 + R_C \cdot C \cdot s)}{\Delta 2(s)} \quad (2.11)$$

$Z_{O2}$  is the open loop output impedance of the second stage;

$$Z_{O2} = DCR2 \cdot \frac{(1 + s \cdot DCR2 / Le) \cdot (1 + s \cdot R_C \cdot C)}{\Delta 2(s)} \quad (2.12)$$

$A_{V2}$  is the second stage AVP loop compensator. A two-pole one-zero compensator is used to get the constant output impedance [64][65][66].

$F_{FF}$  is the feedforward gain of the second stage and  $F_{M2}$  is the modulator gain of the second stage with the feedforward loop. The small-signal models for these will be discussed in the next section.

Then the second stage voltage loop is;

$$T_{V2} = F_{M2} \cdot G_{VD2} \cdot A_{V2} \quad (2.13)$$

The second stage current loop is;

$$T_{I2} = F_{M2} \cdot G_{ID2} \cdot A_{V2} \cdot R_{droop} \quad (2.14)$$

and the second stage system loop is;

$$T2 = \frac{T_{V2}}{1 + T_{I2}} \quad (2.15)$$

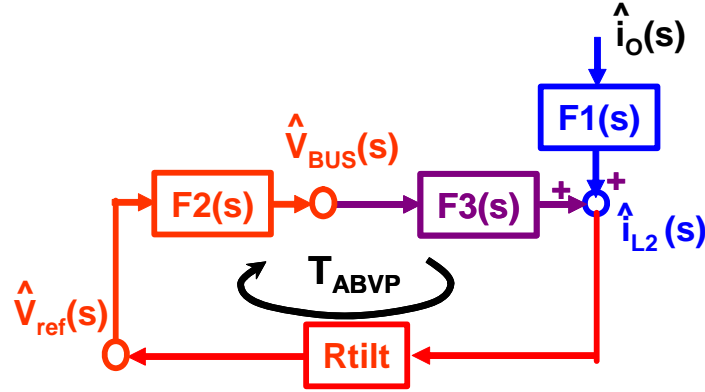


Figure 2.15 Simplified small-signal block diagram of ABVP-AVP system.

$T_m$  is the interaction loop between the first stage and the second stage. The main concern in this section is the instability loop due to the ABVP loop. Thus, assuming the first stage and second stage loops are well-designed following [64][65][66][124][125][126], and there is no interaction between the first stage and the second stage ( $T_m \ll 1$ ), the bus voltage is stable as in Figure 2.13 (a) without the ABVP loop and the bus voltage will exactly follow the reference voltage of the first stage and the second-stage AVP is achieved with the constant impedance. Then the complicated small-signal block diagram in Figure 2.14 can be simplified to one like Figure 2.15. This consists of four blocks,

- $F1(s)$  is the transfer function from the load current to the second-stage inductor current with the AVP loop closed.
- $F2(s)$  is the transfer function from the first-stage reference voltage to the bus voltage with the first-stage voltage loop closed.
- $F3(s)$  is the transfer function from the bus voltage to the second-stage inductor current with the AVP loop and feedforward loop closed.
- $R_{tilt}$  is the constant ABVP gain.

Thus the closed-loop transfer function from the load current to the bus voltage ( $Z_{bus}(s)$ ) is (2.16). This transfer function is very important because the purpose of the ABVP loop is to regulate the bus voltage according to the load current. The dynamics of the bus voltage according to the load current can be predicted with this transfer function and the stability of the ABVP system can be also observed in this transfer function because it contains the system eigen values.

$$\frac{\hat{v}_{BUS}(s)}{\hat{i}_O(s)} = Z_{bus}(s) = \frac{F1(s) \cdot F2(s) \cdot R_{tilt}}{1 - F2(s) \cdot F3(s) \cdot R_{tilt}} \quad (2.16)$$

and the ABVP loop gain is;

$$T_{ABVP} = F2(s) \cdot F3(s) \cdot R_{tilt} \quad (2.17)$$

Assuming the two-stage system without the ABVP loop is stable,  $F1(s)$ ,  $F2(s)$ , and  $F3(s)$  are well-defined functions which are finite. Therefore the positive feedback loop  $T_{ABVP}$  determines the stability of the ABVP system. To know the value of  $T_{ABVP}$ ,  $F1(s)$ ,  $F2(s)$ , and  $F3(s)$  should be derived.

$F2(s)$  can be easily derived from the small-signal model of the first stage, as in (2.18). Figure 2.16 shows the control schematic of the first stage and the shape of  $F2(s)$ .  $F2(s)$  is 0dB until it reaches the bandwidth of the first stage control loop.

$$F2(s) = \frac{\hat{v}_{BUS}}{\hat{v}_{REF}} = \frac{T_{V1}}{1 + T_{V1}} \quad (2.18)$$

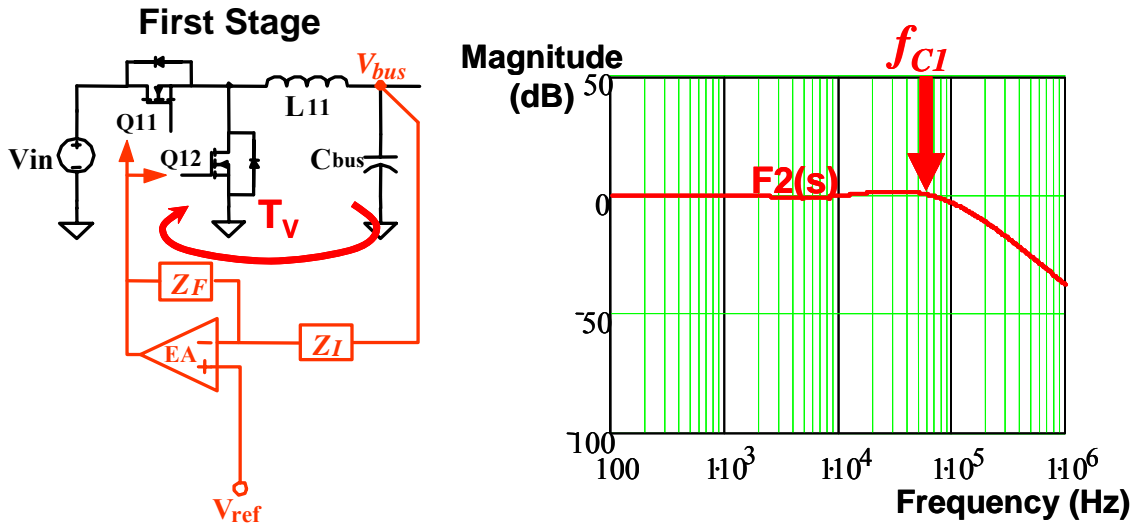
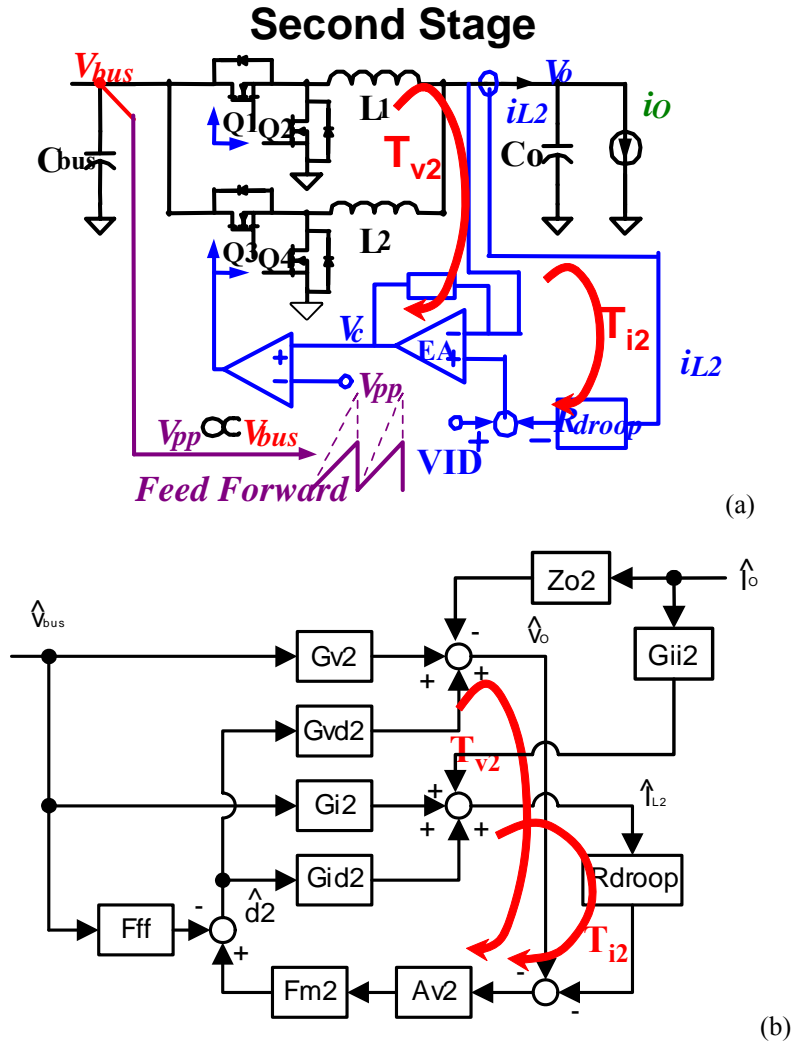


Figure 2.16 The transfer function from the first-stage reference voltage to the bus voltage with the first-stage voltage loop closed;  $F2(s)$ .



**Figure 2.17** The second stage small-signal model (a) The second stage control schematics (b) The small-signal block diagram.

$F1(s)$  and  $F3(s)$  can be derived from the small-signal model of the second stage as in (2.19) and (2.20). Figure 2.17 shows the control schematic of the second stage and the small-signal block diagram. In order to know  $F3(s)$ , the feedforward gain ( $F_{FF}$ ) should be derived.

$$F1(s) = \frac{\hat{i}_{L2}(s)}{\hat{i}_o(s)} = \frac{G_{I12} + \left( G_{I12} + \frac{G_{ID2} \cdot Z_{O2}}{G_{VD2}} \right) \cdot T_{V2}}{(1+T2) \cdot (1+T_{I2})} \quad (2.19)$$

$$F3(s) = \frac{\hat{i}_{L2}(s)}{\hat{v}_{BUS}(s)} = \frac{G_{I2} - F_{FF} \cdot G_{ID2}}{(1+T2) \cdot (1+T_{I2})} \quad (2.20)$$

### 2.3.2. Feedforward Small-Signal Model

In the ABVP-AVP system, in order to reduce the impact of the bus voltage dynamics on the second stage, the bus voltage feedforward loop is used [100]. Figure 2.18 (a) shows the implementation of the bus voltage feedforward from [133][134]. The bus voltage is sensed and converted to the current with the current mirror gain  $k$ . This current charges the ramp capacitor ( $C_r$ ) and the capacitor voltage increases. The external clock is used to reset the ramp voltage with the constant frequency. Therefore, the ramp slope or the ramp peak voltage is proportional to the bus voltage and by modifying this ramp the impact of the bus voltage dynamics on the second stage is reduced.

Figure 2.18 (b) shows the ramp waveform. At the time  $(N-1)Ts$ , the clock resets the ramp voltage and the ramp voltage starts to increase with the slope in proportion to the bus voltage. When the ramp voltage meets the control voltage ( $v_c(t)$ ), the duty cycle is made. This duty cycle ( $d_N$ ) can be calculated by (2.21);

$$v_c(t) = \frac{1}{C_r} \cdot \int_{(N-1)Ts}^{(N-1)Ts+d_N \cdot Ts} [k \cdot v_{BUS}(\tau)] \cdot d\tau \quad (2.21)$$

In [133][134], the small-signal feedforward gain model is derived from (2.21), which, like (2.22) is based on the small signal and the linearity assumptions;

$$F_M = \frac{C_r}{k \cdot Ts \cdot V_{BUS}}, \quad F_{FF} = \frac{D}{V_{BUS}} \quad (2.22)$$

With this feedforward model,  $F3(s)$  can be calculated,

$$F3(s) = \frac{\hat{i}_{L2}(s)}{\hat{v}_{BUS}(s)} = \frac{G_{I2} - F_{FF} \cdot G_{ID2}}{(1+T2) \cdot (1+T_{I2})} = 0 \quad (2.23)$$

$$\text{where } G_{I2} - F_{FF} \cdot G_{ID2} = \frac{D \cdot (1+R_O \cdot C \cdot s)}{R_O \cdot \Delta 2(s)} - \frac{D}{V_{BUS}} \cdot \frac{V_{BUS} \cdot (1+R_O \cdot C \cdot s)}{R_O \cdot \Delta 2(s)} = 0.$$

According to this feedforward model,  $F3(s)$  is then zero and  $T_{ABVP}$  is zero too, which means the feedforward loop completely cancels the impact from the bus voltage to the second stage. However, this is not true. When the bus voltage changes, the second-stage inductor current also

changes, and the system becomes unstable. Therefore a more practical and accurate feedforward model is necessary.

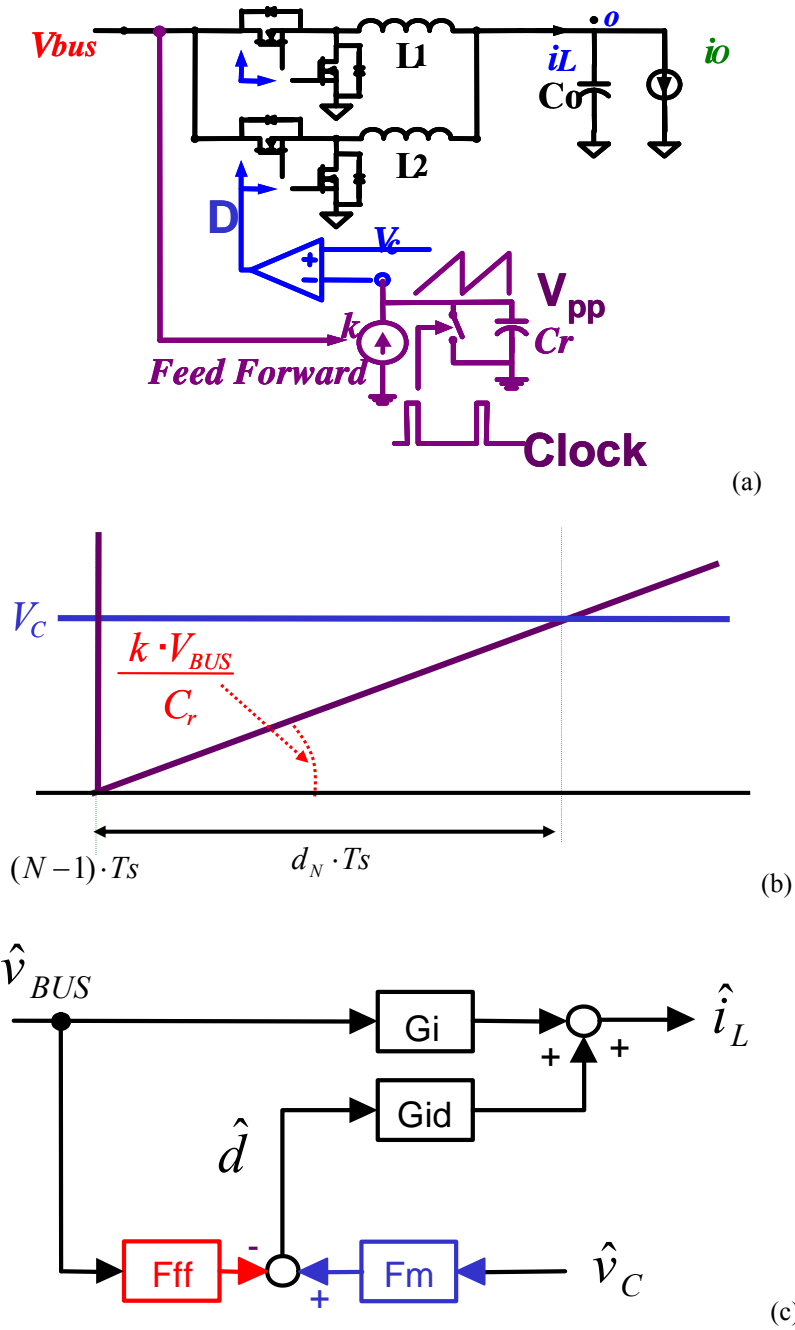
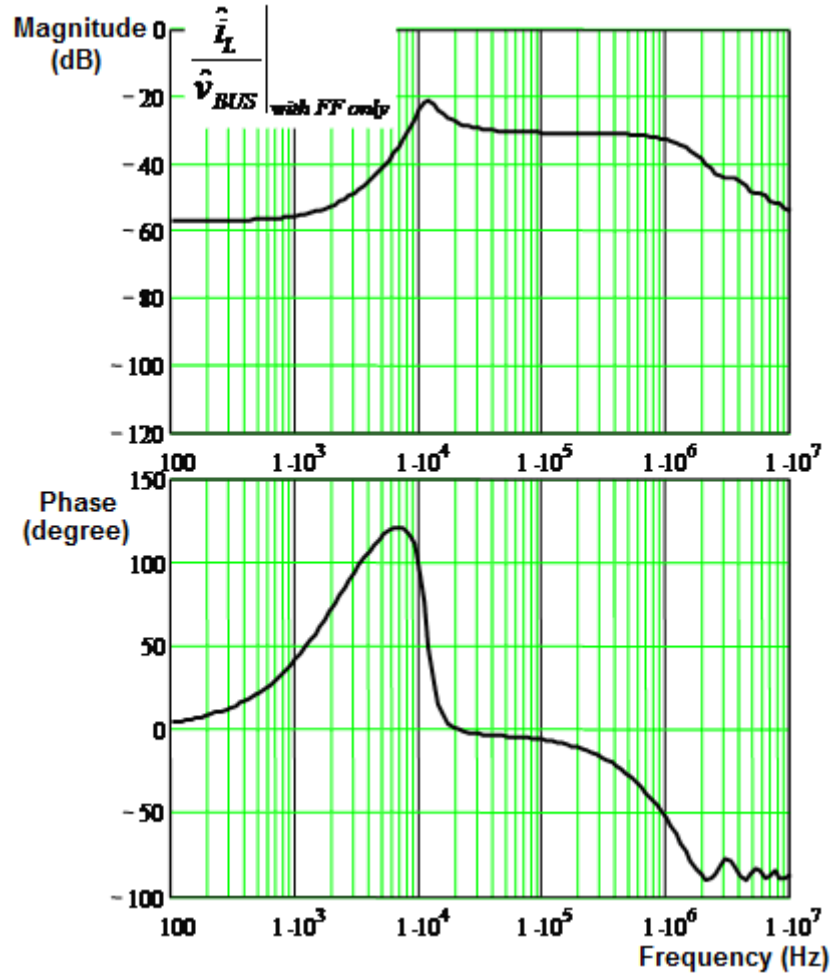


Figure 2.18 The implementation of the bus voltage feedforward loop -  
 (a) The schematics (b) The waveform of the ramp (c) The small-signal block diagram.





**Figure 2.19** The SIMPLIS simulation results of the transfer function from the bus voltage to the second stage inductor current with only the feedforward loop closed.

To evaluate the feedforward model, the system is simulated with only the feedforward loop closed like in Figure 2.18 (a). The transfer function from the control voltage to the inductor current is;

$$\left. \frac{\hat{i}_{L2}(s)}{\hat{v}_{BUS}(s)} \right|_{\text{with FF only}} = G_{I2} - F_{FF} \cdot G_{ID2} \quad (2.24)$$

Figure 2.19 shows the SIMPLIS simulation results of this circuit. With the feedforward model in (2.22), (2.24) is zero whereas there is gain in Figure 2.19.

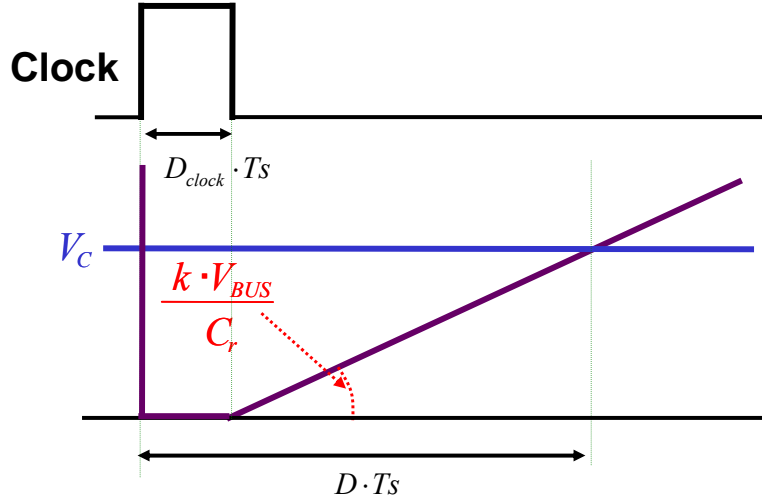


Figure 2.20 The bus voltage feedforward loop and the duty cycle loss from the clock.

In the real implementation, there is the holding time when the clock is on ( $D_{clock} \cdot T_s$ ) during which the switch in Figure 2.18 (a) is turned on and the feedforward ramp remains zero, as in Figure 2.20. Because of this duty cycle loss, the feedforward model is changed to (2.25),

$$F_M = \frac{C_r}{k \cdot T_s \cdot V_{BUS}}, \quad F_{FF} = \frac{D - D_{clock}}{V_{BUS}} \quad (2.25)$$

With this model, the transfer function is not zero,

$$\begin{aligned} \left. \frac{\hat{i}_{L2}(s)}{\hat{v}_{BUS}(s)} \right|_{\text{with FF only}} &= G_{I2} - F_{FF} \cdot G_{ID2} \\ &= \frac{D \cdot (1 + R_O \cdot C \cdot s)}{R_O \cdot \Delta 2(s)} - \frac{D - D_{clock}}{V_{BUS}} \cdot \frac{V_{BUS} \cdot (1 + R_O \cdot C \cdot s)}{R_O \cdot \Delta 2(s)} \\ &= \frac{D_{clock} \cdot (1 + R_O \cdot C \cdot s)}{R_O \cdot \Delta 2(s)} \end{aligned} \quad (2.26)$$

Figure 2.21 shows the comparison between the modified model (2.26) and the SIMPLIS simulation results. The model and the simulation results match at the lowest frequency; however, the model still differs at the higher frequencies. With this model, it is observed that by decreasing the clock on time, the bus voltage-changing effect on the second-stage inductor current can be reduced.

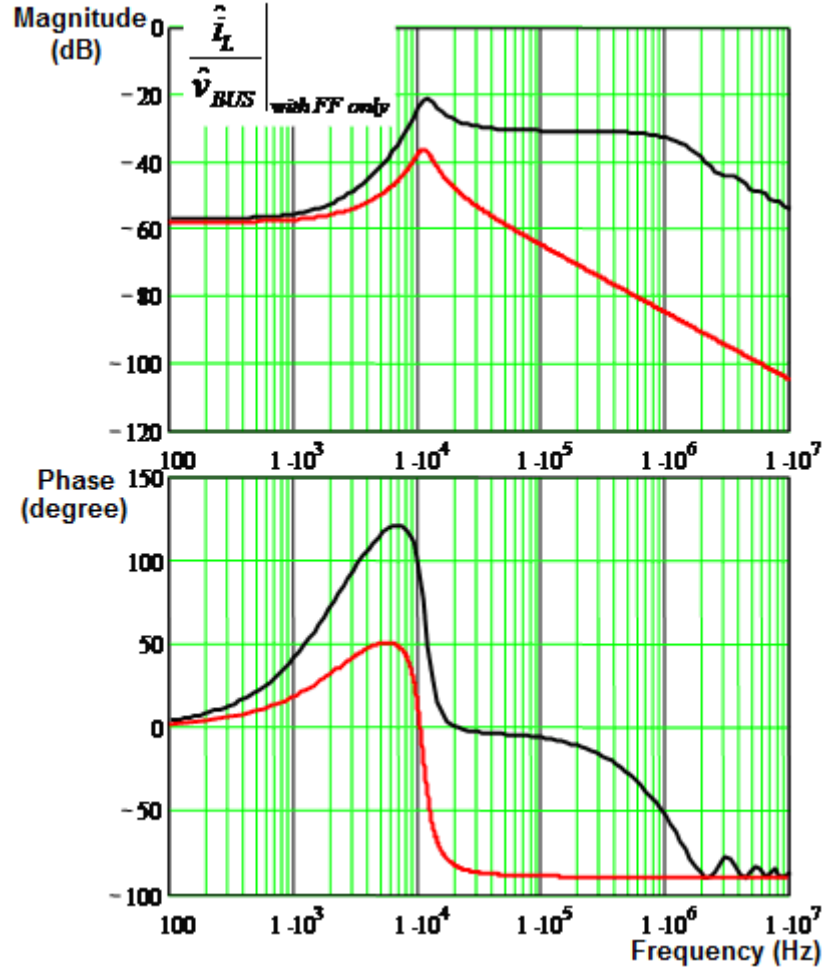


Figure 2.21 The transfer function from the bus voltage to the second-stage inductor current with only the feedforward loop closed. (Black lines : SIMPLIS simulation, Red lines : equation (2.25))

In order to derive a more accurate feedforward model, the derivation starts from the nonlinear equation (2.21).

First, all the parameters are perturbed like Figure 2.22,

$$d_N = D + \hat{d}_N, \quad v_{BUS}(t) = V_{BUS} + \hat{v}_{BUS}(t), \quad v_C(t) = V_C + \hat{v}_C(t) \quad (2.27)$$

where,  $\hat{d}_N, \hat{v}_{BUS}(t), \hat{v}_C(t)$  are the small-signal perturbation, and  $D, V_{bus}, V_C$  are the steady state values.

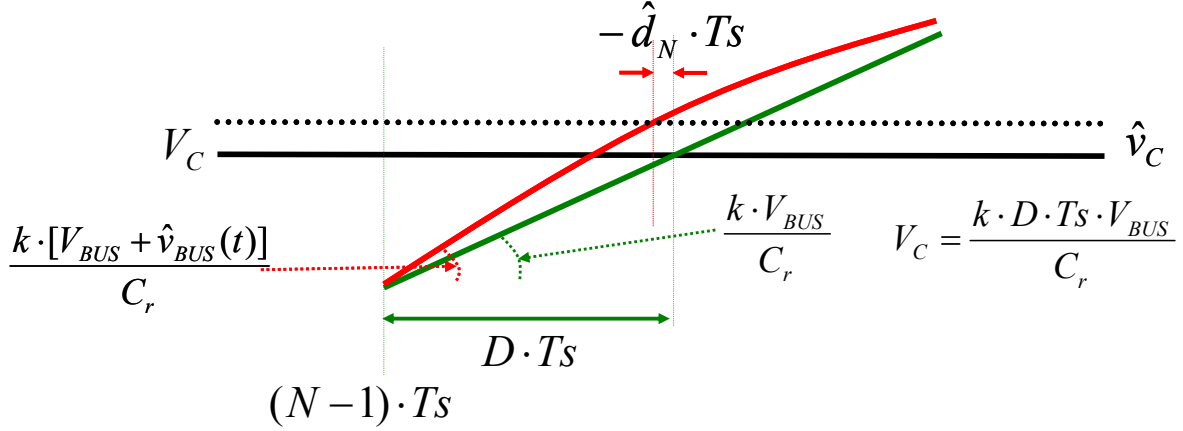


Figure 2.22 The bus voltage feedforward waveform with the perturbations.

By substituting (2.27) into (2.21), we have

$$V_C + \hat{v}_C(t) = \frac{1}{C_r} \cdot \int_{(N-1)Ts}^{(N-1)Ts + (D + \hat{d}_N)Ts} [k \cdot (V_{BUS} + \hat{v}_{BUS}(\tau))] \cdot d\tau \quad (2.28)$$

The equation (2.28) can be rewritten as,

$$V_C + \hat{v}_C(t) = \frac{k \cdot D \cdot Ts \cdot V_{BUS}}{C_r} + \frac{k \cdot Ts \cdot V_{BUS}}{C_r} \cdot \hat{d}_N + \frac{k}{C_r} \int_{(N-1)Ts}^{(N-1)Ts + D \cdot Ts} \hat{v}_{BUS}(\tau) \cdot d\tau + \frac{k}{C_r} \int_{(N-1)Ts + D \cdot Ts}^{(N-1)Ts + (D + \hat{d}_N)Ts} \hat{v}_{BUS}(\tau) \cdot d\tau \quad (2.29)$$

With the small-signal assumption, the last term becomes 0. Then the DC term and AC term can be separated;

$$V_C = \frac{k \cdot D \cdot Ts \cdot V_{BUS}}{C_r} \quad (2.30)$$

$$\hat{d}_N = \frac{C_r}{k \cdot Ts \cdot V_{BUS}} \cdot \hat{v}_C(t) - \frac{1}{Ts \cdot V_{BUS}} \int_{(N-1)Ts}^{(N-1)Ts + D \cdot Ts} \hat{v}_{BUS}(\tau) \cdot d\tau \quad (2.31)$$

Equation (2.31) shows that the effect from the control voltage perturbation and the effect from the bus voltage perturbation can be separated with linear equations. This can be seen in Figure 2.23. This means the block diagram in Figure 2.18 (c) can be used to derive the small-signal model of the feedforward loop. Therefore, the modulator gain  $F_m$  is same as (2.22)

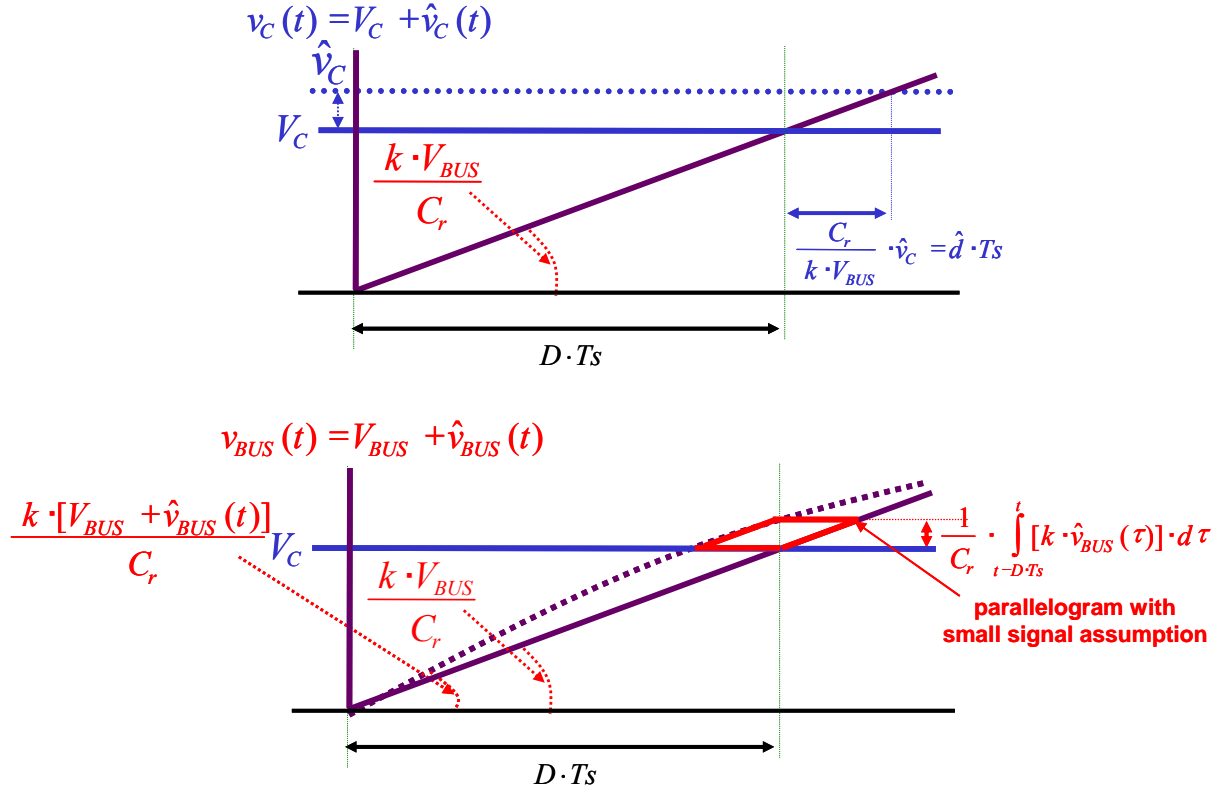


Figure 2.23 The bus voltage feedforward waveform with the perturbations -  
 (a) the control voltage perturbation (b) the bus voltage perturbation.

$$F_M = \frac{C_r}{k \cdot Ts \cdot V_{BUS}} \quad (2.32)$$

The feedforward gain  $F_{FF}$  is determined by equation (2.33),

$$\hat{d}_N = -\frac{1}{Ts \cdot V_{BUS}} \int_{(N-1)Ts}^{(N-1)Ts+D \cdot Ts} \hat{v}_{BUS}(\tau) \cdot d\tau \quad (2.33)$$

With the sampled data modeling technique [138], the discrete time equation (2.33) can be converted to a continuous time equation (2.34),

$$\hat{d}_C(t) = -\frac{1}{Ts \cdot V_{BUS}} \int_{t-D \cdot Ts}^t \hat{v}_{BUS}(\tau) \cdot d\tau \quad (2.34)$$

Then the frequency domain equation is

$$\hat{d}(s) = -\frac{1 - e^{-s \cdot D \cdot Ts}}{s \cdot Ts \cdot V_{BUS}} \cdot \hat{v}_{BUS}(s) \quad (2.35)$$

Therefore, the feedforward gain model is

$$F_{FF}(s) = \frac{1 - e^{-s \cdot D \cdot Ts}}{s \cdot Ts \cdot V_{BUS}} = \frac{D}{V_{BUS}} \cdot \frac{1 - e^{-s \cdot D \cdot Ts}}{s \cdot Ts \cdot D} \quad (2.36)$$

Combining the concept in (2.25), the complete feedforward gain model is

$$F_{FF}(s) = \frac{D - D_{clock}}{V_{BUS}} \cdot \frac{1 - e^{-s \cdot (D - D_{clock}) \cdot Ts}}{s \cdot Ts \cdot (D - D_{clock})} \quad (2.37)$$

This feedforward model can be simplified using the curve fitting method in [132],

$$F_{FF}(s) \approx \frac{D - D_{clock}}{V_{BUS} \cdot \left( 1 + \frac{(D - D_{clock}) \cdot Ts \cdot s}{2} + \left( \frac{(D - D_{clock}) \cdot Ts \cdot s}{\pi} \right)^2 \right)} \quad (2.38)$$

Figure 2.24 shows the comparison between the transfer function with the modified model (2.38) and the SIMPLIS simulation results. They match up well and the feedforward gain model (2.38) is accurate enough to be used in ABVP system modeling.

Using this feedforward model,  $F1(s)$  and  $F3(s)$  are derived, and  $Z_{bus}(s)$  and  $T_{ABVP}$  can be predicted. Figure 2.25 shows the shape of the instability loop gain,  $T_{ABVP}$ . It is observed that the first-stage bandwidth determines the peak value of  $T_{ABVP}$ .

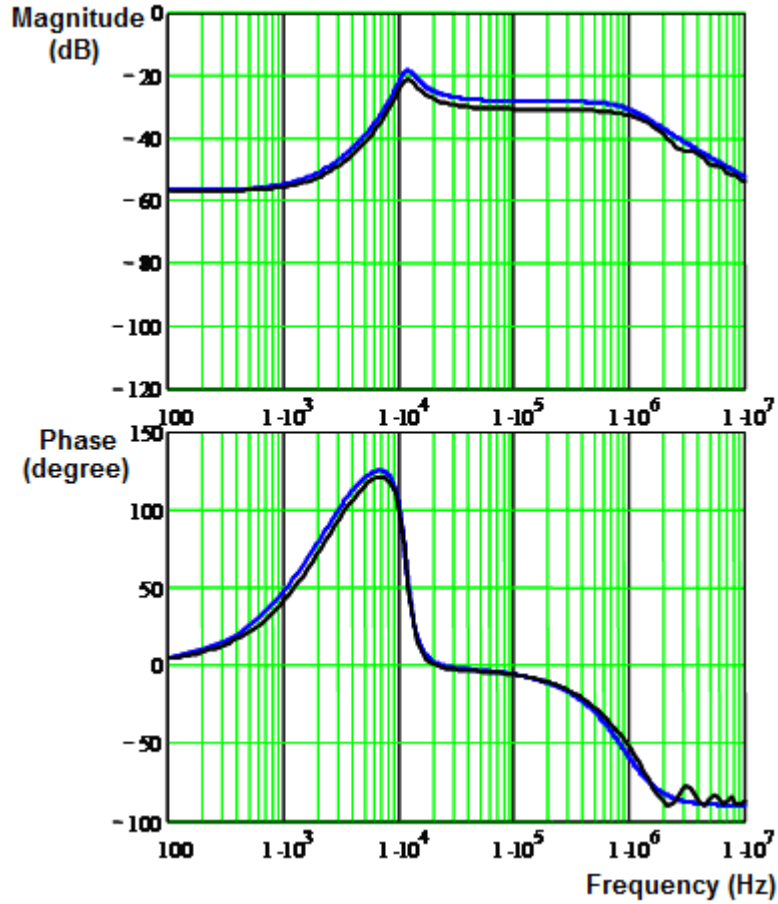


Figure 2.24 The transfer function from the bus voltage to the second-stage inductor current with only the feedforward loop closed. (Black lines : SIMPLIS simulation, Blue lines : equation (2.38))

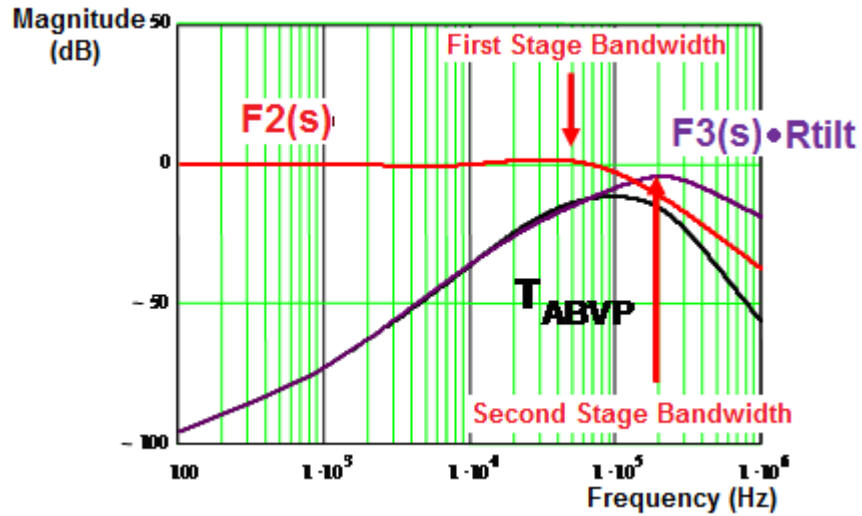


Figure 2.25 The shape of the instability loop  $T_{ABVP}$ .

### 2.3.3. Stability and Dynamics

Figure 2.26 shows the gain and phase of the ABVP instability loop,  $T_{ABVP}$ . It is observed that the phase drops under -180 degree before the peak of the  $T_{ABVP}$  gain. Then, when the  $T_{ABVP}$  reaches 0dB at the high frequency, the phase is always smaller than -180 degree and the system is unstable. Therefore, in order to get a stable system,  $T_{ABVP}$  should be designed to be smaller than 0dB. This can be controlled by the first-stage bandwidth.

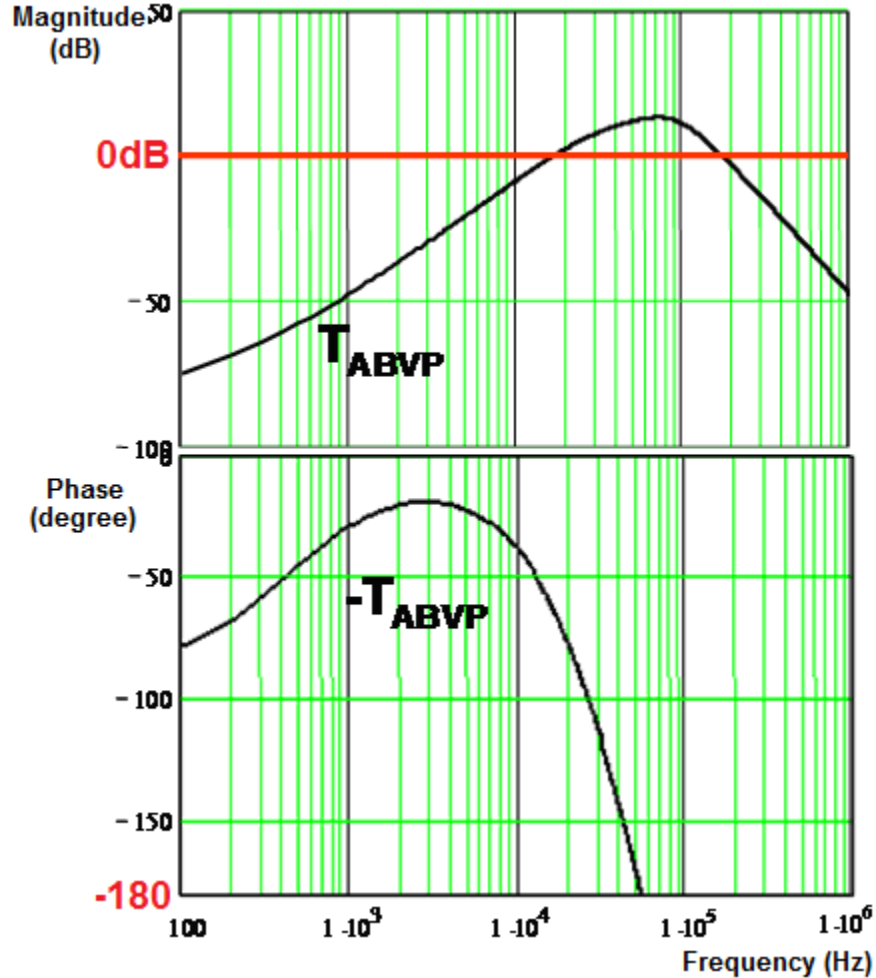


Figure 2.26 The gain and phase of  $T_{ABVP}$ .

Fig. 14 shows the SIMPLIS simulation results of  $T_{ABVP}$  and the stability. When the peak value of  $T_{ABVP}$  is near 0dB, the bus voltage oscillates. By decreasing the first stage bandwidth from 70kHz to 18kHz,  $T_{ABVP}$  becomes much smaller than 0dB, and the bus voltage has no oscillation.



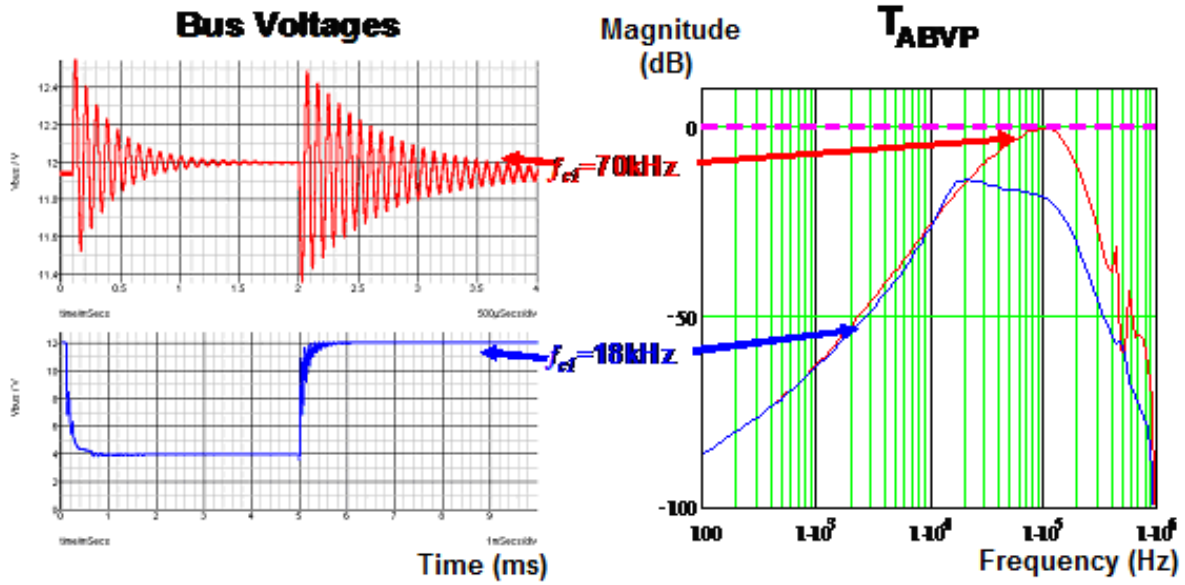


Figure 2.27 The  $T_{ABVP}$  and the stability.

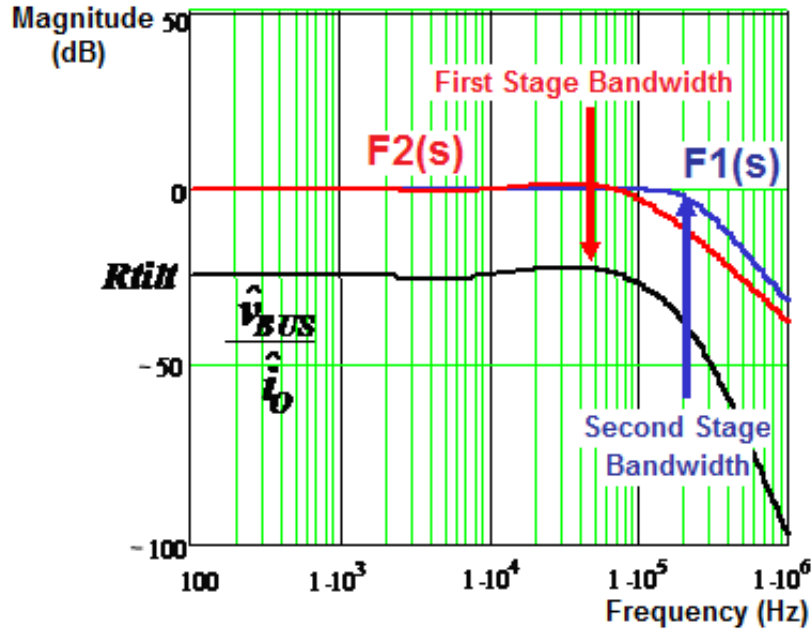


Figure 2.28 The shape of the transfer function from the load current to the bus voltage ( $Z_{bus}(s)$ ).

Using (2.16), in order to get a stable bus voltage,  $T_{ABVP}$  is designed to be much smaller than 0dB, and the transfer function from the load current to the bus voltage becomes

$$\frac{\hat{v}_{BUS}(s)}{\hat{i}_O(s)} = Z_{bus}(s) \approx F1(s) \cdot F2(s) \cdot Rtilt \quad (2.39)$$

Figure 2.28 shows the shape of  $F1(s)$ ,  $F2(s)$ . It is observed that  $F1(s)$  is 0 dB within the second-stage bandwidth, and  $F2(s)$  is 0dB within the first-stage bandwidth. Therefore, within the first-stage bandwidth, (2.39) becomes (2.40),

$$\frac{\hat{v}_{BUS}(s)}{\hat{i}_O(s)} = Z_{bus}(s) \approx R_{tilt} \quad (2.40)$$

The first-stage bandwidth ( $f_{c1}$ ) is a very important parameter for the ABVP loop design. As predicted in Section 2.2, it determines the bus voltage dynamics. In order to get better performance,  $f_{c1}$  should be enlarged; however a high  $f_{c1}$  may result in an unstable system. Therefore,  $f_{c1}$  should be carefully designed considering the  $T_{ABVP}$  loop.

## 2.4. Design and Experimental Results

The ABVP-AVP system is modeled and a stable condition is found in Section 2.3. Using these results, the system is designed and the hardware is built.

The left figure in Figure 2.29 describes the unstable system case. The positive feedback gain  $T_{ABVP}$  is larger than 0dB.  $F3(s)$  is determined by the second stage design, which should be optimized for output regulation and  $R_{tilt}$  is fixed to get the higher light load efficiency. In this case, the system can be stabilized by reducing the first stage bandwidth ( $f_{c1}$ ) like in Figure 2.29.

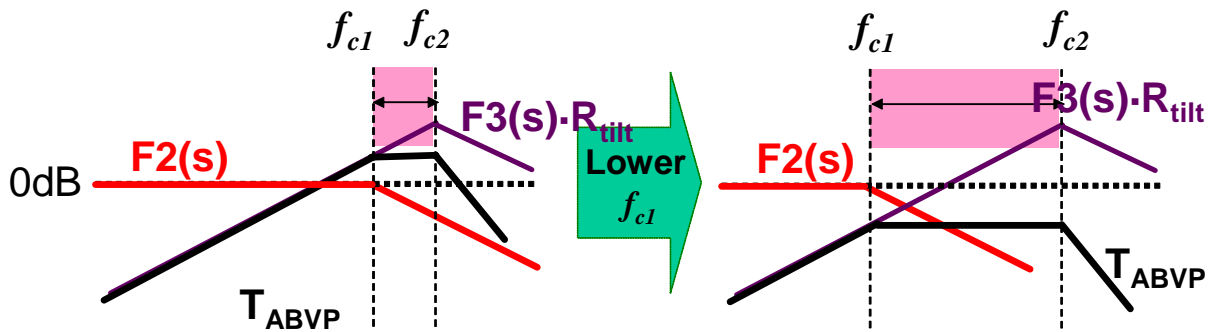


Figure 2.29 The ABVP system is stabilized by lowering the first-stage bandwidth.

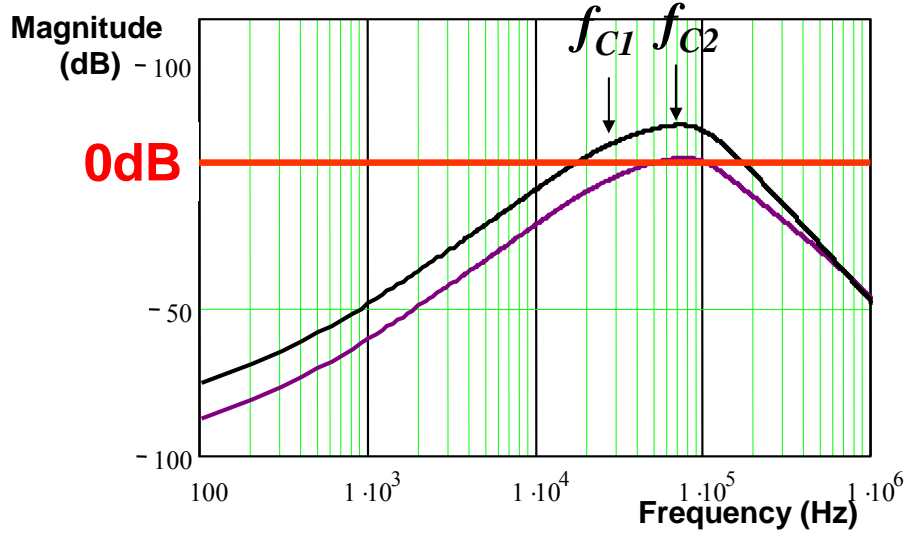


Figure 2.30  $T_{ABVP}$  with a large  $D_{clock}$  (Black) with the small  $D_{clock}$  (Purple).

The black line in Figure 2.30 shows the  $T_{ABVP}$  of the ABVP-AVP hardware discussed in Section 2.2.2. The first-stage bandwidth ( $f_{c1}$ ) is 25kHz with 200kHz switching frequency and the second-stage bandwidth ( $f_{c2}$ ) is 80kHz with 500kHz switching frequency. The bus capacitance is 176 $\mu$ F, the output capacitance is 940 $\mu$ F, the input voltage is 12V and the load-line impedance ( $R_{droop}=R_{LL}$ ) is designed to be 2m $\Omega$ . The inductance of the first stage is 10 $\mu$ H. The inductance of the second stage is 300nH for each phase. The ABVP gain ( $R_{tilt}$ ) is designed to be 125m $\Omega$ . The ABVP loop is unstable because the peak of  $T_{ABVP}$  is larger than 0dB.

In Section 2.3.2, the feedforward model is derived. In order to reduce the impact from the bus voltage to the second stage,  $D_{clock}$  should be minimized. By reducing  $D_{clock}$  to almost zero, the feedforward function is maximized, and  $T_{ABVP}$  is reduced as represented by the purple line in Figure 2.30. Although  $T_{ABVP}$  becomes smaller, it still reaches 0dB and the system is not yet stabilized. A smaller  $f_{c1}$  will stabilize this system. However, the smaller  $f_{c1}$  will result in more bus capacitors and the performance degrades.

Figure 2.31 shows another solution for stabilizing the ABVP-AVP system. In order to reduce the gain of  $T_{ABVP}$ , a low-pass filter is inserted. Then,  $T_{ABVP}$  equation becomes (2.41),

$$T_{ABVP} = F2(s) \cdot F3(s) \cdot R_{tilt} \cdot \frac{1}{1 + s / \omega_p} \quad (2.41)$$

where  $\omega_p = \frac{1}{R_f \cdot C_f}$ .

Figure 2.32 shows the system stabilized with the low-pass filter. With the low-pass filter, the first-stage bandwidth does not have to be reduced and the bus capacitor number is not changed.

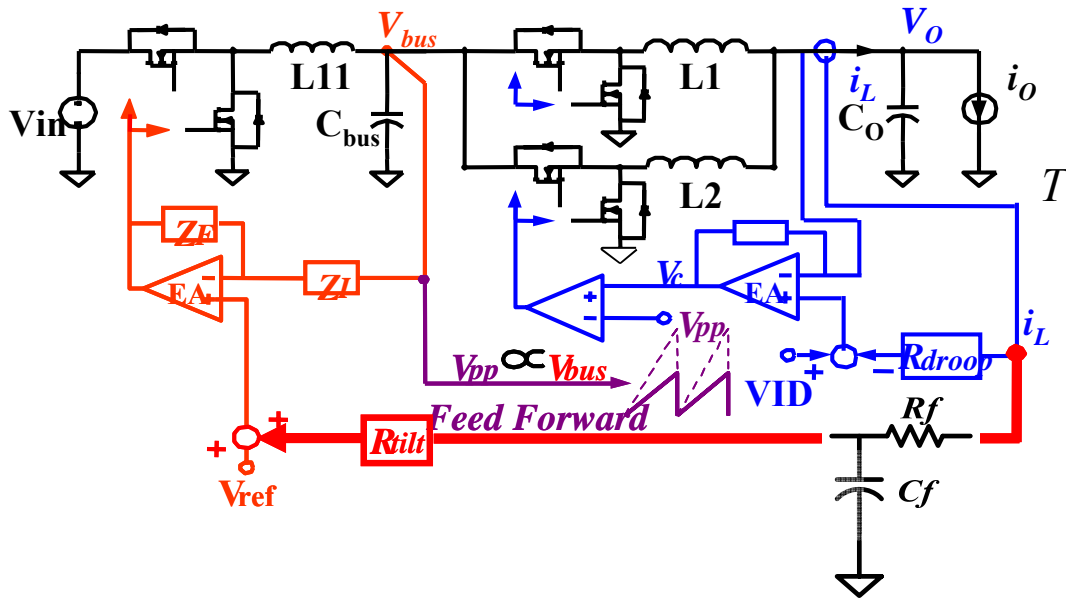


Figure 2.31 ABVP-AVP system with the low-pass filter.

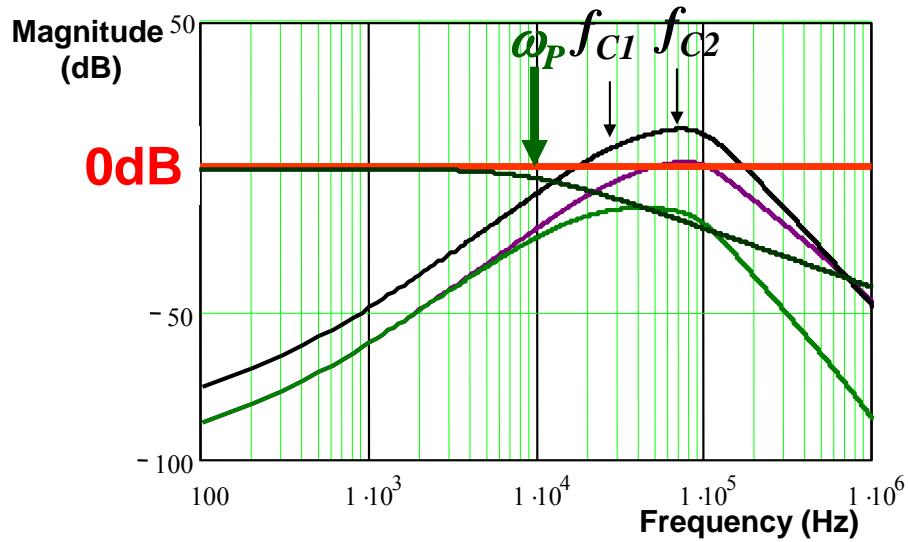


Figure 2.32  $T_{ABVP}$  with the low-pass filter.

The experimental setup is same as Figure 2.31.

- Two-stage VR; Single-phase VR for first stage, two-phase VR for second stage
- $V_{IN} = 12V$ ,  $V_O = 1.26\sim 1.3V$ ,  $V_{BUS} = 3.5 \sim 6V$
- $I_O = 0 \sim 20A$ ,  $R_{droop} = 2m\Omega$ ,  $R_{tilt} = 125m\Omega$
- $L_{11} = 10\mu H$ ,  $L_1=L_2=300nH$
- Output Capacitors :  $2\times 470\mu F$  (ESRE Cap.)
- Bus Capacitors:  $8\times 22\mu F$  (Ceramic Cap.)
- First stage  $F_s = 200kHz$ , first stage bandwidth :  $25kHz$
- Second stage  $F_s = 500kHz$ , second stage bandwidth:  $90kHz$
- First stage controller: LM2639
- Second stage controller: UC3825
- Two additional OPAMPs to realize AVP and ABVP function

The hardware is built with the low-pass filter. The first stage bandwidth is  $25kHz$  and the bus capacitance is only  $176\mu F$ . Figure 2.34 shows the experimental results of the ABVP system. The bus voltage follows the load current with the gain  $R_{tilt}$  ( $125m\Omega$ ) and the output voltage is also well regulated to follow the AVP gain  $R_{droop}$  ( $2m\Omega$ ). Figure 2.34 shows the steady-state bus voltage versus the load current. The bus voltage is regulated using the control strategy in Figure 2.4. Figure 2.35 shows the efficiency data. The ABVP system can increase the light-load efficiency dramatically.

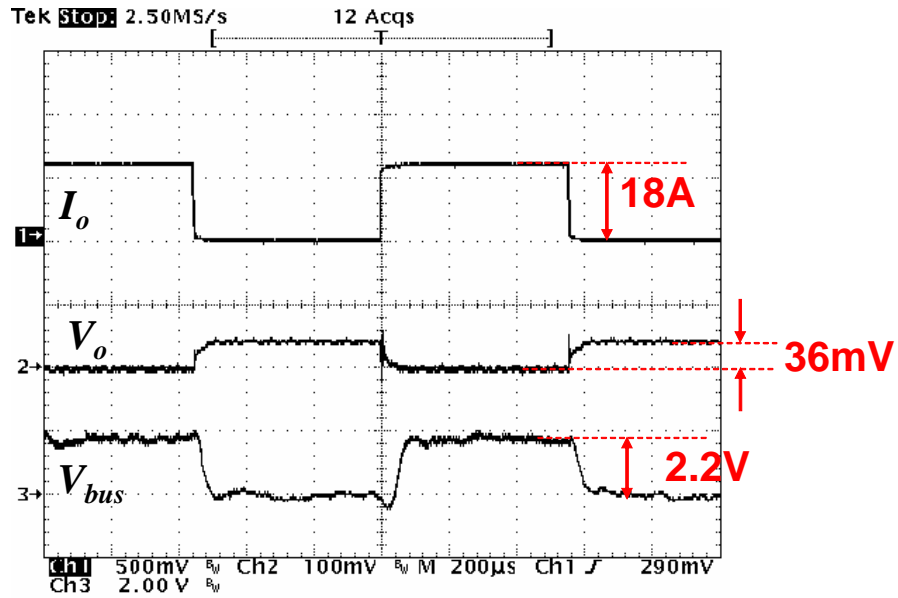


Figure 2.33 The experimental results of ABVP-AVP system (transient response).

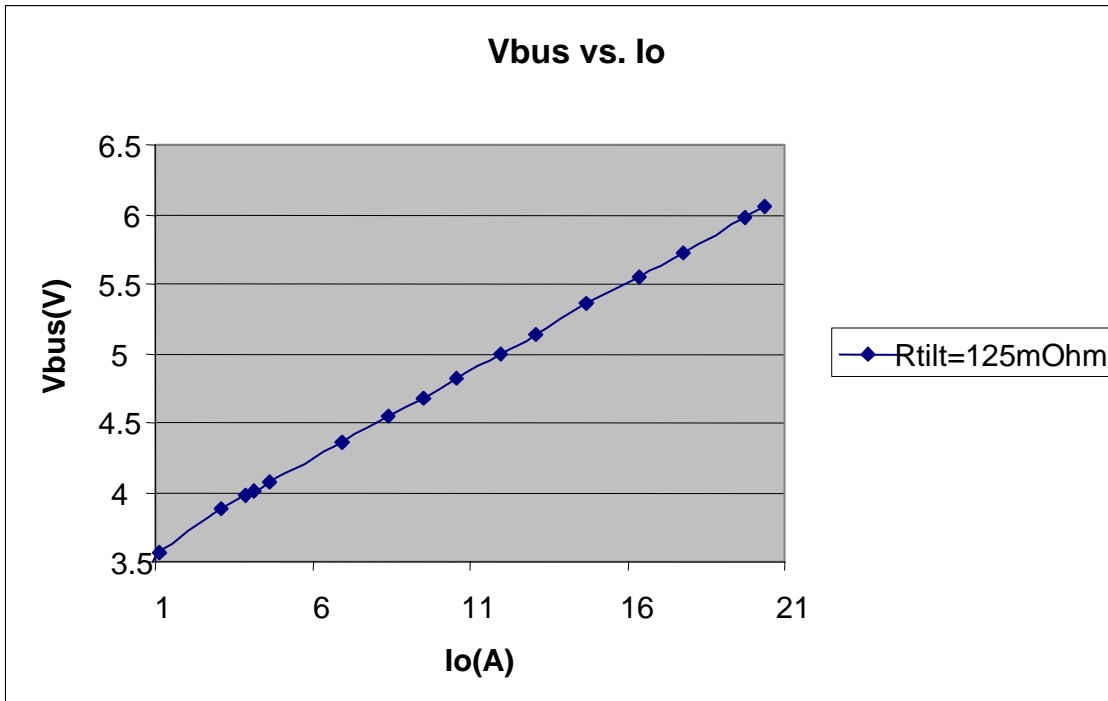


Figure 2.34 The experimental results of ABVP-AVP system (The bus voltage vs. the load current).

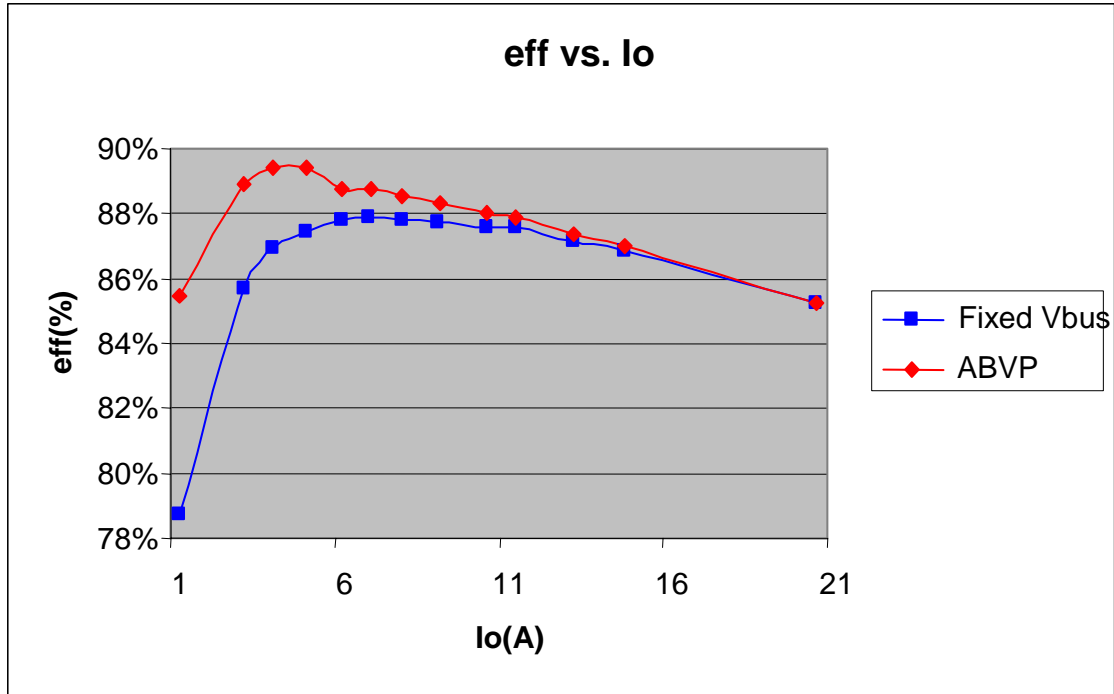


Figure 2.35 The experimental results of ABVP-AVP system (The system efficiency vs. the load current).

## 2.5. Summary

The two-stage architecture is a good solution for the next generation VR. With the ABVP control, the light-load efficiency of the two-stage architecture is much better than the single-stage solution. However, there is a trade off between the stability and the performance. The accurate small-signal model is derived. Using this small-signal model, the stability and the dynamics are analyzed and the ABVP-AVP system is designed and verified with the hardware experiments.





## Chapter 3. Proposed Hysteretic Control Method for Multiphase VR

In the previous chapter, the advanced control method for the two-stage architecture is discussed. With two-stage architecture, the second stage can run with a high switching frequency; and with ABVP control, the light-load efficiency can be much higher than the single-stage VR. However, the switching frequency is still limited by the efficiency. For the desktop and server, the full-load efficiency should be larger than 80%, and with the current device technology and the cost budget, the second-stage switching frequency cannot be larger than 2MHz [101]. For laptop applications, it is more difficult. The full-load efficiency should be larger than 87%, and it is difficult to make the second-stage switching frequency larger than 600kHz [103]. With the conventional linear control method, it is difficult to make the bandwidth larger than one sixth of this limited switching frequency, and a large number of the bulk capacitors are still necessary.

In this chapter, the hysteretic control method is researched as a possibility for dealing with these issues. The hysteretic control method can achieve a fast transient without increasing the switching frequency. First, the existing hysteretic control methods for the multiphase VR are reviewed. Then the drawbacks are identified and the ideas to resolve those drawbacks are presented. Finally, using the proposed control method, the system is modeled, designed, and verified with hardware experiments.

### 3.1. Review of the Existing Hysteretic Control Methods

In Chapter 1, the fast transient control methods are reviewed and one type of hysteretic control method is chosen because of its fast transient response and its capability for high light-load efficiency. For the multiphase VR, the single-phase VRs with this hysteretic control are paralleled, as in Figure 3.1 (a). The current sharing and the AVP functions are achieved without degrading the performance. However, it is very hard to achieve the interleaving function. Figure 3.1 (b) shows the SIMPLIS simulation results of this system. The position (or phase) of the duty

cycle is not controllable, and the interleaving function cannot be achieved. Moreover, it is well known the switching frequency changes with the inductance and the output capacitor parasitics, like ESR ( $R_C$ ) or ESL ( $L_C$ ). Considering the manufacturing tolerances and the effects from the temperature change, the switching frequency in the hysteretic control method is not constant, which is another drawback of the hysteretic control method.

In this section, the existing efforts to resolve these drawbacks are discussed.

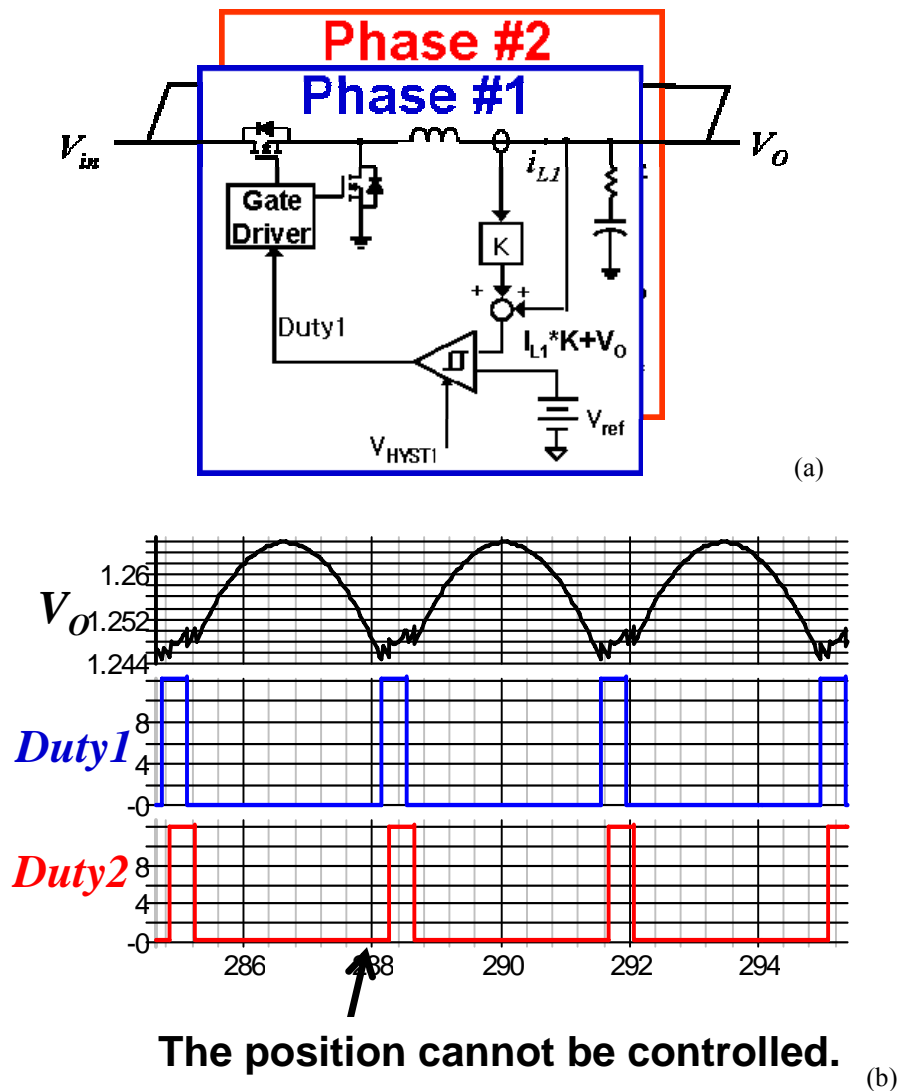


Figure 3.1 Hysteretic control method for the multiphase VR (a) Schematics (b) Steady state simulation results.

### 3.1.1. Hysteretic Control Methods for the Multiphase VR

Many people have tried to realize the hysteretic control method for the multiphase VR [46][47][104][105][106][107][108][109]. First, the voltage mode hysteretic control method is suggested for multiphase VR application, like in Figure 3.2 [104][105][106]. In this control method, using the output voltage ripple the total phase's duty cycles are made, and those duty cycles are distributed to each phase to achieve the interleaving function like Figure 3.2 (b). With this method, the interleaving function is perfectly achieved. However, this solution is not used in the multiphase VR for several reasons. In VR application, the output voltage ripple is very small, and it is difficult to detect it without switching noise. Furthermore, in order to achieve current sharing, additional circuitry such as DSP is necessary, which makes the cost higher [106].

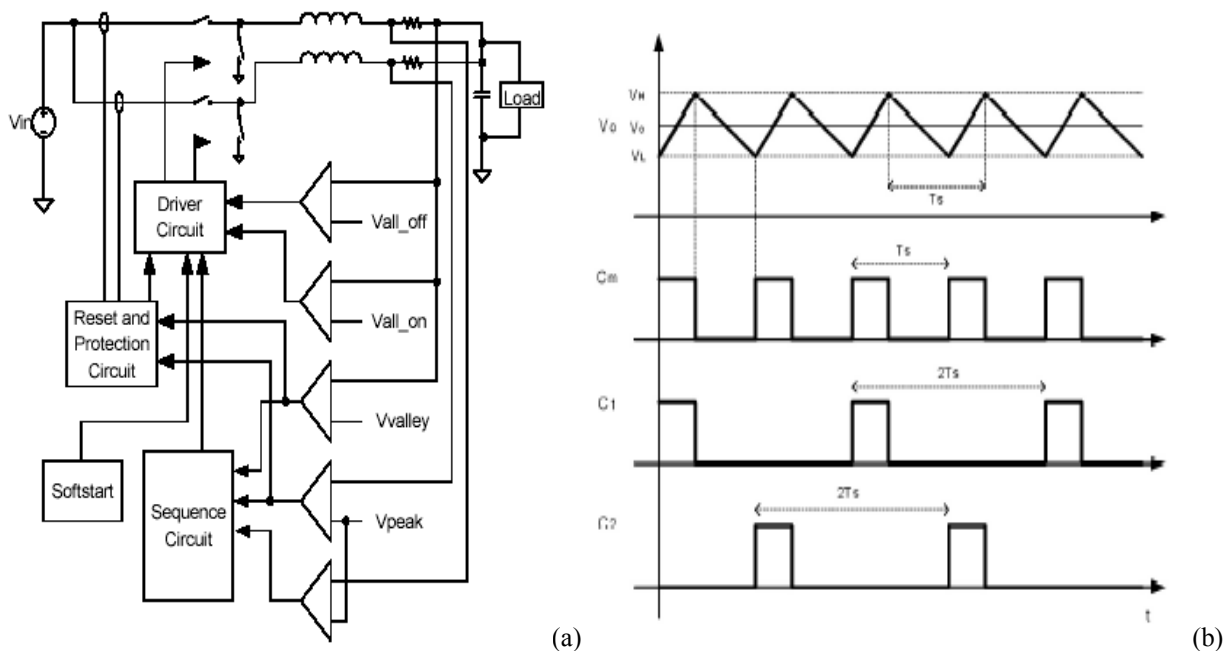


Figure 3.2 The voltage mode hysteretic control method for the multiphase VR [104] -

(a) The schematics (b) The operating principle.

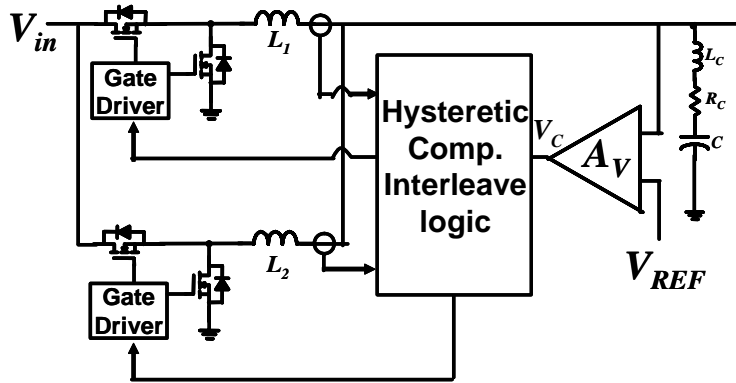


Figure 3.3 The schematics of the current mode hysteretic control method for two- or three-phase VR.

Then the current mode hysteretic control method is used for the multiphase VR [46][47][108][109]. Instead of the output voltage ripple, the inductor current ripple is used to make the duty cycle, which reduces the switching noise. Figure 3.3 shows the schematics of the multiphase VR with the current mode hysteretic control. The duty cycles are made using not only the output voltage information, but also each phase's inductor current information. There are two possible implementations for interleaving among the paralleled phases. Both cases distribute the top switch turn-on signal, which is made using the bottom boundary of the hysteretic band and the inductor current. Then, each inductor current is used to turn off each phase's top switch like the peak current control method [126][132]. With this, current sharing function is achieved.

Two methods can be distinguished based on how the top switch turn-on signal is made. One method is from the IC company National Semiconductor [46][108] and this method is illustrated in Figure 3.4 (a). In this case, the next phase's turn-on signal is made from the former phase's inductor current and the bottom boundary of the hysteretic band. For the two-phase VR example, if the first phase's inductor current touches the bottom boundary of the hysteretic band, the control turns on the second phase's control switch and vice versa. If the inductor current slopes and the hysteretic band widths are same for each phase, the time from the first phase turn-off instant to the second phase turn-on instant,  $t_2$  is the same as the time from the second phase turn-off instant to the first phase turn-on instant  $t_4$ . Furthermore the top switch turn-on durations,  $t_1$  and  $t_3$ , are the same because the inductor current slopes and the hysteretic band widths are same. Because of this, interleaving is achieved. However the feedback signals are no longer regulated within the hysteretic band. Therefore, there is a dc error, and the additional

compensation network with the integrator is necessary to eliminate this dc error, like  $A_V$  in Figure 3.3.

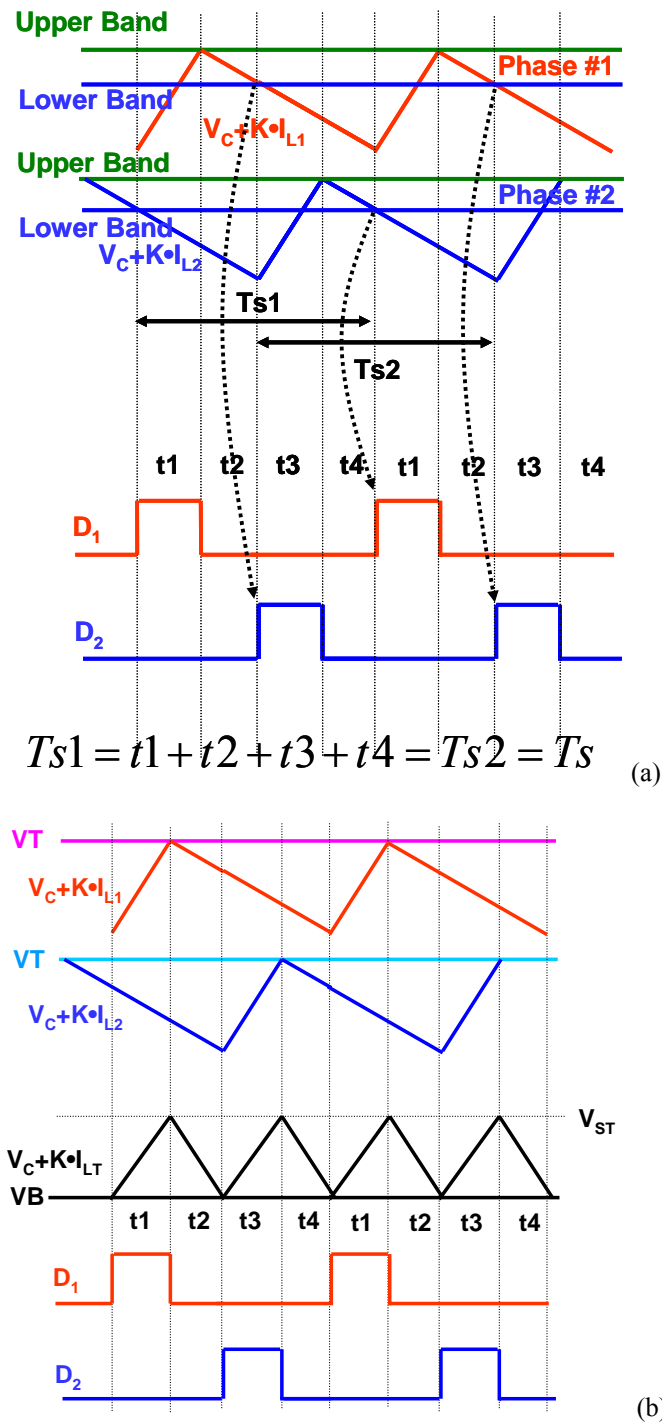
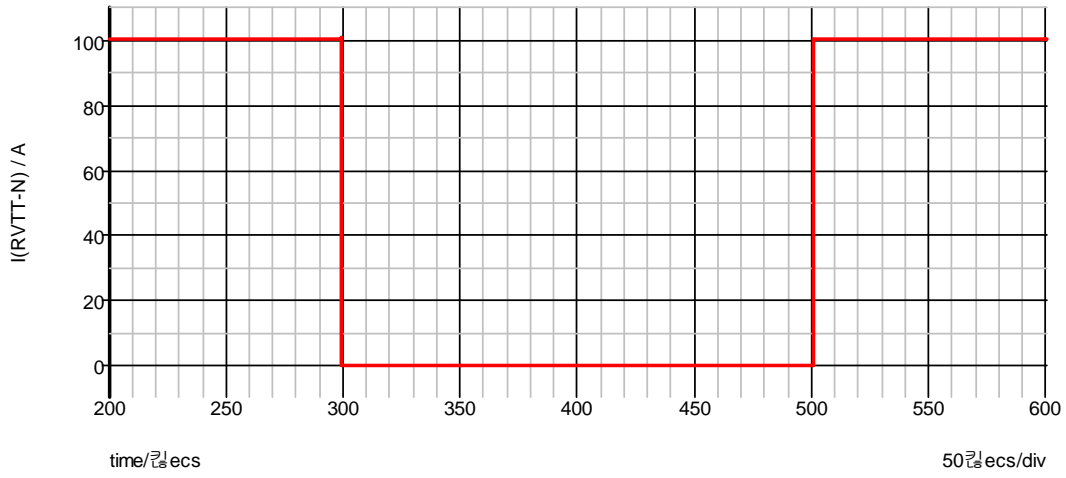


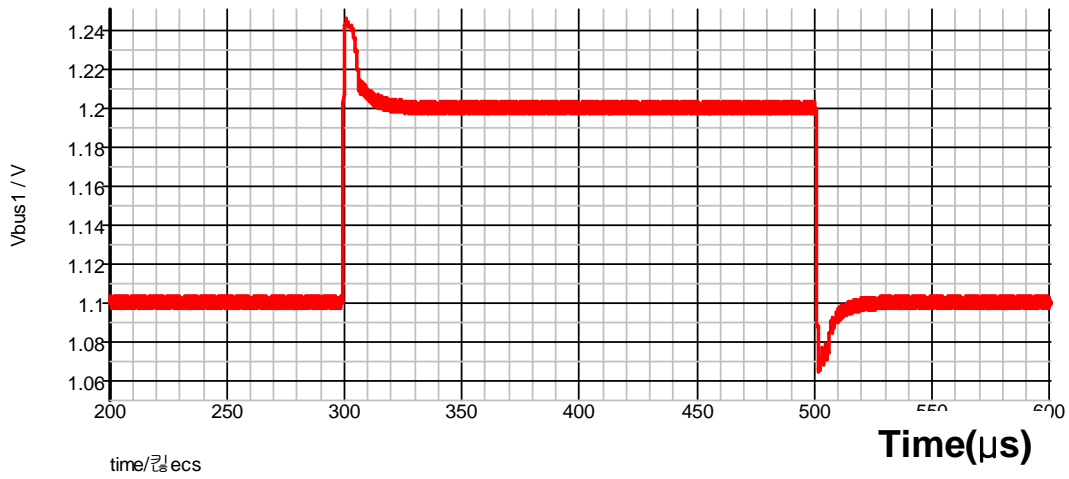
Figure 3.4 The interleaving method of the current mode hysteretic control for two-phase VR - (a) National Semiconductor (b) Analog Devices.

The other implementation is from the IC company Analog Devices [47], and is illustrated in Figure 3.4 (b). In this case, similar to the voltage mode hysteretic control method, the total inductor current is used to make the whole top switch turn-on signals. By distributing these turn-on signals to each phase, interleaving is achieved. In the two-phase VR example, the feedback signal with the total inductor current ( $V_C + K \cdot (I_{L1} + I_{L2})$ ) touches the bottom boundary of the hysteretic band, and the control turns on the first phase's control switch. When the feedback signal of the first phase ( $V_C + K \cdot I_{L1}$ ) touches the top boundary of the hysteretic band, the control turns off the first phase's control switch. Then the feedback signal with the total inductor current also changes the slope, and when it touches the bottom boundary again, it turns on the second phase's top switch. If the inductor current slopes are the same, the time from the first phase turn-off instant to the second phase turn-on instant,  $t2$ , is the same as the time from the second phase turn-off instant to the first phase turn-on instant  $t4$ . The top switch turn on durations,  $t1$  and  $t3$ , are the same because the inductor current slopes and the hysteretic band widths are the same. Because of this, interleaving is achieved. In this implementation, the feedback signals are also no longer regulated within the hysteretic band. Therefore, there is a dc error, and the additional compensation network with the integrator is also necessary, like  $A_V$  in Figure 3.3.

These interleaving methods are not good because of their poor load step-up transient response. Figure 3.5 shows the SIMPLIS simulation results of the VRD 11.0 VR with the hysteretic control method and National's interleaving implementation. This is a four-phase VR with a 300nH inductor for each phase, 300kHz switching frequency for each phase, 12V input voltage, 1.2V VID, 1m $\Omega$   $R_{LL}$ , a load current of 0~100A, and 6 $\times$ 560 $\mu$ F Al-Polymer capacitors as the bulk capacitors. The output capacitors are designed for the load step-down transient with 50mV peak voltage, released from Intel [16]. It is observed that it cannot meet the specification because of the voltage dip at the load step-up transient.



(a)



(b)

**Figure 3.5 SIMPLIS simulation results of the hysteretic control with National's interleaving method - ( $6 \times 560 \mu F$  output capacitors) (a) The load current waveform (b) The output voltage waveform.**

Figure 3.6 shows the zoomed waveforms at the load step-up transient. It can be observed from Figure 3.6 (a) and (d), that the output voltage dips due to the low inductor current slew rate. The inductor current ( $I_{LT}$ ) cannot follow the load current ( $I_O$ ) because of the low total inductor current slew rate and the charge difference between the load current, and the total inductor current is drawn from the output capacitors. Thus the output voltage dips. The reason for the low inductor current slew rate is found in Figure 3.6 (b) and (c). The interleaving function makes the second-phase top switch turn on after the first-phase top switch turns off, and generally each phase can be turned on after the former phase turns off. Because of this, the duty cycles cannot overlap. In this case, the maximum inductor current slew rate at the load step up transient is calculated using

$$\left. \frac{di_{LT}}{dt} \right|_{MAX\_UP} = \frac{V_{IN} - N \cdot V_O}{L} \quad (3.1)$$

where  $V_{IN}$  is the input voltage,  $V_O$  is the output voltage,  $N$  is the phase number, and  $L$  is the inductance of each phase inductor. It is expected that the lower input voltage and the larger phase number will make the maximum inductor current slew rate smaller, and the load step-up transient will be worse. For previous VRs with VRM 9.1 or older specifications [9][10][11][12][13], this is not an issue. For these previous VRs there is AVP function, and the output capacitors are designed for the load step-down transient because the maximum inductor current slew rate at the load step-down transient (3.2) is much smaller than that at the load step-up transient for a two- or three-phase VR.

$$\left. \frac{di_{LT}}{dt} \right|_{MAX\_DOWN} = \frac{N \cdot V_O}{L}. \quad (3.2)$$

However, for recent and future VRs with VRD 10.0 or higher specifications, the phase number is increased to be larger than four phases, and Intel releases the output voltage peak of 50mV for the load step-down case. The load step-up transient then becomes important. Therefore, with this control method, the output capacitors should be designed based on the load step-up case.



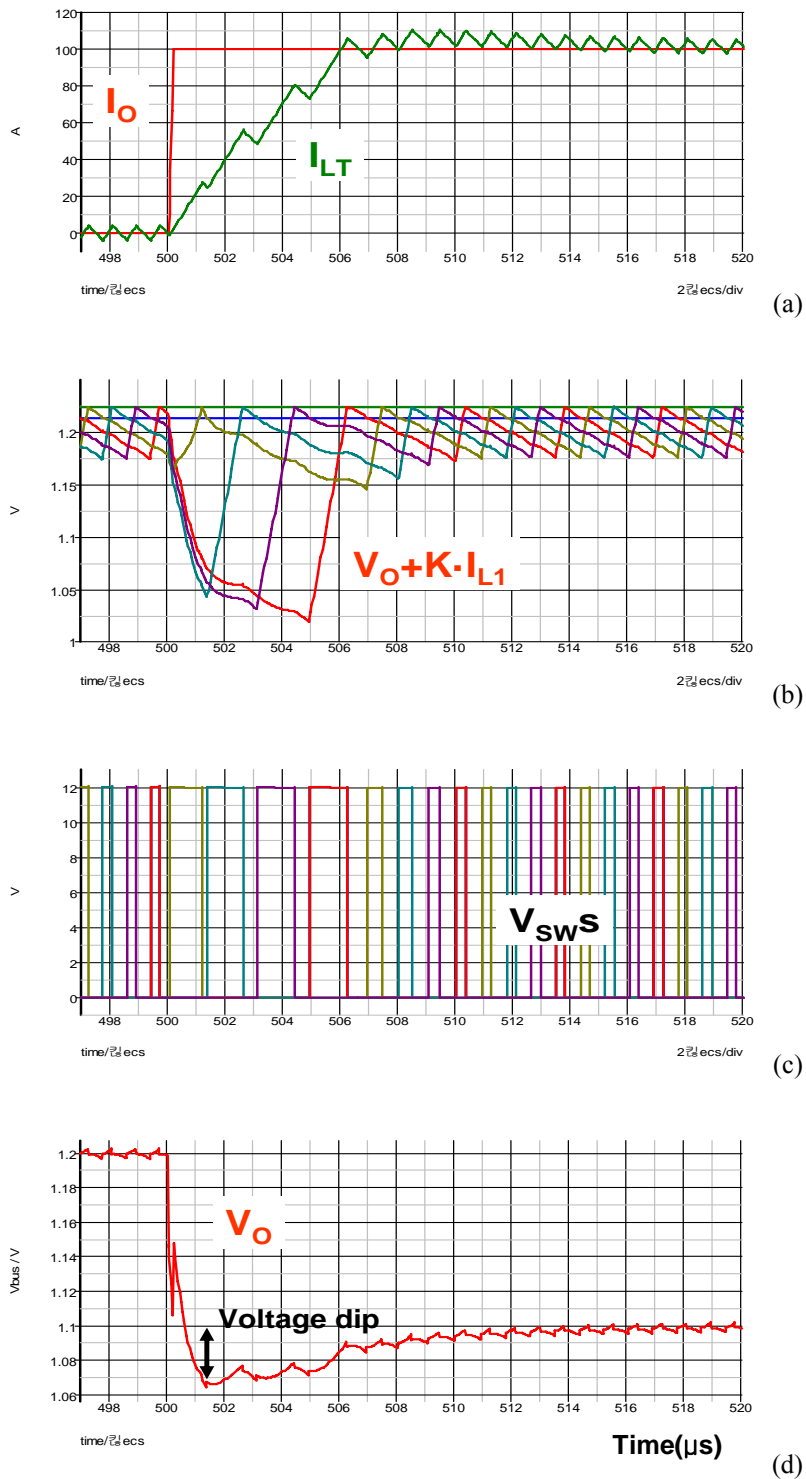
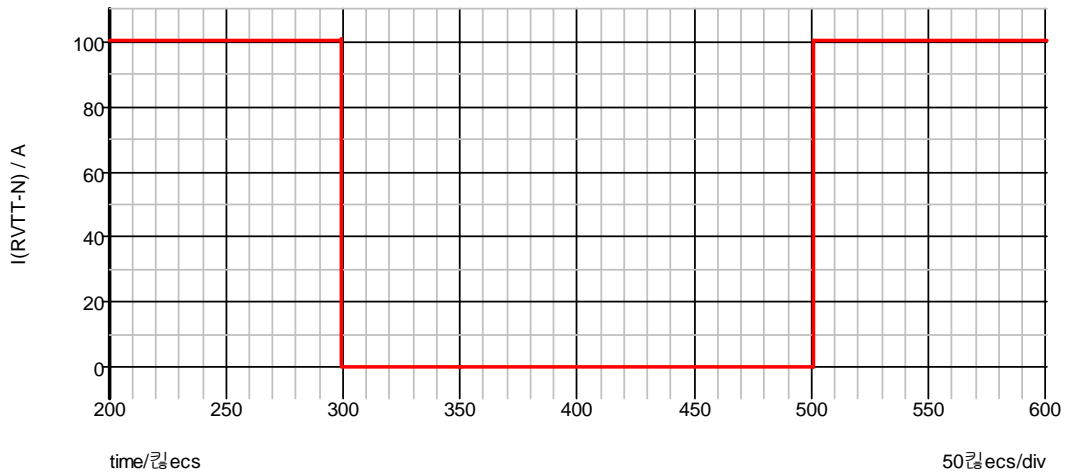
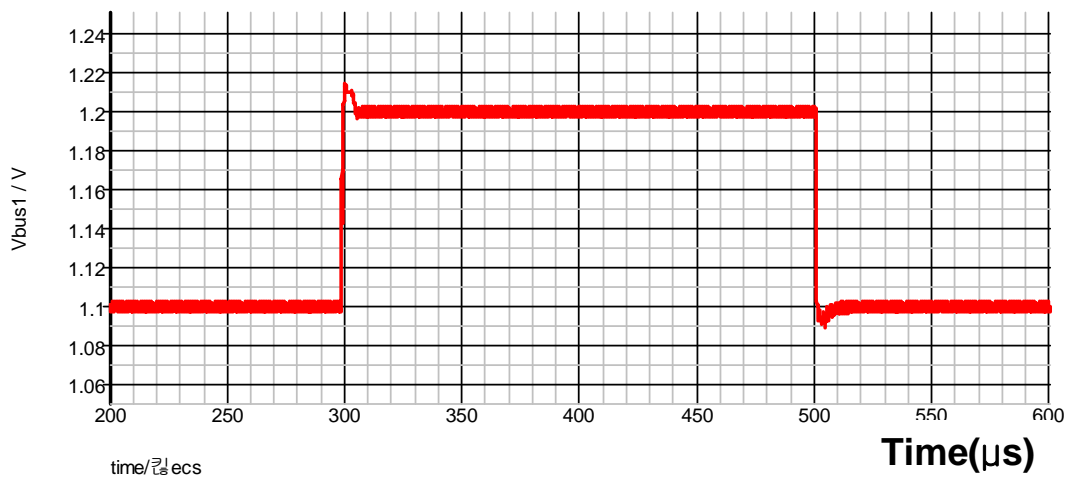


Figure 3.6 SIMPLIS simulation results of the hysteretic control with National's interleaving method (a) The load current and the total inductor current (b) The feedback signals and the hysteretic band (c) The switching node voltages (d) The output voltage.

Figure 3.7 shows the SIMPLIS simulation results of the VRD 11.0 VR with the hysteretic control method and National's interleaving implementation. The output bulk capacitors are increased from  $6 \times 560\mu\text{F}$  Al-Polymer capacitors to  $9 \times 560\mu\text{F}$  Al-Polymer capacitors. With more bulk capacitors, it can meet the specification.



(a)



(b)

**Figure 3.7 SIMPLIS simulation results of the hysteretic control with National's interleaving method - ( $9 \times 560\mu\text{F}$  output capacitors) (a) The load current waveform (b) The output voltage waveform.**

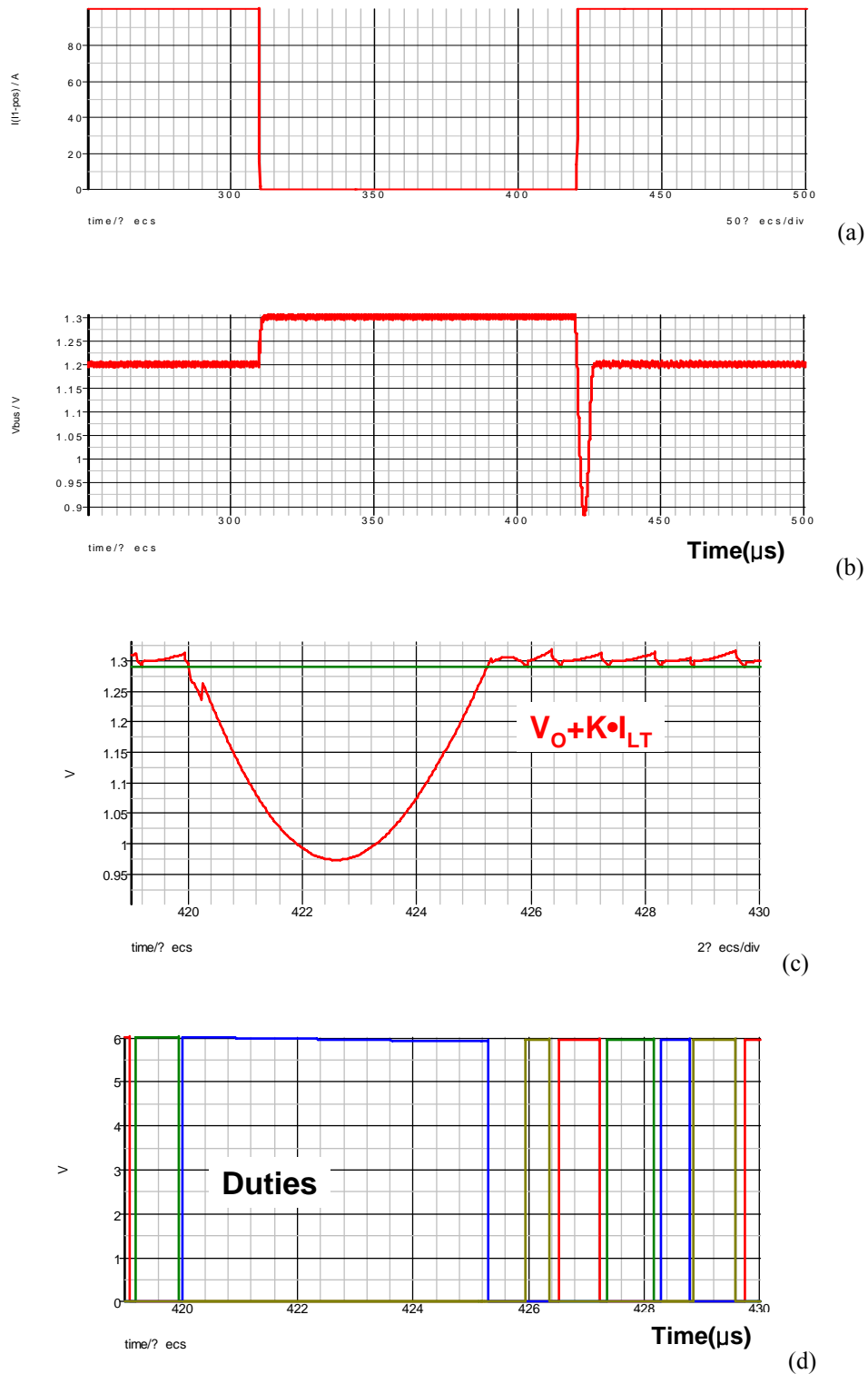
Figure 3.8 shows the SIMPLIS simulation results of the two-stage VR for VRD 11.0 specification with the hysteretic control method and Analog Devices' interleaving implementation. The input voltage is 12V, the bus voltage is 6V; the second stage is a four-phase VR with a 150nH inductor for each phase, 300kHz switching frequency for each phase, 1.3V VID, 1mΩ  $R_{LL}$ , the load current 0~100A, and 6×100μF MLCCs for the bulk capacitors. The output capacitors are designed for the load step-down transient. It is observed that this cannot meet the specification because of the huge output voltage dip at the load step-up transient.

Just as in the case in Figure 3.5, the duty cycles cannot be overlapped. Figure 3.8 (c) and (d) show this. When the transient occurs, the feedback signal with the total inductor current goes below the bottom boundary of the hysteretic band, and only one turn-on signal is made during the transient. Then only one phase delivers the current to the output while the other phases absorb the current. The maximum inductor current slew rate at the load-step up is very small. In this case, the input voltage of the second stage (the bus voltage) is much smaller than the input voltage in the previous case. In addition, the maximum inductor current slew rate at the load step-up is much smaller than in the previous case, while the maximum inductor current slew rate at the load step-down is the same as in the previous case. Therefore, the output voltage dip is much worse than that of the previous case. In order to reduce this, a lot of output capacitors are necessary, which will eliminate the biggest benefit of the hysteretic control method.

In order to resolve this problem, a new interleaving method should be developed that makes the duty cycles overlap during the load step-up transient. Then, the maximum inductor current slew rate can be increased quite a bit;

$$\left. \frac{di_{LT}}{dt} \right|_{MAX} = \frac{N \cdot (V_{IN} - V_O)}{L}. \quad (3.3)$$

With the duty cycle overlap feature, the maximum inductor current slew rate at the load step-up transient is very different from that with the previous interleaving feature. The larger phase number will make the maximum inductor current slew rate larger, and the load step-up transient will be better.



**Figure 3.8** SIMPLIS simulation results of the hysteretic control with Analog Devices' interleaving method (a) The load current waveform (b) The output voltage waveform (c) The feedback signal with the total inductor current (zoomed waveforms) (d) The duty cycles (zoomed waveforms).

### 3.1.2. Hysteretic Control Methods for the Constant Switching Frequency

Not only the interleaving, but also the variable frequency is the big challenge. In order to resolve this problem, the hysteretic control method with constant switching frequency is proposed [112]. It is already studied that by changing the propagation delay, the switching period ( $T_s$ ) can be controlled. With this concept, constant switching frequency can be achieved. Figure 3.9 shows the hysteretic control method with constant frequency. In this method, the reference clock ( $Clk_{IN}$ ) is used and by modifying the delay time ( $t_D$ ), the top switch turn-on instant is controlled and it is synchronized with the reference clock. Figure 3.10 (a) shows the schematics of this control method. The output voltage is fed back to the hysteretic comparator. The output voltage, in contrast with the reference voltage with hysteresis, produces the temporary duty cycles ( $V_{cmp}$ ). This signal is going to two places. The first place is the Phase Locked Loop (PLL) circuitry. The phase of this signal is sensed and compared to the phase of the reference clock by the Phase Frequency Detector (PFD). If the signals are not in phase, the PFD emits an error signal and modifies the voltage ( $V_{TH}$ ) which changes the delay ( $t_D$ ). With this delay and the temporary duty cycles ( $V_{cmp}$ ), the real duty cycles are made. After several iterations, the system reaches steady state, and the turn-on instant of  $V_{cmp}$  is synchronized with the reference clock. At the steady state, the delay ( $t_D$ ) is also constant, and the phase and the frequency of the duty cycle are fixed. By paralleling these modules and phase shifting the clocks, interleaving can be achieved.

However, this idea is difficult to apply to the VR. Figure 3.10 shows the load step-down transient response of the hysteretic control and of the hysteretic control with constant frequency. The hysteretic control with constant frequency has an additional delay ( $t_D$ ) which is made for the constant frequency operation in the steady state. Because of this additional delay, the charge difference ( $Q_{extra}$ ) is larger, and there is a greater output voltage peak.

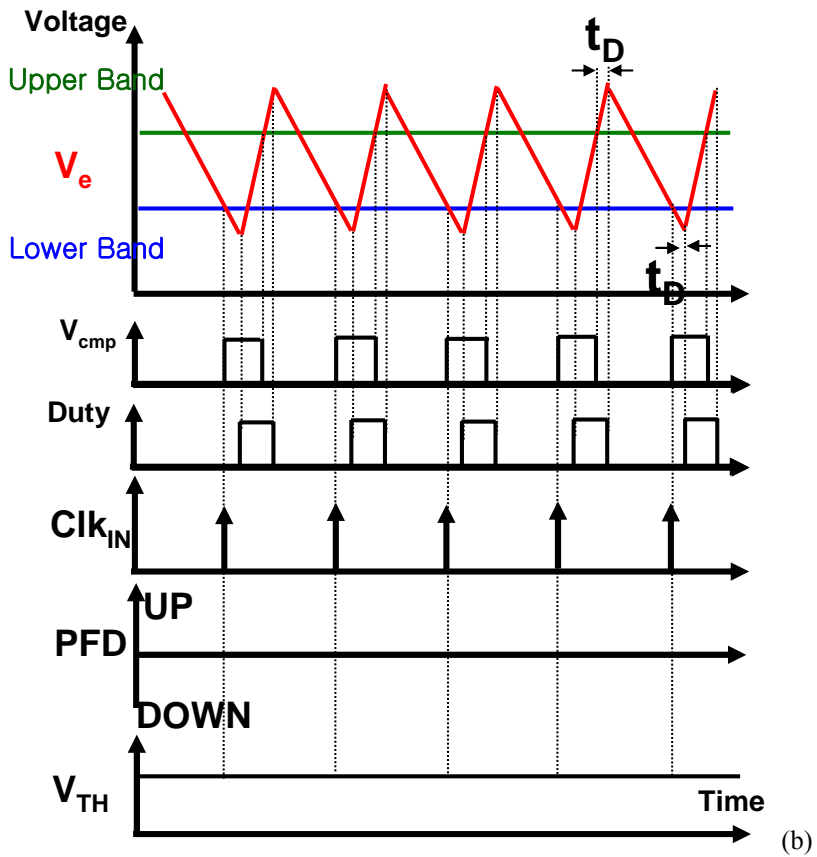
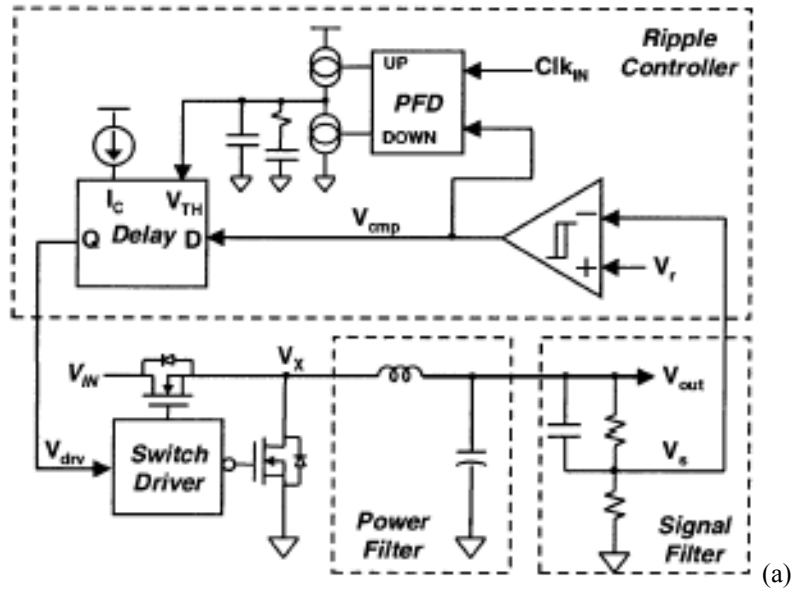
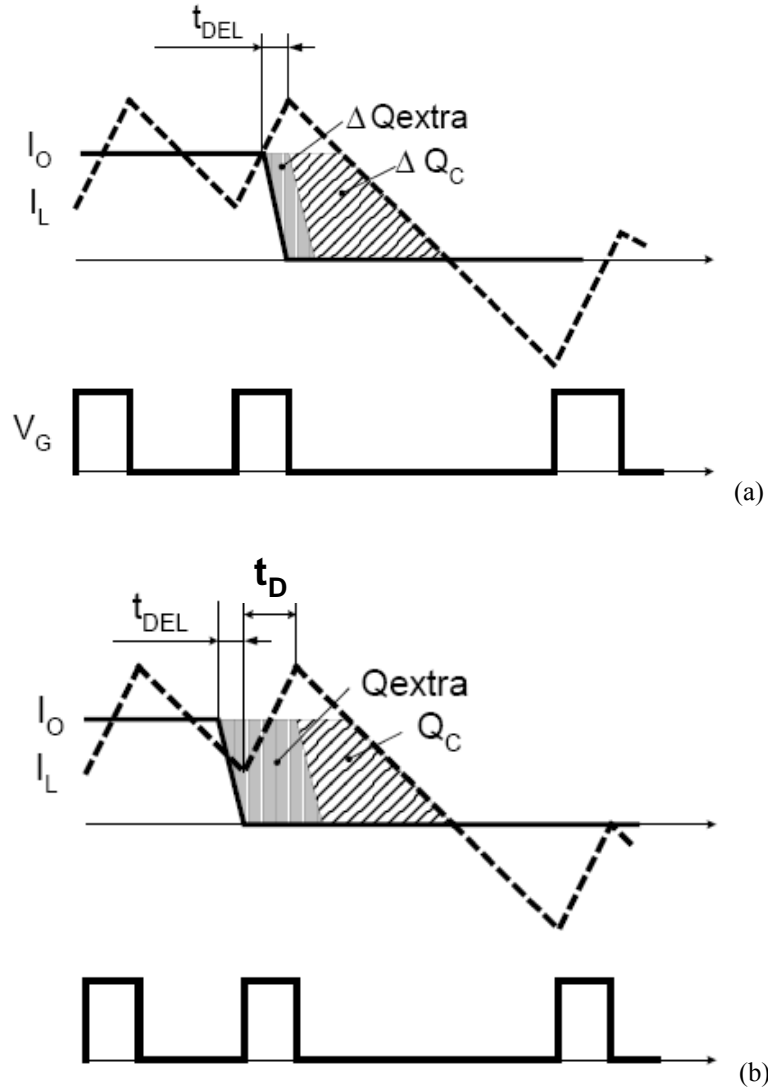
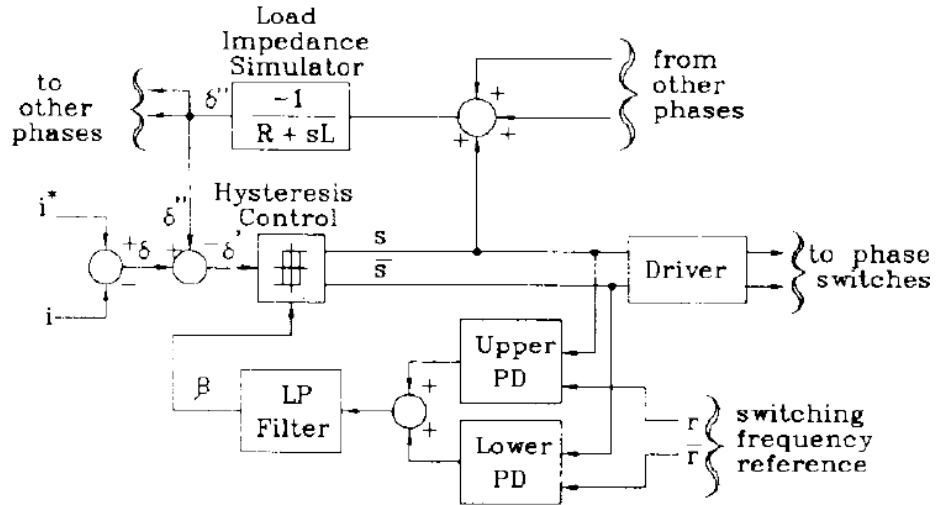


Figure 3.9 The hysteretic control method with the constant frequency (a) The schematics [112] (b) The operating principle.



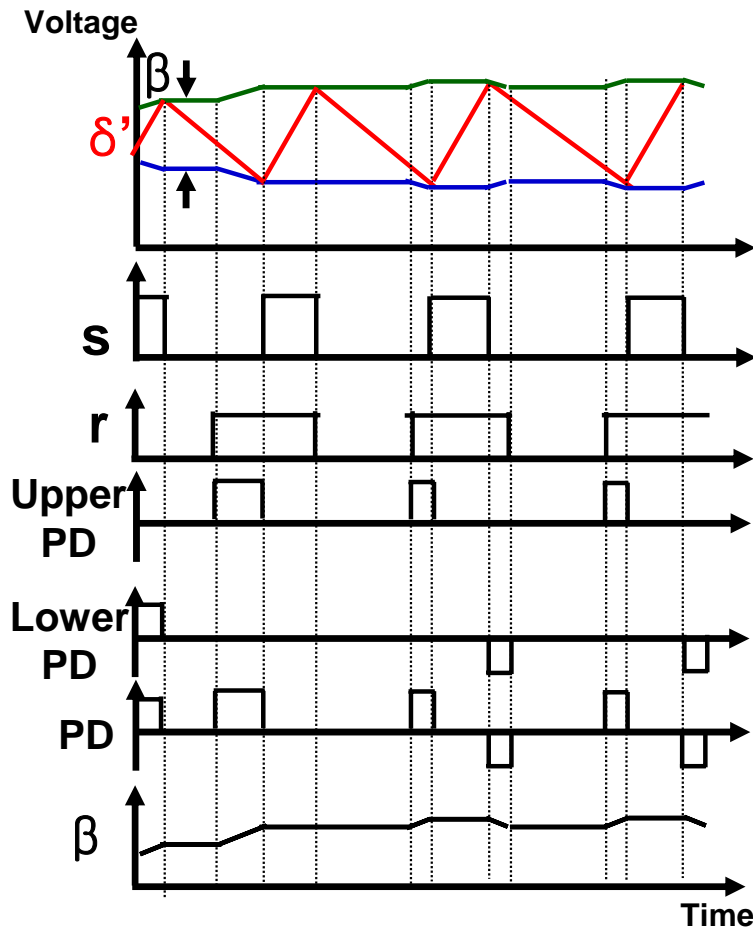
**Figure 3.10** The load step-down transient response (a) The hysteretic control method (b) The hysteretic control method with constant frequency.

Instead of using an additional delay, by modifying the hysteretic band width ( $V_{BAND}$ ), the phase and frequency of the duty cycles can be controlled. Figure 3.11 shows the constant-frequency hysteretic control method in the inverter application [113]. This method uses two phase detectors, *Upper PD* and *Lower PD* and averages two phase errors from the two phase detectors, then the duty cycles are positioned to eliminate this averaged error. In Figure 3.11 (b), the signal  $s$  is controlled to position its middle point to be the same as that of reference signal  $r$ . This control method doesn't have the additional delay and the good transient response is expected.



Basic scheme of PLL hysteresis control.

(a)



(b)

Figure 3.11 The hysteresis control method with the constant switching frequency in the inverter application

(a) The schematics [113] (b) The operating principles.



However, this implementation is not suitable for VR applications in which the duty cycle is too narrow and it is hard to control the positions of both edges. Moreover, the output of the upper phase detector and that of the lower phase detector have a time difference, and signal  $s$  cannot position itself to the exact middle point even though the average phase error is zero, whereas in the multiphase VR, these points should be exact for good interleaving. Therefore, for the multiphase VR application, the new implementation of this concept is proposed in the following section. Moreover, in the VR application, unlike the inverter applications, the load dynamics are much faster and more analysis is necessary to use this control method.

## **3.2. Proposed Hysteretic Control Method**

The last section examined the problem of implementing the interleaving function with the hysteretic control method for VR applications. The conventional interleaving method for multiphase hysteretic control has a drawback at the load step-up transient. And a constant-frequency hysteretic control method is found from inverter application. This section introduces a multiphase hysteretic control method without degrading the transient response based on the control method from inverter application.

### **3.2.1. Proposed Hysteretic Control Method and Its Operating Principles**

The interleaving methods in Section 3.1 are based on the fixed relationship between the phases. The fixed relationship enables the interleaving function even though the switching frequency is varying. However, this idea is not successful for the multiphase VR because this relationship between phases doesn't change at any condition, which means they interleave even during the load transient, and the duty cycles cannot be overlapped. This results in the bad load step-up dynamic response. Therefore, in this section, another approach is used to achieve interleaving.

Figure 3.12 shows the proposed hysteretic control method. Based on the single-phase hysteretic control method in Chapter 1, the hysteretic band width changing loop is attached following the concept from [113]. The additional circuitry consists of the phase frequency detector (PFD) and the low pass filter (LPF). The basic concept is similar to the well-known phase locked loop (PLL), which synchronizes the frequency and phase of the output clock with

the reference clock [111][112]. The frequency and phase of the duty cycle is synchronized with the reference clock by modifying the hysteretic band width.

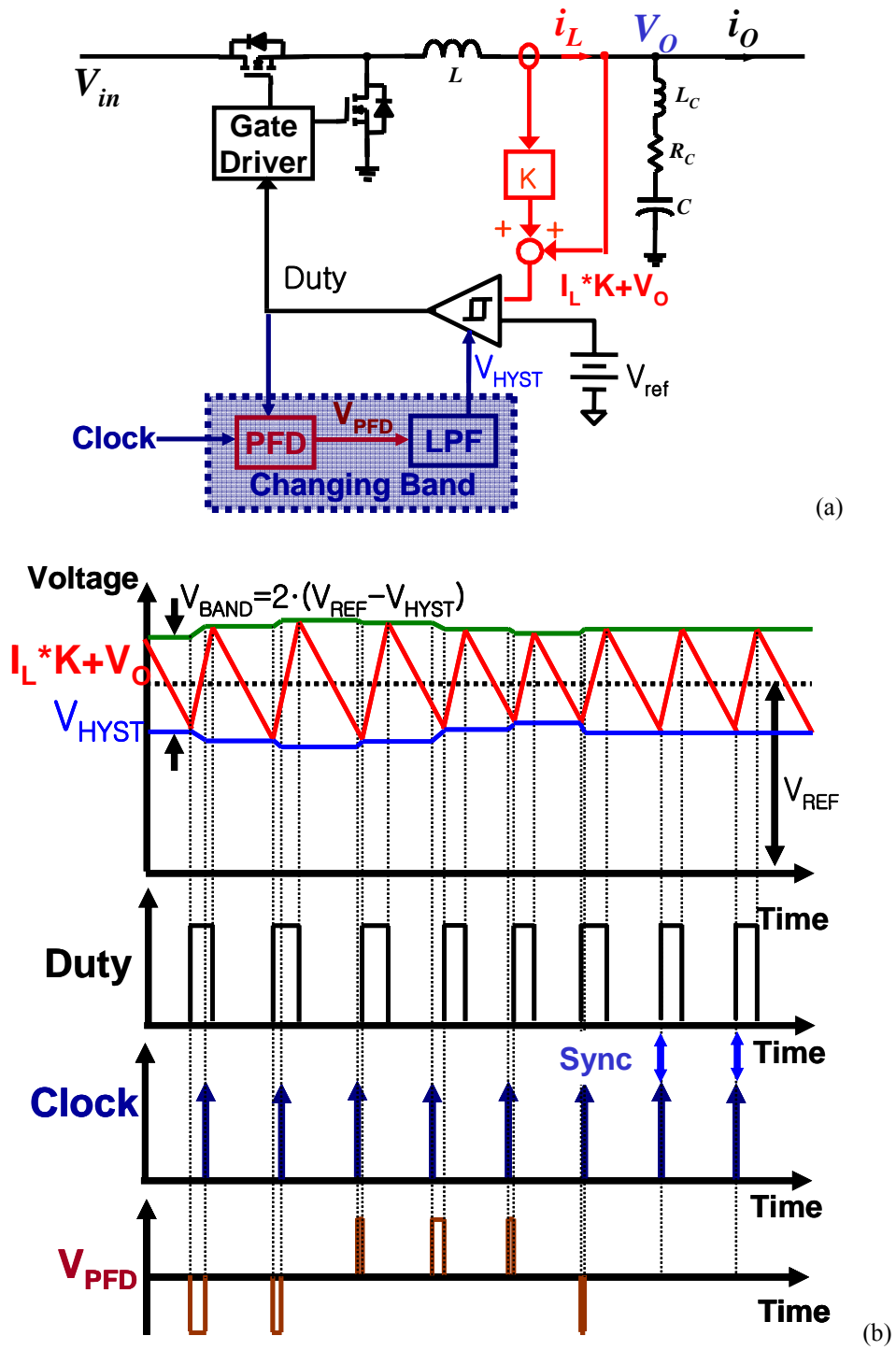


Figure 3.12 The proposed hysteretic control method (a) The schematics (b) The operating principle.

Figure 3.12 (b) shows the operating principles of the proposed hysteretic control method when the load current is constant. The feedback signal ( $I_L \cdot K + V_O$ ) is compared with the hysteretic band, and the duty cycle is made according to the single-phase hysteretic control method in Chapter 1. However, in this control  $V_{HYST}$  is not chosen by the user, but is automatically determined by the additional band width changing loop. If the turn-on edge of the control switch is not synchronized with the external reference clock, the PFD will detect this error and emit an error signal (PFD in Figure 3.12 (b)). By averaging this error signal with LPF,  $V_{HYST}$  is determined. With this  $V_{HYST}$  value, the hysteretic band width ( $V_{BAND}$ ) is determined. Since this hysteretic band width changing loop is similar to the PLL, this loop minimizes the PFD error, and finally the turn-on edge of the control switch is synchronized with the reference clock. Therefore constant frequency operation is achieved at the steady state. Unlike the inverter application in [113], this implementation uses only one PFD and the turn-on edge of the control switch is exactly synchronized with the reference clock and the exact interleaving is achieved at the expense of the slow band changing speed.

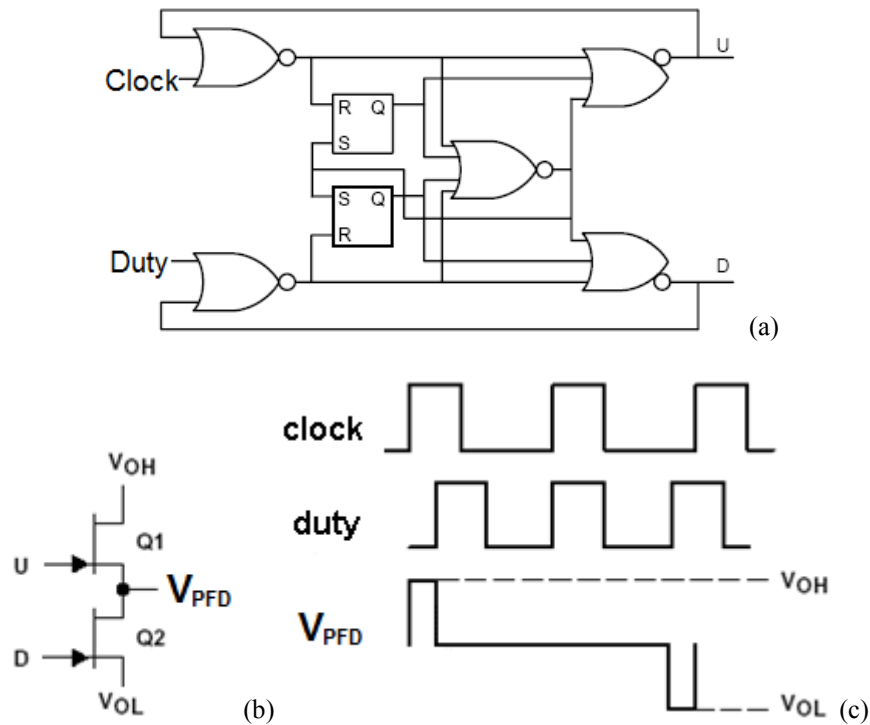


Figure 3.13 The phase frequency detector block (PFD) using TLC2932 [49] (a) The logic implementation of - PFD (b) The charge pump (c) The input and output waveforms.

Figure 3.13 shows an example of the implementation of the phase frequency detector block (PFD) using TLC2932, the PLL IC from Texas Instruments [49]. This block consists of two parts; the phase frequency detector logic and the charge pump. The power of the logic in Figure 3.13 (a) is not enough to produce PFD output voltage ( $V_{PFD}$ ) and the charge pump in Figure 3.13 (b) is necessary. Figure 3.13 (c) is the waveforms of the input and output signals of the PFD block. When the turn-on edge of the clock is ahead, the turn-on edge of duty cycle,  $Q1$  is turned on and  $V_{PFD}$  becomes  $V_{OH}$ . When the turn-on edge of the clock is behind the turn-on edge of the duty cycle,  $Q2$  is turned on and  $V_{PFD}$  becomes  $V_{OL}$ . When these are synchronized both  $Q1$  and  $Q2$  are not turned on and the output remains at the steady-state value of  $V_{PFD}$ , which is determined by the hysteretic band width changing loop. Figure 3.14 verifies this experimentally. Figure 3.14 (a) shows the case when the turn-on edges of the clock and the duty cycle are not synchronized.  $V_{PFD}$  becomes  $V_{OH}$  or  $V_{OL}$  according to the phase error. When  $V_{PFD}$  returns from  $V_{OH}$  or  $V_{OL}$  to the steady-state value, unlike Figure 3.13 (c), it takes some time because of the parasitics of the charge pump. When the turn-on edge of the duty cycle is synchronized to that of the clock,  $V_{PFD}$  remains at the steady state value.

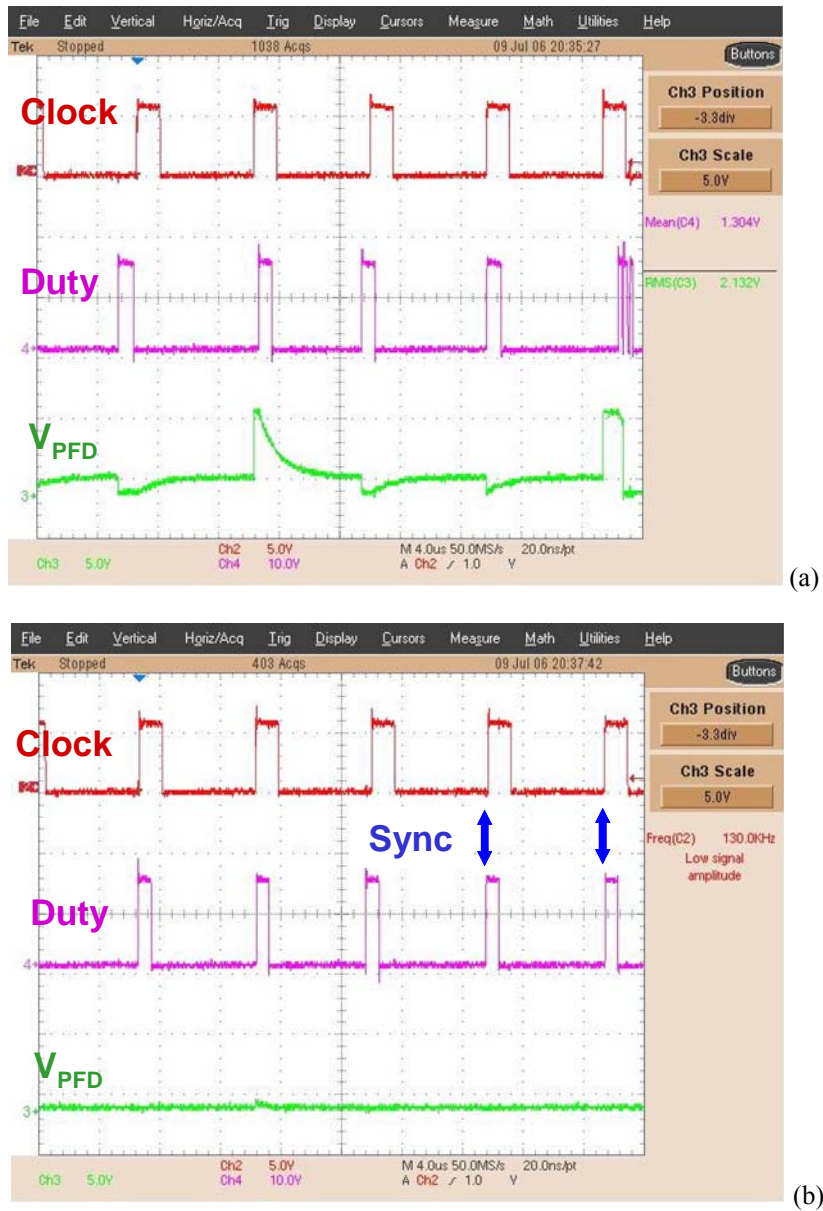


Figure 3.14 The experimental verification of PFD employed in the proposed hysteretic control -  
 (a) The transient state (b) The steady state.

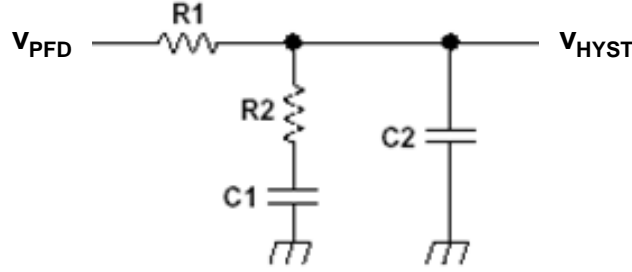


Figure 3.15 The low pass filter.

Figure 3.15 shows the low-pass filter used in Figure 3.12. Following the PLL, two resistors and two capacitors are used. This is discussed in Section 3.3.2 and 3.3.3.

The output regulation is almost same as the conventional hysteretic control for the single-phase VR in Chapter 1. The inductor current is sensed with gain  $K$  and summed with the output voltage. Then this information ( $I_L \cdot K + V_O$ ) is fed back to the hysteretic comparator. The hysteretic band is made inside the controller with the band width signal ( $V_{HYST}$ ) and the reference voltage ( $V_{ref}$ ) following (3.4),

$$V_{BAND} = 2 \cdot (V_{ref} - V_{HYST}). \quad (3.4)$$

Unlike the hysteretic control method in Chapter 1,  $V_{HYST}$  is determined by the hysteretic band width changing loop to synchronize the turn-on edge of the duty cycle to that of the reference clock. In this case, the feedback signal is also regulated within the hysteretic band and the median of the feedback signal is regulated to be same as the reference voltage, like,

$$[I_L \cdot K + V_O]_{Median} = V_{ref}. \quad (3.5)$$

Then the median of the output voltage is regulated following (3.6),

$$[V_O]_{Median} = V_{ref} - K \cdot [I_L]_{Avg}. \quad (3.6)$$

The multiphase VR can be easily implemented by paralleling this single-phase VR with the proposed hysteretic control method, as in Figure 3.16. By phase shifting the reference clock of each phase, interleaving is easily implemented. Figure 3.16 (b) shows the experimental results, and the interleaving is verified with the hardware ( $V_{SW1}$  and  $V_{SW2}$  are the switching node voltage of each phase).

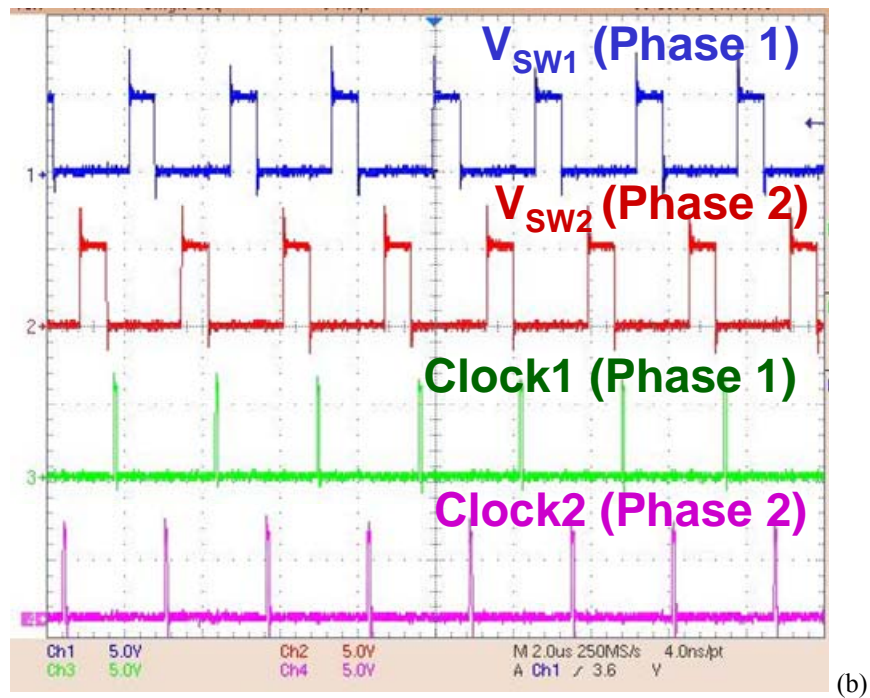
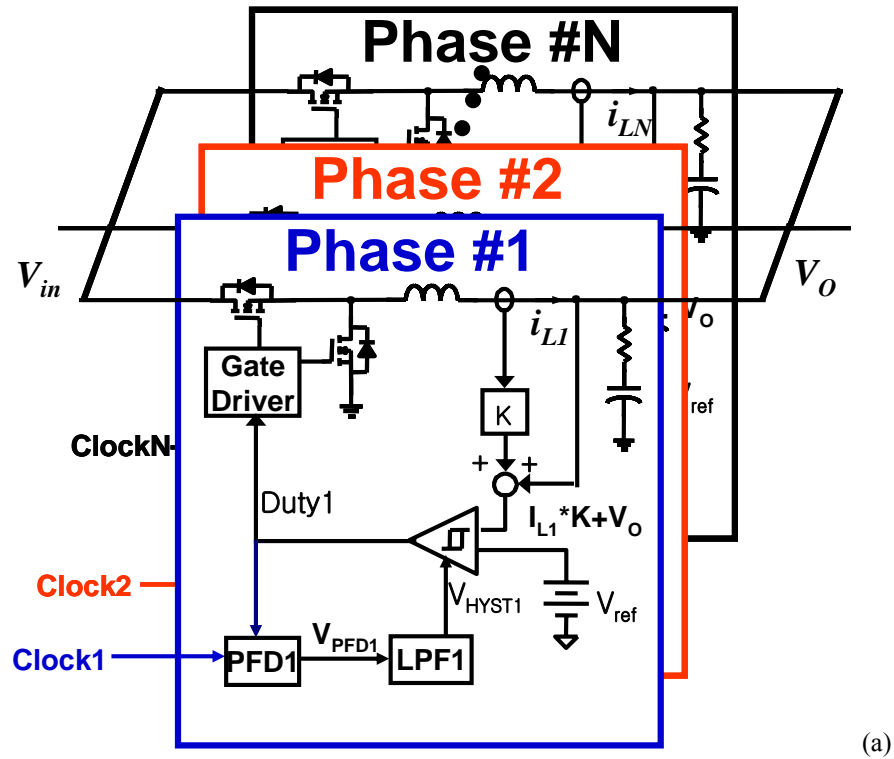


Figure 3.16 The multiphase VR with the proposed hysteretic control method -  
 (a) The schematics (b) The steady state experimental results.

Unlike the other interleaving techniques in Section 3.1, with this control each phase operates independently, and the feedback signal is inside the hysteretic band. Therefore there is no need for an integrator to eliminate the steady state error, and each phase regulates its inductor current and the output voltage following (3.6). The phases have the same output voltage, and the average value of each inductor current is also regulated to be same following (3.7),

$$[V_O]_{Median} = V_{ref} - K \cdot [I_{L1}]_{Avg}, \quad [V_O]_{Median} = V_{ref} - K \cdot [I_{L2}]_{Avg} \quad (3.7)$$

where  $I_{L1}$  is the first phase inductor current, and  $I_{L2}$  is the second phase inductor current. Therefore, current-sharing is achieved.

From (3.7), the total inductor current and the output voltage relationship can be achieved using (3.8),

$$[V_O]_{Median} = V_{ref} - K / 2 \cdot [I_{L1} + I_{L2}]_{Avg} \quad (3.8)$$

This can be generalized as (3.9),

$$[V_O]_{Median} = V_{ref} - K / N \cdot [I_{LT}]_{Avg} = V_{ref} - R_{LL} \cdot [I_{LT}]_{Avg} \quad (3.9)$$

where  $I_{LT}$  is the total inductor current and  $N$  is the phase number. By designing the current sensing gain  $K$  of each phase as  $N \cdot R_{LL}$ , AVP is achieved.

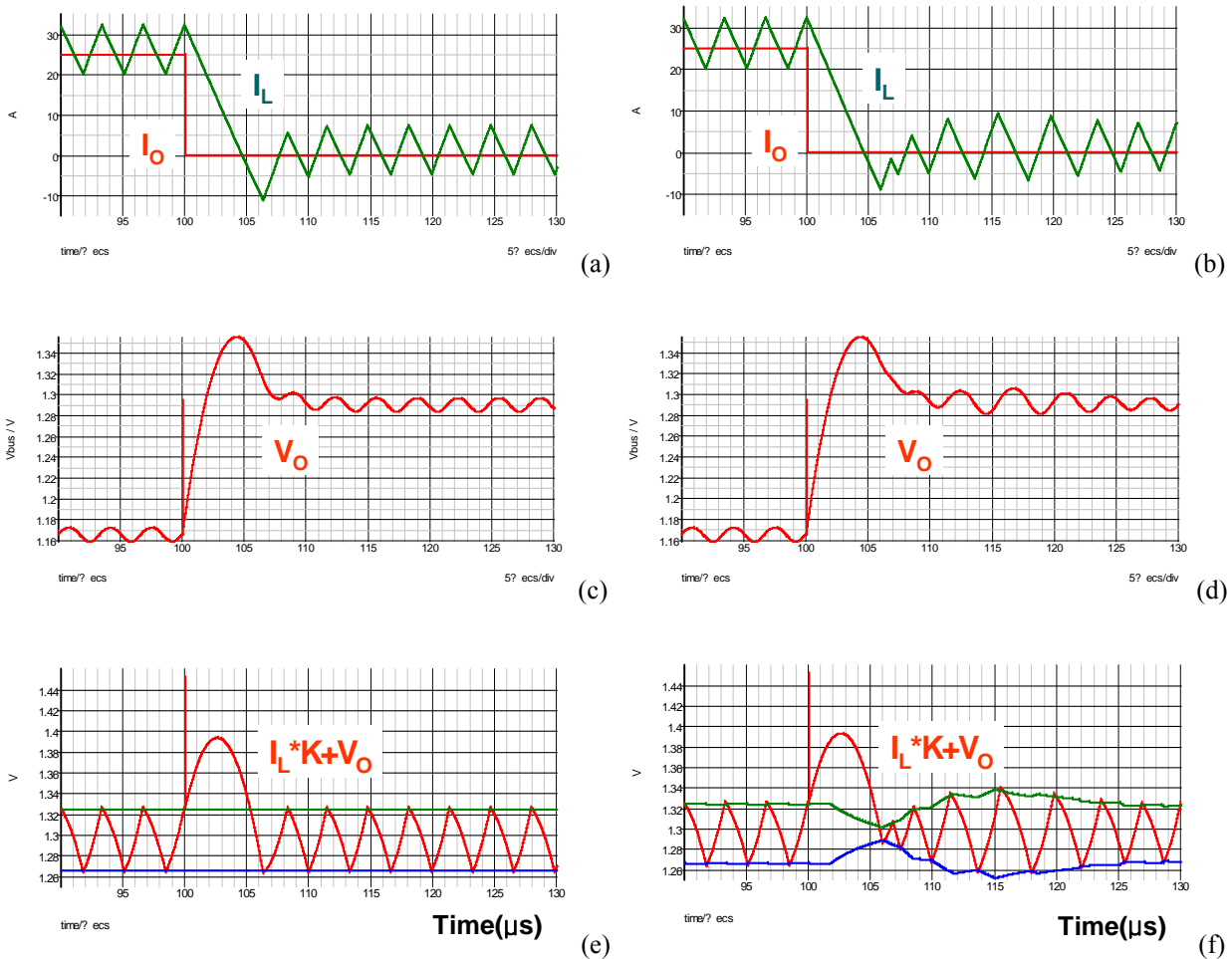
Therefore, with the proposed hysteretic control method, all the required functions for the multiphase VR (AVP, the current sharing, and interleaving functions) are achieved.

### 3.2.2. Transient Response of the Proposed Hysteretic Control Method

In order to understand the transient response of the proposed hysteretic control method, a simulation is performed and compared with the simulation results of the conventional hysteretic control method for the single-phase VR in Chapter 1. Figure 3.17 shows the simulation results of the conventional hysteretic control method and the proposed hysteretic control method. Before the transient, at the steady state, the hysteretic band width of the proposed hysteretic control is almost constant in Figure 3.17 (f). During the transient, in both cases, the inductor current quickly decreases (Figure 3.17 (a) and (b)) and the output voltage quickly increases (Figure 3.17 (c) and (d)); then the feedback signal changes very quickly (Figure 3.17 (e) and (f)). However, the hysteretic band changing dynamics are very slow compared to the feedback signal, and the



feedback signal deviates from the hysteretic band, as shown in Figure 3.17 (f). In the both cases, the output voltage peak is made when the feedback signal is outside the hysteretic band, which says the hysteretic band changing dynamics do not have an impact on the output voltage peak. Therefore, the proposed hysteretic control has the same output voltage peak as the conventional hysteretic control method. After the transient, the hysteretic band width of the proposed hysteretic control method is changed to synchronize the turn-on edge of the control switch to that of the reference clock.



**Figure 3.17** The load step-down transient simulation results (a) The load current and the inductor current with the conventional hysteretic control (b) The load current and the inductor current with the proposed hysteretic control (c) The output voltage with the conventional hysteretic control (d) The output voltage with the proposed hysteretic control (e) The feedback signal and the hysteretic band with the conventional hysteretic control (f) The feedback signal and the hysteretic band with the proposed hysteretic control.

Figure 3.18 shows the load step-up transient comparison between the hysteretic control method with the conventional interleaving method in Section 3.1 (Figure 3.18 (a)) and with the proposed interleaving method (Figure 3.18 (b)). With the conventional interleaving method, the duty cycles cannot overlap and the charge from the output capacitors is large. An output voltage dip is expected. Meanwhile, with the proposed hysteretic control method, the output feedback loop is much faster than the hysteretic band width changing loop and the synchronization between the reference clock and the duty cycle is lost. Then the interleaving function is lost during the transient and the duty cycles can overlap. Therefore, a larger total inductor current slew rate is expected and the charge from the output capacitors will be small.

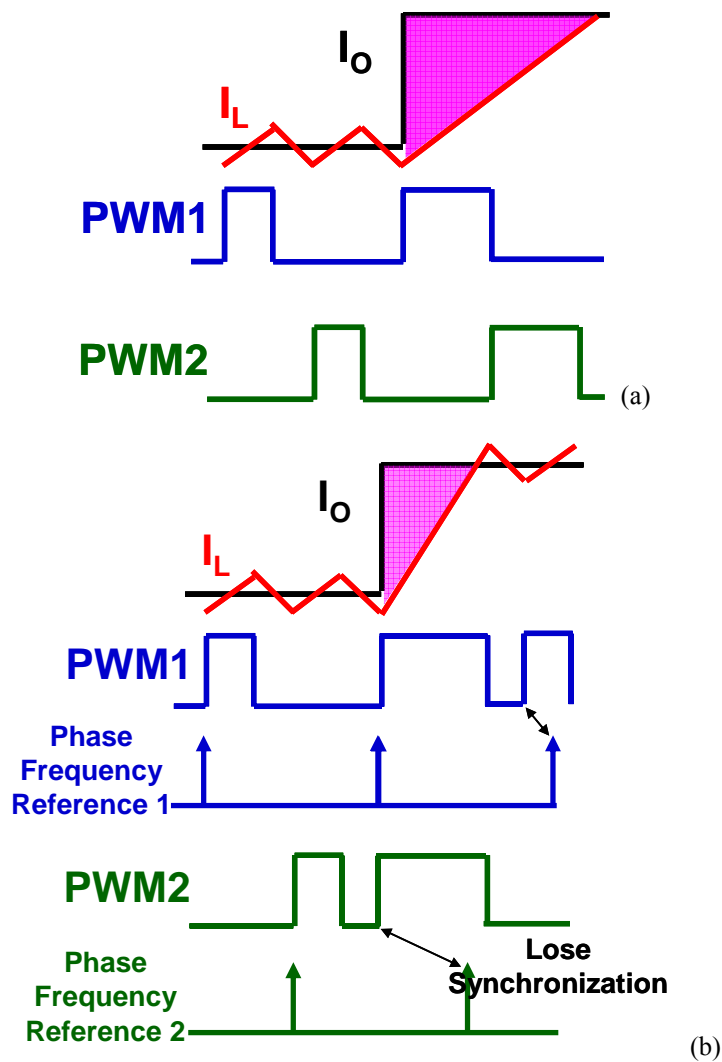
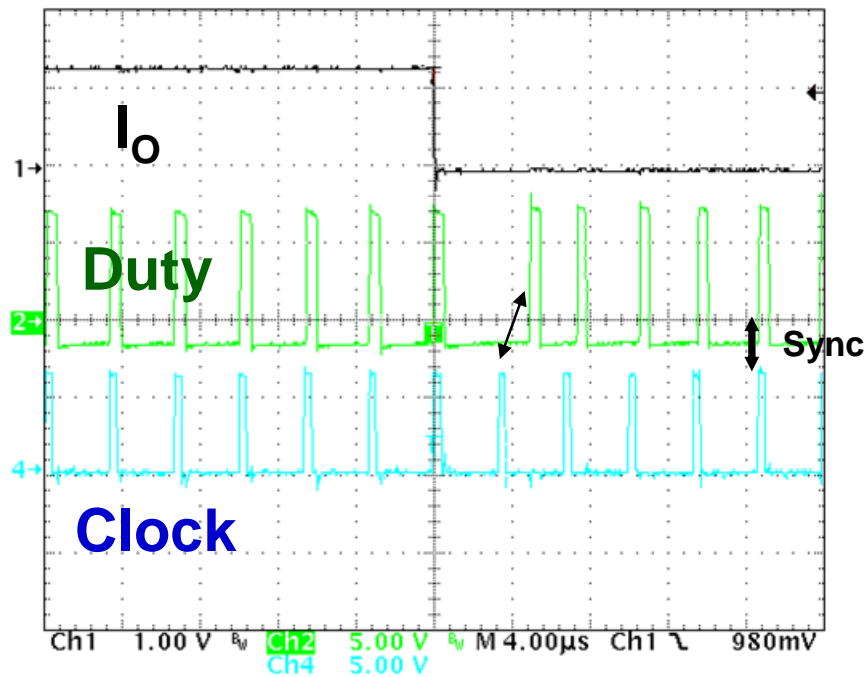
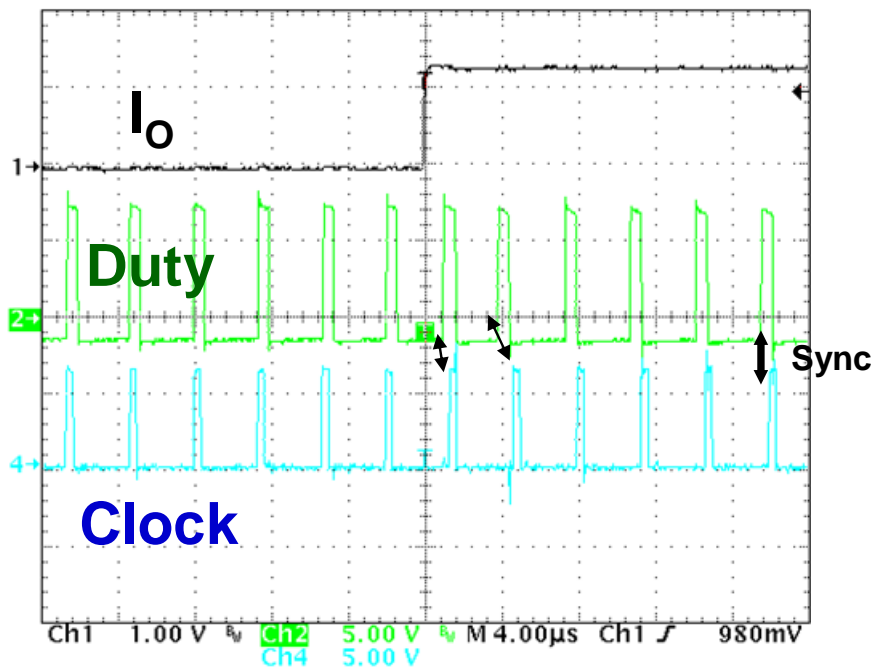


Figure 3.18 The load step-up transient of the hysteretic control method -  
 (a) with the conventional interleaving method (b) with the proposed interleaving method.

Figure 3.19 shows the experimental verification of the transient response. It is observed that the synchronization is lost during the transient as expected.



(a)

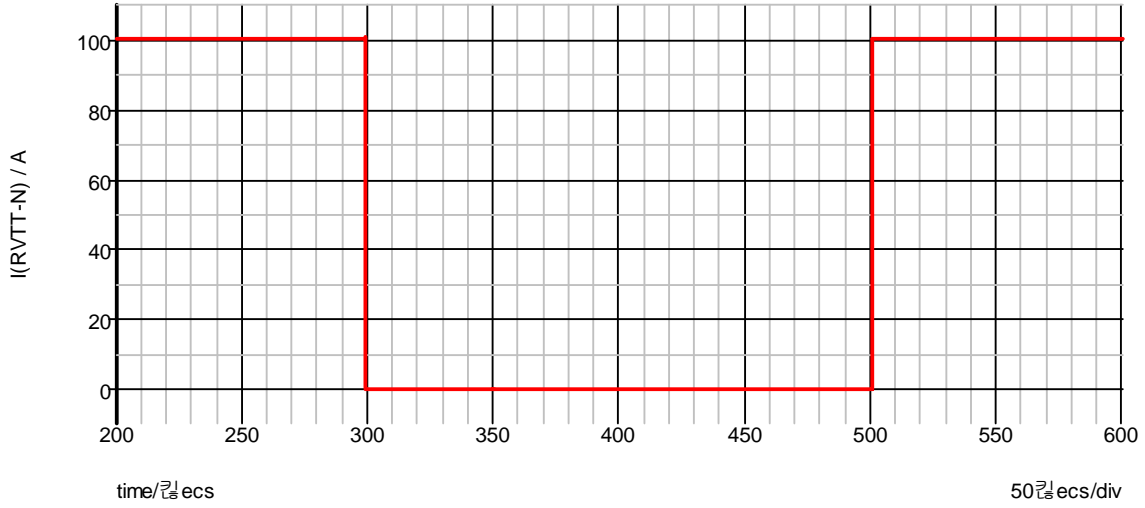


(b)

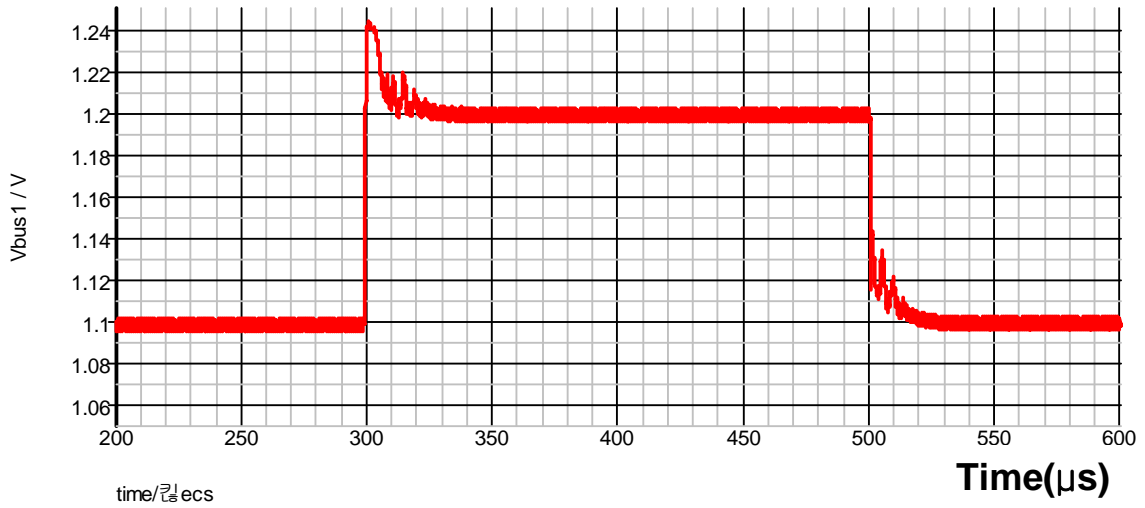
Figure 3.19 The transient experimental results of the proposed hysteretic control method -  
 (a) The load step down (b) The load step up.

Figure 3.20 shows the SIMPLIS simulation results of the VRD 11.0 VR with the proposed hysteretic control method. All the other conditions are the same as the simulation in Figure 3.5. It is a four-phase VR with a 300nH inductor for each phase, 300kHz switching frequency for each phase, 12V input voltage, 1.2V VID, 1m $\Omega$   $R_{LL}$ , a load current of 0~100A, and 6 $\times$ 560 $\mu$ F Al-Polymer capacitors for the bulk capacitors. The output capacitors are designed for the load step-down transient with 50mV peak voltage, as released from Intel [16]. We observe that there is no dip at the load step-up transient. This meets the specification very well, whereas the conventional interleaving method requires an additional 3 $\times$ 560 $\mu$ F bulk capacitors to satisfy the specification.

The proposed hysteretic control method can achieve current sharing, adaptive voltage positioning control, and fast transient response. Furthermore, the interleaving among the phases can be implemented without degrading the other functions. In addition, the constant switching frequency is achieved at the steady state. The additional circuitry may increase the controller cost, but considering that some controllers already have the PLL inside the IC [112], the additional cost on the controller is acceptable.



(a)



(b)

Figure 3.20 SIMPLIS simulation results of the proposed hysteretic control - ( $6 \times 560 \mu\text{F}$  output capacitors) (a) The load current waveform (b) The output voltage waveform.

### 3.2.3. Challenges of the Proposed Hysteretic Control Method

The proposed hysteretic control consists of two loops, the hysteretic control loop and PLL. It is well known that both loops are nonlinear. Predicting the behavior of this quite nonlinear control with the dynamic load is a big challenge.

First, in the hysteretic control method, the output voltage peak is made when the feedback signal is out of the hysteretic band and this output voltage peak is not controlled by the hysteretic controller. In order to design the system, this output voltage peak should be predicted, and a model to predict the output voltage peak is necessary.

Moreover with the proposed hysteretic control method, the output voltage ripples become larger during the transient, but will settle down after some time. The magnitude of this larger ripple and this settling time can be controlled by the hysteretic band width changing loop design. To design this loop, a model is necessary. The next section is about the modeling and design of the proposed hysteretic control method.

### 3.3. Modeling and Design of the Proposed Hysteretic Control Method

The hysteretic control method is one of a nonlinear control method. Obviously no universal technique has been devised for the analysis of all nonlinear control systems. Therefore, many efforts have been made to develop appropriate theoretical tools for each nonlinear control system. These efforts are based on three methods [128][129] [130][131].

- Phase plane analysis: Phase plane analysis is a graphical tool for studying second-order nonlinear systems. Its basic idea is to solve a second-order differential equation graphically, instead of seeking an analytical solution. This analysis is suitable for large signal analysis. This analysis has the fundamental limitation of being applicable only to systems which can be well approximated by second-order dynamics.
- Lyapunov theory: Basic Lyapunov theory comprises two methods introduced by Lyapunov; the indirect method and the direct method. The indirect method is also called the ‘linearization method’. This states the stability properties of a nonlinear system in the close vicinity of the equilibrium point which are the same as in the

linearization approximation. The method serves as the theoretical justification for using linear control for physical systems, which are always inherently nonlinear. The direct method is so-called “Lyapunov analysis.” This method is used to analyze the stability of the nonlinear systems using a scalar energy-like function (Lyapunov function) to see whether it decreases. This method can be applicable to all kinds of control systems, be they time-varying or time-invariant, finite dimensional or infinite dimensional. The limitation of this method is that it is very difficult to find a Lyapunov function for a given system.

- Describing function: The describing function method is an approximation technique for studying nonlinear systems. The basic idea of the method is to approximate the nonlinear components in nonlinear control systems by linear “equivalents,” and then use frequency domain techniques to analyze the resulting systems. This method is not limited to second-order systems, nor is it as difficult to find the related function as with the Lyapunov function. The drawbacks of this method are related to its approximate nature, which means there is the possibility of inaccurate predictions.

The proposed hysteretic control method consists of two nonlinear loops. The first loop is the fast hysteretic control loop ( $T_{MAIN}$ ) and the other is the slow hysteretic band width changing loop ( $T_{BAND}$ ). Figure 3.21 shows these two loops. Because of the speed difference, these loops can be separated. In particular, the output voltage peak is unrelated to  $T_{BAND}$  shown in Figure 3.17 (b), (d), and (f); and by analyzing  $T_{MAIN}$ , the output voltage peak can be predicted. A Buck synchronous converter is used for the VR, and there are only two states in the Buck converter; the inductor current and the capacitor voltage. Therefore, in order to predict the output voltage peak, which is the result of the second order dynamics of VR, the phase plane method is chosen in Section 3.3.1.

In Figure 3.17, it is observed that after the output voltage peak, the feedback signal comes inside the hysteretic band and the hysteretic band changing loop is working to synchronize the turn-on edge of the duty cycle to that of the reference clock; when the feedback signal is outside the hysteretic band, this loop is saturated because the phase error is not reduced even though the hysteretic band width changes.  $T_{BAND}$  can be separated into two modes; when the feedback signal

is inside the hysteretic band and when it is outside the hysteretic band. Only a very large disturbance in  $T_{MAIN}$  makes the feedback signal outside the band, which means when the feedback signal is inside the hysteretic band, there is very small disturbance in  $T_{MAIN}$ . Then the small-signal assumption can be used to analyze  $T_{BAND}$  dynamics. Therefore, in Section 3.3.2, the linearization (based on the Lyapunov indirect theory) using the sampled data model is performed and  $T_{BAND}$  is analyzed.

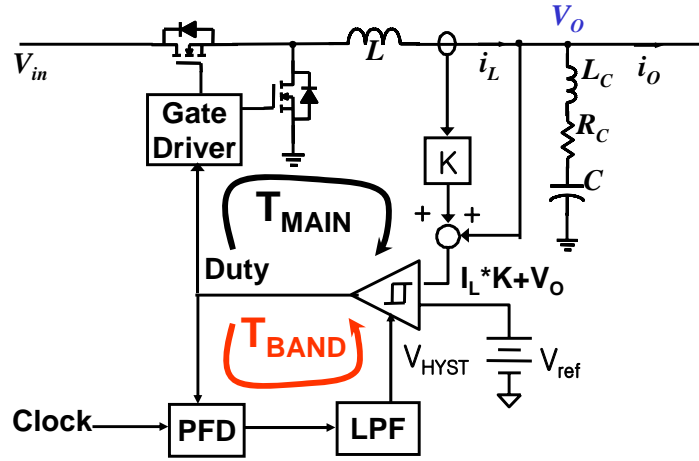


Figure 3.21 The proposed hysteretic control has two loops,  $T_{MAIN}$  and  $T_{BAND}$ .

### 3.3.1. Phase Plane and Transient Analysis

Many people have tried to create a good model for the hysteretic control method. Among them is the geometric approach, or the phase plane analysis using the phase portrait [124][125][126] [127][128][129][130][135][136][137], which is a very good analyzing tool for the fast transient hysteretic control. This is because in this control, our interest is the large-signal performance and the small-signal assumption, or the averaging assumption is no longer valid. Using this approach, the large-signal response can be predicted and the output capacitors can be designed.

Assuming the pulse-width modulated dc/dc converter is a piecewise linear system, the synchronized buck converter can be simplified, like in Figure 3.22. When the duty is ‘1’, the system is an on-state linear system and can be modeled with the linear equation (3.10).



$$\begin{bmatrix} \dot{V}_o \\ \dot{I}_L \end{bmatrix} = \begin{bmatrix} -\frac{R_C}{L} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} V_o \\ I_L \end{bmatrix} + \begin{bmatrix} \frac{R_C}{L} \\ \frac{1}{L} \end{bmatrix} V_{IN} + \begin{bmatrix} -\frac{I_o}{C} \\ 0 \end{bmatrix} \quad (3.10)$$

When the duty is '0', the system is an off-state linear system and can be modeled as (3.11).

$$\begin{bmatrix} \dot{V}_o \\ \dot{I}_L \end{bmatrix} = \begin{bmatrix} -\frac{R_C}{L} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} V_o \\ I_L \end{bmatrix} + \begin{bmatrix} -\frac{I_o}{C} \\ 0 \end{bmatrix} \quad (3.11)$$

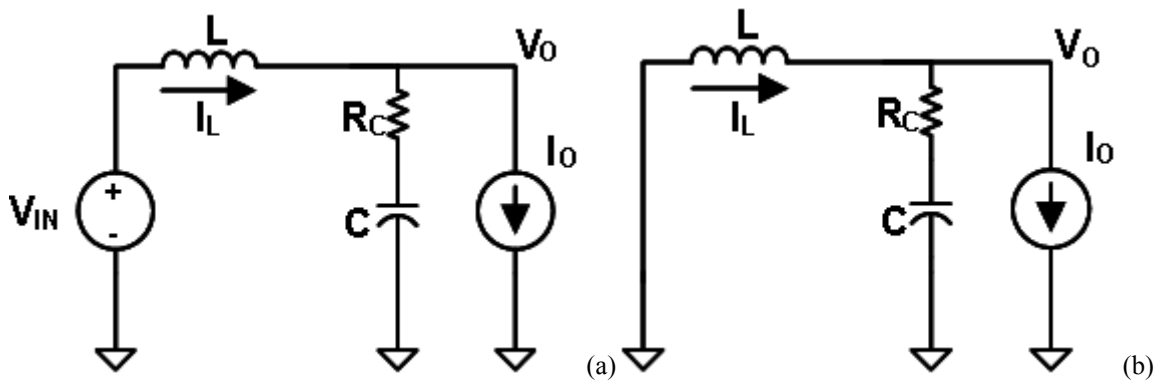


Figure 3.22 The piecewise linear model of the Buck converter (a) On state (b) Off state.

Table 3.1 Equilibrium points

State	ON	OFF
Equilibrium points $(I_L, V_o)$	$(I_o, V_{IN})$	$(I_o, 0)$

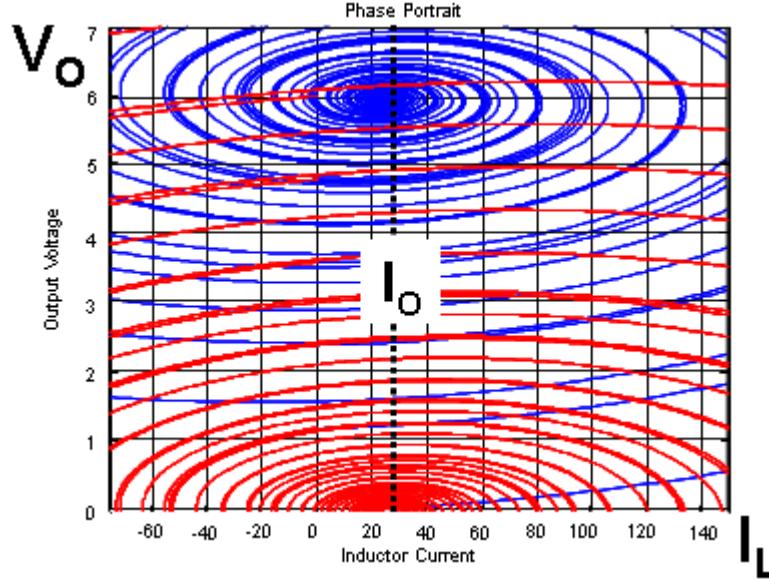


Figure 3.23 The phase portrait of the piecewise linear model (blue lines: on state, red lines: off state).

Each linear system has only one equilibrium point, which is easily calculated (see Table 3.1). In the linear system, every state variable converges at the equilibrium point as time goes towards infinity, and the state trajectories can be drawn in the phase portrait according to the linear equations, as in Figure 3.23.

The linear equations (3.10) and (3.11) can be calculated using MATLAB or MathCAD; however, in order to get the analytic expression, the simplified state plane model is necessary. With the assumption that the state trajectory is for the short time ( $t < \pi \cdot \sqrt{L \cdot C}$ ) and the inductance is not too small, like  $4L \gg C \cdot R_C^2$ , (3.10) is solved as,

$$V_o(t) = V_{IN} + (V_{O0} - V_{IN}) \cdot \cos\left(\frac{t}{\sqrt{L \cdot C}}\right) + \left[ \sqrt{\frac{L}{C}} \cdot (I_{L0} - I_{Load}) - \frac{R_C}{2} \cdot \sqrt{\frac{C}{L}} \cdot (V_{O0} - V_{IN}) \right] \cdot \sin\left(\frac{t}{\sqrt{L \cdot C}}\right), \quad (3.12)$$

$$I_L(t) = I_{Load} + (I_{L0} - I_{Load}) \cdot \cos\left(\frac{t}{\sqrt{L \cdot C}}\right) + \left[ -\sqrt{\frac{C}{L}} \cdot (V_{O0} - V_{IN}) + \frac{R_C}{2} \cdot \sqrt{\frac{C}{L}} \cdot (I_{L0} - I_{Load}) \right] \cdot \sin\left(\frac{t}{\sqrt{L \cdot C}}\right) \quad (3.13)$$

where  $(I_{L0}, V_{O0})$  is the initial state.

From Equations (3.12) and (3.13), the state plane equation for the on state is calculated as

$$C \cdot [V_o(t) - R_C \cdot (I_L(t) - I_{L0}) - V_{IN}]^2 + L \cdot [I_L(t) - I_{L0}]^2 = C \cdot [V_{O0} - V_{IN}]^2 + L \cdot [I_{L0} - I_{L0}]^2 \quad (3.14)$$

and (3.11) is solved as,

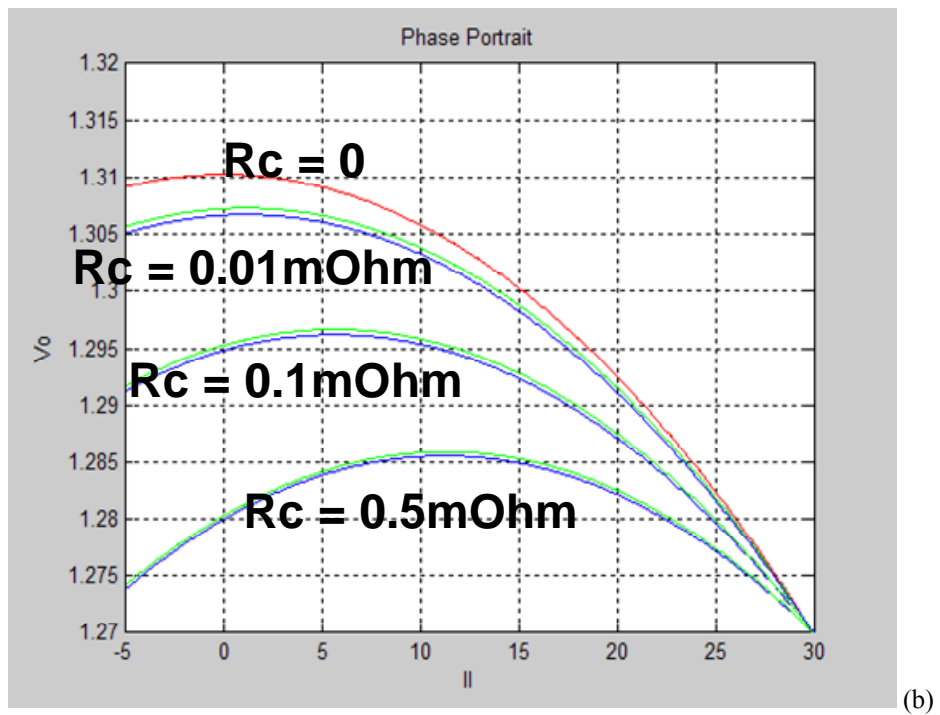
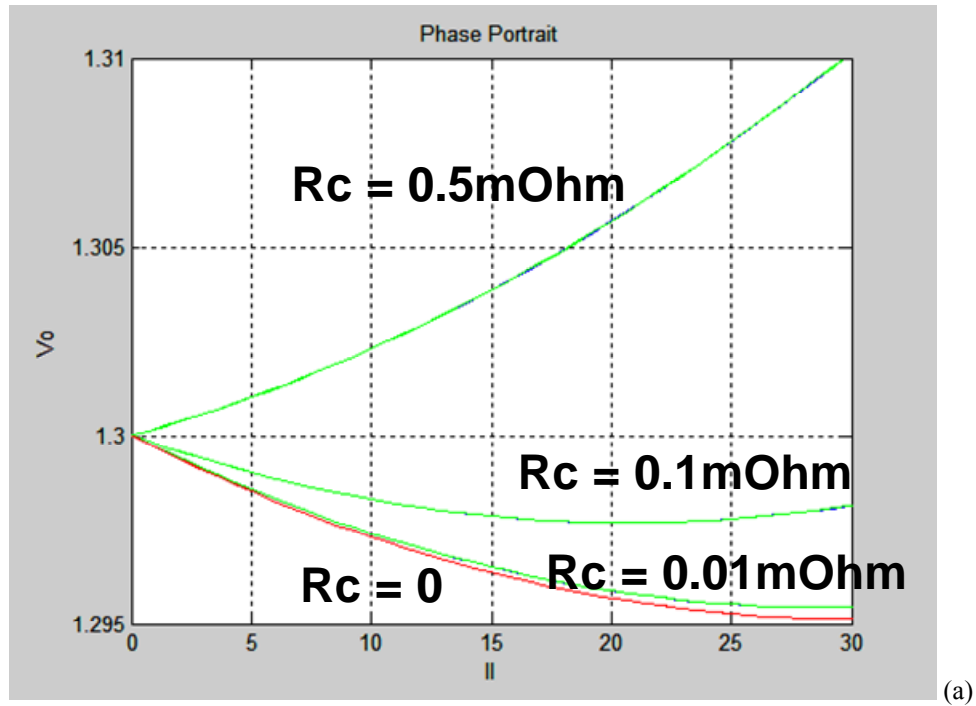


Figure 3.24 The state plane model verification (Blue lines; SIMPLIS Simulation, Green lines; State Plane Model, Red lines; State Plane Model when  $R_c=0$ ) (a) On state (b) Off state.

$$V_o(t) = V_{o0} \cdot \cos\left(\frac{t}{\sqrt{L \cdot C}}\right) + \left[ \sqrt{\frac{L}{C}} \cdot (I_{L0} - I_{Load}) - \frac{R_C}{2} \cdot \sqrt{\frac{C}{L}} \cdot V_{o0} \right] \cdot \sin\left(\frac{t}{\sqrt{L \cdot C}}\right), \quad (3.15)$$

$$I_L(t) = I_{Load} + (I_{L0} - I_{Load}) \cdot \cos\left(\frac{t}{\sqrt{L \cdot C}}\right) + \left[ -\sqrt{\frac{C}{L}} \cdot V_{o0} + \frac{R_C}{2} \cdot \sqrt{\frac{C}{L}} \cdot (I_{L0} - I_{Load}) \right] \cdot \sin\left(\frac{t}{\sqrt{L \cdot C}}\right). \quad (3.16)$$

From Equations (3.15) and (3.16), the state plane equation for the on state is calculated as,

$$C \cdot [V_o(t) - R_C \cdot (I_L(t) - I_{L0})]^2 + L \cdot [I_L(t) - I_{L0}]^2 = C \cdot [V_{o0}]^2 + L \cdot [I_{L0} - I_{L0}]^2 \quad (3.17)$$

Figure 3.24 verifies Equation (3.14) and (3.17). The blue lines are SIMPLIS simulation results and the green lines are from Equation (3.14) and (3.17). They match well.

The controller switches these on and off states by using the duty signal to regulate the output voltage or the inductor current within the steady-state operating ranges. The control law determines the switching action. Because the hysteretic control feeds back the direct inductor current and the output voltage information to the comparator, the control law is easily drawn in a phase portrait like Figure 3.25. The upper boundary of the hysteretic band is

$$I_L \cdot K + V_o = V_{ref} + V_{BAND} / 2. \quad (3.18)$$

The lower boundary of the hysteretic band is

$$I_L \cdot K + V_o = V_{ref} - V_{BAND} / 2. \quad (3.19)$$

If the initial state is  $(I_{L0}, V_{o0})$ , the state follows the off-state trajectory and when it touches the lower boundary of the hysteretic band, the hysteretic controller changes the system status to the on state. Then the state follows the on-state trajectory. When it touches the upper boundary, the system is changed to the off state. With these actions, the state slides within the hysteretic band and finally it makes a limit cycle around the steady-state operating point. This limit cycle represents the inductor current and the output voltage ripples. Therefore the states are regulated in one operating point by the control law.

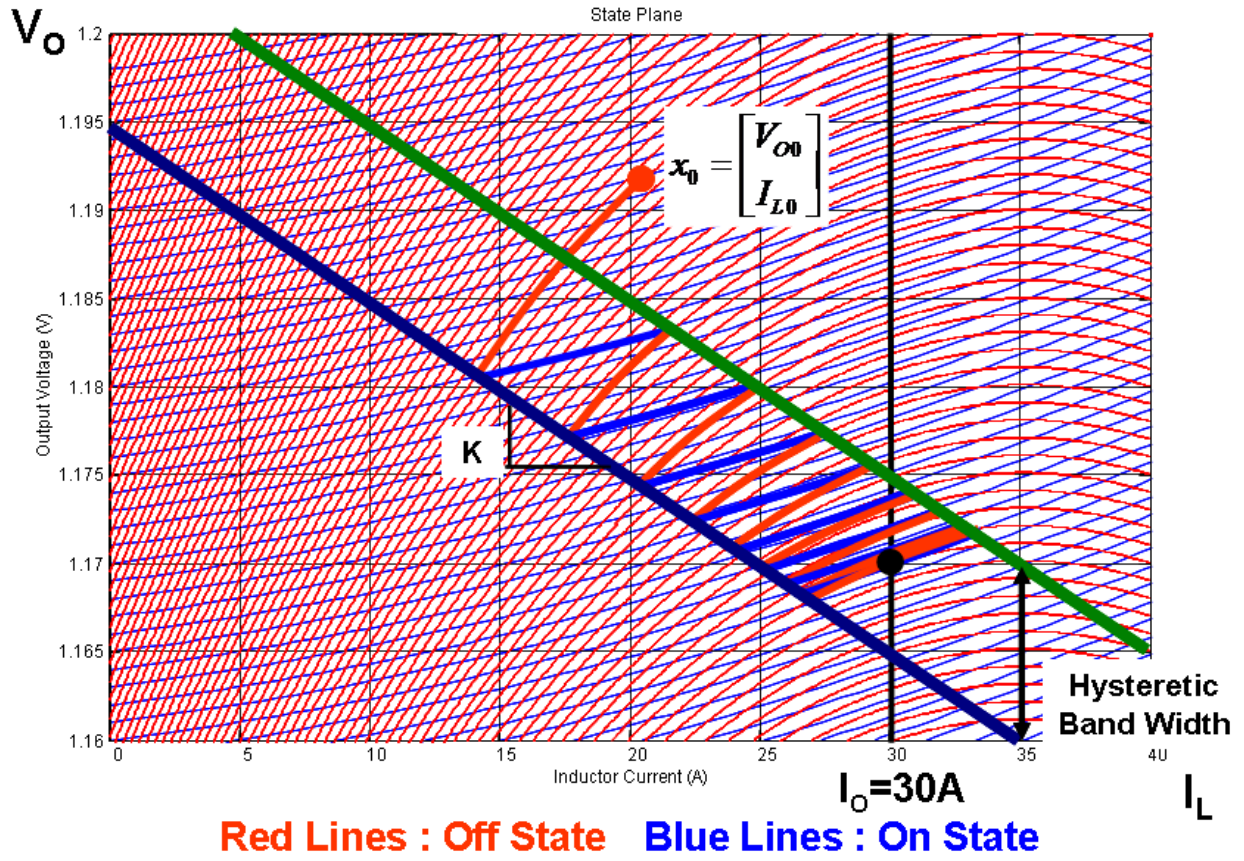


Figure 3.25 The phase portrait of the buck converter with the hysteretic control method.

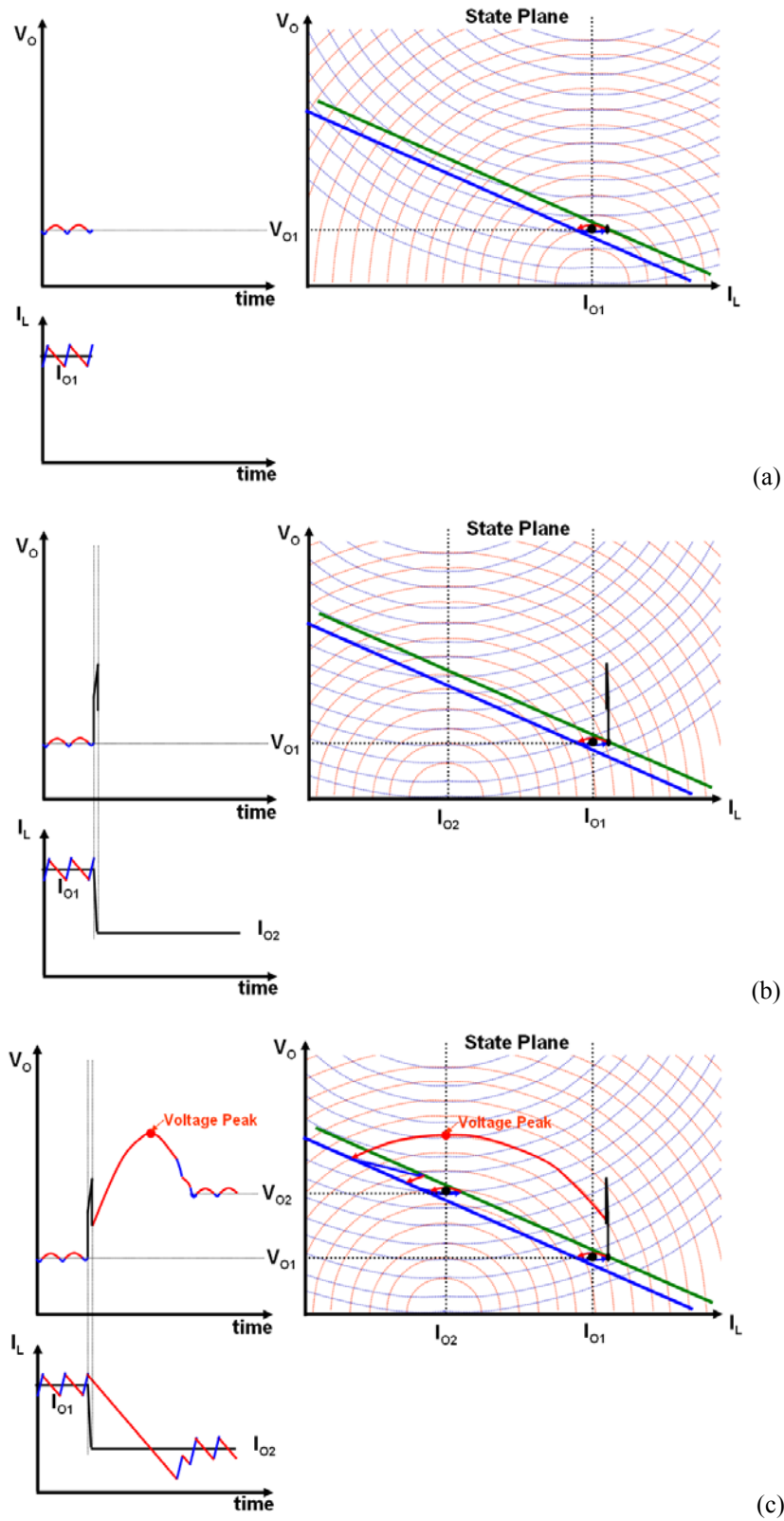


Figure 3.26 The state plane and the load step-down transient with the constant hysteretic band width (a) The load current is  $I_{O1}$  (b) The load current transient from  $I_{O1}$  to  $I_{O2}$  (c) The load current is  $I_{O2}$ .

Figure 3.26 shows the state portrait of the system with the constant hysteretic band width at the load step down transient. Figure 3.26 (a) shows the steady-state phase portrait when the load current is constant as  $I_{O1}$ . Following the concept outlined in the previous pages, the output voltage is regulated as  $V_{O1}$  and the inductor current is also regulated near  $I_{O1}$ . There are steady-state output voltage ripples and inductor current ripples, and these are making the limit cycles in the state plane. Then the load transient occurs as in Figure 3.26 (b). Because the load transition is much faster than the states transition, the states are moved only by the ESL and the ESR of the output capacitors. Therefore, during this period, there is just the jump. After the load current transition occurs, like Figure 3.26 (c), the load current is again constant as  $I_{O2}$ , and the states follow the new state trajectories based on the constant load current  $I_{O2}$ . Following the concept in Figure 3.25, the states reach the new operating point and the output voltage and the inductor current are regulated as  $V_{O2}$  and  $I_{O2}$ . For the load step-up transient, the concept is the same.

Figure 3.27 shows the simulation results of the proposed hysteretic control method for the load step-down transient. Figure 3.27 (d) shows the state portrait, and the corresponding time domain simulation results are in Figure 3.27 (a), (b), and (c). When the load current is  $I_{O1}$ , the steady-state operating point is  $A$ , and the state makes a limit cycle around that value. Assuming the hysteretic band width changing loop is well-designed, the hysteretic band is also in the steady state, and the hysteretic band is constant like the solid lines in Figure 3.27 (d). When the load current steps down from  $I_{O1}$  to  $I_{O2}$ , the whole state trajectories move to the left, just like the constant hysteretic band width case, because the equilibrium points are moved from  $I_{O1}$  to  $I_{O2}$ . The worst case for the output voltage peak is when the load step-down occurs at point  $\alpha$ , because point  $\alpha$  is the farthest point from the new equilibrium point  $B$  and it will make the largest state trajectory. During this load transition period, the parasitic parameters, such as ESL and ESR of the output capacitors, make point  $\alpha$  move to point  $\beta$ , just as with the constant hysteretic band width. Then the state can not stay around the point  $A$ ; instead, the state moves toward the new operating point  $B$  following the state trajectory, which can be derived from the linear equation (3.12). Meanwhile, the hysteretic band slowly changes from the solid lines values to the dotted lines values. It is observed that the peak voltage has nothing to do with this hysteretic band change, for the peak voltage is made when the state is out of the hysteretic band.

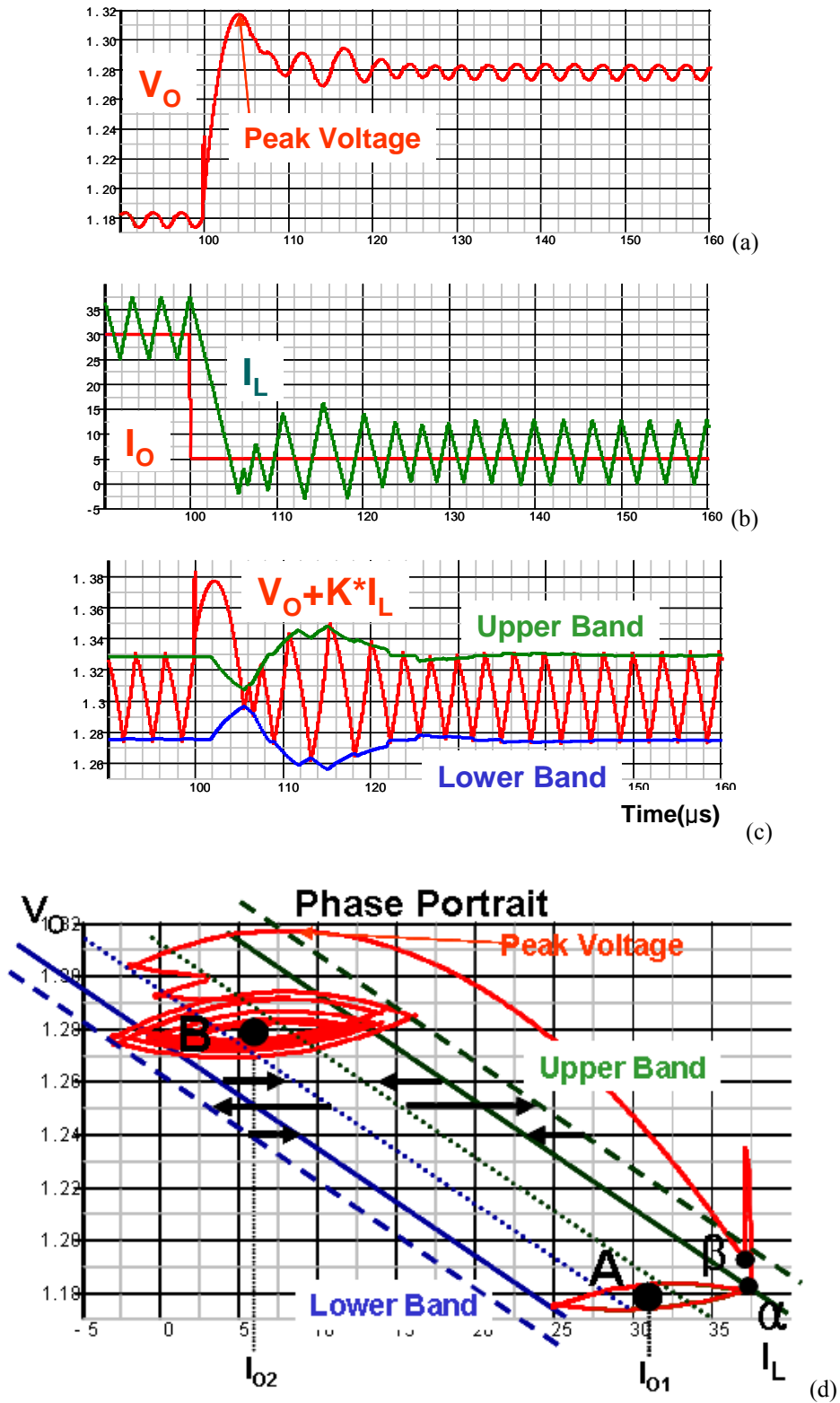


Figure 3.27 The load step down SIMPLIS simulation results of the proposed hysteretic control (a) The output voltage ( $V_o$ ) (b) The load current ( $I_o$ ) and the inductor current ( $I_L$ ) (c) The feedback signal and the hysteretic band (d) The phase portrait.



With the first big state trajectory, the peak voltage is made, and after this big state trajectory the state is regulated within the slowly changing hysteretic band. Therefore, the transient response can be separated into two parts: the first period with the large state trajectory, which is not relevant to the hysteretic band width changing loop, and the second period, in which the state is within the changing hysteretic band. The first part is analyzed with the phase portrait.

In order to predict the output voltage peak, all the points in Figure 3.27 (d) should be calculated.

1. According to (3.6), point A is  $(I_{O1}, V_{REF}-I_{O1}\cdot K)$ .
2. Assuming the inductor current ripple is  $\Delta I_L$ , point  $\alpha$  is,  
 $(I_{O1} + \Delta I_L/2, V_{REF}-I_{O1}\cdot K + R_C \cdot \Delta I_L/2)$ .
3. Assuming the load current change is  $\Delta I_O$ , point  $\beta$  is,  
 $(I_{O1} + \Delta I_L/2, V_{REF}-I_{O1}\cdot K + R_C \cdot (\Delta I_L/2 + \Delta I_O))$ .
4. From point  $\beta$  to the peak voltage point, the states follows the state trajectory with the load current  $I_{O2}$ . This state trajectory can be calculated from equation (3.17).
5. The peak voltage is when  $dv/dt$  is 0 and from (3.11)

$$\frac{dV_O}{dt} = -\frac{R_C}{L} \cdot V_{O\_peak} + \frac{1}{C} \cdot I_L - \frac{I_O}{C} = 0 \quad (3.20)$$

6. With equation (3.20) and (3.17), the peak voltage is calculated as,

$$V_{O\_peak} = -R_C \cdot (I_{L0} - I_O) + \sqrt{V_{O0}^2 + \frac{L}{C} \cdot (I_{L0} - I_O)^2} \quad (3.21)$$

where the initial state is point  $\beta$ .

In Equation (3.21), it is observed that by designing the inductance and the capacitance of the system, the output voltage peak is designed. Generally, in today's VR applications, the inductance is designed for efficiency; therefore the number of the output capacitors is designed for the output voltage peak.

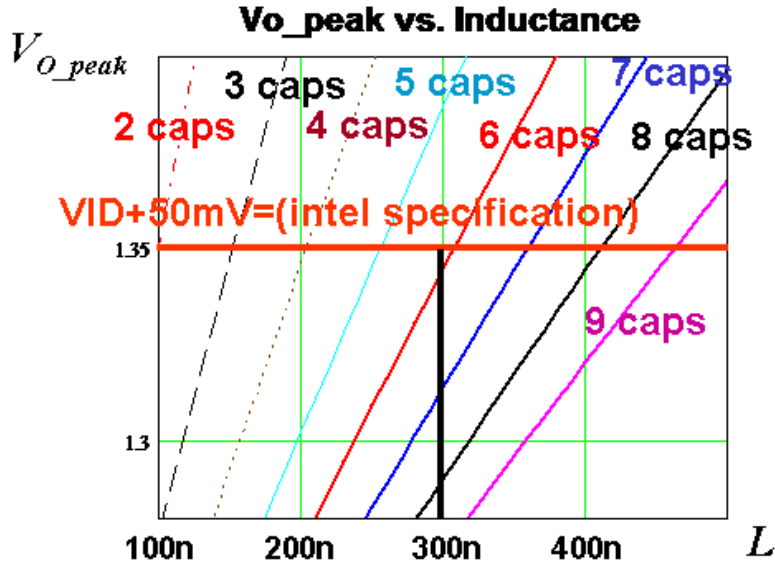


Figure 3.28 The relationship between the inductance, the output voltage peak and the output capacitors for the two-phase hysteretic controlled VR ( $V_{ID}=1.3V$ ,  $R_{droop}=2.5m\Omega$ ,  $F_s=300kHz$ ,  $di_o/dt=200A/\mu s$ ).

In VR applications, the output capacitors are designed to reduce the output peak voltage. Using Equation (3.21), the output voltage peak can be predicted according to the given inductance and the output capacitor type. Figure 3.28 shows the relationship between the inductance, the output voltage peak and the output capacitors for the two-phase hysteretic controlled VR when  $V_{ID}=1.3V$ ,  $R_{droop}=2.5m\Omega$ ,  $F_s=300kHz$ , and  $di_o/dt=200A/\mu s$ , assuming  $100\mu F$  ceramic capacitors are used for the output capacitors. In the VRD 11.0 specification, the peak voltage is  $V_{ID}+50mV$ . The inductance is related to the efficiency, and the inductance is chosen as  $300nH$ . Then the output capacitors are chosen to be  $6 \times 100\mu F$  ceramic capacitors.

Figure 3.29 shows the SIMPLIS simulation results of the proposed hysteretic control method with one  $T_{BAND}$  design. The output capacitors are designed for the output voltage peak when the feedback signal is outside the hysteretic band, just as the case in Figure 3.27. Therefore this peak is within the specification ( $V_{ID}+50mV$ ). However, this system cannot meet the specification because of the second output voltage peak in Figure 3.29. The reason for the second output voltage peak can be found in Figure 3.29 (d). The largest state trajectory is made with a very large hysteretic band width. The hysteretic band width is determined by the hysteretic band width changing loop ( $T_{BAND}$ ). Therefore, the design of  $T_{BAND}$  is very important to achieving the good design of the proposed hysteretic control. In order to design  $T_{BAND}$ , a good model is necessary.

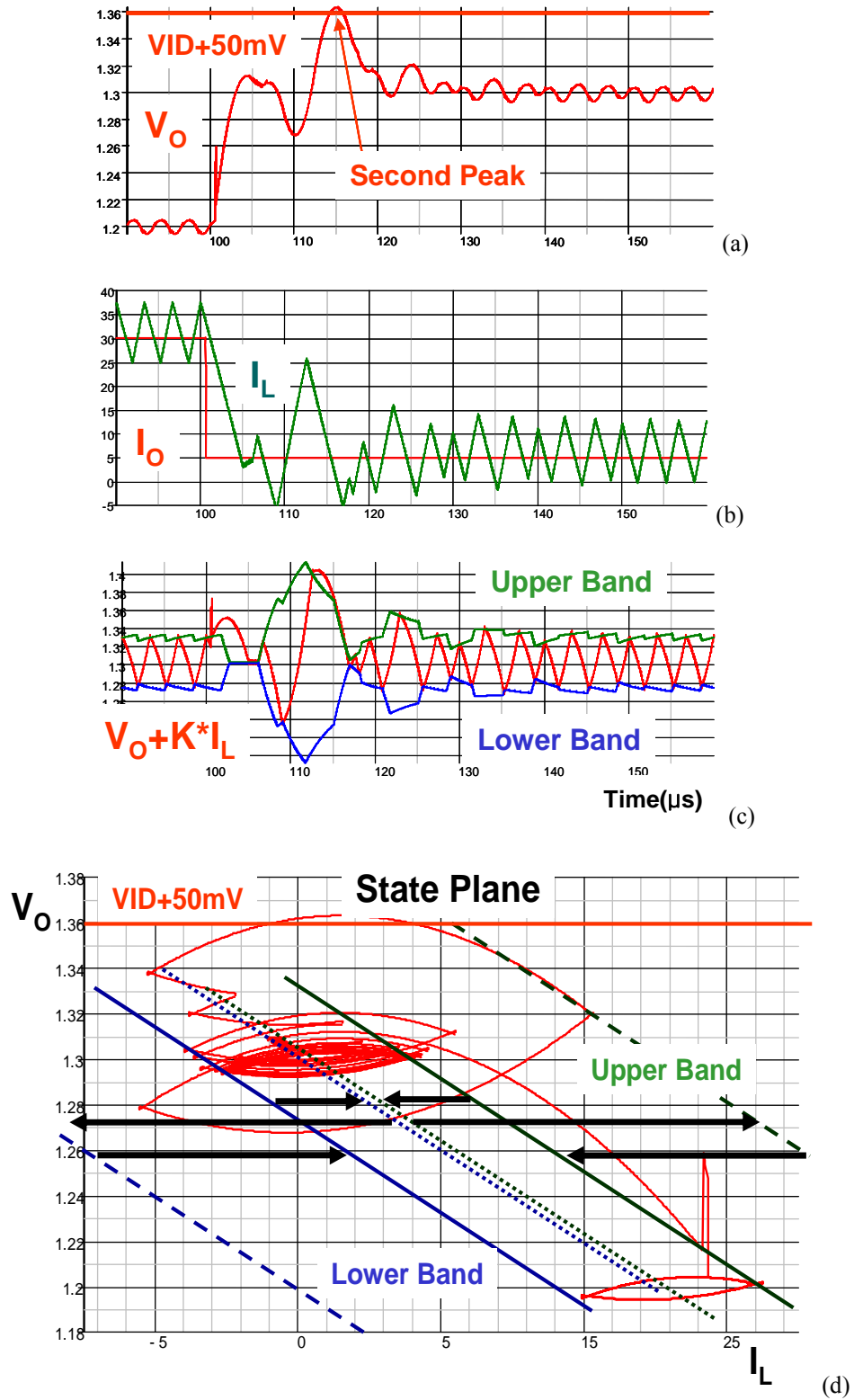


Figure 3.29 The load step-down SIMPLIS simulation results of the proposed hysteretic control with improper  $T_{BAND}$  design (a) The output voltage ( $V_o$ ) (b) The load current ( $I_o$ ) and the inductor current ( $I_L$ ) (c) The feedback signal and the hysteretic band (d) The phase portrait.

### 3.3.2. Linearized Sampled Data Model for the Hysteretic Band Changing Loop

After the first big state trajectory, the state is regulated by the hysteretic band width changing loop and, as observed in Figure 3.27, with the proper design of  $T_{BAND}$  there is no large signal behavior after the first big state trajectory because the large transient is already passed, and the inductor current and the output voltage are already near the operating point B. Therefore, the small-signal assumption can be used to model  $T_{BAND}$ . Figure 3.30 shows the block diagram of the hysteretic band width changing loop.  $T_{BAND}$  consists of two parts. One is a low pass filter to make the  $V_{HYST}$  signal continuous. The schematics of this low-pass filter are shown in Figure 3.15, and the transfer function can be written as,

$$F_{LPF}(s) = \frac{\hat{v}_{HYST}}{\hat{v}_{PFD}} = \frac{s/\omega_z + 1}{(s/\omega_{p1} + 1) \cdot (s/\omega_{p2} + 1)} \quad (3.22)$$

where  $\omega_z = \frac{1}{C1 \cdot R2}$ ,  $\omega_{p1} = \frac{1}{C1 \cdot (R1 + R2)}$ , and  $\omega_{p2} = \frac{1}{C2 \cdot R2}$ , with the assumptions  $R1 \gg R2$ ,  $C1 \gg C2$ .

Due to this low-pass filter, the averaging assumption can also be used too. With the small-signal assumption and the averaging assumption, the system can be linearized. The other part can be modeled as the transfer function,  $F_{COMP}(s)$ , from  $V_{HYST}$  to  $V_{PFD}$ .

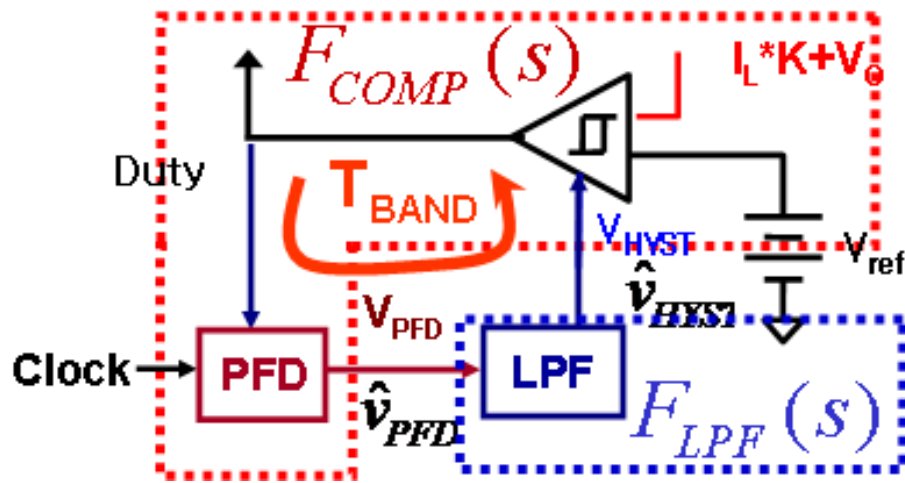


Figure 3.30 The block diagram of the hysteretic band width changing loop.

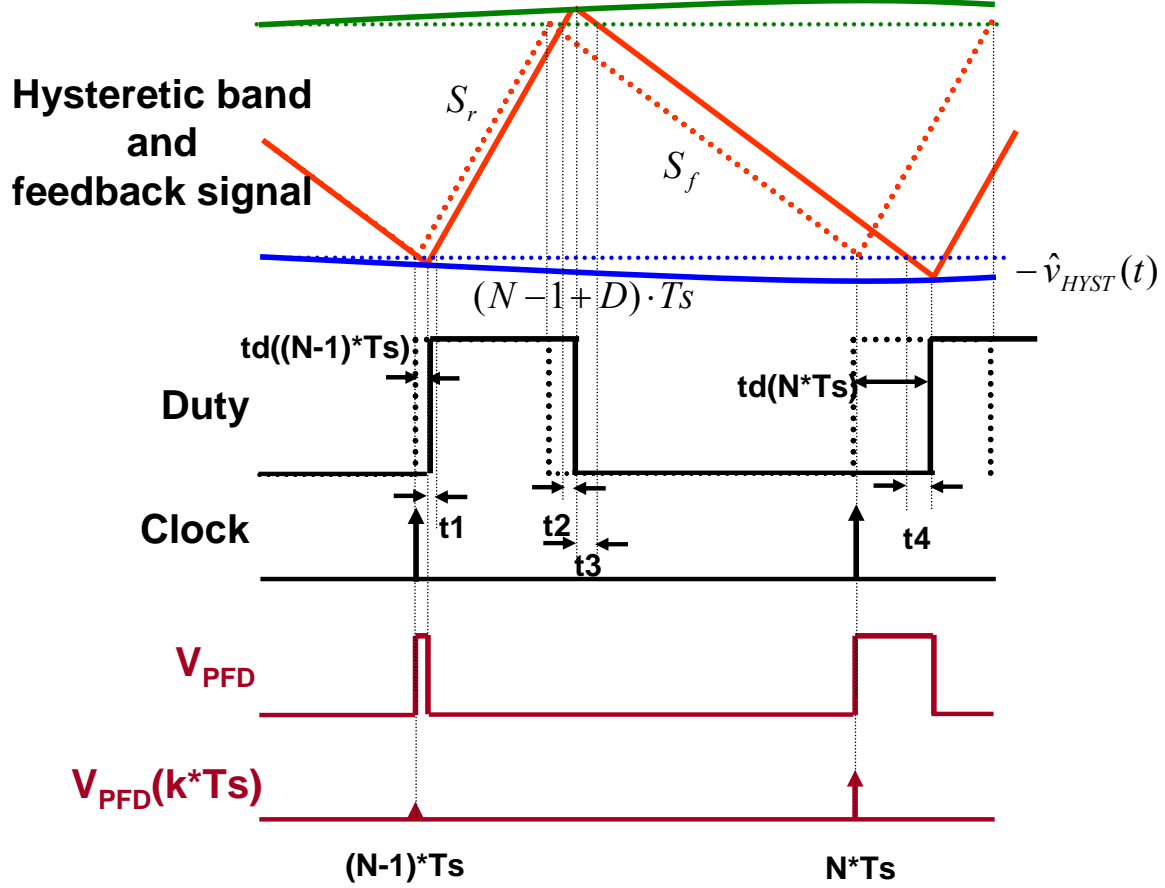

 Figure 3.31 The linearized model derivation for  $F_{COMP}(s)$ .

Figure 3.31 shows the model derivation procedure using the sampled data modeling method [138]. With a small perturbation, there is the phase error between the duty and the reference clock, and the PFD output is like  $V_{PFD}$  in Figure 3.31. Using the small-signal assumption, the  $V_{PFD}$  is treated as a sampled signal at the clock instance, and the magnitude of this sampled signal is the average value of  $V_{PFD}$ . In order to derive this sampled signal,  $V_{PFD}(k \cdot Ts)$ , the time differences  $t1$ ,  $t2$ ,  $t3$ , and  $t4$  in Figure 3.31 are derived.  $t1$  can be derived from the rising slope of the feedback signal,  $S_r$ , and the  $V_{HYST}$  perturbation at the time  $(N-1) \cdot Ts$ ,  $\hat{v}_{HYST}((N-1) \cdot Ts)$ ,

$$t1 = \frac{\hat{v}_{HYST}((N-1) \cdot Ts)}{S_r}. \quad (3.23)$$

Similar to this,  $t2$ ,  $t3$  can be derived from the rising and falling slope of the feedback signal and the  $V_{HYST}$  perturbation at the time  $(N-1+D) \cdot Ts$ ,  $\hat{v}_{HYST}((N-1+D) \cdot Ts)$ ,

$$t2 = \frac{\hat{v}_{HYST}((N-1+D) \cdot Ts)}{S_f}, \quad t3 = \frac{\hat{v}_{HYST}((N-1+D) \cdot Ts)}{S_r}. \quad (3.24)$$

$t4$  can be derived from the falling slope of the feedback signal, and the  $V_{HYST}$  perturbation at the time  $N \cdot Ts$ ,  $\hat{v}_{HYST}(N \cdot Ts)$ ,

$$t4 = \frac{\hat{v}_{HYST}(N \cdot Ts)}{S_f}. \quad (3.25)$$

Therefore the difference equation for the time error,  $t_d$ , is derived as

$$t_d(N \cdot Ts) = t_d((N-1) \cdot Ts) - \frac{\hat{v}_{HYST}((N-1) \cdot Ts)}{S_r} - \left( \frac{1}{S_r} + \frac{1}{S_f} \right) \cdot \hat{v}_{HYST}((N-1+D) \cdot Ts) - \frac{\hat{v}_{HYST}(N \cdot Ts)}{S_f}. \quad (3.26)$$

Then, the difference equation for  $\hat{v}_{PFD}$  is derived as

$$\hat{v}_{PFD}(N \cdot Ts) = \hat{v}_{PFD}((N-1) \cdot Ts) - \left( \frac{\hat{v}_{HYST}((N-1) \cdot Ts)}{S_r} + \left( \frac{1}{S_r} + \frac{1}{S_f} \right) \cdot \hat{v}_{HYST}((N-1+D) \cdot Ts) + \frac{\hat{v}_{HYST}(N \cdot Ts)}{S_f} \right) \cdot \frac{V_{OH} - V_{OL}}{2}. \quad (3.27)$$

Then using the sampled data modeling technique, the frequency domain model is derived from Equation (3.27) as,

$$\frac{\hat{v}_{PFD}(s)}{\hat{v}_{HYST}(s)} = F_{COMP}(s) = \frac{[1 - D + D \cdot e^{-s \cdot Ts} + e^{-s(1-D) \cdot Ts}] \cdot L \cdot (V_{OH} - V_{OL})}{2 \cdot s \cdot (R_C + K) \cdot (D - D^2) \cdot V_{IN} \cdot Ts^2}. \quad (3.28)$$

$F_{COMP}(s)$  looks like an integrator with some delays near the switching frequency, like in Figure 3.32. This is because the phase is the integration of the switching frequency [111]. In order to get continuous  $V_{HYST}$ , the low-pass filter should have an integrator inside it. Therefore the hysteretic band width changing loop has two integrators inside it, which makes the system unstable. Then the compensator is necessary. This is why a one-zero and two-pole low-pass filter is used like Figure 3.15 and Equation (3.22). Using these values for the zero and poles,  $T_{BAND}$  is compensated and designed to be stable.

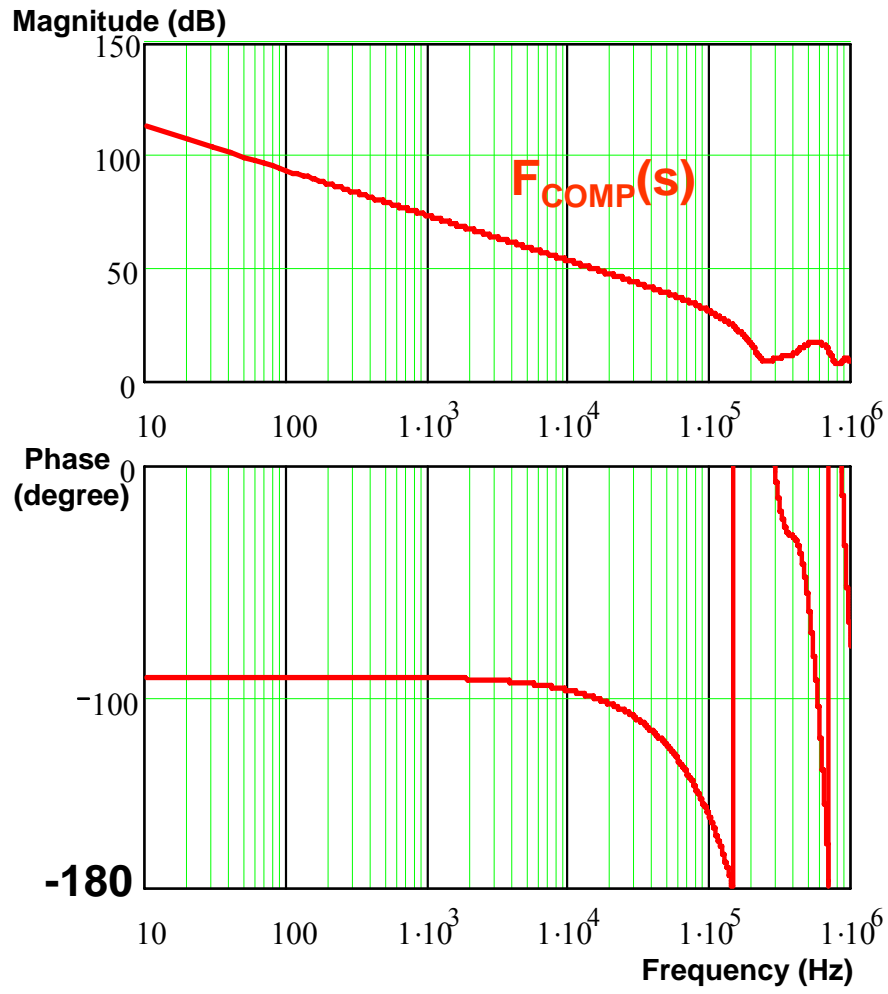


Figure 3.32 The bode plot of the transfer function,  $F_{COMP}(s)$ .

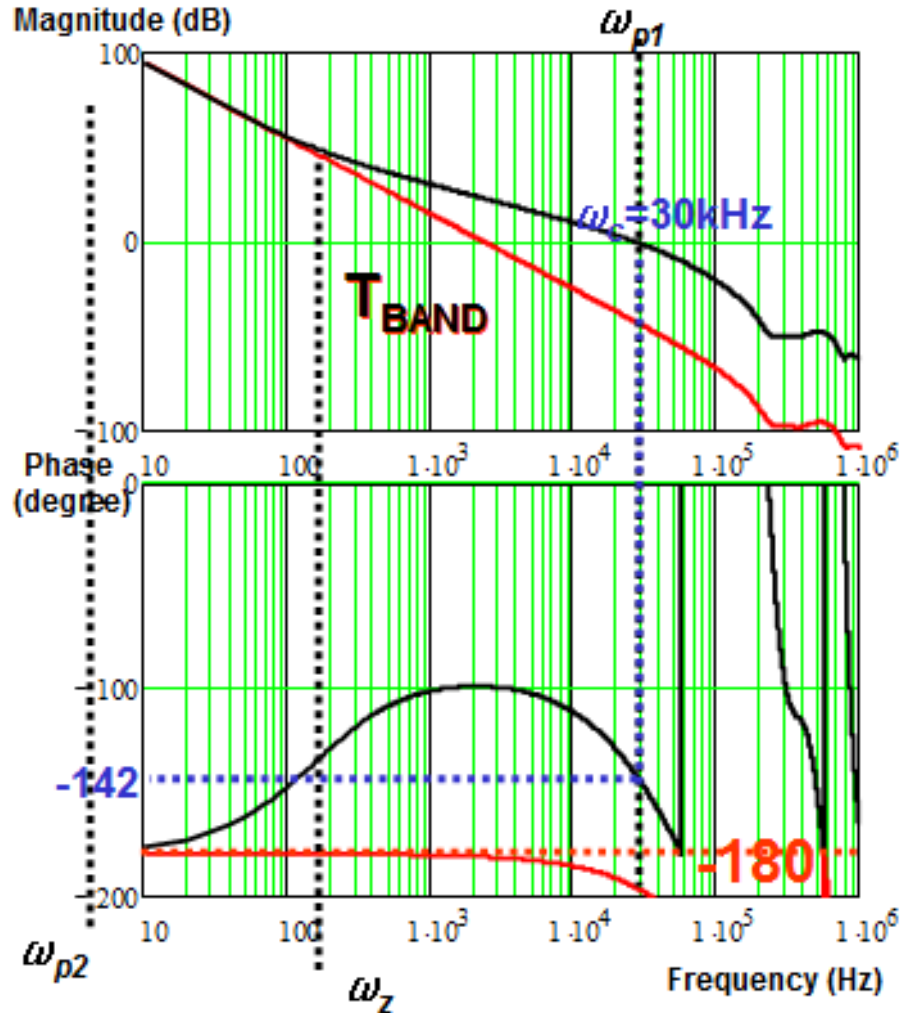


Figure 3.33 The bode plot of the hysteretic band width changing loop (Red lines; without compensation, Black lines; with compensation).

Figure 3.33 shows the bode plot of the hysteretic band width changing loop. Without the proper design of the low-pass filter, like the red line in Figure 3.33, the loop is unstable. Therefore, one zero should be below one-tenth of the bandwidth to boost the phase margin, and one pole should be before the switching frequency to reduce the switching ripples at  $V_{HYST}$ . With this design, the improperly designed system in Figure 3.29 becomes the system in Figure 3.27.



### 3.4. The Proposed Hysteretic Control Method with the Repetitive Load

When the CPU is in active mode, the software can create  $I_O$  transients with all possible amplitudes and reoccurrence frequencies up to several MHz. From the VR specifications, AVP should be achieved within 100kHz load frequency. Therefore, the dynamics of VR with the repetitive load should be examined.

Figure 3.34 shows the SIMPLIS simulation results when the load repetitive frequency is 10kHz. The single-phase VR with the proposed hysteretic control method is simulated with 300nH inductance and 300kHz switching frequency. The system is properly designed and AVP is achieved. The switching frequency is constant as 300kHz. Figure 3.35 shows the SIMPLIS simulation results when the load repetitive frequency is 70kHz with the same VR, and it can be observed that AVP is achieved. However, the peak voltage can be larger than the specification and the switching frequency is not constant, which indicates the hysteretic band width changing loop is not working properly. This problem should be resolved. Figure 3.36 shows the SIMPLIS simulation results when the load repetitive frequency is 500kHz. AVP is not achieved because the load repetitive frequency is too high and it is filtered by the output capacitors. In this case, the output voltage follows the load line with the average value of the load current. The switching frequency is constant as 300kHz. Figure 3.37 shows the SIMPLIS simulation results when the load repetitive frequency is 5MHz. Just as the 500kHz case, the output voltage follows the load line with the average value of the load current and the switching frequency is constant as 300kHz.

Therefore it is observed that when the load repetitive frequency is lower than several tens of kHz, the system is working well and when the load repetitive frequency is higher than several hundreds of kHz, the system is also working well. There is an overshoot problem when the load repetitive frequency is between several tens of kHz and several hundreds of kHz.

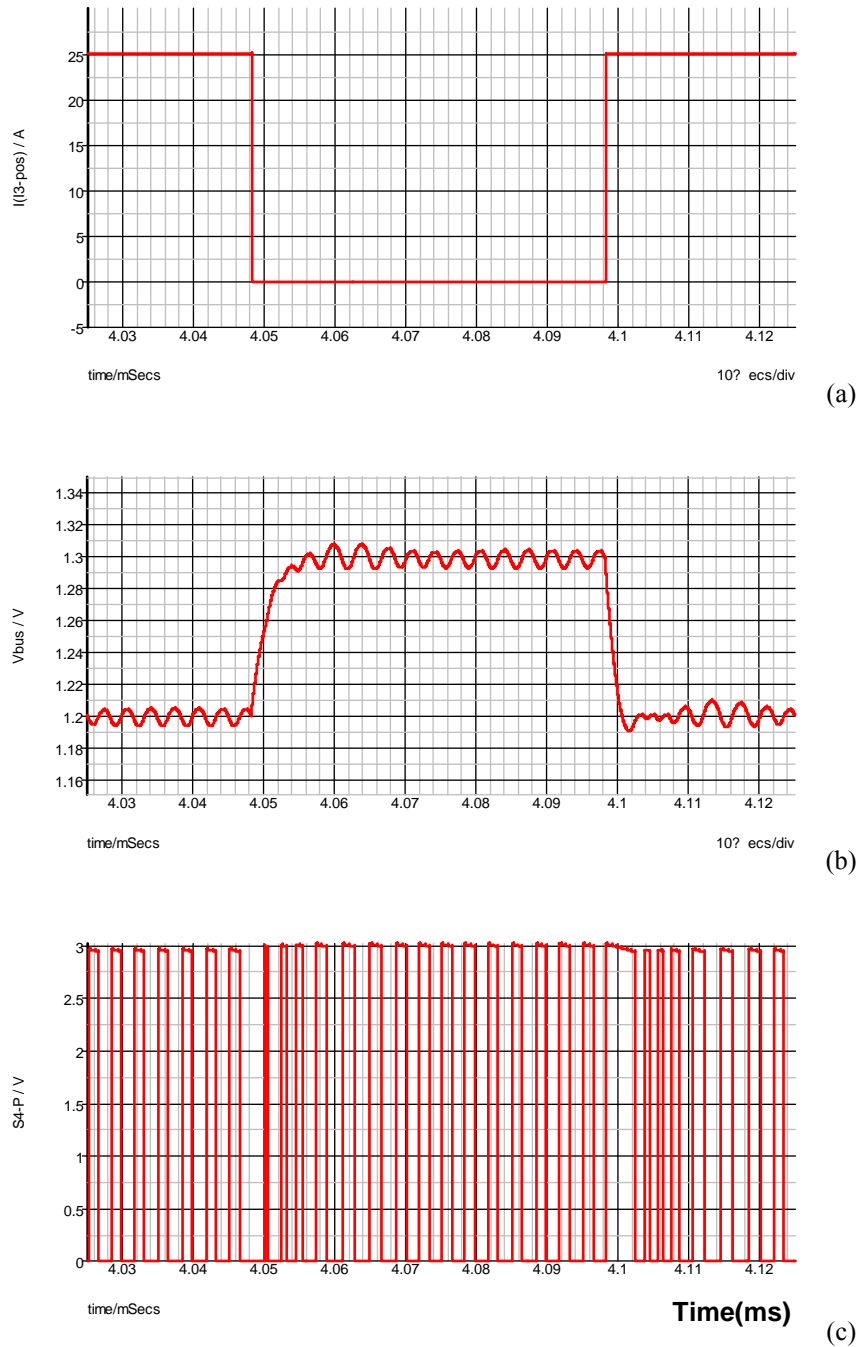
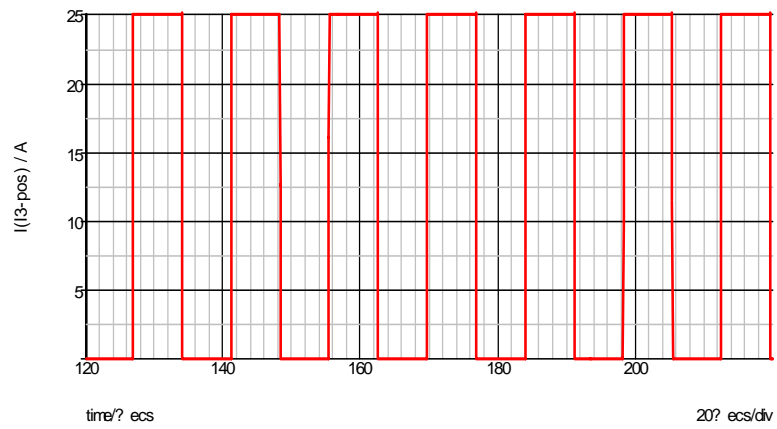
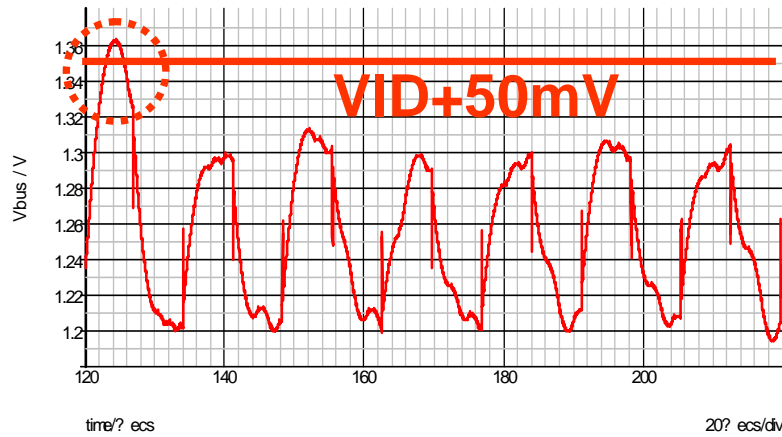


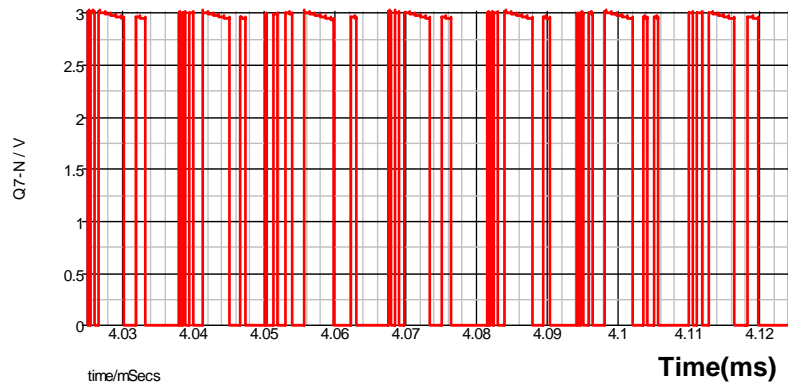
Figure 3.34 SIMPLIS simulation results of the proposed hysteresis control with 10kHz repetitive load (a) The load current (b) The output voltage (c) The duty cycles.



(a)

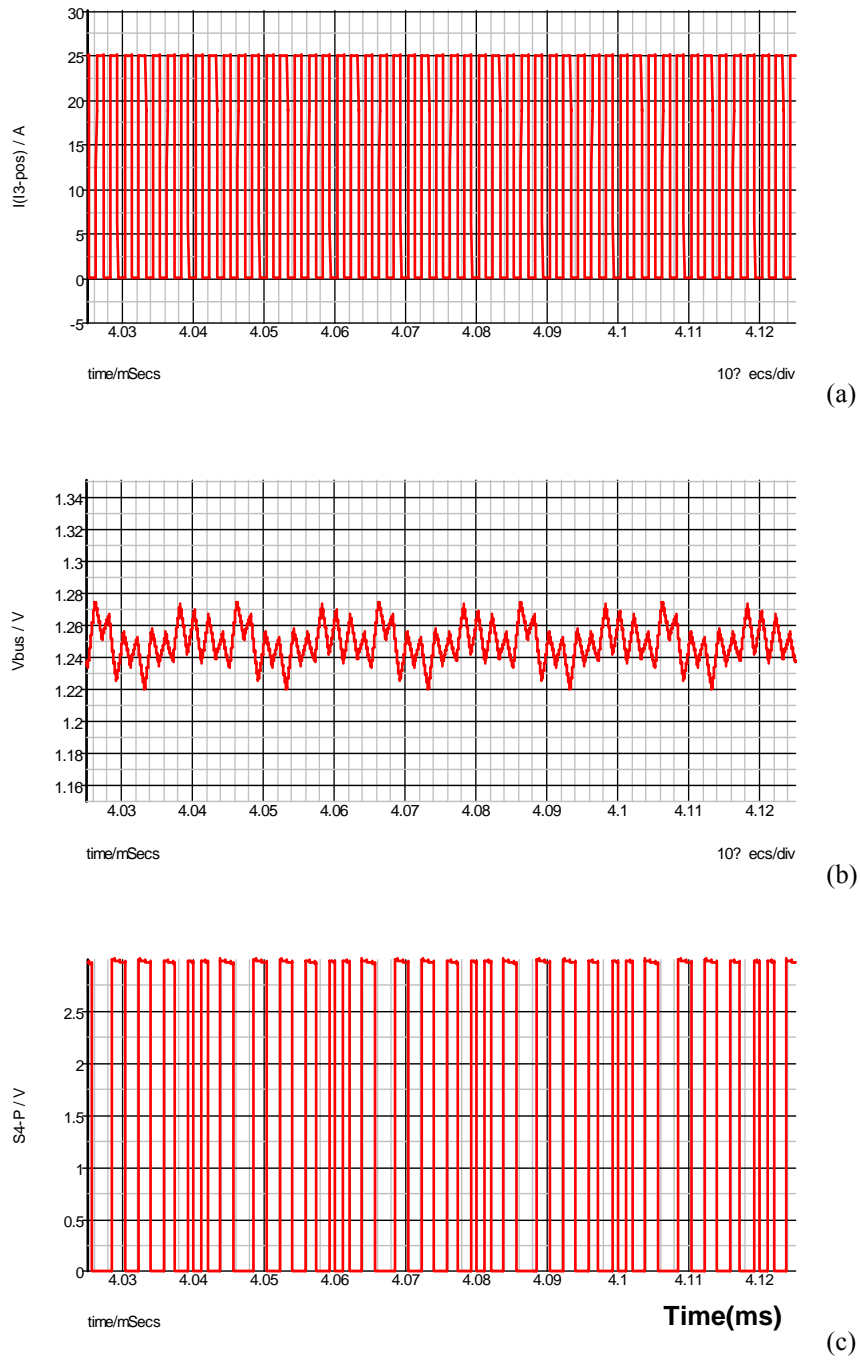


(b)

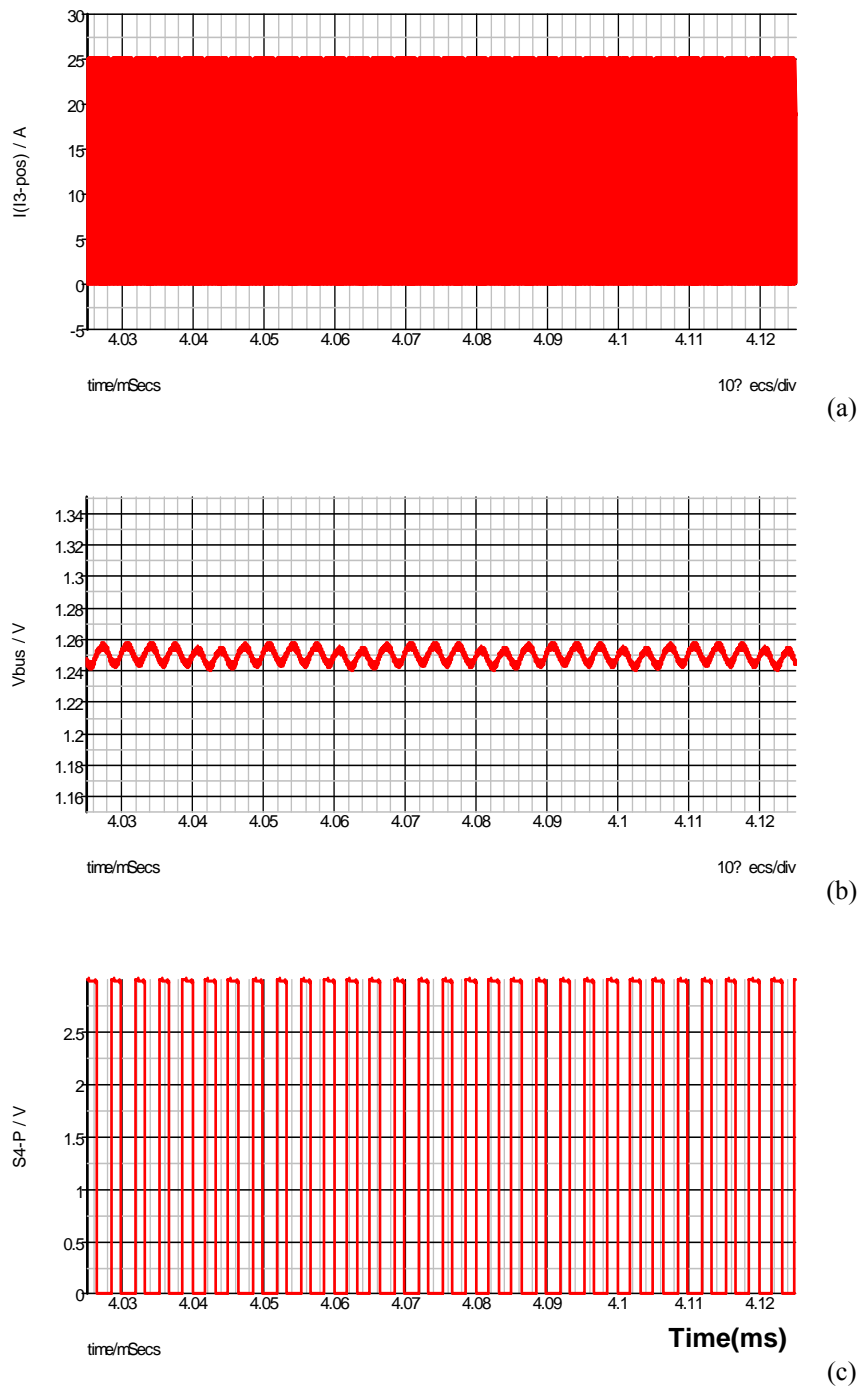


(c)

Figure 3.35 SIMPLIS simulation results of the proposed hysteretic control with 70kHz repetitive load (a) The load current (b) The output voltage (c) The duty cycles.



**Figure 3.36 SIMPLIS simulation results of the proposed hysteresis control with 500kHz repetitive load (a) The load current (b) The output voltage (c) The duty cycles.**



**Figure 3.37 SIMPLIS simulation results of the proposed hysteretic control with 5MHz repetitive load (a) The load current (b) The output voltage (c) The duty cycles.**

Figure 3.38 shows the reason for the output voltage overshoot problem. When the load transient occurs, the synchronization between the duty cycles and the reference clock is lost and the hysteretic band width changing loop starts to enlarge the hysteretic band width to synchronize them. During this action, the load transient can occur again. Then, the control wants to regulate the output with this larger hysteretic band width, and the larger output voltage peak is made. Therefore, to reduce this output voltage overshoot, the hysteretic band width should be limited. The relationship of the output voltage peak and the hysteretic band width is calculated from Equations (3.13) and (3.21) with the maximum load transition from  $I_{O2}$  to  $I_{O1}$  as

$$V_{O0} = R_C \cdot (I_{L0} - I_{O1}) + VID - K \cdot I_{O1} + R_C \cdot (I_{O1} - I_{O2}), \quad (3.29)$$

$$V_{BAND\_MAX} = 2 \cdot (I_{L0} \cdot K + V_{O0} - R_C \cdot (I_{O1} - I_{O2}) - VID), \text{ and} \quad (3.30)$$

$$VID + 50mV = -R_C \cdot (I_{L0} - I_{O2}) + \sqrt{V_{O0}^2 + \frac{L}{C} \cdot (I_{L0} - I_{O2})^2}. \quad (3.31)$$

The hysteretic band width should be smaller than the solution for  $V_{BAND\_MAX}$  from the above equations. In order to guarantee this, the hysteretic band width limiter is used like Figure 3.39. With this limiter, the output voltage is within the specification, as in Figure 3.40.

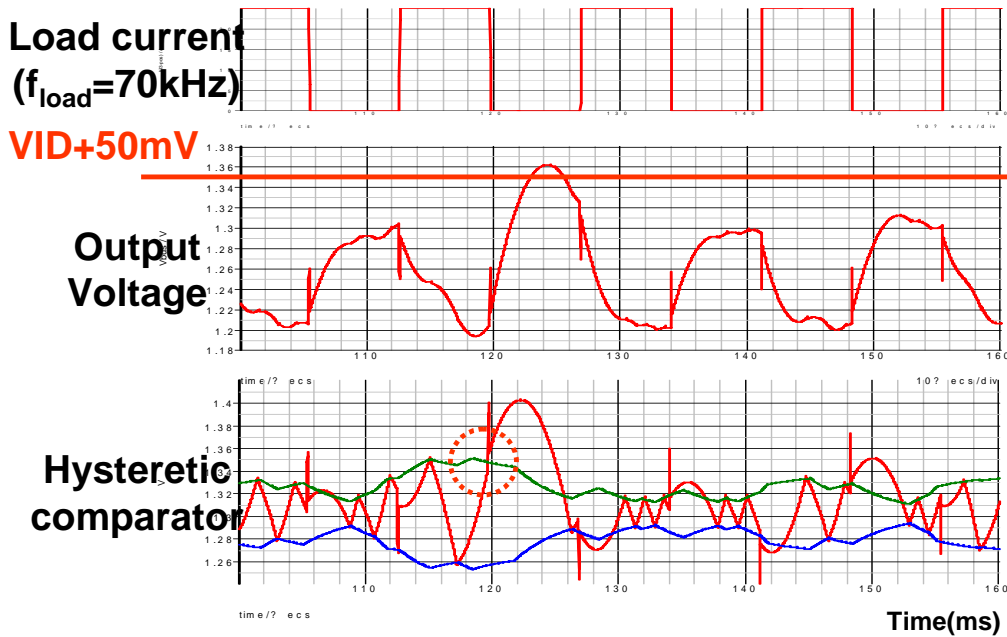


Figure 3.38 The reason of the larger output voltage peak; SIMPLIS simulation results of the proposed hysteretic control (70kHz repetitive load).

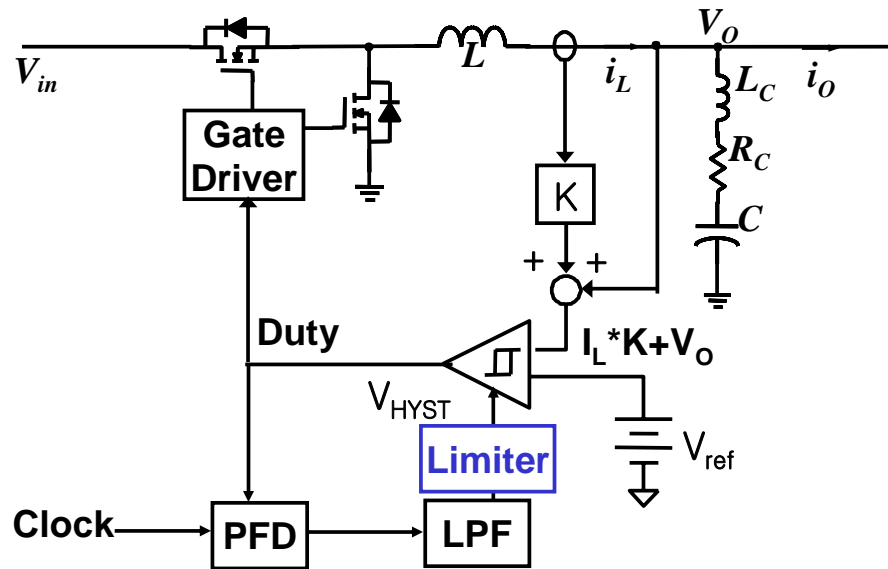


Figure 3.39 The proposed hysteretic control method with the hysteretic band width limiter.

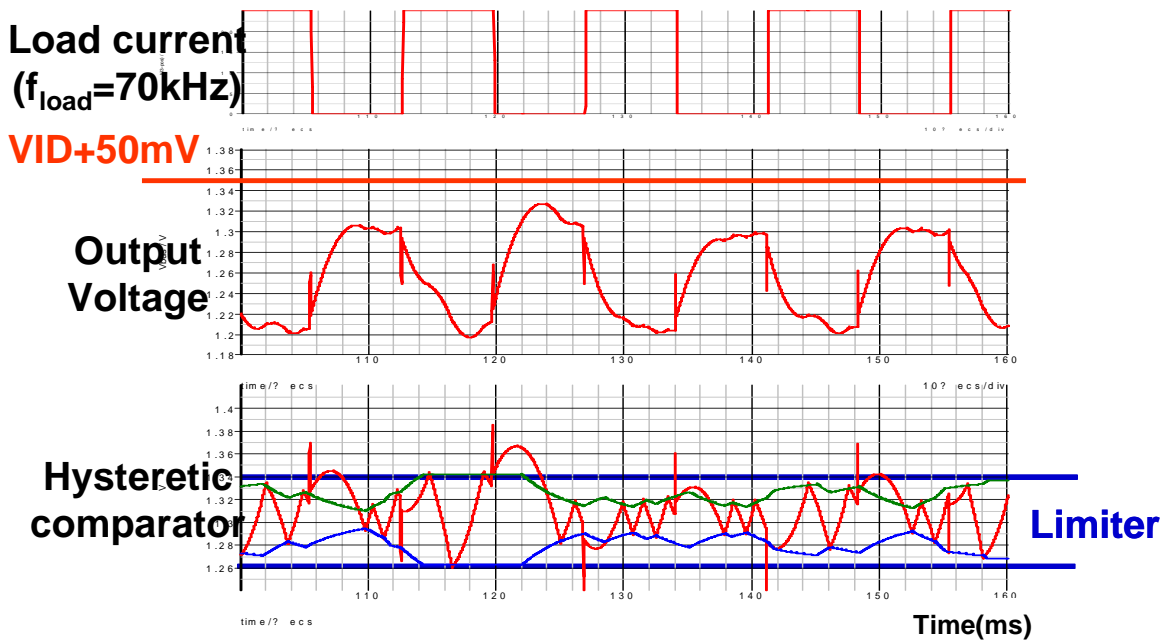


Figure 3.40 SIMPLIS simulation results of the proposed hysteretic control with the hysteretic band width limiter (70kHz repetitive load).

### 3.5. Hardware Verification

#### 3.5.1. Proposed Hysteretic Control Method for 12V Input Voltage VR

Figure 3.41 shows the experimental waveforms of a two-phase VR with the proposed hysteretic control method.

- Two-phase VR
- $V_{IN} = 12V$ ,  $V_{ID} = 1.3V$
- $I_O = 0 \sim 27A$ ,  $di/dt = 200A/\mu s$ ,  $R_{LL} = 2m\Omega$
- $L = 300nH$  for each phase
- $F_s = 300kHz$
- Bulk Capacitors :  $4 \times 100\mu F$  (MLCCs)
- Cavity Capacitors :  $10\mu F \times 24$ ,  $22\mu F \times 10$
- Hysteretic controller : TPS5210
- PLL controller : TLC2932
- Clock generator : LM2639
- Additional OPAMPs are used for DCR sensing.

AVP is well achieved. With the load current of 27A changing, the output voltage changes 54mV, which verifies the load impedance  $R_{LL}$  is 2m $\Omega$ . The interleaving is achieved at the steady state. It is found that when the transient occurs, the interleaving function is lost for several switching periods. After that, the interleaving function is again achieved. The output voltage ripples are enlarged during the transient, but settle down at the steady state.

For the load step-down transient, the output voltage peak is only 30mV with  $4 \times 100\mu F$  (MLCCs) bulk capacitors. Additionally, the total output capacitance is 860 $\mu F$ , whereas the VR with the conventional linear control method with this bandwidth is at least 50kHz for 300kHz switching frequency needs 1600 $\mu F$ . With the proposed hysteretic control method, almost half the output capacitors can be removed.



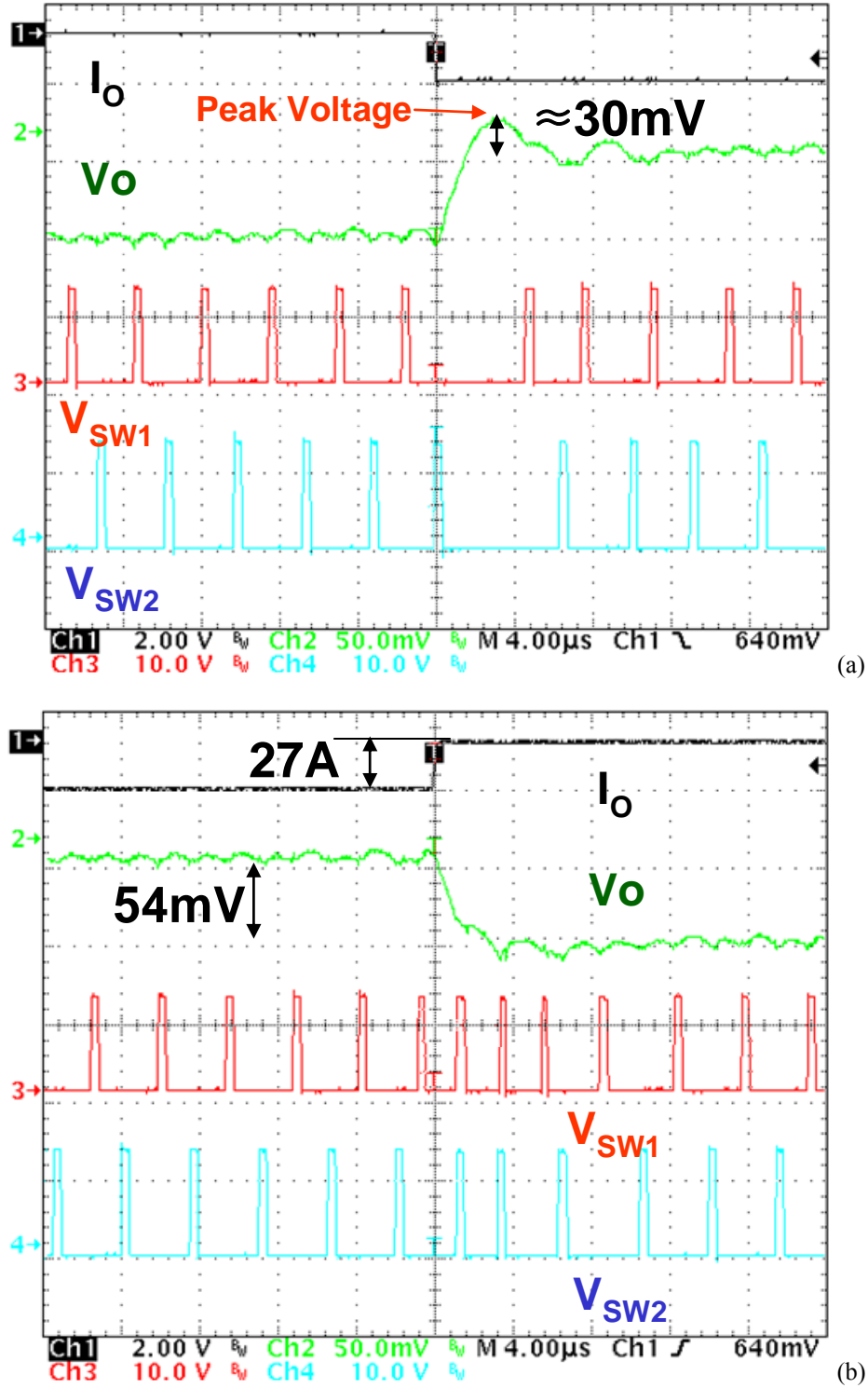


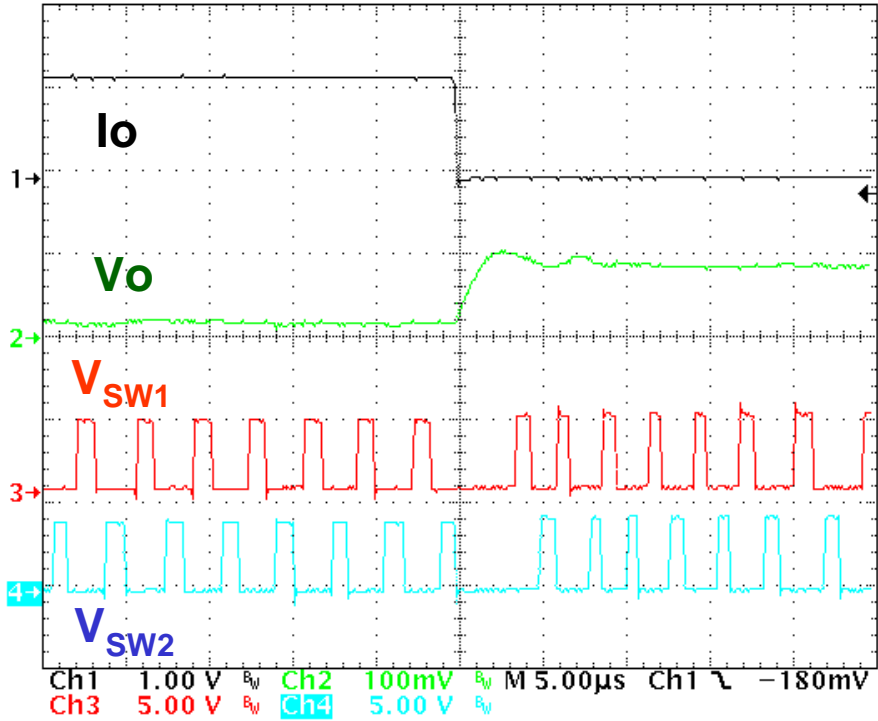
Figure 3.41 The experimental results of two-phase VR with the proposed hysteretic control (a) The load step-down transient (b) The load step-up transient.

### 3.5.2. Proposed Hysteretic Control Method for the Second Stage VR

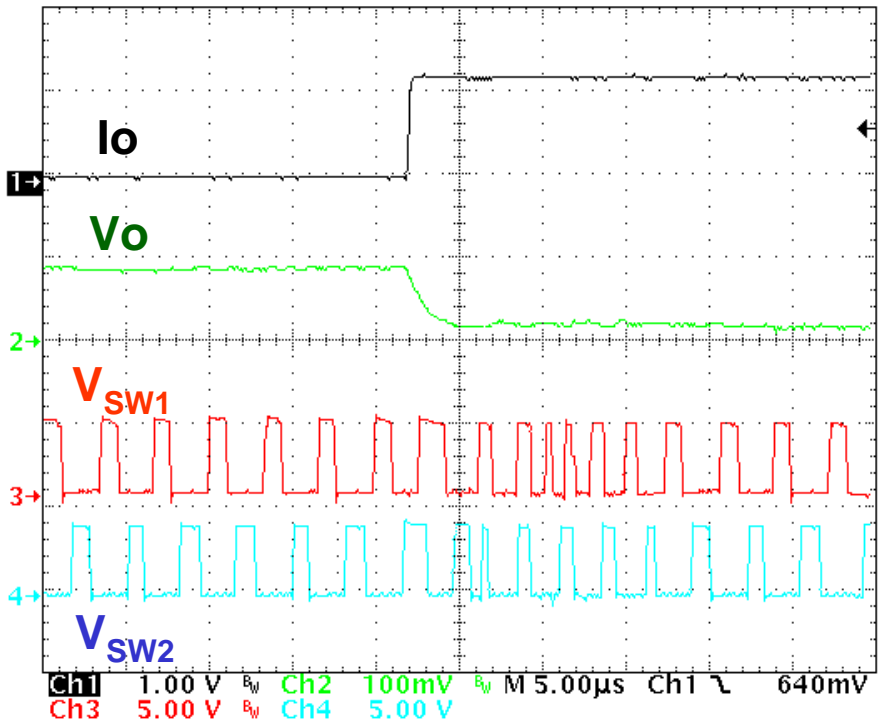
Figure 3.42 shows the experimental waveforms of the two-phase VR with the proposed hysteretic control method used for the second stage of the two-stage VR. As mentioned in Section 3.2, the conventional interleaving method for the multiphase hysteretic control method cannot be used for the low-input-voltage VR. This experiment verifies that the proposed hysteretic control method is good for the low-input-voltage VR, which can be used as the second stage of the two-stage VR.

- Two-phase VR
- $V_{IN} = 4V$ ,  $V_{ID} = 1.3V$
- $I_O = 0 \sim 24A$ ,  $R_{LL} = 2.5m\Omega$
- $L = 300nH$  for each phase
- $F_s = 300kHz$
- Bulk Capacitors :  $2 \times 100\mu F$  (MLCCs)
- Cavity Capacitors :  $10\mu F \times 24$ ,  $22\mu F \times 10$
- Hysteretic controller : TPS5210
- PLL controller : TLC2932
- Clock generator : LM2639

Similar to the previous case, the AVP and the interleaving is well achieved at the steady state. During the transient, the interleaving function is lost and the transient response is very fast. Figure 3.43 shows the zoomed waveforms for the load step-up transient. When the load step-up occurs, the output voltage decreases and the duty cycles are enlarged. With the overlapping duty cycles, the load step-up transient is also good.



(a)



(b)

Figure 3.42 The experimental results of the second stage VR with the proposed hysteretic control-  
 (a) The load step-down transient (b) The load step-up transient.

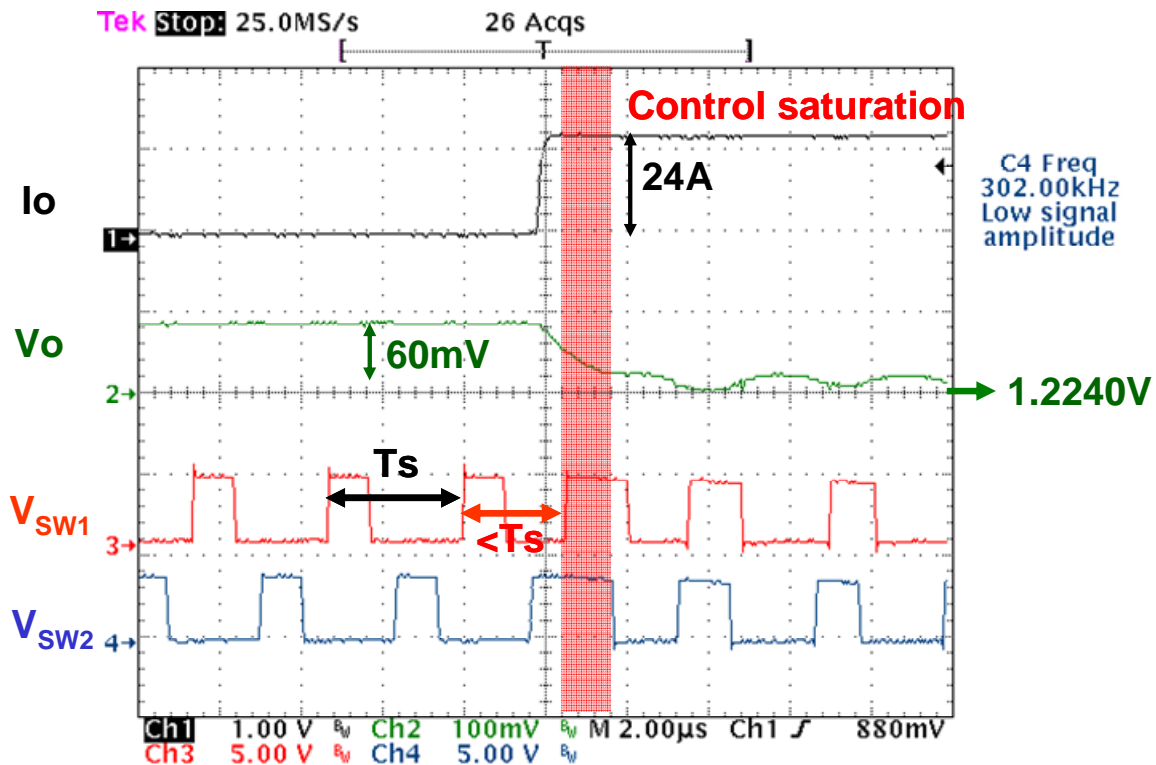


Figure 3.43 The experimental results for the load step-up transient (zoomed).

### 3.6. Summary

This chapter proposes the hysteretic control method for the multiphase VR. This method can increase control speed without increasing the switching frequency. By increasing the control speed with the proposed control method, the output capacitors can be reduced by almost half. Models to analyze and design this control method are suggested and two prototypes are built to verify the analysis and design of the proposed hysteretic control method.

## Chapter 4. Performance Enhancements of the Proposed Hysteretic Control Method with Coupled Inductor

### 4.1. Performance Enhancements of the Proposed Hysteretic Control Method and the Challenge

In the previous chapter, a multiphase hysteretic control method is proposed, with which the speed of the VR is higher without increasing the switching frequency. The control speed is fast enough to saturate the controller during the transient and the transient response, particularly the output voltage peak, is determined by the power stage parameters. Recalling the peak output voltage equation (3.21) and the modification of the initial state from  $\beta$  ( $I_{L0}$ ,  $V_{O0}$ ) to  $\alpha$  ( $I_{La}$ ,  $V_{Oa}$ ) in Figure 3.27, the peak output voltage equation becomes,

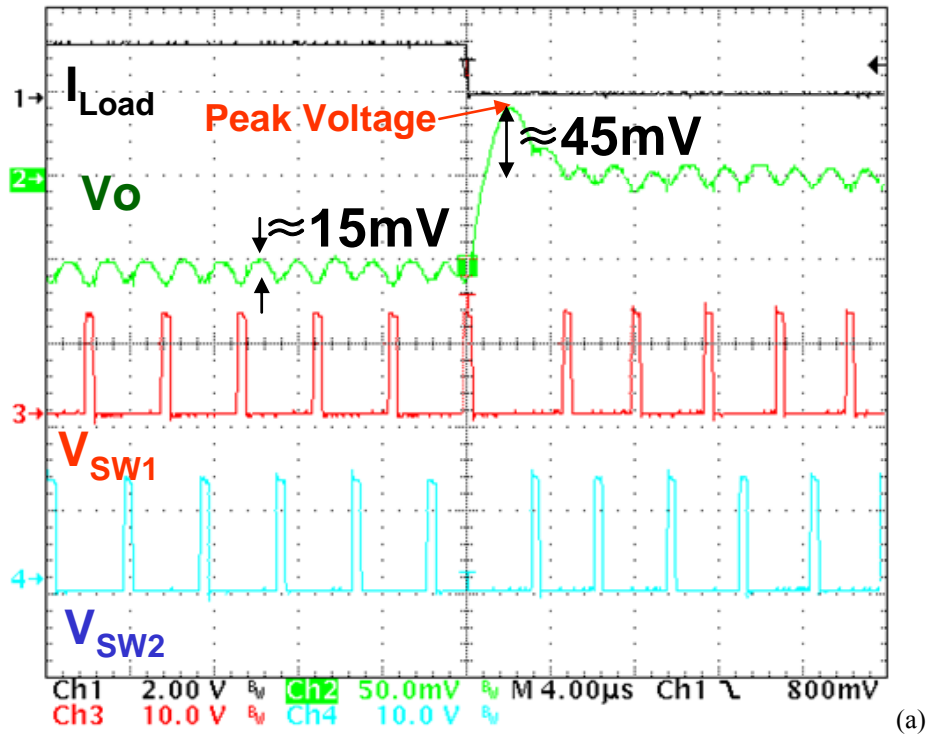
$$V_{O\_peak} = -R_C \cdot (I_{La} - I_O) + \sqrt{(V_{Oa} + R_C \cdot \Delta I_O)^2 + \frac{L}{C} \cdot (I_{La} - I_O)^2} \quad (4.1)$$

The point  $\alpha$  ( $I_{La}$ ,  $V_{Oa}$ ) is determined not by the output capacitor parameters, but by the steady-state parameters of the switching frequency, the steady-state hysteretic band width and the steady-state operating point A. Then using Equation (4.1), the relationship between the output capacitors and the peak output voltage is found. It is observed that by decreasing the inductance, the output capacitors can be reduced with the given peak output voltage. In order to verify this, taking the example in Section 3.5.1, the hardware is built reducing the inductance from 300nH to 150nH. Then the bulk output capacitors are reduced by half, from  $4 \times 100\mu\text{F}$  to  $2 \times 100\mu\text{F}$ . The total output capacitance is reduced from 860 $\mu\text{F}$  to 660 $\mu\text{F}$ .

- Two-phase VR
- $V_{IN} = 12\text{V}$ ,  $V_{ID} = 1.3\text{V}$
- $I_O = 0 \sim 27\text{A}$ ,  $di/dt = 200\text{A}/\mu\text{s}$ ,  $R_{LL} = 2\text{m}\Omega$
- **$L = 150\text{nH}$  for each phase**

- $F_s = 300\text{kHz}$
- Bulk Capacitors :  $2 \times 100\mu\text{F}$  (MLCCs)
- Cavity Capacitors :  $10\mu\text{F} \times 24, 22\mu\text{F} \times 10$
- Hysteretic controller : TPS5210
- PLL controller : TLC2932
- Clock generator : LM2639
- Additional OPAMPs are used for DCR sensing.

Figure 4.1 shows the measured waveforms of this two-phase VR hardware. AVP is achieved very easily, and the output voltage peak is within the specification,  $V_{ID} + 50\text{mV}$ . Therefore, it is verified that by decreasing the inductance, the output capacitors can be reduced.



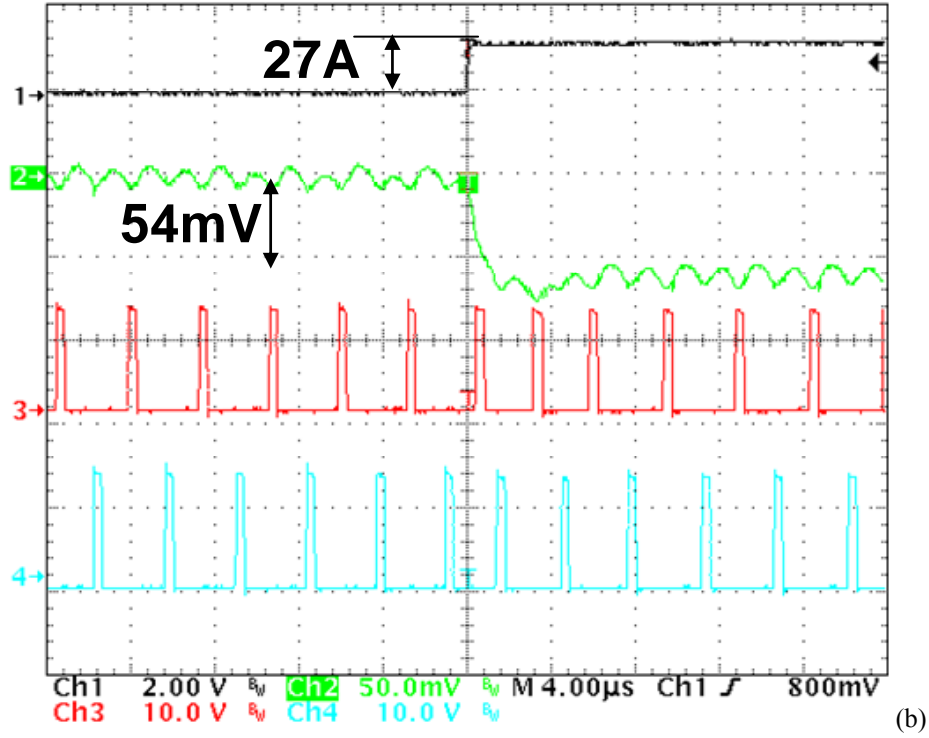


Figure 4.1 The experimental results of two-phase VR with the proposed hysteretic control (a) The load step-down transient (b) The load step-up transient.

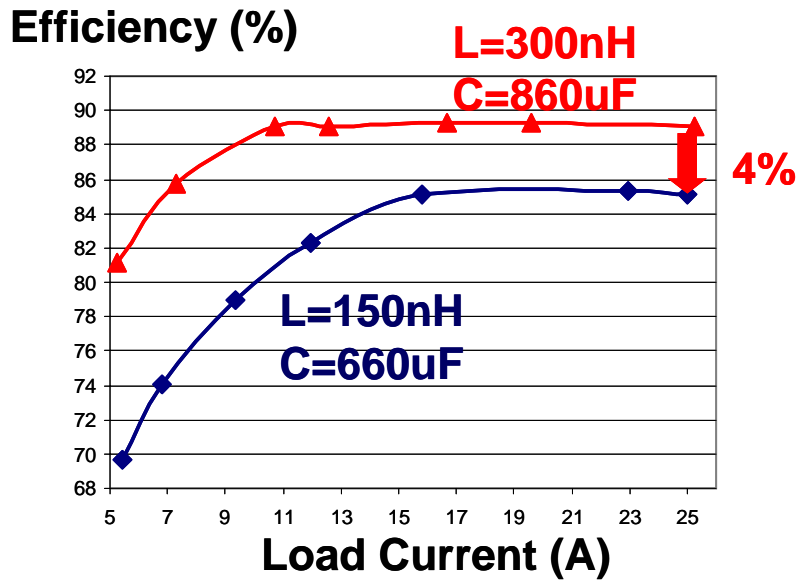


Figure 4.2 The measured efficiencies (Red line: two-phase VR with 300nH, 860µF, Blue line: two-phase VR with 150nH, 660µF).

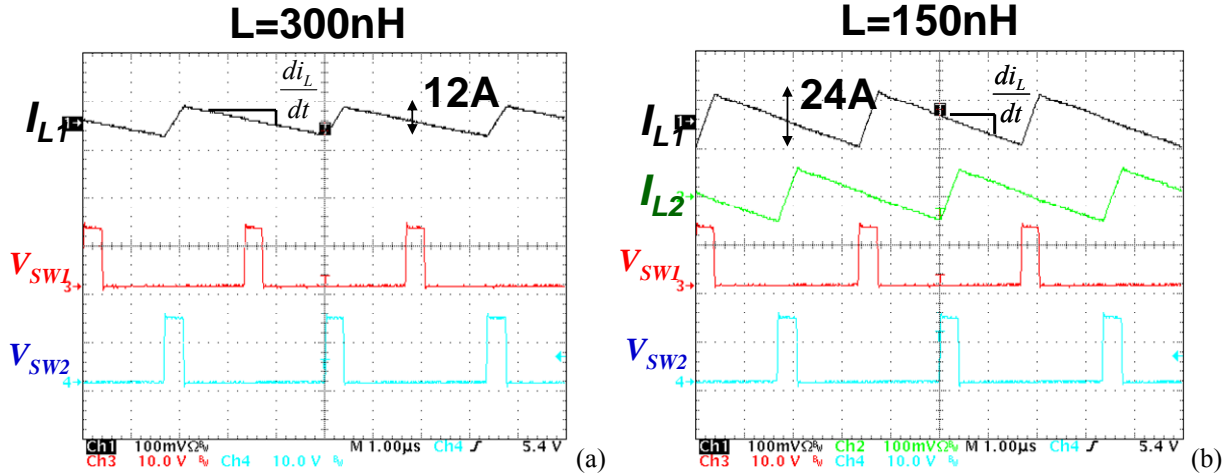


Figure 4.3 The measured current waveforms of two-phase VR (a) with 300nH, 860 $\mu$ F (b) with 150nH, 660 $\mu$ F.

However, the efficiency suffers from the low inductance. Figure 4.2 shows the efficiency measurement data. The efficiency drops about 4% at the full load. For the light load, it is much worse. The reason for this efficiency drop can be found in the inductor current waveforms, which are shown in Figure 4.3. By decreasing the inductance, the inductor current slew rate ( $di_L/dt$ ) increases and the transient response becomes faster while the inductor current ripple increases from 12App to 24App. The larger inductor current ripple results in a larger turn-off loss which dominates the switching loss and the conduction loss also increases because the inductor root mean square (rms) current increases.

Therefore, in order to enhance the transient performance of the proposed hysteretic control method without degrading the efficiency, a nonlinear inductor, which can increase the inductor current slew rate while reducing the inductor current ripple, is necessary. In 2000, CPES proposed the nonlinear coupled inductor, for VR applications [115][116]. Better performance is expected with this coupled inductor.



## 4.2. Overview of the Coupled Inductor in VR Application

The basic principles of the coupled inductor for use with the multiphase VR have been thoroughly studied by Pit-Leong Wong in his dissertation [115]. This section gives a summary of the coupled inductors concept he proposed.

Figure 4.4 shows the core implementation of the coupled inductor proposed in [115]. The coupled inductor is implemented by two sets of windings on one magnetic core. There are three air gaps in the three legs,  $g_1$ ,  $g_2$ , and  $g_c$ . The flux generated by the winding of  $L_1$  goes through all three legs. The flux generated by the winding of  $L_2$  has a similar path. Therefore there is flux interaction between the windings, represented by the dotted line in Figure 4.4, and this indicates the coupling effect between these two inductors.

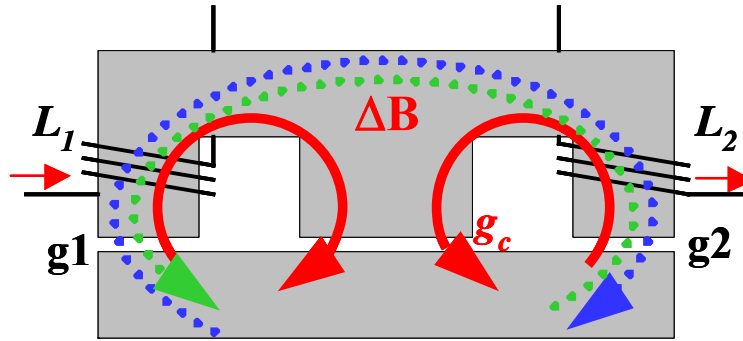


Figure 4.4 The coupled inductor proposed in [115].

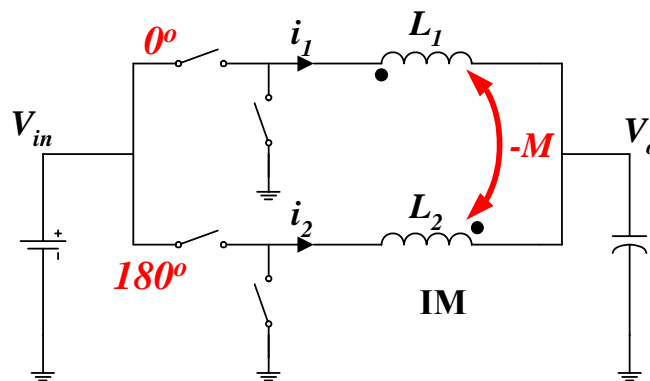


Figure 4.5 2 phase VR with coupled inductor.

Figure 4.5 shows the two-phase VR with the coupled inductor. The direction of the two windings' connection is represented by the dots. The coupled inductor has different equivalent inductances for steady-state and transient responses.

For simplicity, the two self-inductances built on the same core are considered to be the same ( $L_1=L_2=L_s$ ). Then

$$M = \alpha \cdot L_s \quad (4.2)$$

where  $\alpha$  is the coupling coefficient between the two windings ( $0 < \alpha < 1$ ).

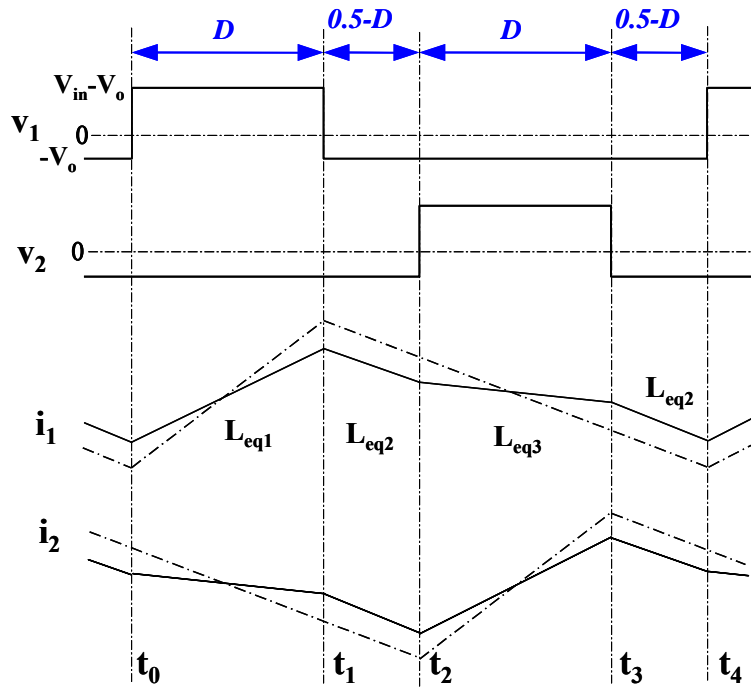


Figure 4.6 The steady-state inductor voltage and current waveforms for the discrete and coupled inductors [115].

Figure 4.6 shows the steady-state inductor voltage and the current waveforms for the discrete and coupled inductors. The inductor voltage waveforms for both cases are the same. For the inductor current waveforms, the solid lines correspond to the coupled inductor case, while the dashed lines correspond to the discrete inductor case. There are four switching intervals during one switching cycle. Due to the different voltages across the coupled inductor in these four intervals, there are four different inductances for each interval. The equivalent inductances for each phase can be derived as follows;

$$L_{eq1} = \frac{L_S^2 - M^2}{L_S - \frac{D}{D'} \cdot M}, \quad (4.3)$$

$$L_{eq2} = L_S - M, \text{ and} \quad (4.4)$$

$$L_{eq3} = \frac{L_S^2 - M^2}{L_S - \frac{D'}{D} \cdot M}. \quad (4.5)$$

During time interval  $(t_3-t_4)$ , the voltages applied to the two inductors are exactly the same as the voltage applied during time interval  $(t_1-t_2)$ . Thus, the equivalent inductance in this time interval is same as  $L_{eq2}$ . There are three different equivalent inductances in a switching cycle.

Based on the equivalent inductances, the effects of the coupling inductors on converter performance both in steady-state operations and during transient responses can be analyzed. The steady-state criterion is the current ripple because it has a direct impact on converter efficiency. The transient criterion is the current slew rate during transient responses.  $L_{eq1}$  determines the steady state ripple, and  $L_{eq2}$  determines the transient responses. Therefore, a nonlinear inductor whose inductances are different for the steady state and the transient state is achieved.

With the same transient equivalent inductance  $L_{eq2}$ , the transient responses are expected to be the same. Based on the same transient equivalent inductance, the relationship between the steady-state inductor current ripples of discrete and coupled inductors can be determined and compared as follows;

$$\frac{I_{pp\_cp}}{I_{pp\_nc}} = \frac{L_{nc}}{L_{eq1}} = \frac{1 - \frac{D}{D'} \cdot \alpha}{1 + \alpha} \quad (4.6)$$

where  $I_{pp\_cp}$  is the steady-state inductor current ripple size of the coupled inductor,  $I_{pp\_nc}$  is the steady state inductor current ripple size of the discrete inductor and  $L_{nc}$  is the inductance of the discrete inductor.

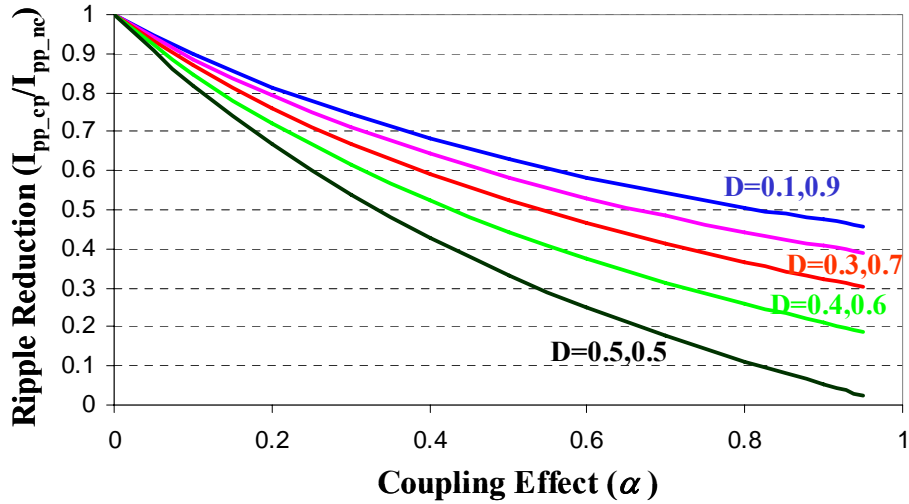


Figure 4.7 Steady-state current ripple reductions in coupled inductors [115].

The current ripple reductions by the coupled inductors are functions of steady-state duty cycle  $D$  and coupling effects  $\alpha$ . The relationship shown in (4.6) is plotted in Figure 4.7. The steady-state duty cycle closer to 0.5 results in more effective current ripple reduction. Stronger coupling effects give smaller current ripples. Therefore, in order to get the same transient response and smaller steady-state inductor current ripples, the coupled inductors should be designed to have  $L_s$  and  $\alpha$  as large as possible while maintaining the same  $L_{eq2}$ .

Figure 4.8 shows the AC flux and the current waveforms of the discrete inductor and the coupled inductor. From 4.8 (a) and (b), it is verified that the phase inductor current ripple is reduced with the coupled inductor while the total inductor current is the same, which means the transient responses are same. For the core structure shown in Figure 4.4, the magnetic analog circuit can be easily derived, as shown in Figure 4.8 (c).  $R_1$ ,  $R_2$  and  $R_C$  in the figure represent the magnetic reluctances of the three legs. The AC fluxes in the two outer legs, ( $\phi_1$  and  $\phi_2$ ), are determined only by the time integral of the voltage (which is more simply stated as volt-seconds) across the corresponding winding. Therefore, for both the discrete and coupled inductor cases, the AC fluxes are same as Figure 4.8 (d). Based on this, Pit-Leong Wong has proposed a current source model.

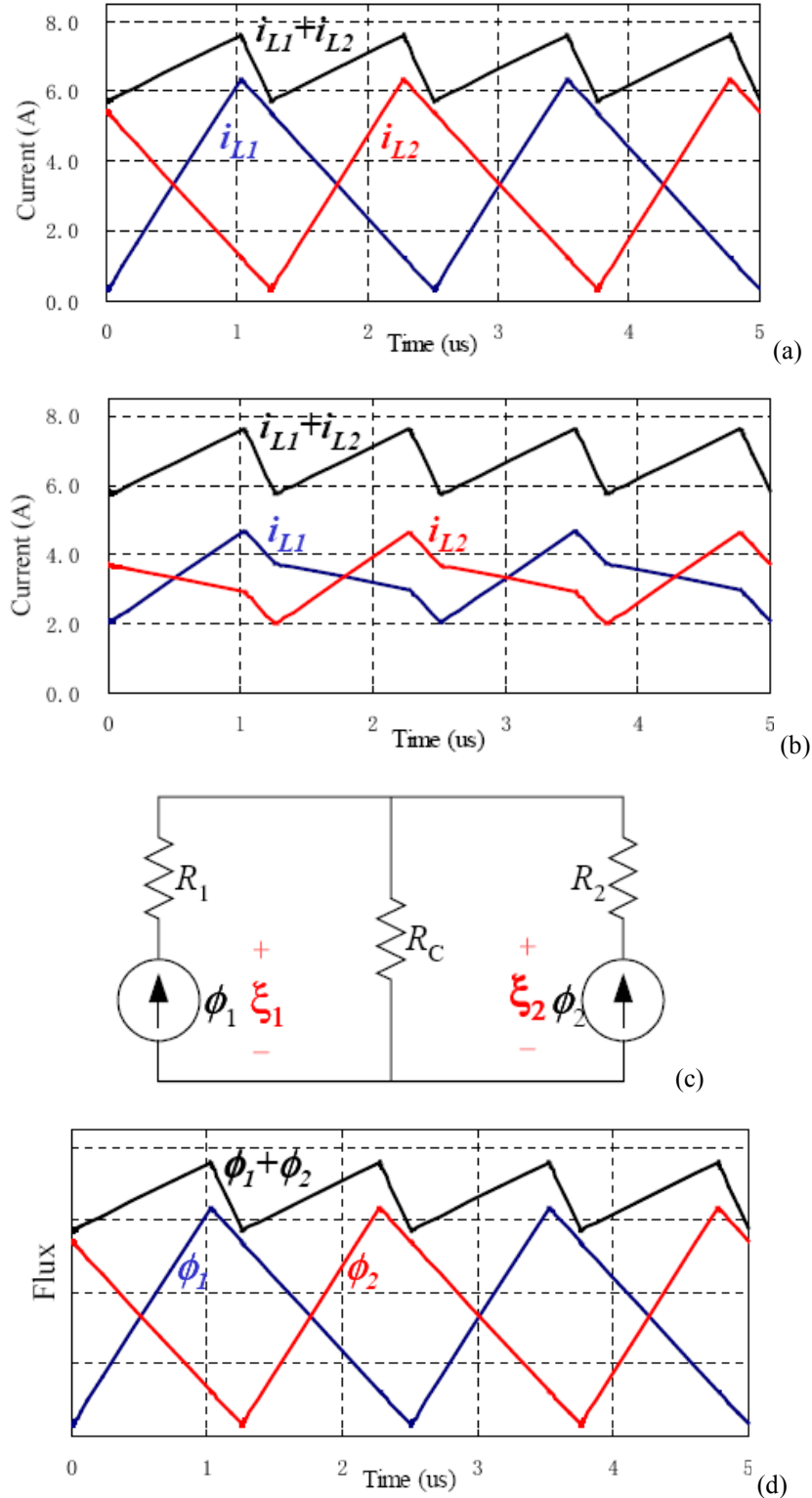


Figure 4.8 The AC flux and the current waveforms of the discrete inductor and the coupled inductor [115] (a) The inductor current waveforms (discrete inductors) (b) The inductor current waveforms (coupled inductor  $\alpha=0.5$ ) (c) The flux source reluctance model of the coupled inductor (d) The AC flux of both the inductors.

According to Faraday's law, the winding volt-seconds determine the flux in the corresponding core leg, as shown in (4.7),

$$N \cdot \phi = \int v \cdot dt \quad (4.7)$$

and the relationship between the magnetomotive forces (MMFs:  $\xi_1$  and  $\xi_2$ ) and fluxes in the windings can be described as follows,

$$N_1 \cdot i_1 = (R_1 + R_C) \cdot \phi_1 + R_C \cdot \phi_2 \text{ and} \quad (4.8)$$

$$N_2 \cdot i_2 = (R_2 + R_C) \cdot \phi_2 + R_C \cdot \phi_1 \quad (4.9)$$

From (4.7), (4.8), and (4.9),

$$i_1 = \frac{(R_1 + R_C)}{N_1^2} \cdot \int v_1 \cdot dt + \frac{R_C}{N_1 \cdot N_2} \cdot \int v_2 \cdot dt \text{ and} \quad (4.10)$$

$$i_2 = \frac{(R_2 + R_C)}{N_2^2} \cdot \int v_2 \cdot dt + \frac{R_C}{N_1 \cdot N_2} \cdot \int v_1 \cdot dt \quad (4.11)$$

The definitions of self-inductances  $L_{11}$  and  $L_{22}$ , mutual inductance  $L_{12}$ , self-inductor currents  $i_{11}$  and  $i_{22}$ , mutual currents  $i_{12}$  and  $i_{21}$ , and coupling coefficients  $\alpha_{12}$  and  $\alpha_{21}$  are as follows,

$$L_{11} = \frac{N_1^2}{R_1 + R_C}, \quad L_{22} = \frac{N_2^2}{R_2 + R_C}, \quad L_{12} = L_{21} = \frac{N_1 \cdot N_2}{R_C}, \quad (4.12)$$

$$i_{11} = \frac{\int v_1 \cdot dt}{L_{11}}, \quad i_{22} = \frac{\int v_2 \cdot dt}{L_{22}}, \quad i_{12} = \frac{\int v_2 \cdot dt}{L_{12}}, \quad i_{21} = \frac{\int v_1 \cdot dt}{L_{21}}, \text{ and} \quad (4.13)$$

$$\alpha_{12} = \frac{i_{12}}{i_{22}} = \frac{L_{22}}{L_{12}} = \frac{R_C}{R_2 + R_C} \cdot \frac{N_2}{N_1}, \quad \alpha_{21} = \frac{i_{21}}{i_{11}} = \frac{L_{11}}{L_{21}} = \frac{R_C}{R_1 + R_C} \cdot \frac{N_1}{N_2}. \quad (4.14)$$

Then Equations (4.10) and (4.11) become,

$$i_1 = i_{11} + \alpha_{12} \cdot i_{22} \text{ and} \quad (4.15)$$

$$i_2 = i_{22} + \alpha_{21} \cdot i_{11} \quad (4.16)$$

Therefore the current source model can be drawn like Figure 4.9 (b).

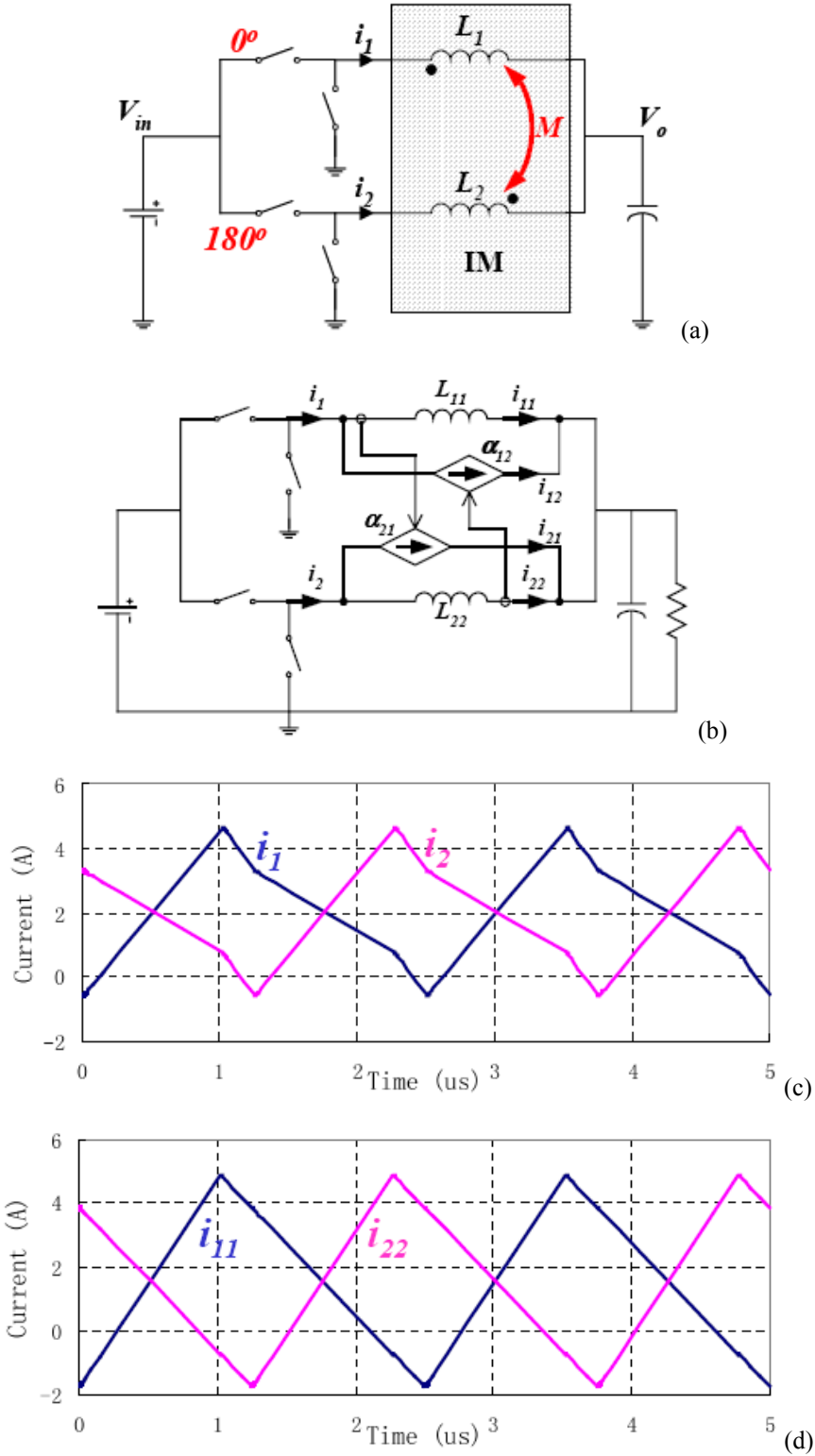


Figure 4.9 The current source model for the coupled inductor [115] (a) The two-phase VR with the coupled inductor (b) The circuit diagram with the current source model (c) The inductor currents (d) The self-inductor currents.

Figure 4.9 (c) and (d) show the simulation waveforms. The self-inductor currents represent the current waveforms made with the self inductances, and the real inductor currents are distorted by the other phase's current waveform with the weight of the coupling coefficient. Therefore, by increasing the coupling coefficient, smaller inductor current ripples can be achieved.

Since Pit-Leong Wong has proposed the coupled inductor for VR applications, many efforts have been made to implement the coupled inductor in VR applications. Figure 4.10 shows the implementation from Volterra [120]. They made the cell structure and the multiphase can be easily implemented. With this implementation, the winding in the coupled inductor cell should be around the core and this long winding results in higher copper loss. To improve this, the twisted core concept was proposed by CPES, as illustrated in Figure 4.11 [123]. The basic concept is to twist the core around the copper instead of winding the copper to reduce the copper loss. Figure 4.11 (b) shows the simplest implementation for the two-phase twisted-core coupled inductor. This coupled inductor is chosen for the hardware verification in Section 4.4.

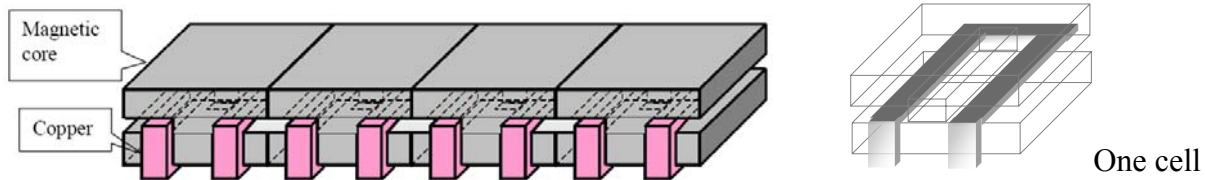


Figure 4.10 A scalable multiphase surface mount coupled inductor structure proposed by Volterra [120].

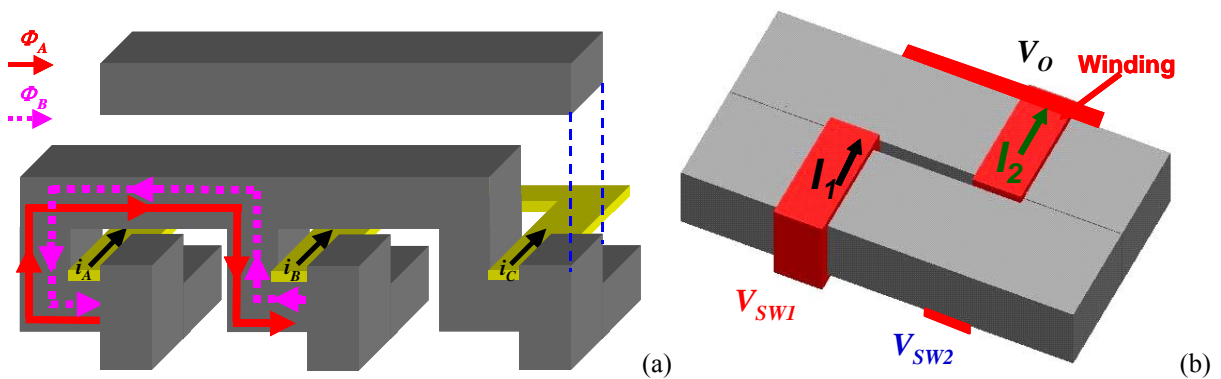


Figure 4.11 The twisted-core coupled inductor [123] (a) The multiphase implementation (b) The simplest two-phase implementation.



### 4.3. The Proposed Hysteretic Control with the Coupled Inductor

The two-phase VR with the hysteretic control method proposed in Chapter 3 is redrawn in Figure 4.12. This control method is immune to the switching noise because there is a large inductor current ramp, and this ramp has information for only one phase. Therefore, although there is some switching noise, there is no false turn-on issue. Figure 4.13 shows the two-phase coupled inductor VR with the proposed hysteretic control method. Each phase inductor current has the other phase's current information following (4.15) and (4.16). If there is some switching noise, both phases may turn on together, like Figure 4.13 (b). Then the interleaving cannot be achieved, and each phase's inductor current ripple and the output voltage ripple will be larger. This may result in lower efficiency, and it may not meet the specification. In order to get the proper operation of the proposed hysteretic control method with the coupled inductor, inductor current information which is not affected by the other phase's switching should be used. Fortunately, in the last section, the self-inductor current is defined. This current can be sensed with the DCR current-sensing network in Figure 4.14 (a) because it is related the voltage across the inductor, and DCR current sensing network uses this information to sense the current. The outputs of the DCR current sensing network are,

$$v_{CS1} = DCR11 \cdot \frac{1 + \frac{L_{11}}{DCR11} \cdot s}{1 + R_{CS1} \cdot C_{CS1} \cdot s} \cdot i_{11}, \quad v_{CS2} = DCR22 \cdot \frac{1 + \frac{L_{22}}{DCR22} \cdot s}{1 + R_{CS2} \cdot C_{CS2} \cdot s} \cdot i_{22} \quad (4.20)$$

where  $DCR11 = (1 + \alpha) \cdot DCR1$  and  $DCR22 = (1 + \alpha) \cdot DCR2$ .

By designing  $R_{CS1} \cdot C_{CS1} = L_{11}/DCR11$ , and  $R_{CS2} \cdot C_{CS2} = L_{22}/DCR22$ , the self-inductor currents are sensed. Then the current ramps are like Figure 4.9 (d), and the system works like Figure 4.14 (b). With this control method, current sharing is achieved and the average value of the self-inductor currents are the same ( $[i_{11}]_{Avg} = [i_{22}]_{Avg}$ ). Then each inductor current is controlled to be same ( $[i_1]_{Avg} = [i_{11} + \alpha \cdot i_{22}]_{Avg} = [i_{22} + \alpha \cdot i_{11}]_{Avg} = [i_2]_{Avg}$ ). From Equation (3.9), assuming  $DCR11 = DCR22$  and  $DCR1 = DCR2 = DCR$ , the output voltage is regulated like Equation (4.21). By designing  $K = 2 \cdot R_{LL}/DCR$ , AVP is achieved.

$$[V_O]_{Median} = V_{ref} - \frac{K \cdot DCR11}{2} \cdot [i_{11} + i_{22}]_{Avg} = V_{ref} - \frac{K \cdot DCR}{2} \cdot [i_1 + i_2]_{Avg} \quad (4.21)$$



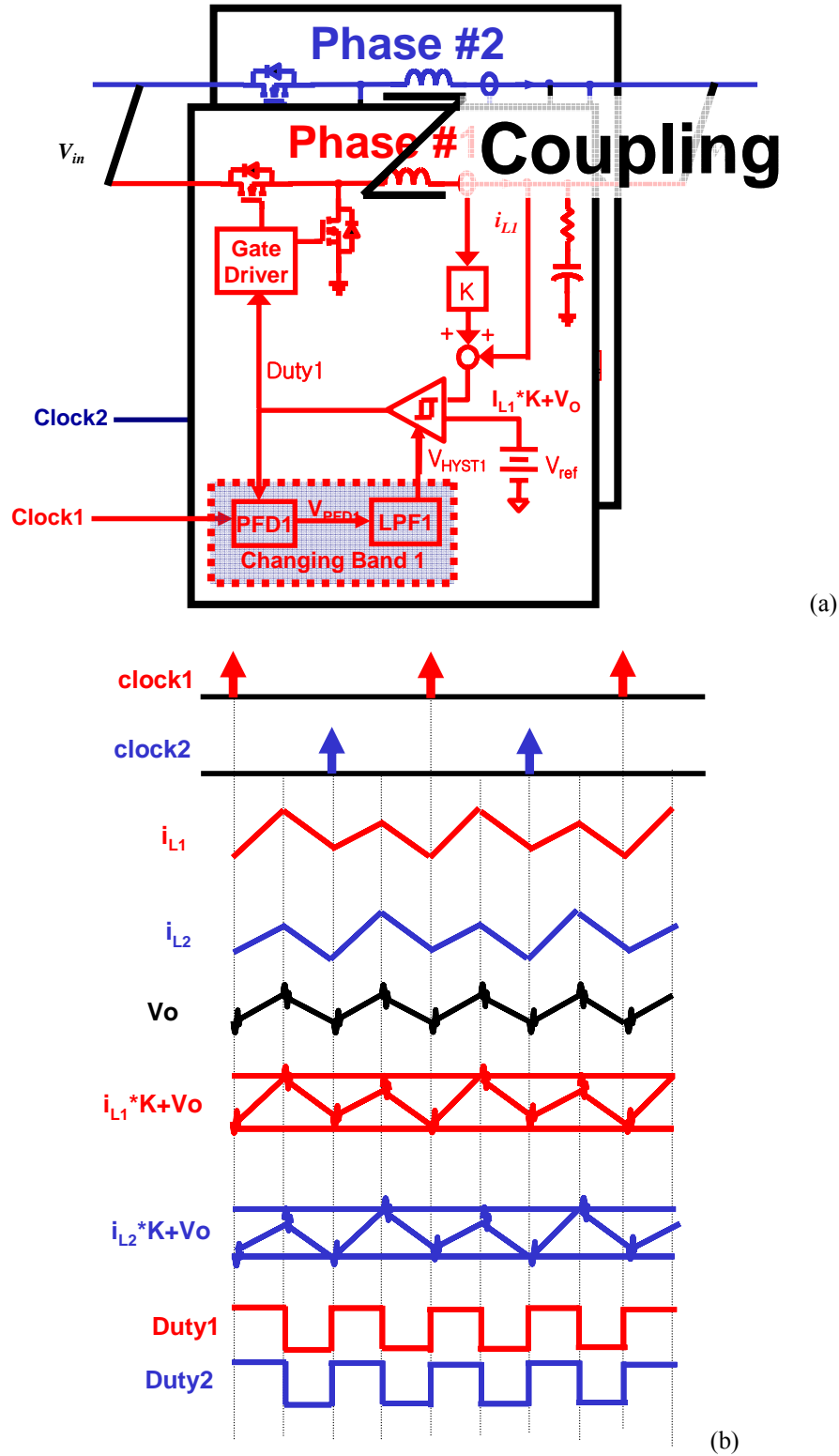
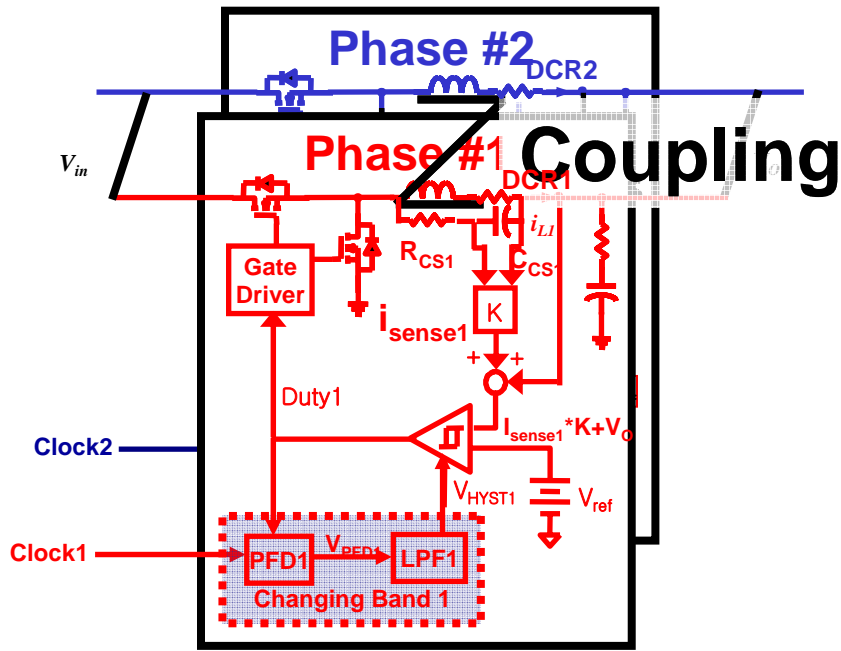
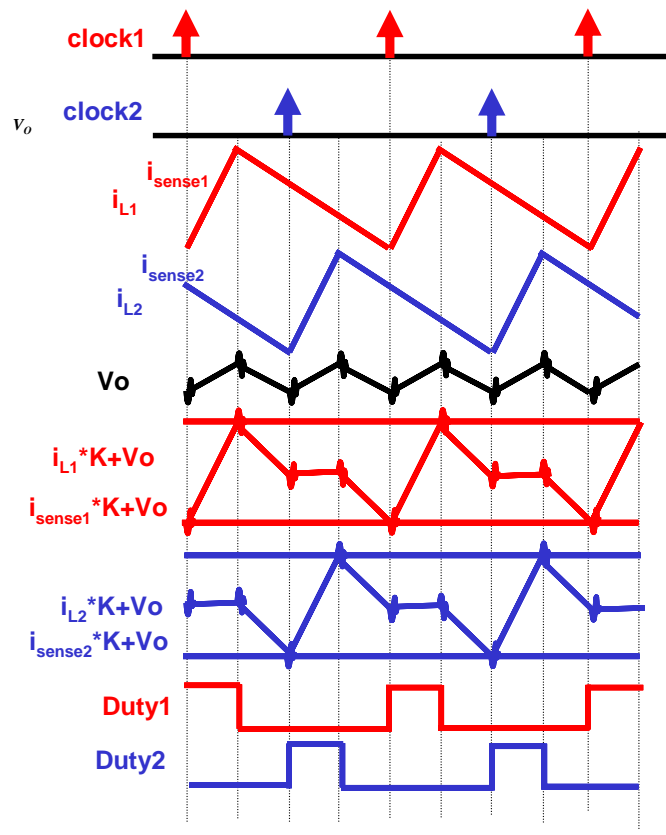


Figure 4.13 The proposed hysteretic control method with the coupled inductor -  
 (a) The schematics (b) The operating principles.



(a)



(b)

Figure 4.14 The proposed hysteretic control method with the coupled inductor and DCR current sensing -  
 (a) The schematics (b) The operating principles.

#### 4.4. Hardware Verifications

The twisted-core coupled inductor in Figure 4.11 (b) is employed in the two-phase VR with the proposed hysteretic control. The hardware specifications are;

- Two-phase VR
- $V_{IN} = 12V$ ,  $V_{ID} = 1.3V$
- $I_O = 0 \sim 27A$ ,  $di_o/dt = 200A/\mu s$ ,  $R_{LL} = 2m\Omega$
- $L_{SS}=L_{eq1} = 300nH$ ,  $L_{TR}=L_{eq2}=150nH$  Coupled inductor
- $F_s = 300kHz$
- Bulk Capacitors :  $2 \times 100\mu F$  (MLCCs)
- Cavity Capacitors :  $10\mu F \times 24$ ,  $22\mu F \times 10$
- Hysteretic controller : TPS5210
- PLL controller : TLC2932
- Clock generator : LM2639
- Additional OPAMPs are used for DCR sensing.

Figure 4.15 (b) shows the inductor current waveforms of this two-phase VR hardware. The inductor current slew rate ( $di_L/dt$ ) is same as that of 150nH discrete inductor in Figure 4.15 (a), while the inductor current ripple size is reduced by half. The inductor current ripple size is same as the 300nH discrete inductor case. Therefore, with this coupled inductor, good performance is expected.

Figure 4.16 shows the measured efficiency data. The efficiency of the VR with the coupled inductor is 4% larger than that of the VR with 150nH discrete inductor at full load.

Figure 4.17 shows the measured waveforms of this two-phase VR with coupled inductor and the proposed hysteretic control method. AVP is achieved very well, and the output voltage peak is within the specification;  $V_{ID} + 50mV$ . Therefore, using the coupled inductor and the proposed hysteretic control method, the output capacitors can be further reduced without degrading the system efficiency.

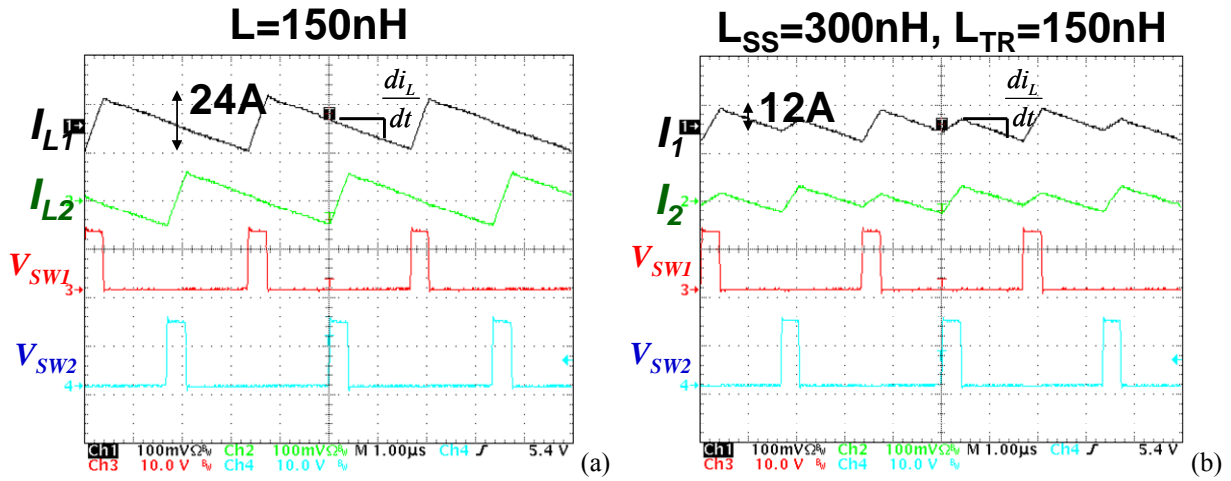


Figure 4.15 The inductor current waveforms of two-phase VR (a) with discrete inductors (b) with coupled inductor.

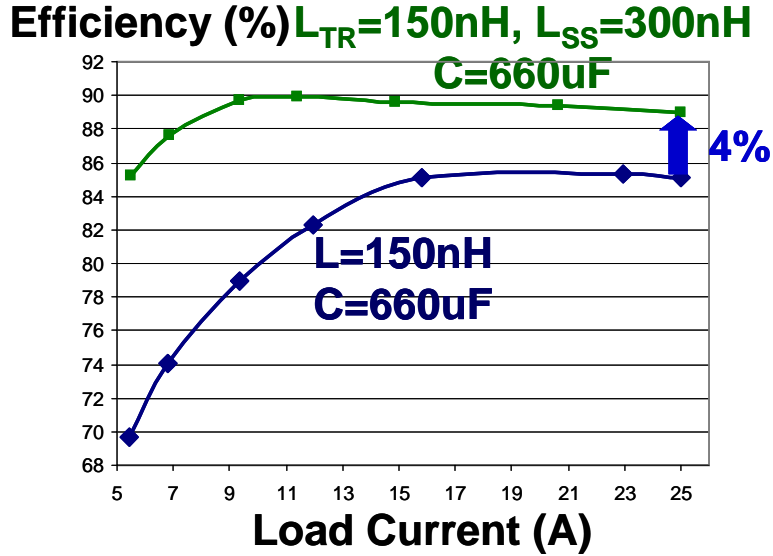


Figure 4.16 The measured efficiencies (Blue line: two-phase VR with 150nH, 660 $\mu\text{F}$ , Green line: two-phase VR with the coupled inductor  $L_{TR}=150\text{nH}$ ,  $L_{SS}=300\text{nH}$ , 660 $\mu\text{F}$ ).

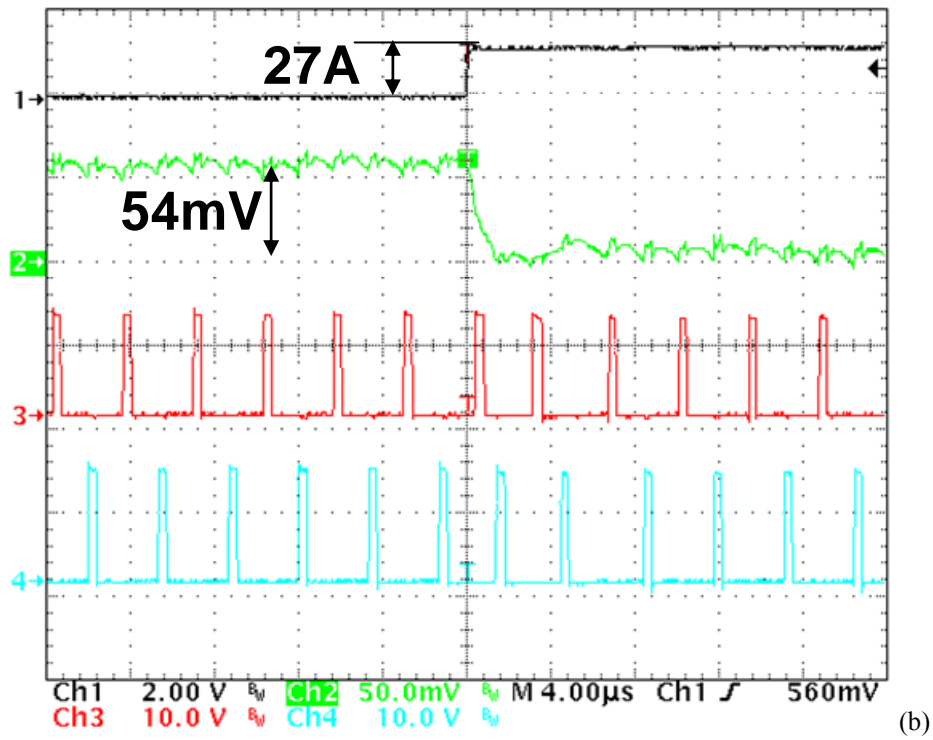
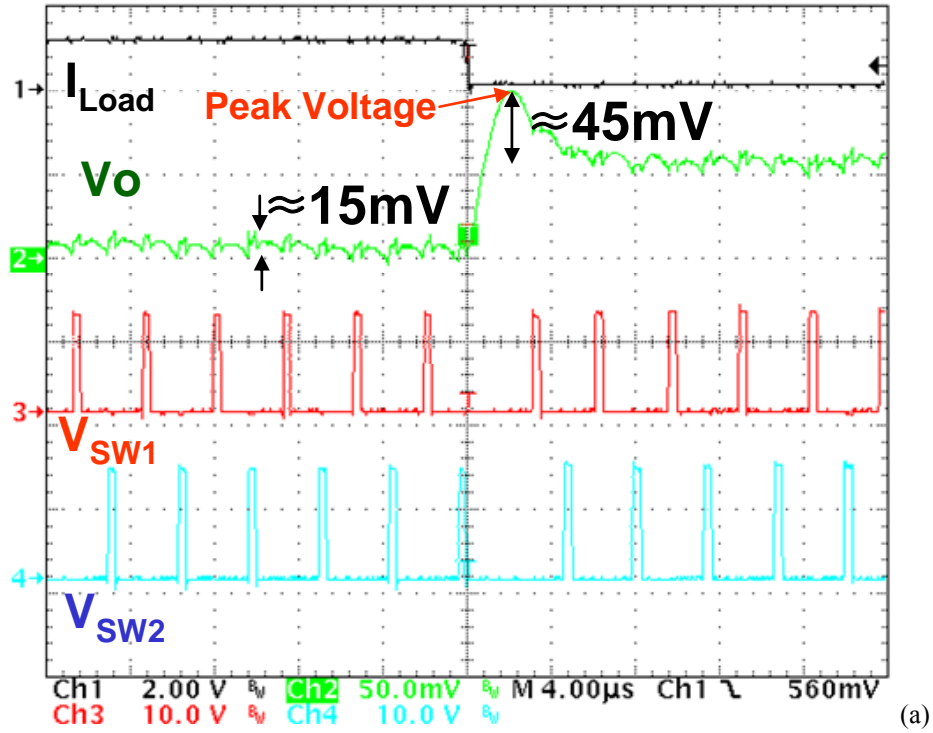


Figure 4.17 The experimental results of two-phase coupled inductor VR with the proposed hysteretic control  
 (a) The load step-down transient (b) The load step-up transient.

## **4.5. Summary**

The hysteretic control proposed in Chapter 3 saturates the controller during the transient. The output voltage peak is determined by the inductance and the output capacitors. By decreasing the inductance, the output capacitor number can be reduced. However, the low inductance makes the system efficiency lower. To avoid low efficiency from the low inductance, the coupled inductor is employed. With the coupled inductor, the transient inductance can be reduced while keeping the steady-state inductance constant. The hardware is built and it is verified that the capacitors can be reduced while keeping the same efficiency. The proposed hysteretic control method with the coupled inductor is a good solution for future VRs.



## Chapter 5. Conclusions and Future Work

The future microprocessor meets the big challenge of power dissipation, and this challenges the voltage regulator with a fast transient, high current, extremely low output voltage, and light-load efficiency. With the today's technology, many decoupling capacitors will be necessary, which will increase the size and cost of the VR. Therefore finding the ways to deal with those challenges without increasing the size and cost of VR is the biggest issue. This dissertation focuses on this issue with the two approaches; the two-stage approach and the nonlinear control approach.

### 5.1. Summary

The easiest way to increase the speed of VR is with higher switching frequency operation. However, higher switching frequency results in system efficiency degradation. Using the two-stage architecture, the VR can run with the higher switching frequency, which may reduce the VR's cost and size. For a 300kHz two-phase VR, the output capacitance is 1600 $\mu$ F with 50kHz bandwidth. With the two-stage architecture, the second stage switching frequency can be 600kHz, with an output capacitance of 940 $\mu$ F with 80kHz bandwidth. However, the low light-load efficiency of the two-stage architecture is a drawback. This reduced light-load efficiency occurs because the bus voltage is optimized for full-load efficiency, instead of light-load efficiency. By adaptively positioning the bus voltage according to the load current, the light-load efficiency can be improved. This is the Adaptive Bus Voltage Positioning (ABVP) control method for the two-stage VR. The performance of the ABVP system is related to the first-stage bandwidth, and with the higher first stage bandwidth better ABVP performance is achieved. However, with the higher first stage bandwidth, the ABVP system becomes unstable. To get the system stable, the first stage bandwidth is designed to be too low, such as one-hundredth of the switching frequency, and this causes slow ABVP dynamics. This in turn degrades the ABVP performance and requires a large number of bus capacitors, which increases the size and cost. In order to push the first-stage bandwidth higher, a stability analysis must be performed. There is a positive feedback loop in ABVP system because the second-stage inductor current is fed back to

the first stage with the positive gain ' $R_{tilt}$ '. To analyze this, a small signal model is suggested and the new feedforward small-signal model is derived. The previous feedforward small-signal model is not accurate enough to predict this positive feedback loop ( $T_{ABVP}$ ). With the new feedforward small signal-model proposed in Chapter2,  $T_{ABVP}$  can be predicted. The ABVP system is stable when the magnitude of  $T_{ABVP}$  is smaller than 0dB. The peak magnitude of  $T_{ABVP}$  is determined by the first-stage bandwidth. The magnitude of  $T_{ABVP}$  can be reduced by designing the second-stage feedforward gain to be as large as possible. Using a low-pass filter with the corner frequency slightly lower than the first stage bandwidth, the peak magnitude of  $T_{ABVP}$  can be reduced too. With these measures in place, the ABVP system is designed to be stable while pushing first-stage bandwidth as high as possible (about one-tenth of the switching frequency in the example). Then, in the design example, the ABVP dynamics is improved to be about five times faster, and the amount of bus capacitors is reduced about ten times. With the hardware, the ABVP-AVP system and its design are verified.

With the nonlinear control approach, in order to get a faster system and reduce the size and cost, the hysteretic control method for the multiphase VR is proposed. The hysteretic control method is very good because of its fast transient capability and the high light-load efficiency with DCM operation. With the parallel operation, AVP and current-sharing functions are achievable. However, in order to use the hysteretic control method for multiphase VR applications, these are not enough; the interleaving function must be implemented as well. There are some interleaving methods for use with hysteretic control. However, with these methods, the load step-up dynamics are not good, and they require more output capacitors. With the existing interleaving method, the system is interleaved not only at the steady state but also during the transient, and the duty cycles of each phase cannot be overlapped during the load step-up transient. This reduces the inductor current slew rates, which determines the speed of the system. For the four-phase VR design with VRD 11.0 specifications,  $9 \times 560\mu\text{F}$  Al-polymer bulk capacitors are necessary to deal with the load step-up transient. In order to reduce the need for more output capacitors, the multiphase hysteretic control method is proposed. Using the phase locked loop (PLL), this method locks the phase and frequency of the duty cycles to the reference clocks by modifying the hysteretic band width. By phase shifting the reference clocks, the interleaving function is achieved at the steady state. During the load transient state, the phase locking function is eliminated by designing the PLL to be slow and the system reacts quickly to

the load change without the interruption from the phase-locking function (interleaving function). Therefore, during the load step-up transient, the duty cycles of each phase can be overlapped to get the highest inductor current slew rate. With the proposed hysteretic control method, for the same four-phase VR design with VRD 11.0 specifications the bulk output capacitors can be reduced from 9 to 6×560uF Al-polymer bulk capacitors.

The proposed hysteretic control method should be analyzed and designed to meet the required specifications before it is used. During the transient, the controller is saturated and the output voltage peak should be predicted. For this purpose, the phase plane analysis is suggested. Using the phase plane model, the load transient dynamics are analyzed, the output voltage peak is predicted and the output capacitors are designed to meet the required specifications. Although the output capacitors are properly designed for the output voltage peak during the controller saturation, there can be another output voltage peak due to the improper PLL design. The model to properly design the hysteretic band width changing loop is necessary. Using the sampled data-modeling technique, the linearized model is derived. With this model, the hysteretic band width changing loop is designed, and the improper output voltage peak can be eliminated. However with the repetitive load dynamics, there is another issue. If the transient occurs before the hysteretic band width changing loop settles down, the transient may start with the large hysteretic band width, and the output voltage peak can exceed the specification. To prevent this, the hysteretic band width limiter is inserted. Using hardware, the proposed hysteretic control method and its design are verified. A two-phase VR with 300kHz switching frequency is built, and the output capacitance is only 860μF comparing to 1600μF output capacitance with the 50kHz bandwidth linear control method. This is about a 46% capacitor reduction.

The performance of the proposed hysteretic control can be further enhanced with the coupled inductor. The proposed hysteretic control method saturates the controller during the transient and the transient peak voltage is determined by the power stage parameters, the inductance and the output capacitors. It is shown that by decreasing the inductance, the output capacitors are reduced. However, small inductance results in low efficiency. In order to resolve this problem, the coupled inductor is used. The coupled inductor is the nonlinear inductor which has two separate inductances for the transient and the steady state. With the coupled inductor, the transient inductance can be reduced with the constant steady-state inductance. Therefore, the transient speed can be faster without reducing the system's efficiency. However, the coupled

inductor cannot be used directly in the hysteretic control because each phase's inductor current with the coupled inductor has the all phase information, and along with the switching noise, this may ruin the interleaving function. Therefore, the current information, which has only each phase's information, is necessary. In the coupled inductor, this current information can be sensed with the DCR current sensing method. The proposed hysteretic control method with the coupled inductor can be implemented using the DCR current sensing network. The two-phase VR with 300kHz switching frequency is built, and the output capacitance is only 660 $\mu$ F, in contrast with 860 $\mu$ F output capacitance with the proposed hysteretic control only. This is about a 23% capacitor reduction. And compared to the 50kHz bandwidth conventional linear control method, that is about a 60% capacitor reduction.

Table 5.1 summarizes the output capacitor reduction with the proposed technologies.

**Table 5.1 The technology and the output capacitance for two-phase VR hardware in this dissertation.**

Technology	Linear Control ( $f_c=50\text{kHz}$ )	Two Stage ( $f_c=80\text{kHz}$ )	Proposed Hysteretic Control	Proposed Hysteretic Control with Coupled Inductor
Output capacitance	1600 $\mu$ F	940 $\mu$ F	860 $\mu$ F	660 $\mu$ F

## 5.2. Future Work

The analysis and design of the hysteretic control method in Chapter 3 is based on the assumption that each phase is independent of the others. This is true when the each phase's inductor current ramp is much larger than the ramp from the output voltage ripple in the feedback signal. Therefore, for some applications with a very low  $R_{LL}$  or with very small output capacitors, more analysis is necessary. The coupling effect from the output voltage should be analyzed.

With the proposed hysteretic control method and the coupled inductor, more study is necessary to optimize the system. In this dissertation, the transient inductance is arbitrarily chosen to show the benefit of the system. A smaller transient inductance results in smaller output capacitors for the transient, while the steady-state output voltage ripple size increases. A guide for careful design of the transient inductance in the coupled inductor should be researched.



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